2. ADC Architectures and CMOS Circuits

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Integrated Circuits and Systems
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1. ADC Classification

2. Flash Techniques

3. Sub-Ranging, Time-Interleaving and Pipelining Techniques

4. Successive-Approximation Techniques

5. Integrating Techniques

6. Delta-Sigma Modulation Techniques

7. Time-Domain Techniques
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ADC Families

Classification based on architecture approach:

- **Flash**
- **Sub-ranging**
- **Pipeline**
- **SAR**
- **Integrating**
- **Delta-Sigma**

Distinctive characteristics:
- Feedforward vs feedback control
- Single vs multiple stages
- Amplitude vs time domains

Typically mixed solutions...
ADC Evolution

\[ FOM_S = SNDR_{\text{max}} + 10 \log \frac{f_{\text{nyq}}}{2P_D} \]

\[ FOM_W = \frac{P_D}{f_{\text{nyq}} \cdot 2^{\text{ENOB}}} \]

\[ FOM_S \approx 85\text{dB} \]

\[ FOM_W \approx 5\mu\text{J/conv-step} \]

EPSCO DATRAC, B.M. Gordon, 1953

11-bit 50kSps 500W SAR ADC

0.5m x 0.4m x 0.65m, 70kg

Vacuum tube technology

W. Kester, Analog-Digital Conversion

ADC Evolution

$$FOM_S = SNDR_{max} + 10 \log \frac{f_{nyq}}{2P_D}$$

$$FOM_W = \frac{P_D}{f_{nyq} \cdot 2\text{ENOB}}$$

$$FOM_S \approx 85\text{dB}$$

$$FOM_W \approx 5\mu\text{J/conv-step}$$

+60 years

State-of-art ADC
Solid-state technologies

B. Murmann, ADC Performance Survey

http://www.stanford.edu/~murmann/adcsurvey.html

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ADC Evolution

- **Performance enhancement:**
  - Architecture strategy
  - Circuit design
  - Integration technology

- **Still room for further improvement?**

\[
SNR_{\text{max}} = \frac{\left(\frac{V_{FS}}{2\sqrt{2}}\right)^2}{KT/C_s} \frac{f_s}{f_{\text{nyq}}}
\]

\[
P_{\text{min}} = \frac{C_s V_{FS} f_s V_{DD}}{I_{DD}}
\]

\[
P_{\text{min}}|_{V_{FS}=V_{DD}} \simeq C_s f_s V_{FS}^2
\]

\[
E_{\text{min}} = \frac{P_{\text{min}}}{f_{\text{nyq}}} = 8KT \cdot SNR_{\text{max}}
\]

State-of-art ADC
Solid-state technologies

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Basic Flash Architecture

Building **blocks**: e.g. single-ended 3-bit flash ADC

- **Threshold generator**: $V_{FS} = V_{DD}$
- **Latched comparator array**
- **thermometer code**
- **Digital encoder**
- **combinational only logic**

- $V_{in} \rightarrow f_s$
- $V_{th1}$
- $V_{thk}$
- $V_{th7}$
- $d_{out}$
Basic Flash Architecture

Building blocks:

- Threshold generator: \( V_{FS} = V_{DD} \)
- Latched comparator array
- Thermometer code
- Digital encoder (natural binary code)

- e.g. single-ended 3-bit flash ADC

1 clock cycle conversion time

Area and power scaling by \( 2^{ENOB} \)

Distortion due to technology mismatching

Area and power scaling by \( 2^{ENOB} \)
Latched Comparator Design

Compact **CMOS** circuit:

\[ \phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases} \]
Latched Comparator Design

- **Compact CMOS circuit:**

  - **Non-overlapped clock phases:**
    - \( \phi_1 \)
    - \( \phi_2 \)

  - \( \phi_x = \begin{cases} 
    H & \text{closed} \\
    L & \text{open} 
  \end{cases} \)

  - **1/\( f_s \) clock**

  - **Pre-charging phase**
  - **Decision phase**

- **High-speed operation**

- **Each comparator crosses at different threshold \( V_{thk} \)**

- **Threshold voltage offset?**

- **Positive feedback to speed-up comparison**

- **Symmetrical loading**
Comparator Optimization

By attaching an array of level shifters:

\[
t_k = \text{sign} \left[ V_{ref} - \left( V_{ref} + \frac{C_1}{C_1 + C_2} (V_{ref} - V_{in}) + \frac{C_2}{C_1 + C_2} (V_{DD} - V_{ref}) \right) \right]
\]
Comparator Optimization

By attaching an array of level shifters:

- All comparators latch at the same level \( V_{\text{ref}} \)
- Single comparator design
- Low quiescent power (resistor-less thresholds)
- Capacitor area overhead
- Input capacitance increased
- Slower operation

\[
t_k = \text{sign} \left[ V_{\text{ref}} - \left( V_{\text{ref}} + \frac{C_{1k}}{C_{1k} + C_{2k}} (V_{\text{ref}} - V_{\text{in}}) + \frac{C_{2k}}{C_{1k} + C_{2k}} (V_{DD} - V_{\text{ref}}) \right) \right]
\]
Comparator Optimization

- By attaching an array of level shifters:

\[ \phi_x = \begin{cases} 
    H & \text{closed} \\
    L & \text{open}
\end{cases} \]

\[ V_{\text{ref}} = \frac{V_{\text{DD}}}{2} \]

- **Area** and **power** overheads (x2)
- **Higher symmetry** requirements
- **Interference rejection**
- **Full-scale** extension (+6dB)
- **SNR** enhancement (+3dB)
- **Distortion** cancellation (even harmonics)
Comparators Offset

- MOSFET $V_{TH}$ mismatching effects:

\[ \sigma^2(V_{off}) = \sigma^2(\Delta V_{TH1,2}) + \left(\frac{g_{m3,4}}{g_{m1,2}}\right)^2 \sigma^2(\Delta V_{TH3,4}) \]

$\sigma(V_{off}) \approx \sigma(\Delta V_{TH1,2}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$

\[ \left(\frac{W}{L}\right)_{1,2} \gg \left(\frac{W}{L}\right)_{3,4} \]

Pelgrom's Law

\[ \text{CMOS technology} \]

\[ \text{Distortion due to DNL} \]

\[ d_{max} \]

\[ d_{out} \]

\[ V_{LSB} \]

\[ V_{in} \]

\[ V_{FS} \]

\[ DNL \]

\[ + \frac{V_{LSB}}{2} \]

\[ \frac{V_{LSB}}{2} \]
Comparators Offset

- **Thermometer code bubbles!**

- **Error** propagation at encoding...

\[ \sigma(V_{off}) = \frac{A_{VT_H}}{\sqrt(WL)_{1,2}} \]

- **Latched comparator array**

- **Gaussian probability distribution**

- **Large device area** (WL) and input **capacitance** penalties
Comparators Offset

- Thermometer code **bubbles!**

- **Digitally assisted** analog design:

\[ \sigma(V_{off}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}} \]
Comparators Offset

- Thermometer code **bubbles!**

- **Digitally assisted** analog design:

\[ \sigma(V_{off}) = \frac{A_{VT H}}{\sqrt{(WL)_{1,2}}} \]

(WL) large enough to limit bubble distance to 1 code:

\[
\begin{array}{ccc|c}
  t_{k-1} & t_k & t_{k+1} & b_k \\
  0 & X & X & 0 \\
  1 & X & 0 & t_k \\
  (1) & X & 1 & 1 \\
\end{array}
\]
Comparators Offset

More on digitally assisted analog design: an stochastic flash ADC

Comparators Offset

More on digitally assisted analog design: an stochastic flash ADC

\[ \sigma(V_{off}) = \frac{A_{VT\text{H}}}{\sqrt{(WL)_{1,2}}} \]

- Almost digital
- Compact area
- Non-linearity compensation required
- Power consumption

Digital full-adders

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Sub-Range Flash ADC

- **Building blocks:**
  - S/H
  - Flash ADC
  - Flash DAC
  - Encoder

- **Two-step** coarse-fine data conversion scheme

- **ENOB splitting** can be chosen asymmetric depending on circuits...
Sub-Range Flash ADC

▶ Building blocks:

\[ V_{in} \rightarrow \text{S/H} \rightarrow \text{Flash ADC} \rightarrow \text{Flash DAC} \rightarrow \text{MSB} \rightarrow \text{Encoder} \rightarrow d_{out} \]

- Coarse stage
- Fine stage

▶ Two-step coarse-fine data conversion scheme

▶ ENOB splitting can be chosen asymmetric depending on circuits...

Better ENOB scaling of comparators and passive components!

- e.g. Number of comparators for 8-bit flash ADC:
  - single-stage \( \times (2^{\frac{ENOB}{2}} - 1) = 255 \times 2^{\frac{ENOB}{2}} \)
  - two-stage \( \times 2(2^{\frac{ENOB}{2}} - 1) = 30 \times 2^{\frac{ENOB}{2}+1} \)

▶ Speed reduction (x2)

- Non-linearity caused by mismatching between coarse ADC-DAC, and between coarse-fine ADC
Sub-Range Flash ADC

**Circuit** implementation:

- **V_{in}**
- **S/H**
- **Flash ADC**
- **Flash DAC**
- **Flash ADC**
- **Encoder**
- **V_{fine}**
- **d_{out}**

**Non-linearity caused by non-unitary gain in MSB subtraction**

**Compact SC** implementation:

- **V_{in}**
- **V_{ref}**
- **V_{fine}**
- **d_{MSB}**
- **d_{MSB-1}**
- **V_{FS} \equiv V_{DD}**

**1/f_s**

Coarse stage

Clock

- \( \phi_1 \)
- \( \phi_2 \)

1/f_s

coarse

fine

- H closed
- L open

\( \phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open}
\end{cases} \)

Single-ended version

To coarse flash ADC

To fine flash ADC
**Time-Interleaved Flash ADC**

- **Two-step CMOS comparator:**

  \[ \phi_x = \begin{cases} 
  H & \text{closed} \\
  L & \text{open} 
  \end{cases} \]

  - **analog inverter-based**
  - **Compact area**
  - **Offset insensitive!**
  - **Poor power supply rejection ratio (PSRR)**

  - **Sampling + auto-zero**
  - **Subtraction + quantization**

  \[ \Delta V_{\text{bias}} = V_{\text{thk}} - V_{\text{in}} \]
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Time-Interleaved Flash ADC

**Counter-phase** two-step CMOS comparator:

- **Offset insensitive!**
- **Compact area**
- **Higher speed** (x2)

- Poor power supply rejection ratio (**PSRR**)
- **Higher jitter** sensitivity (both clock edges)

\[ \phi_x = \begin{cases} 
    H & \text{closed} \\
    L & \text{open} 
\end{cases} \]
Time-Interleaved Flash ADC

Extending the same idea to multiple time-interleaving:

- Overall equivalent high-speed conversion
- Each flash ADC operates at low-speed (1/N)
- Large area (xN)
- High latency (xN)
- Complex synchronization

\[
\phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases}
\]
Pipeline ADC

- Combination of **cascaded sub-ranging** and **time-interleaving**:

  ![Diagram of Pipeline ADC](image)

  - $V_{in}$
  - Stage 1: $d_p$ bit
  - Stage 2: $d_q$ bit
  - Stage M: $d_r$ bit
  - MSB Time Alignment
  - LSB
  - $d_{out}$

  - $V_{in}$
  - S/H
  - Flash ADC $p$-bit
  - Flash DAC $p$-bit
  - $f_s$
  - $d_p$

  - Sub-converter functions:
    - Sampling and hold (S/H)
    - Sub-range quantization
    - Residue computation and scaling

- Sub-converter functions:
Pipeline ADC

- Combination of **cascaded sub-ranging** and **time-interleaving**:

\[
SNR_{eq} = \frac{S_{in}}{2^{-2p}N_1 + 2^{-2(p+q)}N_2 + \ldots + 2^{-2(p+q+\ldots+r)}N_M}
\]

- **Simpler** flash sub-ADCs
- **Performance depends on first-stage only**
- **No speed** reduction
- **High latency** (\(xM\))
Pipeline ADC

Simple 1-bit stage case study:

\[
V_{out} = 2 \left( V_{in} - V_{ref} + (-1)^{d_k} \frac{V_{FS}}{4} \right) + V_{ref}
\]

SC implementation of each stage:

![Diagram of Pipeline ADC with SC implementation](image-url)
Pipeline ADC

Simple 1-bit stage case study:

Stage 1 \rightarrow Stage 2 \rightarrow Stage M

\( d_{MSB} \rightarrow d_{MSB-1} \rightarrow d_{LSB} \)

Time Alignment

\( M \rightarrow d_{out} \)

SC implementation of each stage:

single-ended version

\[ V_{in} \rightarrow V_{out} \]

\[ d_k = 1 \]

\[ V_{out} = V_{in} - \frac{C_s}{C_f} \left( V_{ref} + (-1)^{d_k} \frac{V_{FS}}{2} - V_{in} \right) \]
Pipeline ADC

**Simple 1-bit stage** case study:

\[
V_{out} = V_{in} - \frac{C_s}{C_f} \left( V_{ref} + (-1)^{d_{MSB}} \frac{V_{FS}}{2} - V_{in} \right)
\]

\[
V_{out} = 2 \left( V_{in} - V_{ref} + (-1)^{d_k} \frac{V_{FS}}{4} \right) + V_{ref}
\]

\[
C_f \equiv C_s
\]

**SC implementation** of each stage:

- **Simplest** flash sub-ADCs
- **Inherently linear** single bit quantization
- **Noise** contributions from stage 2 → **multi-bit** first stage
- **Offset** sensitivity
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**Successive Approximation ADC**

► **Building blocks:**

![Diagram of Successive Approximation Register (SAR)](diagram)

- **S/H**
- **Flash DAC**
- **Digital state-machine (algorithm)**
- **Successive Approximation Register (SAR)**
- **V_{in}**
- **V_{res}**
- **V_{dac}**
- **f_{s}**
- **N_{fs}**
- **d_{out}**

**Equations:**

- \( V_{in} \rightarrow S/H \)
- \( S/H \rightarrow V_{res} \)
- \( V_{res} + \rightarrow \)
- \( \rightarrow V_{dac} \)
- \( V_{dac} \rightarrow \text{approximation} \)
- \( \text{approximation} \rightarrow \text{SAR} \)
- \( \text{SAR} \rightarrow d_{out} \)
- \( f_{s} \rightarrow S/H \)
- \( f_{s} \rightarrow \)
Successive Approximation ADC

- **Building blocks:**

  ![Diagram](https://via.placeholder.com/150)

- **Analog minimalist**
- **Very low-power consumption**
- **Speed requirements (xN)**
- **Performance limited by flash DAC**
Successive Approximation ADC

Circuit implementation:

\[ V_{in} \rightarrow S/H \rightarrow V_{res} \rightarrow \text{Successive Approximation Register (SAR)} \]

\[ V_{dac} \rightarrow N \rightarrow d_{out} \]

\[ V_{FS} \equiv 2V_{ref} \quad \text{single-ended version} \]
2. ADC Architectures and CMOS Circuits

Successive Approximation ADC

**Circuit** implementation:

\[ V_{in} \rightarrow \text{S/H} \rightarrow V_{res} \rightarrow \text{Successive Approximation Register (SAR)} \]

\[ V_{dac} \]

\[ V_{FS} = 2V_{ref} \] single-ended version

\[ \phi_x = \begin{cases} H & \text{closed} \\ L & \text{open} \end{cases} \]

\[ \frac{1}{Nf_s} \]

\[ d_{MSB} \]

\[ d_{MSB-1} \]

\[ d_{LSB} \]
Successive Approximation ADC

**Circuit implementation:**

\[ V_{in} \xrightarrow{S/H} V_{res} \xrightarrow{\text{Successive Approximation Register (SAR)}} V_{out} \]

\[ \frac{C_s}{2^N} + \sum_{i=1}^{N} \frac{C_s}{2^i} \equiv C_s \]

\[ \phi_x = \begin{cases} \text{H closed} \\ \text{L open} \end{cases} \]

\[ 1/Nf_s \]

\[ d_{MSB} \]

\[ d_{MSB-1} \]

\[ \ldots \]

\[ d_{LSB} \]

\[ V_{FS} \equiv 2V_{ref} \quad \text{single-ended version} \]

\[ \text{Signal baseline} \]

\[ V_{ref} \]

\[ C_{off} \]

\[ \text{to SAR} \]
Successive Approximation ADC

Circuit implementation:

\[ V_{\text{res}} = V_{\text{in}} - V_{\text{off}} \]

\[ + \left[ \frac{(-1)^{d_{\text{MSB}}}}{2} + \frac{(-1)^{d_{\text{MSB}}}}{4} + \cdots + \frac{(-1)^{d_{\text{LSB}}}}{2^N} \right] V_{\text{ref}} \]

\[ \frac{C_s}{2^N} + \sum_{i=1}^{N} \frac{C_s}{2^i} = C_s \]
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Single-Slope ADC

Building blocks:

\[ \phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases} \]

\[ f_{\text{clk}} = (2^N - 1) f_s \]

\[ t_{\text{pwm}} = RC \frac{V_{\text{in}}}{V_{\text{ref}}} \]

\[ d_{\text{out}} = t_{\text{pwm}} f_{\text{clk}} = (2^N - 1) f_s RC \frac{V_{\text{in}}}{V_{\text{ref}}} \]
Single-Slope ADC

Building blocks:

- Analog minimalist
- Very low-power
- Speed requirements ($\times 2^N$)
- Technological sensitivity ($RC$)

$$t_{pwm} = RC \frac{V_{in}}{V_{ref}}$$

$$d_{out} = t_{pwm} f_{clk} = (2^N - 1) f_s RC \frac{V_{in}}{V_{ref}}$$

$$f_{clk} = (2^N - 1) f_s$$
Dual-Slope ADC

► Building blocks:

\[ V_{in} \equiv \frac{t_1}{t_2} V_{ref} \]

\[ d_{out} = \frac{d_1}{d_2} \propto \frac{V_{in}}{V_{ref}} \]

▲ Analog minimalist
▲ Very low-power
▼ Speed requirements \((x2^N)\)
▲ Technology independence \((RC)\)
Integrate-and-Fire ADC

- **Building blocks:**

  \[
  d_{out} = \frac{1}{fs} = \frac{I_{in}}{CV_{th}fs}
  \]

  - **Current-mode** sensors (e.g. imagers)
  - **Very low-power**
  - **Speed** requirements adapted to signal
  - **Technology sensitivity (C)**
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Delta-Sigma Modulator ADC

- General **single-loop DSM** architecture:
Delta-Sigma Modulator ADC

- General **single-loop DSM** architecture:

  ![Diagram of a single-loop DSM ADC](image)

  - **Noise-shaper filter:**
    - In-band **high-gain**
    - Either continuous- $H(s)$ or **discrete-time** $H(z)$

  - **Flash ADC and DAC blocks can be relaxed!**

- **DSM signal vs quantization noise** behavior?

  ![Diagram of DSM signal vs quantization noise](image)

  \[
  STF = \frac{H}{1 + H} \quad \rightarrow 1
  \]
  \[
  NTF = \frac{1}{1 + H} \quad \rightarrow 0
  \]
Delta-Sigma Noise Shaping

Simplest architecture: first-order (N=1) 1-bit (B=1) single-loop DSM

Single-bit feedback DAC is intrinsically linear
Delta-Sigma Noise Shaping

**Simplest** architecture: **first-order** \((N=1)\) **1-bit** \((B=1)\) single-loop DSM

\[
H(z) = \frac{z^{-1}}{1 - z^{-1}}
\]

\[
\begin{align*}
STF &= \frac{H}{1 + H} \equiv z^{-1} \\
NTF &= \frac{1}{1 + H} \equiv 1 - z^{-1}
\end{align*}
\]

- Single-bit feedback DAC is **intrinsically linear**
- **Oversampling** is needed

\[
OSR = \frac{f_s}{2BW} \gg 1
\]
Delta-Sigma Noise Shaping

- **Simplest** architecture: **first-order** \((N=1)\) **1-bit** \((B=1)\) single-loop DSM

\[
V_{in} \rightarrow S/H \rightarrow \frac{z^{-1}}{1-z^{-1}} \rightarrow \text{comparator} \rightarrow d_{mod}
\]

\[
H(z) = \frac{z^{-1}}{1-z^{-1}}
\]

- **Single-bit feedback DAC is intrinsically linear**
- **Oversampling** is needed
- **Higher order** \((N>1)\) shaping to avoid signal to quantization noise correlation (harmonics)

\[
\begin{align*}
STF &= \frac{H}{1+H} \equiv z^{-1} \quad \text{(delay)} \\
NTF &= \frac{1}{1+H} \equiv 1-z^{-1} \quad \text{(differentiator)}
\end{align*}
\]
Delta-Sigma Noise Shaping

Higher-order \((N)\) noise shaping:

- **Sharper** noise shaping
- **Signal to quantization noise uncorrelation** (continuous spectra)
- **Possibility of loop instability** for \(N>2\)
- **Coefficients** optimization!
DSM ADC Design

- **N-order B-bit** single loop architecture:

- **Multi-bit** quantization:
  - Resolution added to overall DR
  - **Internal full-scale** reduction
  - Feedback DAC **not intrinsically linear**

- **High-order** filtering:
  - Sharper noise shaping
  - Stability issues

**Ideal** dynamic range:

\[
DR = \frac{3\pi}{2} \left(2^B - 1\right)^2 \left(2N + 1\right) \left(\frac{OSR}{\pi}\right)^{2N+1} \text{(N+0.5)-bit/oct(OSR)}
\]

\[
DR[\text{dB}] = 6.7 + 20 \log \left(2^B - 1\right) + 10 \log \left(2N + 1\right) + 20 (N + 0.5) \log \frac{OSR}{\pi}
\]
DSM ADC Design

**Feedforward cancellation:**

- $k_{f1} = 1$
- $V_{in}$
- $V_{in} \rightarrow S/H \rightarrow k_{i1} \rightarrow \frac{z^{-1}}{1-z^{-1}} \rightarrow k_{i2} \rightarrow \frac{z^{-1}}{1-z^{-1}} \rightarrow +\rightarrow \pm V_{fs}$
- $d_{mod}$

**Resonator attenuation:**

- $k_{g1}$
- $V_{in} \rightarrow S/H \rightarrow k_{i1} \rightarrow \frac{z^{-1}}{1-z^{-1}} \rightarrow k_{i2} \rightarrow \frac{z^{-1}}{1-z^{-1}} \rightarrow +\rightarrow \pm V_{fs}$
- $d_{mod}$

- **Internal full scale low occupancy**
- **Additional adder stage in front of quantizer**
- **Extra noise shaping at band edge**
- **Zero sensitivity to coefficient matching**
DSM SC Circuits

**Fully-differential** 2nd-order single-bit example:

\[ k_{i1} = \frac{C_{s1}}{C_{i1}} \quad k_{i2} = \frac{C_{s2}}{C_{i2}} \quad k_{f1} = \frac{C_{f1}}{C_{f2}} = 1 \]
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Voltage-to-Frequency ADC

Building blocks:

- **Voltage-controlled oscillator (VCO)**

Implicit sub-ranging:

\[ f_{VCO} = (2^{MSB} - 1) f_s \ll (2^N - 1) f_s \]
Voltage-to-Frequency ADC

Building blocks:

- **Low frequency** ($f_{\text{coarse}} < < 2^{\text{ENOB}} f_s$), unlike integrating ADCs
- **Low-voltage** operation

- **Non-linearity** $V_{\text{in}} - I_{\text{bias}}$ and $I_{\text{bias}} - f_{\text{VCO}}$
- **Technology sensitivity**