2. ADC Architectures and CMOS Circuits

Francesc Serra Graells

francesc.serra.graells@uab.cat
Departament de Microelectrònica i Sistemes Electrònics
Universitat Autònoma de Barcelona

paco.serra@imb-cnm.csic.es
Integrated Circuits and Systems
IMB-CNM(CSIC)
1. ADC Classification
2. Flash Techniques
3. Sub-Ranging, Time-Interleaving and Pipelining Techniques
4. Successive-Approximation Techniques
5. Integrating Techniques
6. Delta-Sigma Modulation Techniques
7. Time-Domain Techniques
1. ADC Classification

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7. Time-Domain Techniques
ADC Families

Classification based on architecture approach:

- Flash
- Sub-ranging
- Pipeline
- SAR
- Integrating
- Delta-Sigma
- Time-Domain

High speed

High dynamic range

Distinctive characteristics:
- Feedforward vs feedback control
- Single vs multiple stages
- Amplitude vs time domains

Typically mixed solutions...
ADC Evolution

\[ FOM_S = SNDR_{max} + 10 \log \frac{f_{nyq}}{2P_D} \]

\[ FOM_W = \frac{P_D}{f_{nyq} \cdot 2\text{ENOB}} \]

\[ FOM_S \approx 85\text{dB} \]

\[ FOM_W \approx 5\mu\text{J/conv-step} \]

EPSCO DATRAC, B.M. Gordon, 1953

11-bit 50KSps 500W SAR ADC

0.5m x 0.4m x 0.65m, 70Kg

Vacuum tube technology

W. Kester, Analog-Digital Conversion

ADC Evolution

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Vacuum tube technology

W. Kester, Analog-Digital Conversion


State-of-art ADC
Solid-state technologies

B. Murmann, ADC Performance Survey

http://www.stanford.edu/~murmann/adcsurvey.html
2. ADC Architectures and CMOS Circuits

ADC Evolution

Performance enhancement:
- Architecture strategy
- Circuit design
- Integration technology

Still room for further improvement?

\[
SNR_{\text{max}} = \frac{(V_{FS}/2\sqrt{2})^2}{KT/C_s} \frac{f_s}{f_{\text{nyq}}}
\]

\[
P_{\text{min}} = C_s V_{FS} f_s V_{DD} / I_{DD}
\]

\[
P_{\text{min}}|_{V_{FS}=V_{DD}} \simeq C_s f_s V_{FS}^2
\]

\[
E_{\text{min}} = \frac{P_{\text{min}}}{f_{\text{nyq}}} = 8KT \cdot SNR_{\text{max}}
\]
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Basic Flash Architecture

Building blocks: e.g. single-ended 3-bit flash ADC

Threshold generator

$V_{FS} \equiv V_{DD}$

Latched comparator array

$V_{th7}$

$V_{thk}$

$V_{th1}$

Latched comparator array

$T_7$

$T_k$

$T_1$

thermometer code

Digital encoder

natural binary code

$2^{ENOB} - 1$

combinational only logic

$V_{in}$

$V_{out}$

$V_{s}$

$V_{fs}$
2. ADC Architectures and CMOS Circuits

Basic Flash Architecture

Building blocks:
- Threshold generator
- Latched comparator array
- Thermometer code
- Digital encoder

e.g. **single-ended** 3-bit flash ADC

- 1 clock cycle conversion **time**
- Area and power **scaling** by \(2^{ENOB}\)
- Distortion due to technology **mismatching**

\[ V_{in} \rightarrow \text{ADC} \rightarrow d_{out} \]

\[ V_{FS} \equiv V_{DD} \]

\[ V_{th1} \]

\[ V_{thk} \]

\[ V_{th7} \]

\[ t_1 \]

\[ t_k \]

\[ t_7 \]

\[ \times (2^{ENOB} - 1) \]

\[ f_s \]

\[ d_{out} \]
Latched Comparator Design

Compact **CMOS** circuit:

\[
\phi_x = \begin{cases} 
H &: \text{closed} \\
L &: \text{open} 
\end{cases}
\]
Latched Comparator Design

- Compact **CMOS** circuit:

  ![Comparator Diagram]

  **Non-overlapped clock phases**

  \[ \phi_x = \begin{cases} 
  \text{H closed} & \text{if } x = 1 \\
  \text{L open} & \text{if } x = 0 
  \end{cases} \]

  **High-speed operation**

  - Each comparator crosses at **different** threshold \( V_{thk} \)

  **Threshold voltage offset?**

  - Positive feedback to speed-up comparison
  - Symmetrical loading
Comparator Optimization

- By attaching an array of level shifters:

\[ \phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases} \]

\[ t_k = \text{sign} \left[ V_{\text{ref}} - \left( V_{\text{ref}} + \frac{C_{1k}}{C_{1k} + C_{2k}} (V_{\text{ref}} - V_{\text{in}}) + \frac{C_{2k}}{C_{1k} + C_{2k}} (V_{DD} - V_{\text{ref}}) \right) \right] \]
Comparator Optimization

- By attaching an array of **level shifters**:

  ![Comparator Diagram](image)

  - All comparators latch at the **same** level ($V_{\text{ref}}$)
  - **Single** comparator design
  - Low quiescent **power** (resistor-less thresholds)
  - Capacitor **area** overhead
  - Input **capacitance** increased
  - **Slower** operation

  $$ t_k = \text{sign} \left[ V_{\text{ref}} - \left( V_{\text{ref}} + \frac{C_{1k}}{C_{1k} + C_{2k}} (V_{\text{ref}} - V_{\text{in}}) + \frac{C_{2k}}{C_{1k} + C_{2k}} (V_{\text{DD}} - V_{\text{ref}}) \right) \right] $$

  $$ t_k = \text{sign} \left[ \frac{C_{1k}}{C_{1k} + C_{2k}} (V_{\text{in}} - V_{\text{ref}}) - \frac{C_{2k}}{C_{1k}} (V_{\text{DD}} - V_{\text{ref}}) \right] $$

  - Effective signal
  - Effective $k$-threshold
Comparator Optimization

By attaching an array of level shifters:

- Interference rejection
- Full-scale extension (+6dB)
- SNR enhancement (+3dB)
- Distortion cancellation (even harmonics)

\[ \phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases} \]

\[ V_{ref} = \frac{V_{DD}}{2} \]

- Area and power overheads (x2)
- Higher symmetry requirements
Comparators Offset

- **MOSFET $V_{TH}$ mismatching** effects:

\[
\sigma^2(V_{off}) = \sigma^2(\Delta V_{TH1,2}) + \left(\frac{g_{m3,4}}{g_{m1,2}}\right)^2 \sigma^2(\Delta V_{TH3,4})
\]

\[
\sigma(V_{off}) \approx \sigma(\Delta V_{TH1,2}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}
\]

\[
\left(\frac{W}{L}\right)_{1,2} \gg \left(\frac{W}{L}\right)_{3,4}
\]

Pelgrom's Law

\[
\Delta V_{TH}
\]

CMOS technology

Distortion due to **DNL**

- $d_{max}$
- $d_{out}$
- $V_{LSB}$
- $V_{in}$
- $V_{FS}$

\[
DNL + \frac{V_{LSB}}{2}
\]

\[
- \frac{V_{LSB}}{2}
\]
Comparators Offset

Temperature code **bubbles**!

Error propagation at encoding...

\[ \sigma(V_{off}) = \frac{A_{VT}}{\sqrt{WL}} \]

**Large device area** (WL) and input **capacitance** penalties
Comparators Offset

- Thermometer code **bubbles!**

- Digitally assisted analog design:

\[ \sigma(V_{off}) = \frac{A_{VT \text{H}}}{\sqrt{(WL)_{1,2}}} \]
Comparators Offset

- Thermometer code **bubbles**!

- **Digitally assisted** analog design:

\[ \sigma(V_{off}) = \frac{A_{VTH}}{\sqrt{WL}_{1,2}} \]

(WL) large enough to limit bubble **distance** to 1 code:
Comparators Offset

More on digitally assisted analog design: an stochastic flash ADC

---

Comparators Offset

More on digitally assisted analog design: an stochastic flash ADC

![Diagram of digital full-adders]

\[ \sigma(V_{off}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}} \]

- Almost digital
- Compact area
- Non-linearity compensation required
- Power consumption

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Sub-Range Flash ADC

Building blocks:

- **Two-step** coarse-fine data conversion scheme
- **ENOB splitting** can be chosen asymmetric depending on circuits...
Sub-Range Flash ADC

▶ Building blocks:

Coarse stage

Fine stage

- Two-step coarse-fine data conversion scheme
- ENOB splitting can be chosen asymmetric depending on circuits...
- Better ENOB scaling of comparators and passive components!

\[ V_{in} \rightarrow S/H \rightarrow \text{Flash ADC} \rightarrow \text{Flash DAC} \rightarrow \text{Encoder} \rightarrow d_{out} \]

**Speed** reduction (x2)

Non-linearity caused by **mismatching** between coarse ADC-DAC, and between coarse-fine ADC

<table>
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<th>Class</th>
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<th>Pipeline</th>
<th>SAR</th>
<th>Integ</th>
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</table>

\[ V_{in} \rightarrow \text{ADC} \rightarrow d_{out} \]

\[ f_s \]

- e.g. Number of comparators for 8-bit flash ADC:
  - single-stage \( \times (2^{ENOB} - 1) = 255 \propto 2^{ENOB} \div 2^{ENOB} - 1 \)
  - two-stage \( \times 2(2^{ENOB} - 1) = 30 \propto 2^{ENOB} + 1 \)
Sub-Range Flash ADC

**Circuit implementation:**

- **Coarse stage**
- **Fine stage**

\[
\phi = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases}
\]

\[
V_{in} \rightarrow \text{S/H} \rightarrow f_s \rightarrow \text{Flash ADC} \rightarrow \text{Flash DAC} \rightarrow V_{fine} \rightarrow \text{Flash ADC} \rightarrow \text{Encoder} \rightarrow d_{out}
\]

- Non-linearity caused by non-unitary gain in MSB subtraction

**Compact SC implementation:**

- Single-ended version

\[
V_{FS} \equiv V_{DD}
\]
Time-Interleaved Flash ADC

- **Two-step** CMOS comparator:

```
\[ \phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases} \]
```

- **Single-ended version**

- **Offset insensitive!**
- **Compact area**
- **Poor power supply rejection ratio (PSRR)**

\[ \Delta V_{bias} = V_{thk} - V_{in} \]
Time-Interleaved Flash ADC

- **Counter-phase** two-step CMOS comparator:

  - **Offset** insensitive!
  - **Compact** area
  - **Higher speed** (x2)

\[ \phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases} \]

- Poor power supply rejection ratio (PSRR)
- Higher *jitter* sensitivity (both clock edges)
Time-Interleaved Flash ADC

- Extending the same idea to multiple **time-interleaving**:

- Overall equivalent **high-speed** conversion
- Each flash ADC operates at **low-speed** \((1/N)\)

\[ \phi_x = \begin{cases} H & \text{closed} \\ L & \text{open} \end{cases} \]

**Advantages**:
- Large **area** \((xN)\)
- High **latency** \((xN)\)
- Complex **synchronization**
Pipeline ADC

> Combination of **cascaded sub-ranging** and **time-interleaving**: 

![Pipeline ADC Diagram]

Sub-converter functions:
- Sampling and hold (S/H)
- **Sub-range** quantization
- **Residue** computation and scaling
Pipeline ADC

- Combination of **cascaded sub-ranging** and **time-interleaving**:

![Diagram of Pipeline ADC]

- **Simpler** flash sub-ADCs
- **Performance depends on first-stage only**
- **No speed reduction**
- **High latency** ($\times M$)

\[
SNR_{eq} = \frac{S_{in}}{2^{-2p}N_1 + 2^{-2(p+q)}N_2 + \ldots + 2^{-2(p+q+\ldots+r)}N_M}
\]
Pipeline ADC

Simple 1-bit stage case study:

\[ V_{in} \rightarrow \text{Stage 1} \rightarrow \text{Stage 2} \rightarrow \cdots \rightarrow \text{Stage M} \]

\[ d_{MSB} \rightarrow d_{MSB-1} \rightarrow d_{LSB} \]

Time Alignment

M \rightarrow d_{out}

SC implementation of each stage:

\[ V_{out} = 2 \left( V_{in} - V_{ref} + (-1)^{d_k} \frac{V_{FS}}{4} \right) + V_{ref} \]
Pipeline ADC

Simple 1-bit stage case study:

\[
\begin{align*}
V_{in} &\rightarrow \text{Stage 1} \rightarrow \text{Stage 2} \rightarrow \text{Stage M} \\
&\downarrow d_{MSB} \downarrow d_{MSB-1} \downarrow d_{LSB} \\
&\text{Time Alignment} \\
&\rightarrow M \rightarrow d_{out}
\end{align*}
\]

SC implementation of each stage:

\[
\begin{align*}
\phi_1 & \text{ sampling + quantization (1)} \\
\phi_2 & \text{ residue (>0) + scaling}
\end{align*}
\]

\[
V_{out} = V_{in} - \frac{C_s}{C_f} \left( V_{ref} + \left( -1 \right)^{\frac{d_k}{2}} \frac{V_{FS}}{2} - V_{in} \right)
\]
### Pipeline ADC

- **Simple 1-bit stage** case study:

\[
V_{out} = V_{in} - \frac{C_s}{C_f} \left( V_{ref} + (-1)^d \frac{V_{FS}}{2} - V_{in} \right)
\]

\[
V_{out} = 2 \left( V_{in} - V_{ref} + (-1)^d \frac{V_{FS}}{4} \right) + V_{ref}
\]

\[C_f \equiv C_s\]

- **Single-ended version**

- **Simplest** flash sub-ADCs

- **Inherently linear** single bit quantization

- **Noise** contributions from stage 2 → **multi-bit** first stage

- **Offset** sensitivity
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Successive Approximation ADC

Building blocks:

- **S/H** (Sample and Hold)
- **V_{in}**
- **V_{res}**
- **f_s**
- **N_{fs}**
- **N**
- **d_{out}**
- **V_dac**
- **V_{ref}**
- **Flash DAC**
- **N-bit**
- **digital state-machine (algorithm)**
- **residue**
- **Successive Approximation Register (SAR)**
Successive Approximation ADC

- **Building blocks:**

  - Successive Approximation Register (SAR)
  - Flash DAC
  - S/H
  - Analog minimalist
  - Very low-power consumption
  - Speed requirements \( \times N \)
  - Performance limited by flash DAC

\[
V_{in} \xrightarrow{\text{S/H}} V_{res} \xrightarrow{\text{digital state-machine (algorithm)}} d_{out}
\]
Successive Approximation ADC

**Circuit implementation:**

\[ V_{res} = V_{in} + V_{off} - \left( \frac{d_{MSB}}{2} + \frac{d_{MSB}}{4} + \cdots + \frac{d_{LSB}}{2^N} \right) V_{ref} \]

\[ V_{FS} \equiv 2V_{ref} \text{ single-ended version} \]
Successive Approximation ADC

**Circuit implementation:**

\[ V_{res} = V_{in} + V_{off} - \left( \frac{d_{MSB}}{2} + \frac{d_{MSB}}{4} + \cdots + \frac{d_{LSB}}{2^N} \right) V_{ref} \]

where:

- \( V_{res} \) is the voltage at the output of the comparator.
- \( V_{in} \) is the input voltage.
- \( V_{off} \) is the offset voltage of the comparator.
- \( d_{MSB}, d_{MSB-1}, \ldots, d_{LSB} \) are the bits represented by the comparator.
- \( V_{ref} \) is the reference voltage.

The circuit consists of:

- **S/H** (Sample and Hold) circuit.
- **Flash DAC** (Digital-to-Analog Converter).
- **Successive Approximation Register (SAR)**

The SAR register is updated at each clock cycle, with the bit values being shifted to the right. The output bit values are connected to the comparator, which determines the next bit to be shifted. The process continues until all bits have been shifted out.

The clock signal drives the SAR, controlling the bit shifting process. The output of the SAR is a binary representation of the input voltage, which is then converted to a digital signal.

The circuit also includes a feedback loop to maintain the signal baseline, ensuring accurate measurement of the input voltage.

\[ \phi_x = \begin{cases} H & \text{closed} \\ L & \text{open} \end{cases} \]

The clock signal drives the SAR, controlling the bit shifting process. The output of the SAR is a binary representation of the input voltage, which is then converted to a digital signal.

The circuit also includes a feedback loop to maintain the signal baseline, ensuring accurate measurement of the input voltage.

The output of the SAR is connected to the comparator, which determines the next bit to be shifted. The process continues until all bits have been shifted out.

The feedback loop ensures that the signal baseline is maintained, allowing for accurate measurement of the input voltage.
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Single-Slope ADC

**Building blocks:**

\[ V_{in} \rightarrow \text{S/H} \]

\[ \phi_{init} \]

\[ f_s \]

\[ -V_{ref} \rightarrow \text{op amp} \]

\[ V_{ramp} \]

\[ \phi_{init} \]

\[ \phi_{pwm} \]

\[ R \]

\[ C \]

\[ t_{pwm} = RC \frac{V_{in}}{V_{ref}} \]

\[ d_{out} = t_{pwm} f_{clk} = (2^N - 1) f_s RC \frac{V_{in}}{V_{ref}} \]

\[ \phi_x = \begin{cases} H & \text{closed} \\ L & \text{open} \end{cases} \]

\[ V_{in} \rightarrow \text{ADC} \]

\[ d_{out} \]

\[ f_{clk} = (2^N - 1) f_s \]

**Pulse-width modulation (PWM):**

\[ \text{clock} \]

\[ \phi_{init} \]

\[ \phi_{pwm} \]

\[ V_{ramp} \]

\[ V_{ref} \]

\[ \frac{V_{ref}}{RC} \]

\[ V_{in} \]

\[ 1/f_s \]

\[ t_{pwm} \]

\[ \text{time} \]
Single-Slope ADC

Building blocks:

- Analog minimalist
- Very low-power

\[ t_{\text{pwm}} = RC \frac{V_{\text{in}}}{V_{\text{ref}}} \]

\[ d_{\text{out}} = t_{\text{pwm}} f_{\text{clk}} = (2^N - 1) f_s \frac{RC}{V_{\text{ref}}} \frac{V_{\text{in}}}{V_{\text{ref}}} \]

- Speed requirements \((x 2^N)\)
- Technological sensitivity \((RC)\)
Dual-Slope ADC

Building blocks:

\[ V_{in} \equiv \frac{t_1}{t_2} V_{ref} \]

\[ d_{out} = \frac{d_1}{d_2} \propto \frac{V_{in}}{V_{ref}} \]

- Analog minimalist
- Very low-power
- Speed requirements \((x2^N)\)
- Technology independence \((RC)\)
Integrate-and-Fire ADC

Building blocks:

\[ d_{out} = \frac{1}{f_s} = \frac{I_{in}}{CV_{th}f_s} \]

▲ Current-mode sensors (e.g. imagers)
▲ Very low-power
▲ Speed requirements adapted to signal
▼ Technology sensitivity (C)

\[ \phi_x = \begin{cases} H & \text{closed} \\ L & \text{open} \end{cases} \]

Asynchronous counter

pulse-density modulation (PDM)
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Delta-Sigma Modulator ADC

- General **single-loop DSM** architecture:
Delta-Sigma Modulator ADC

- General single-loop DSM architecture:

  ![Diagram of Delta-Sigma Modulator ADC]

- Noise-shaper filter:
  - In-band high-gain
  - Either continuous- \( H(s) \) or discrete-time \( H(z) \)

- Flash ADC and DAC blocks can be relaxed!

- DSM signal vs quantization noise behavior?

\[
\begin{align*}
\text{STF} &= \frac{H}{1+H} \\
\text{NTF} &= \frac{1}{1+H}
\end{align*}
\]

\( H \to \infty \) \( \to 1 \)

\( H \to \infty \) \( \to 0 \)
Delta-Sigma Noise Shaping

- **Simplest** architecture: **first-order** \((N=1)\) **1-bit** \((B=1)\) single-loop DSM

![Diagram of first-order Delta-Sigma modulator]

- Single-bit feedback DAC is **intrinsically linear**

\[
V_{in} \rightarrow S/H \rightarrow \frac{z^{-1}}{1-z^{-1}} \rightarrow \text{int} \rightarrow \text{comparator} \rightarrow d_{mod}
\]

\[
\pm V_f \rightarrow \text{S/H} \rightarrow \text{int} \rightarrow d_{mod}
\]
Delta-Sigma Noise Shaping

**Simplest** architecture: first-order \((N=1)\) 1-bit \((B=1)\) single-loop DSM

\[
H(z) = \frac{z^{-1}}{1 - z^{-1}}
\]

\[
\begin{align*}
STF &= \frac{H}{1 + H} \equiv z^{-1} \\
NTF &= \frac{1}{1 + H} \equiv 1 - z^{-1}
\end{align*}
\]

- Single-bit feedback DAC is **intrinsically linear**
- **Oversampling** is needed

\[
OSR = \frac{f_s}{2BW} \gg 1
\]
Delta-Sigma Noise Shaping

**Simplest** architecture: **first-order** \((N=1)\) **1-bit** \((B=1)\) single-loop DSM

\[
H(z) = \frac{z^{-1}}{1 - z^{-1}}
\]

\[
\begin{align*}
STF &= \frac{H}{1 + H} \equiv z^{-1} \\
NTF &= \frac{1}{1 + H} \equiv 1 - z^{-1}
\end{align*}
\]

- **Single-bit feedback DAC is intrinsically linear**
- **Oversampling** is needed
- Higher order \((N>1)\) shaping to avoid signal to quantization noise correlation (harmonics)
Delta-Sigma Noise Shaping

▲ **Higher-order** \((N)\) noise shaping:

\[
\begin{align*}
V_{in} & \xrightarrow{S/H} k_1 \xrightarrow{S/H} k_2 \xrightarrow{\text{integrators}} d_{mod}
\end{align*}
\]

- **First integrator**:
  - Gain coefficients
  - Possibility of loop instability for \(N > 2\)

- **Second integrator**:
  - Signal to quantization noise uncorrelation (continuous spectra)

▲ **Sharper** noise shaping

▲ **Signal to quantization noise uncorrelation** (continuous spectra)

▼ **Possibility of loop instability** for \(N > 2\)

▲ **Coefficients** optimization!

![Graph showing log(power) vs log(frequency) and BW vs fs/2 with 40dB/dec slope](image-url)
DSM ADC Design

- **N-order B-bit** single loop architecture:

  - **multi-bit (B) quantization**

  \[ V_{in} \rightarrow S/H \rightarrow H(z) \rightarrow d_{mod} \]

  \[ f_s \]

- **Ideal** dynamic range:

  \[
  DR = \frac{3\pi}{2} (2^B - 1)^2 (2N + 1) \left( \frac{OSR}{\pi} \right)^{2N+1}
  \]

  \[
  DR[\text{dB}] = 6.7 + 20 \log \left( 2^B - 1 \right) + 10 \log (2N + 1) + 20 \left( N + 0.5 \right) \log \frac{OSR}{\pi}
  \]

- **Multi-bit** quantization:

  - Resolution added to overall DR
  - Internal full-scale reduction
  - Feedback DAC **not intrinsically linear**

- **High-order** filtering:

  - **Sharper** noise shaping
  - **Stability** issues

```
DR = \frac{3\pi}{2} (2^B - 1)^2 (2N + 1) \left( \frac{OSR}{\pi} \right)^{2N+1}

DR[\text{dB}] = 6.7 + 20 \log \left( 2^B - 1 \right) + 10 \log (2N + 1) + 20 \left( N + 0.5 \right) \log \frac{OSR}{\pi}
```
DSM ADC Design

- **Feedforward cancellation:**

  
  ![Feedforward cancellation diagram]

  - Internal full scale
  - Low occupancy

- **Resonator attenuation:**

  
  ![Resonator attenuation diagram]

  - Extra noise shaping at band edge
  - Zero sensitivity to coefficient matching
DSM SC Circuits

- **Fully-differential** 2nd-order single-bit example:

![DSM SC Circuits Diagram]

\[
k_{i1} = \frac{C_{s1}}{C_{i1}} \quad k_{i2} = \frac{C_{s2}}{C_{i2}} \quad k_{f1} = \frac{C_{f1}}{C_{f2}} = 1
\]
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3. Sub-Ranging, Time-Interleaving and Pipelining Techniques

4. Successive-Approximation Techniques

5. Integrating Techniques

6. Delta-Sigma Modulation Techniques

7. Time-Domain Techniques
Voltage-to-Frequency ADC

Building blocks:

- Voltage-controlled oscillator (VCO)
- Coarse counter
- Encoder

[Diagram showing the components of the Voltage-to-Frequency ADC]
Voltage-to-Frequency ADC

- **Building blocks:**
  - Voltage-controlled oscillator (VCO)
  - coarse counter
  - fine register
  - encoder

- **All-MOS circuit implementation**
- **Low-voltage operation**
- **Non-linearity** $V_{in} - I_{bias}$ and $I_{bias} - f_{VCO}$
- **Technology sensitivity**

**ADC Architectures and CMOS Circuits**