2. ADC Architectures and CMOS Circuits

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1. ADC Classification
2. Flash Techniques
3. Sub-Ranging, Time-Interleaving and Pipelining Techniques
4. Successive-Approximation Techniques
5. Integrating Techniques
6. Delta-Sigma Modulation Techniques
7. Time-Domain Techniques
1. ADC Classification

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ADC Families

- Classification based on **architecture** approach:
  - Flash
  - Sub-ranging
  - Pipeline
  - SAR
  - Integrating
  - Delta-Sigma
  - Time-Domain
  - High speed
  - High dynamic range

- Distinctive **characteristics**:
  - Feedforward vs feedback control
  - Single vs multiple stages
  - Amplitude vs time domains

- Typically **mixed** solutions...
ADC Evolution

\[ FOM_S = SNDR_{max} + 10 \log \frac{f_{nyq}}{2P_D} \]

\[ FOM_W = \frac{P_D}{f_{nyq} \cdot 2^{\text{ENOB}}} \]

\[ FOM_S \approx 85\text{dB} \]

\[ FOM_W \approx 5\mu\text{J/conv-step} \]

EPSCO DATRAC, B.M. Gordon, 1953

11-bit 50kSps 500W SAR ADC

0.5m x 0.4m x 0.65m, 70kg

Vacuum tube technology

W. Kester, Analog-Digital Conversion

ADC Evolution

\[ FOM_S = SNDR_{max} + 10 \log \frac{f_{nyq}}{2P_D} \]
\[ FOM_W = \frac{P_D}{f_{nyq} \cdot 2^{\text{ENOB}}} \]

\[ FOM_S \simeq 85\text{dB} \]
\[ FOM_W \simeq 5\mu\text{J/conv-step} \]

+60years

State-of-art ADC
Solid-state technologies

B. Murmann, *ADC Performance Survey*

http://www.stanford.edu/~murmann/adcsurvey.html

EPSCO DATRAC, B.M. Gordon, 1953
11-bit 50kSps 500W SAR ADC
0.5m x 0.4m x 0.65m, 70kg
Vacuum tube technology

W. Kester, *Analog-Digital Conversion*


170dB

10fJ/conv-step

11-bit

ADC Evolution

▶ **Performance** enhancement:
  - Architecture strategy
  - Circuit design
  - Integration technology

▶ Still room for further improvement?

\[
SNR_{\text{max}} = \frac{(V_{FS}/2\sqrt{2})^2}{KT/C_s} \frac{f_s}{f_{nyq}}
\]

\[
P_{\text{min}} = C_s V_{FS} f_s V_{DD} I_{DD}
\]

\[
P_{\text{min}}|_{V_{FS} = V_{DD}} \simeq C_s f_s V_{FS}^2
\]

\[
E_{\text{min}} = \frac{P_{\text{min}}}{f_{nyq}} \equiv 8KT SNR_{\text{max}}
\]
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Basic Flash Architecture

Building blocks:

- Threshold generator
- Latched comparator array
- Thermometer code
- Digital encoder

Threshold generator:

\[ V_{FS} = V_{DD} \]

Latched comparator array:

- \( V_{th1} \)
- \( V_{thk} \)
- \( V_{th7} \)

Thermometer code:

\[ t_1 \times (2^{ENOB} - 1) \]

Digital encoder:

\[ d_{out} \]

Example single-ended 3-bit flash ADC
Basic Flash Architecture

- **Building blocks:**

  - **Threshold generator:** $V_{FS} = V_{DD}$
  - **Latched comparator array:** $V_{th_1}$, $V_{th_k}$, $V_{th_7}$
  - **thermometer code**

- **Conversion time:** 1 clock cycle

- **Area and power scaling:** by $2^{ENOB}$

- **Distortion due to technology mismatching**

- **Examples:** single-ended 3-bit flash ADC

- **Digital encoder**
  - Natural binary code
  - $d_{out}$
  - $f_s$
Latched Comparator Design

- Compact CMOS circuit:

\[ \phi_x = \begin{cases} 
  \text{H closed} & \text{clock phases} \\
  \text{L open} & \text{non-overlapped} 
\end{cases} \]

\[ \frac{1}{f_s} \]

\[ t_k \rightarrow V_{in} \rightarrow M1 \rightarrow M2 \rightarrow V_{thk} \]

\[ \phi_1 \quad M3 \quad \phi_2 \quad M4 \quad \phi_1 \]

\[ \phi_2 \]

\[ t_k \rightarrow \bar{t}_{k} \]
Latched Comparator Design

▶ Compact CMOS circuit:

Non-overlapped clock phases

\[ \phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases} \]

Clock phases

Pre-charging phase

Decision phase

High-speed operation

Each comparator crosses at different threshold \( V_{thk} \)

Threshold voltage offset?

Positive feedback to speed-up comparison

Symmetrical loading
Comparator Optimization

- By attaching an array of level shifters:

\[ t_k = \text{sign} \left[ V_{\text{ref}} - \left( V_{\text{ref}} + \frac{C_{1k}}{C_{1k} + C_{2k}} (V_{\text{ref}} - V_{\text{in}}) + \frac{C_{2k}}{C_{1k} + C_{2k}} (V_{\text{DD}} - V_{\text{ref}}) \right) \right] \]
Comparator Optimization

- By attaching an array of level shifters:

- All comparators latch at the same level ($V_{\text{ref}}$)
- Single comparator design
- Low quiescent power (resistor-less thresholds)
- Capacitor area overhead
- Input capacitance increased
- Slower operation

\[
\phi_x = \begin{cases} 
H & \text{closed} \\
L & \text{open} 
\end{cases}
\]

\[
t_k = \frac{C_{1k}}{C_{1k} + C_{2k}} \text{sign} \left[ (V_{\text{in}} - V_{\text{ref}}) - \frac{C_{2k}}{C_{1k}} (V_{\text{DD}} - V_{\text{ref}}) \right]
\]

\[
t_k = \text{sign} \left[ V_{\text{ref}} - \left( V_{\text{ref}} + \frac{C_{1k}}{C_{1k} + C_{2k}} (V_{\text{ref}} - V_{\text{in}}) + \frac{C_{2k}}{C_{1k} + C_{2k}} (V_{\text{DD}} - V_{\text{ref}}) \right) \right]
\]
Comparator Optimization

- By attaching an array of **level shifters**: 
  
  ![Comparator Diagram](image)

  - **Interference rejection**
  - **Full-scale extension** (+6dB)
  - **SNR enhancement** (+3dB)
  - **Distortion cancellation** (even harmonics)

- **Area** and **power** overheads (x2)

- **Higher symmetry** requirements

\[
V_{ref} = \frac{V_{DD}}{2}
\]

\[
V_{ind} = V_{inp} - V_{inn}
\]
Comparators Offset

- MOSFET $V_{TH}$ mismatching effects:

$$\sigma^2(V_{off}) = \sigma^2(\Delta V_{TH1,2}) + \left(\frac{g_{mg3,4}}{g_{mg1,2}}\right)^2 \sigma^2(\Delta V_{TH3,4})$$

$$\sigma(V_{off}) \approx \sigma(\Delta V_{TH1,2}) = \frac{A_{VT\text{H}}}{\sqrt{(WL)_{1,2}}}$$

$\left(\frac{W}{L}\right)_{1,2} \gg \left(\frac{W}{L}\right)_{3,4}$

Pelgrom's Law

\[\text{CMOS technology}\]

- Distortion due to DNL

\[\text{Pelgrom's Law}\]
Comparators Offset

Thermometer code **bubbles!**

Error propagation at encoding...

Latched comparator array

![Diagram of latched comparator array with thermometer code bubbles and Gaussian probability distribution](image)

$$\sigma(V_{off}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$$

**Large device area** (WL) and input **capacitance** penalties
Comparators Offset

- Thermometer code **bubbles**!

- **Digitally assisted** analog design:

\[ \sigma(V_{off}) = \frac{A_{VTH}}{\sqrt{WL}_{1,2}} \]
Comparators Offset

- Thermometer code **bubbles!**
- *Digitally assisted* analog design:

\[
\sigma(V_{off}) = \frac{A_{VT_H}}{\sqrt{(WL)_{1,2}}}
\]

(WL) large enough to limit bubble **distance** to 1 code:
Comparators Offset

More on digitally assisted analog design: an stochastic flash ADC

Comparators Offset

More on digitally assisted analog design: an stochastic flash ADC

\[ \sigma(V_{off}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}} \]

- Almost digital
- Compact area
- Non-linearity compensation required
- Power consumption

\[ \frac{V_{inp} - V_{inn}}{\sigma(V_{off})} \]

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Sub-Range Flash ADC

Building blocks:

Two-step coarse-fine data conversion scheme

ENOB splitting can be chosen asymmetric depending on circuits...
Sub-Range Flash ADC

Building blocks:

- **Coarse stage**
  - Flash ADC
  - ENOB/2 bit
  - MSB

- **Fine stage**
  - Flash DAC
  - ENOB/2 bit
  - LSB

- Encoder

- **Encoder output**: $d_{out}$

- **Input voltage**: $V_{in}$

- **Sampling frequency**: $f_s$

**Speed reduction** (x2)

**Non-linearity caused by mismatching** between coarse ADC-DAC, and between coarse-fine ADC

**Two-step** coarse-fine data conversion scheme

**ENOB splitting** can be chosen asymmetric depending on circuits...

**Better ENOB scaling** of comparators and passive components!

e.g. Number of comparators for 8-bit flash ADC:

- Single-stage: $\times (2^{ENOB} - 1) = 255 \propto 2^{ENOB}

- Two-stage: $\times 2(2^{ENOB} - 1) = 30 \propto 2^{ENOB + 1}$

\[ \frac{2^{ENOB}}{2} - 1 \]
Sub-Range Flash ADC

**Circuit implementation:**

- **S/H**
  - $V_{in}$
  - $f_s$

- **Flash ADC**
  - ENOB/2 bit

- **Flash DAC**
  - ENOB/2 bit

- **Coarse stage**
  - $1/f_s$
  - coarse
  - fine

- **Fine stage**
  - $V_{fine}$

- **Encoder**
  - $d_{out}$

- **Clocks**
  - $\phi_1$
  - $\phi_2$

**Compact SC implementation:**

- **Single-ended version**
  - $V_{in}$
  - $V_{ref}$
  - $V_{FS} \equiv V_{DD}$

**Non-linearity caused by non-unitary gain in MSB subtraction**

- **Non-linearity**
  - caused by non-unitary gain in MSB subtraction

- **Encoder**
  - $d_{MSB}$
  - $d_{MSB-1}$
Time-Interleaved Flash ADC

**Two-step** CMOS comparator:

- **φ₁** sampling + auto-zero
- **φ₂** subtraction + quantization

- Analog inverter-based
- Offset insensitive!
- Compact area
- Poor power supply rejection ratio (PSRR)

\[ \Delta V_{\text{bias}} = V_{\text{thk}} - V_{\text{in}} \]
Time-Interleaved Flash ADC

- **Counter-phase** two-step CMOS comparator:

  - **Offset** insensitive!
  - **Compact area**
  - **Higher speed** (x2)

  \[ \phi_x = \begin{cases} 
  H & \text{closed} \\
  L & \text{open} 
  \end{cases} \]

  - Poor power supply rejection ratio (PSRR)
  - Higher jitter sensitivity (both clock edges)
Time-Interleaved Flash ADC

- Extending the same idea to multiple **time-interleaving**:

![Time-Interleaved Flash ADC Diagram]

- Overall equivalent **high-speed** conversion
- Each flash ADC operates at **low-speed** (1/N)

- Large **area** (xN)
- High **latency** (xN)
- Complex **synchronization**
Pipeline ADC

- Combination of **cascaded sub-ranging** and **time-interleaving**:

- **Stage 1**
  - p-bit
  - MSB
  - Time Alignment
  - LSB

- **Stage 2**
  - q-bit
  - Time Alignment

- **Stage M**
  - r-bit
  - Time Alignment

Sub-converter functions:
- Sampling and hold (S/H)
- **Sub-range** quantization
- **Residue** computation and scaling
Pipeline ADC

► Combination of **cascaded sub-ranging** and **time-interleaving**:

![Diagram of Pipeline ADC](image)

- **Stage 1**: 2^-p, p-bit
- **Stage 2**: 2^-q, q-bit
- **Stage M**: r-bit

**Performance** depends on the **first-stage only**.

- **Simpler** flash sub-ADCs
- **No speed reduction**
- **High latency** (xM)

**SNR eq** = \( \frac{S_{in}}{2^{-2pN_1} + 2^{-2(p+q)N_2} + \ldots + 2^{-2(p+q+r)N_M}} \)
Pipeline ADC

Simple 1-bit stage case study:

\[
V_{out} = 2 \left( V_{in} - V_{ref} + (-1)^{d_k} \frac{V_{FS}}{4} \right) + V_{ref}
\]

SC implementation of each stage:

![Diagram of single-ended version](image)
Pipeline ADC

► Simple 1-bit stage case study:

\[ V_{in} \rightarrow \text{Stage 1} \rightarrow \text{Stage 2} \rightarrow \text{Stage M} \]

\[ d_{MSB} \rightarrow d_{MSB-1} \rightarrow d_{LSB} \]

Time Alignment

\[ M \rightarrow d_{out} \]

**SC implementation** of each stage:

\[ \phi_1 \text{ sampling + quantization (1)} \]

\[ \phi_2 \text{ residue (>0) + scaling} \]

\[ V_{out} = V_{in} - \frac{C_s}{C_f} \left( V_{ref} + (-1)^{d_k} \frac{V_{FS}}{2} - V_{in} \right) \]
Pipeline ADC

Simple 1-bit stage case study:

\[ V_{out} = V_{in} - \frac{C_s}{C_f} \left( V_{ref} + (-1)^{d_{MSB}} \frac{V_{FS}}{2} - V_{in} \right) \]

\[ V_{out} = 2 \left( V_{in} - V_{ref} + (-1)^{d_k} \frac{V_{FS}}{4} \right) + V_{ref} \]

\[ C_f \equiv C_s \]

- **Simplest** flash sub-ADCs
- **Inherently linear** single bit quantization
- **Noise** contributions from stage 2 \( \rightarrow \) **multi-bit** first stage
- **Offset** sensitivity
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Successive Approximation ADC

Building blocks:

- **S/H**
- **Flash DAC**
- **Successive Approximation Register (SAR)**

- **V_{in}**
- **V_{res}**
- **V_{dac}**
- **N**
- **d_{out}**

Digital state-machine (algorithm)
Successive Approximation ADC

- Building blocks:

  - S/H
  - Flash
  - DAC
  - Successive Approximation Register (SAR)

  - residue
  - digital state-machine (algorithm)

- Analog **minimalist**
- Very **low-power** consumption
- Speed requirements (xN)
- Performance limited by **flash DAC**

---

E.g. 4-bit SAR ADC

- $V_{in} \rightarrow \text{ADC} \rightarrow d_{out}$
- $f_s$
- $Nf_s$
- $d_{out} = 1011$
- $V_{FS}$
- $V_{d_{out}}$
- $d_{out}$
- $V_{F_S}$
- $1/Nf_s$
- $V_{in}$
- $d_{out}$
- $0$
- MSB
- LSB
- time
- $d_3$, $d_2$, $d_1$, $d_0$
Successive Approximation ADC

Circuit implementation:

\[ V_{\text{in}} \rightarrow S/H \rightarrow V_{\text{res}} \rightarrow + \rightarrow \text{Successive Approximation Register (SAR)} \rightarrow \text{Flash DAC} \rightarrow N\text{-bit} \rightarrow d_{\text{out}} \]

\[ V_{\text{FS}} \equiv 2V_{\text{ref}} \text{ single-ended version} \]

\[ \phi_x = \begin{cases} H & \text{closed} \\ L & \text{open} \end{cases} \]

\[ \frac{1}{Nf_s} \]

\[ \phi_{\text{init}} \]

\[ V_{\text{res}} \]

\[ V_{\text{ref}} \]

\[ \phi_1 \]

\[ \bar{d}_{\text{MSB}} \quad \bar{d}_{\text{MSB}-1} \quad \ldots \quad \bar{d}_{\text{LSB}} \]

\[ \tilde{d}_{\text{MSB}} \quad \tilde{d}_{\text{MSB}-1} \quad \ldots \quad \tilde{d}_{\text{LSB}} \]
Successive Approximation ADC

Circuit implementation:

\[ V_{in} \rightarrow S/H \rightarrow V_{res} \rightarrow + \rightarrow \text{Successive Approximation Register (SAR)} \rightarrow V_{dac} \rightarrow N_{fs} \rightarrow d_{out} \]

\[ V_{FS} \equiv 2V_{ref} \quad \text{single-ended version} \]

\[ \phi_x = \begin{cases} H & \text{closed} \\ L & \text{open} \end{cases} \]

\[ 1/N_{fs} \quad \text{clock} \]

\[ \phi_1 \]

\[ d_{MSB} \]

\[ d_{MSB-1} \]

\[ d_{LSB} \]

\[ d_{LSB} \]

\[ V_{in} \rightarrow \frac{C_s}{2} \quad \frac{C_s}{4} \quad \ldots \quad \frac{C_s}{2^N} \quad \frac{C_s}{2^N} \rightarrow + \rightarrow V_{ref} \rightarrow \text{to SAR} \]

signal baseline

\[ V_{ref} \]

\[ V_{off} \]

\[ C_{off} \]
Successive Approximation ADC

Circuit implementation:

\[ V_{in} \xrightarrow{S/H} V_{res} \rightarrow \int (C_{s} + \sum_{i=1}^{N} \frac{C_{s}}{2^i}) \Rightarrow \] 

\[ V_{dac} \rightarrow V_{out} \]

\[ \frac{C_{s}}{2^N} + \sum_{i=1}^{N} \frac{C_{s}}{2^i} \equiv C_{s} \]
Successive Approximation ADC

Circuit implementation:

\[ V_{res} = V_{in} - V_{off} + \left[ \frac{(-1)^{d_{MSB}}}{2} + \frac{(-1)^{d_{MSB-1}}}{4} + \cdots + \frac{(-1)^{d_{LSB}}}{2^N} \right] V_{ref} \]

\[ \frac{C_s}{2^N} + \sum_{i=1}^{N} \frac{C_s}{2^i} = C_s \]

\[ V_{FS} \equiv 2V_{ref} \text{ single-ended version} \]
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2. ADC Architectures and CMOS Circuits

Single-Slope ADC

Building blocks:

\[ d_{out} = t_{pwm} f_{clk} = (2^N - 1) f_s RC \frac{V_{in}}{V_{ref}} \]

\[ t_{pwm} = RC \frac{V_{in}}{V_{ref}} \]

\[ f_{clk} = (2^N - 1) f_s \]
Single-Slope ADC

Building blocks:

- Analog minimalist
- Very low-power
- Speed requirements \((x2^N)\)
- Technological sensitivity \((RC)\)

\[ d_{out} = t_{pwm} f_{clk} = (2^N - 1)f_s RC \frac{V_{in}}{V_{ref}} \]

\[ t_{pwm} = RC \frac{V_{in}}{V_{ref}} \]
Dual-Slope ADC

- Building blocks:

  ![Diagram of Dual-Slope ADC]

  \[ V_{in} \equiv \frac{t_1}{t_2} V_{ref} \]

  \[ d_{out} = \frac{d_1}{d_2} \propto \frac{V_{in}}{V_{ref}} \]

- Analog minimalist
- Very low-power
- Speed requirements \((x2^N)\)
- Technology independence (RC)
Integrate-and-Fire ADC

Building blocks:

\[
d_{\text{out}} = \frac{1}{f_s} = \frac{I_{\text{in}}}{C V_{\text{th}} f_s}
\]

▲ Current-mode sensors (e.g. imagers)

▲ Very low-power

▲ Speed requirements adapted to signal

▼ Technology sensitivity (C)
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Delta-Sigma Modulator ADC

- General single-loop DSM architecture:

![Diagram of Delta-Sigma Modulator ADC]
**Delta-Sigma Modulator ADC**

- General *single-loop DSM* architecture:

  ![Diagram of Delta-Sigma Modulator ADC](image)

- **Noise-shaper filter:**
  - In-band *high-gain*
  - Either continuous- $H(s)$ or discrete-time $H(z)$

- Flash ADC and DAC blocks can be relaxed!

**DSM signal vs quantization noise behavior?**

\[
\begin{align*}
STF &= \frac{H}{1 + H} \\
NTF &= \frac{1}{1 + H}
\end{align*}
\]
Delta-Sigma Noise Shaping

- **Simplest** architecture: **first-order** \((N=1)\) **1-bit** \((B=1)\) single-loop DSM

![Diagram of Delta-Sigma Noise Shaping]

- Single-bit feedback DAC is **intrinsically linear**
Delta-Sigma Noise Shaping

**Simplest** architecture: **first-order** \((N=1)\) **1-bit** \((B=1)\) single-loop DSM

\[
H(z) = \frac{z^{-1}}{1 - z^{-1}}
\]

\[
STF = \frac{H}{1 + H} \equiv z^{-1} \quad (delay)
\]

\[
NTF = \frac{1}{1 + H} \equiv 1 - z^{-1} \quad (differentiator)
\]

\(\text{Oversampling} \) is needed

\(\text{Single-bit feedback DAC is intrinsically linear} \)

\(\text{20dB/dec} \)
## Delta-Sigma Noise Shaping

**Simplest architecture:** first-order \((N=1)\) 1-bit \((B=1)\) single-loop DSM

\[
H(z) = \frac{z^{-1}}{1 - z^{-1}}
\]

\[
\begin{align*}
STF &= \frac{H}{1 + H} \equiv z^{-1} & \text{(delay)} \\
NTF &= \frac{1}{1 + H} \equiv 1 - z^{-1} & \text{(differentiator)}
\end{align*}
\]

- Single-bit feedback DAC is **intrinsically linear**
- **Oversampling** is needed
- Higher order \((N>1)\) shaping to avoid signal to quantization noise correlation (harmonics)
Delta-Sigma Noise Shaping

- **Higher-order** \((N)\) noise shaping:

\[
\begin{align*}
V_{in} &\rightarrow \text{S/H} & k_{i1} &\rightarrow \frac{z^{-1}}{1-z^{-1}} & k_{i2} &\rightarrow \frac{z^{-1}}{1-z^{-1}} & \square &\rightarrow d_{mod} \\
& & f_s & & & & & \\
\end{align*}
\]

- **Sharper** noise shaping

- **Signal to quantization noise uncorrelation** (continuous spectra)

- **Possibility of loop instability** for \(N>2\)

- **Coefficients** optimization!
DSM ADC Design

**N-order B-bit** single loop architecture:

- Multi-bit (B) quantization

\[ V_{\text{in}} \rightarrow S/H \rightarrow H(z) \rightarrow d_{\text{mod}} \rightarrow f_s \]

**Ideal** dynamic range:

\[ DR = \frac{3\pi}{2} (2^B - 1)^2 (2N + 1) \left( \frac{OSR}{\pi} \right)^{2N+1} \]

\[ DR[\text{dB}] = 6.7 + 20 \log(2^B - 1) + 10 \log(2N + 1) + 20 (N + 0.5) \log \frac{OSR}{\pi} \]

**Multi-bit** quantization:

- Resolution added to overall DR
- Internal full-scale reduction
- Feedback DAC not intrinsically linear

**High-order** filtering:

- Sharper noise shaping
- Stability issues
DSM ADC Design

**Feedfoward** cancellation:

-\[ k_{f1} \equiv 1 \]

\[ V_{in} \]

\[ \pm V_{f_s} \]

\[ d_{mod} \]

**Resonator** attenuation:

\[ k_{g1} \]

\[ V_{err} \]

\[ \text{Extra noise shaping at band edge} \]

\[ \text{Zero sensitivity to coefficient matching} \]
DSM SC Circuits

- **Fully-differential** 2nd-order single-bit example:

Input sampler reuse for DAC feedback

Common mode

\[ k_{i1} = \frac{C_{s1}}{C_{i1}} \quad k_{i2} = \frac{C_{s2}}{C_{i2}} \quad k_{f1} = \frac{C_{f1}}{C_{f2}} = 1 \]
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Voltage-to-Frequency ADC

Building blocks:

- Voltage-controlled oscillator (VCO)
- Coarse counter
- Fine register
- Encoder

Implicit sub-ranging:

\[ f_{VCO} = (2^{MSB} - 1) f_s \ll (2^N - 1) f_s \]
Voltage-to-Frequency ADC

Building blocks:

- Voltage-controlled oscillator (VCO)
- S/H
- Non-linearity $V_{in} - I_{bias}$ and $I_{bias} - f_{VCO}$

**Low frequency** ($f_{coarse} << 2^{ENOB} f_s$), unlike integrating ADCs

**Low-voltage** operation

**Non-linearity** $V_{in} - I_{bias}$ and $I_{bias} - f_{VCO}$

**Technology sensitivity**

$Q$