5. Low-Power OpAmps

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Integrated Circuits and Systems
IMB-CNM(CSIC)
1. Low-Voltage vs Low-Current

2. Subthreshold Operation

3. Class-AB Output Stages

4. Rail-to-Rail Topologies

5. Inverter-Based Pseudo-Differential Multi-Stages Architectures
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Low-Voltage vs Low-Current

- OpAmp overall **power** consumption:

\[ P_{DD} = I_{DD} \times V_{DD} \]
Low-Voltage vs Low-Current

OpAmp overall power consumption:

Alternative supply sources (battery, solar cell, scavenging)

Poor power scaling

Limited by technology

Low-voltage circuit techniques:

- Rail-to-rail
- Inverter-based
- Supply multipliers
- Back gate ...
Low-Voltage vs Low-Current

► OpAmp overall **power** consumption:

\[ P_{DD} = I_{DD} \times V_{DD} \]

▲ **Strong** power savings

▼ Limited by **noise** and **bandwidth**

► **Low-current** circuit techniques:
  - Subthreshold
  - Class-AB
  - Dynamic biasing
  - Duty cycle ...

▲ **Alternative supply sources**
  (battery, solar cell, scavenging)

▼ **Poor** power scaling

▼ Limited by **technology**

► **Low-voltage** circuit techniques:
  - Rail-to-rail
  - Inverter-based
  - Supply multipliers
  - Back gate ...
Low-Voltage vs Low-Current

OpAmp overall **power** consumption:

\[ P_{DD} = I_{DD} \times V_{DD} \]

▲ **Strong** power savings

▼ Limited by **noise** and **bandwidth**

▲ Alternative supply **sources** (battery, solar cell, scavenging)

▼ **Poor** power scaling

▼ Limited by **technology**

▲ **Low-voltage** circuit techniques:
  - Rail-to-rail
  - Inverter-based
  - Supply multipliers
  - Back gate ...

▼ **Conflicts** can arise between low-current and low-voltage design techniques!
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Optimizing MOSFET Biasing

► Each transistor has its own **purpose** and **requirements**!

![MOSFET biasing diagram]

- $I_{bias}$
- $V_{inn}$
- $V_{in}$
- $V_{out}$
- $C_{comp}$

*e.g. single-ended two-stage Miller OpAmp*
Optimizing MOSFET Biasing

- Each transistor has its own **purpose** and **requirements**!

![Optimizing MOSFET Biasing Diagram]

e.g. single-ended two-stage Miller OpAmp

- good current matching
Optimizing MOSFET Biasing

▶ Each transistor has its own **purpose** and **requirements**!

- M1
- M2
- M3
- M4
- M5
- M6
- M7
- M8

\[ I_{bias} \quad V_{in} \quad V_{out} \quad V_{inp} \quad C_{comp} \]

- **e.g. single-ended two-stage Miller OpAmp**
  - good **current matching**
  - good **transconductance**
Optimizing MOSFET Biasing

► Each transistor has its own **purpose** and **requirements**!

e.g. single-ended two-stage Miller OpAmp

- good current matching
- good transconductance

Forward saturation example (neglecting CLM):

\[
\beta \frac{(V_{GB} - V_{TH})^2}{2n} \]

\[
\sigma \left( \frac{\Delta I_D}{I_D} \right) \downarrow \\
I_{Se} \frac{V_{GB} - V_{TH}}{nV_t} \\
log I_D \\
log I_S \\
V_{out} \\
V_{in} \\
V_{inn} \\
M1 \quad M2 \\
M3 \quad M4 \\
M5 \quad M6 \\
M7 \quad M8
Optimizing MOSFET Biasing

Each transistor has its own **purpose** and **requirements**!

- **IC-based** circuit design:
  - \( I_C >> 1 \) e.g. good current matching
  - \( I_C ~ 1 \) **optimized transconductance/power**
  - \( I_C << 1 \) e.g. translinear \( e^x \) functions

- Individual operating point selection by **sizing** + **biasing**:

\[
I_S = 2n/\beta U_i^2
\]
\[
I_C \approx \frac{I_D}{I_S}
\]

\[
M \times \left( \frac{W}{L} \right)
\]

inversion coefficient

- \( g_{m0} \) vs. \( I_D / I_C \)
  - Weak
  - Moderate
  - Strong inversion

\[
g_{m0} \propto \sqrt{\frac{2\beta}{nI_D}}
\]

\[
\frac{1}{nU_i}
\]

\[
\log I_C
\]
Specific Current Generator

- **I<sub>S</sub>-based** current reference:

![Diagram of I<sub>S</sub>-based current generator]

1. **PTAT voltage**
2. **I<sub>S</sub>-based current**
3. **V<sub>bias**
4. **V<sub>ptat**

Neglecting CLM

\[
M I_{bias} = \frac{N \beta_I}{2N} (V_{bias} - V_{TH} - n V_{ptat})^2
\]

\[
(M + 1) I_{bias} = \beta_I (V_{bias} - V_{TH} - \frac{n}{2} V_{ptat}) V_{ptat}
\]

\[
Q = \left[ \frac{\ln P}{2(M + 1)} \left( \sqrt{\frac{M}{N}} + \sqrt{\frac{M}{N} + M + 1} \right) \right]^2
\]

\[
I_{bias} = Q I_{S7}
\]

- By using \(I_{bias}\) for biasing circuits, IC selection is **independent** from technology

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Specific Current Generator

- **I_s-based** current reference:

- As a side effect, temperature compensated voltage references can be also obtained:

  \[ V_{\text{ref}} = 2n \sqrt{\frac{QX}{Y}} U_t + V_{TH} \]

  \[ V_{TH}(T) = V_{TH}(T_0) - \alpha \left( \frac{T}{T_0} - 1 \right) \]

  \[ \sqrt{\frac{QX}{Y}} = \frac{1}{2n U_t(T_0)} \alpha \]

  \[ V_{\text{ref}} \equiv \alpha + V_{TH}(T_0) \]

- By using I_{bias} for biasing circuits, IC selection is independent from technology

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Output Operation Class

- OpAmp power investment:

\[ V_{in} \rightarrow - \rightarrow + \rightarrow V_{out} \]

noise performance  

- driving capability

Output stage operation modes:

\[ I_{outp} \rightarrow + \rightarrow V_{outp} \]

\[ I_{outn} \rightarrow - \rightarrow V_{outn} \]
Output Operation Class

- **OpAmp power investment:**

  - Input: $V_{in}$
  - Output: $V_{out}$
  - Noise performance
  - Driving capability

- **Output stage operation modes:**

  - Class-A
  - Class-B
  - Class-G/H
  - Class-AB
  - Class-C
  - Class-E/F
  - Class-D
Basic CMOS Topologies

- **Inverter-like stage:**

![Inverter-like stage diagram]

- **Push-pull type stage:**

![Push-pull type stage diagram]
Basic CMOS Topologies

**Inverter-like stage:**

- High **voltage gain**
- Intrinsic high **output impedance** \((1/g_{md})\)
- Suitable for **capacitive loads only**
- Optimized **full-scale**

**Push-pull type stage:**

- Unity **voltage gain**
- Intrinsic low **output impedance** \((1/g_{ms})\)
- Suitable for any type of **load impedance**
- Reduced **full-scale**

**Biassing circuitry** to control \(I_{bias}\) against PVT (CMOS process, supply voltage and temperature) corners and to reach high Class-AB **m**-values?
Class-AB Stage Examples

▶ Translinear loops:

\[ I_{bias}, M1, M2, M3, M4, M5, I_{in}, I_n, I_p, V_{in}, V_{out}, I_{out} \]
Class-AB Stage Examples

**Translinear** loops:

\[
\begin{align*}
\text{weak inversion sat.} & \quad \frac{I_{\text{bias}}}{(W/L)_1} \cdot \frac{I_p}{(W/L)_3} = \frac{I_n}{(W/L)_2} \cdot \frac{I_{\text{in}}}{(W/L)_4} \\
\text{strong inversion sat.} & \quad \sqrt{\frac{I_{\text{bias}}}{\beta_1}} + \sqrt{\frac{I_p}{\beta_3}} = \sqrt{\frac{I_n}{\beta_2}} + \sqrt{\frac{I_{\text{in}}}{\beta_4}}
\end{align*}
\]

![Translinear loops diagram](image-url)
Class-AB Stage Examples

**Translinear** loops:

\[
\frac{I_{\text{bias}}}{(W/L)_1} \cdot \frac{I_p}{(W/L)_3} = \frac{I_n}{(W/L)_2} \cdot \frac{I_{\text{in}}}{(W/L)_4}
\]

\[
\sqrt{\frac{I_{\text{bias}}}{\beta_1}} + \sqrt{\frac{I_p}{\beta_3}} = \sqrt{\frac{I_n}{\beta_2}} + \sqrt{\frac{I_{\text{in}}}{\beta_4}}
\]

- **Weak inversion sat.**
- **Strong inversion sat.**

\[V_{\text{in}} \rightarrow M1 \rightarrow M2 \rightarrow M3 \rightarrow M4 \rightarrow I_{\text{bias}} \rightarrow V_{\text{out}}\]

- **High supply voltage typically required...**

\[V_{\text{in}} \rightarrow M1 \rightarrow M2 \rightarrow M3 \rightarrow M4 \rightarrow M5 \rightarrow I_{\text{bias}} \rightarrow V_{\text{ref}} \rightarrow V_{\text{out}}\]

\[V_{\text{in}} \rightarrow M1 \rightarrow M2 \rightarrow M3 \rightarrow M4 \rightarrow M5 \rightarrow M6 \rightarrow I_{\text{bias}} \rightarrow V_{\text{ref}} \rightarrow V_{\text{out}}\]

**Inverter based version**
Class-AB Stage Examples

Class-A + \textit{dynamic} biasing:
Class-AB Stage Examples

Class-A + **dynamic** biasing:

- **discrete** time (e.g. SC OpAmps)
- **continuous** time (e.g. RC OpAmps)

- **Area** overhead
- **Noise excess** from biasing

![Diagram of Class-AB stages with discrete and continuous time examples]

AC response:
- Input: $V_{in}$
- Output: $V_{out}$
- Currents: $I_n$, $I_p$, $I_{bias}$

DC response:
- Input: $V_{in}$
- Currents: $I_{bias}$
- Output: $V_{out}$
Class-AB Stage Examples

- **Telescopic** topologies:

  - Asymmetrical differential pairs

  ![Telescopic Circuits]

  - **M3**: Constant voltage bias so $V_{in} \equiv V_{ref}$ → $I_p \equiv I_{bias}$
  - PVT compensated by **symmetry**...

  ![Classical Circuits]

  - $I_p \leq 2I_{bias}$
  - $2I_{bias}$
  - $I_p \gg 2I_{bias}$
  - $V_{tel} \uparrow$
  - $V_{in} \uparrow$

- **Output range**
Class-AB Stage Examples

- **Telescopic** topologies:

  \[ I_p = \frac{\beta_2}{2n} (V_{inp} - V_{TH} - nV_x)^2 \]

  \[ I_{bias} = \frac{\beta_1}{2n} (V_{inn} - V_{TH} - nV_x)^2 \]

  \[ \sqrt{\frac{2nI_p}{\beta_2}} - \sqrt{\frac{2nI_{bias}}{\beta_1}} = V_{ind} \]

- **Output range**

- **Half-circuit analysis** for strong inversion saturation

- **Full-circuit analysis** for \( M1=M2 \)

  \[ \sqrt{I_p} = \sqrt{I_{bias}} + \sqrt{\frac{\beta}{2n}} V_{ind} \]

  \[ \sqrt{I_n} = \sqrt{I_{bias}} - \sqrt{\frac{\beta}{2n}} V_{ind} \]
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Why Rail-to-Rail?

- Optimization of signal **full-scale** \( V_{FS} \) and probably dynamic range (DR)

- Compatibility with low **supply voltages** (e.g. battery-powered, energy scavenging)

- Required by **CMFB** in fully differential signal processing

- Already available at OpAmp **output** when no cascode is used:

\[
\begin{align*}
V_{inc} &\approx V_{ref} \\
V_{in} &\approx V_{ref} \\
V_{inc} &\approx V_{in}
\end{align*}
\]

**Necessary at OpAmp input?**

- Required for certain **feedback** configurations!
OpAmp Input Transconductance

- **Overall gain** performance:

\[ |G(DC)| = g_{in} r_{out} \]

- **Input transconductor** for rail-to-rail?
OpAmp Input Transconductance

- **Overall gain** performance:

\[ |G(DC)| = g_{in}r_{out} \]

- **Input** transconductor for rail-to-rail?

- **Complementary** differential pair

\[ V_{inc} \]

- NMOS differential pair
- PMOS differential pair
OpAmp Input Transconductance

- Overall **gain** performance:

\[ |G(\text{DC})| = g_{\text{in}} r_{\text{out}} \]

- **Complementary** differential pair

- **Non-constant** transconductance (gain):

- **Specific OpAmp biasing techniques** are required for rail-to-rail complementary differential pairs
3-Times Current Mirror

Complementary differential pair raw input \textit{transconductance}:

\begin{align*}
g_{\text{in}} \quad \rightarrow \quad g_{\text{mgp}} \quad \rightarrow \quad g_{\text{mgn}} \quad \rightarrow \quad 0 \quad \rightarrow \quad \frac{V_{DD}}{2} \quad \rightarrow \quad V_{DD} \quad \rightarrow \quad V_{\text{inc}}
\end{align*}
3-Times Current Mirror

- Complementary differential pair raw input **transconductance**:

  ![Complementary differential pair diagram](image)

- **Equalization in strong inversion**:

  \[ g_{mgn} + g_{mgp} \equiv \text{const} \]

  \[ \sqrt{2n\beta_n I_{biasn}} + \sqrt{2n\beta_p I_{biasp}} \equiv \text{const} \]

  e.g. \[ \frac{(W/L)_p}{(W/L)_n} = \frac{\beta_{un}}{\beta_{up}} \approx 3 \]

  \[ \sqrt{I_{biasn}} + \sqrt{I_{biasp}} \equiv \text{const} \]

  \[ \sqrt{I_{biasn}} + \sqrt{I_{biasp}} = \begin{cases} 
  \sqrt{4I_{bias}} + \sqrt{0} = 2\sqrt{I_{bias}} & \text{NMOS} \\
  \sqrt{I_{bias}} + \sqrt{I_{bias}} = 2\sqrt{I_{bias}} & \text{N+PMOS} \\
  \sqrt{0} + \sqrt{4I_{bias}} = 2\sqrt{I_{bias}} & \text{PMOS}
  \end{cases} \]
3-Times Current Mirror

_equalization in **strong inversion:**

\[
\sqrt{I_{biasn}} + \sqrt{I_{biasp}} = \begin{cases} 
\sqrt{4I_{bias}} + \sqrt{0} = 2\sqrt{I_{bias}} & \text{NMOS} \\
\sqrt{I_{bias}} + \sqrt{I_{bias}} = 2\sqrt{I_{bias}} & \text{N+PMOS} \\
\sqrt{0} + \sqrt{4I_{bias}} = 2\sqrt{I_{bias}} & \text{PMOS}
\end{cases}
\]
3-Times Current Mirror

Equalization in **strong inversion**:

\[ \sqrt{I_{biasn}} + \sqrt{I_{biasp}} = \begin{cases} \sqrt{4I_{bias}} + \sqrt{0} = 2\sqrt{I_{bias}} & \text{NMOS} \\ \sqrt{I_{bias}} + \sqrt{I_{bias}} = 2\sqrt{I_{bias}} & \text{N+PMOS} \\ 0 + \sqrt{4I_{bias}} = 2\sqrt{I_{bias}} & \text{PMOS} \end{cases} \]

▲ **Compact** bias control

▼ **Non-exact** solution
Current Switch

- Equalization in **weak inversion**:

\[ g_{mn} + g_{mp} \equiv \text{const} \]

\[ \frac{I_{biasn}}{nU_t} + \frac{I_{biasp}}{nU_t} \equiv \text{const} \]

\[ I_{biasn} + I_{biasp} \equiv \text{const} \]

- **Compact** bias control

- Transconductance equalization **sensitivity** to reference voltage
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Cascade vs Cascode

- Low supply voltage by avoiding cascoding circuit structures

\[
|G(DC)| \propto g_{m1} \left( \frac{1}{g_{md1}} \frac{g_{m2}}{g_{md2}} \right)
\]

\[
GBW = \frac{g_{m1}}{2\pi C_{load}}
\]
Cascade vs Cascode

► Low **supply voltage** by avoiding cascoding circuit structures

▲ **OpAmp gain** drop may be compensated by **multistage** topologies

▼ Increase in **power** consumption

▼ **Multipole frequency compensation** can be tricky!

\[
|G(\text{DC})| \propto \frac{g_{mg1}}{g_{md1}} \frac{g_{mg2}}{g_{md2}}
\]

\[
\text{GBW} = \frac{g_{mg1}}{2\pi C_{\text{load}}}
\]

\[
V_{\text{satp}}
\]

\[
|G(\text{DC})| \propto \left(\frac{g_{mg1}}{g_{md1}}\right) \left(\frac{g_{mg2}}{g_{md2}}\right)
\]

\[
\text{GBW} = \frac{g_{mg1}}{2\pi C_{\text{comp}}} < \frac{g_{mg2}}{2\pi C_{\text{load}}}
\]
3-Stage Nested Miller OTA

▶ Inverter as transconductance basic building block

\[ GBW = \frac{g_{m1}}{2\pi C_{comp1}} \quad f_{p2} = \frac{g_{m2}}{2\pi C_{comp2}} \quad f_{p3} = \frac{g_{m3}}{2\pi C_{load}} \]
3-Stage Nested Miller OTA

▶ Inverter as transconductance basic building block

▲ Phase margin save design

\[
\frac{f_{p2}}{GBW} = \frac{g_{m1}}{2\pi C_{comp1}}, \quad f_{p2} = \frac{g_{m2}}{2\pi C_{comp2}}, \quad f_{p3} = \frac{g_{m3}}{2\pi C_{load}}
\]

\[
\phi_m = 90^\circ - \arctan\left(\frac{GBW}{f_{p2}}\right) - \arctan\left(\frac{GBW}{f_{p3}}\right)
\]

▼ Increase in power consumption

▼ Bandwidth reduction
Nested Gm-C Compensation

- Combination of nested loops involving:
  - Positive/negative transconductors
  - Miller compensation capacitors

- Pseudo-differential structures:

  e.g. 3-stage OTA