4. Full-Custom Analog Design Methodology

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Integrated Circuits and Systems
IMB-CNM(CSIC)
1. Device Sizing

2. Process and Mismatching Simulation

3. The Art of Analog Layout

4. Physical Verification

5. Parasitics Extraction

6. DFM Techniques
1. Device Sizing

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6. DFM Techniques
Full-Custom Analog IC Design Flow

From circuit **idea to layout** masks...

**EDA-assisted methodology**

**Schematic flow**
- System-level schematic entry
- Architecture HDL simulation
- Block HDL specification
- Circuit-level schematic entry
- Automatic circuit optimization

**Physical flow**
- PCell-based layout entry
- Design rule checker
- Layout versus schematic
- Parasitics extraction
- Post-layout simulation
- Tape-out

EDA-assisted methodology

*From circuit idea to layout masks...*
Full-Custom Analog IC Design Flow

- From circuit **idea to layout** masks...

**EDA-assisted methodology**

Device sizing is an intermediate key point!
**Full-Custom Schematic Design**

- **Architecture** selection according to system and application specifications:

  - System-level schematic entry
  - Architecture HDL simulation
  - Block HDL specification
  - Circuit-level schematic entry
  - Automatic circuit optimization

  - Signal processing performance
  - Communications standards
  - Power constraints
  - Testbility requirements
  - ... and many more!

  ![Diagram of Full-Custom Schematic Design]

  - Amplifier limiter
  - Antialiasing
  - \( \Delta \Sigma \) modulator
  - Decimator
  - DAC
  - Quantizer
  - Feedback DAC

  - First integrator
  - Second integrator
  - Noise shaper

  e.g. \( \Delta \Sigma \) modulation ADC architecture
Full-Custom Schematic Design

- System modeling through any hardware description language (HDL)

```c
void cm_zinteg2lim(ARGS) {
    inp = INPUT(inp); /* Retrieving input values */
    clk = INPUT_STATE(clk);
    pos_edge = PARAM(pos_edge); /* Retrieving parameters */
    out_max = PARAM(out_max);
    ...
    switch (ANALYSIS) {
        case TRANSIENT:
            if ((clk_mem==ONE) && (clk==ZERO)) { /* Neg. clk edge */
                if (pos_edge==FALSE)
                    action = SAMPLING_INTEGRATION;
            } else {
                if ((clk_mem==ZERO) && (clk==ONE)) { /* Pos. clk edge*/
                    if (pos_edge==TRUE)
                        action = SAMPLING_INTEGRATION;
                } else { /* No clock edge */
                    action = HOLDING;
                }
            }
            ...
            switch (action) {
                case SAMPLING_INTEGRATION:
                    *inp_mem = inp;
                    out = *out_mem + *inp_mem;
                    if (out<out_min) { out = out_min; } /* Limiter */
                    if (out>out_max) { out = out_max; }
                    *out_mem = out;
                    break;
                case HOLDING:
                    out = *out_mem;
            }
    }
}
```

- Architecture description
- **Simplified** modeling
- Second order effects are **neglected**

---

**e.g. XSpice**
Full-Custom Schematic Design

- HDL numerical simulation of the full system using **event-based** engines
  - Architecture evaluation
  - Simulation **speed-up** by orders of magnitude
  - **Ideal** response (maximum possible performance)

```vhdl
# sm-arch.sub
.subckt dsm_arch vin dclk dout
  asumin [{v(vin)} {v(vdac)}] {v(verr)} msumin
  .model msumin usummer(sign=[1.0 -1.0])
  akip {v(verr)} {v(vin1)} mki1
  .model mki1 kgain(k=0.3)
  azint1 {v(vin1)} {d(dclk)} {v(vout1)} mzi1
  .model mzi1 zinteg2lim(pos_edge=0 out_ic=0.0 + out_min=-5.0 out_max=5.0)
  akip2 {v(vout1)} {v(vin2)} mki2
  .model mki2 kgain(k=0.7)
  azint2 {v(vin2)} {d(dclk)} {v(vout2)} mzi2
  .model mzi2 zinteg2lim(pos_edge=0 out_ic=0.0 + out_min=-5.0 out_max=5.0)
  akff {v(vout1)} {v(fkff)} mkff
  .model mkff kgain(k=2.0)
  asumout [{v(vout2)} {v(fkff)}] {v(vin)}
  + {v(vout)} msumout
  .model msumout usummer(sign=[1.0 1.0 1.0])
  aquant {v(vquant)} {d(-dclk)} {d(dout)} mquant
  .model mquant quant2lsym(inp_th=0.0 out_ic=0 pos_edge=0 + t_rise=1e-9 t_fall=1e-9)
  adac {d(dout)} {v(vdac)} mdac
  .model mdac dac2lsym(out_level=2.0)
.ends
```

- System-level schematic entry
- **Architecture HDL simulation**
- Block HDL specification
- **Circuit-level schematic entry**
- **Automatic circuit optimization**

![](image.png)
Full-Custom Schematic Design

- Choosing most suitable **circuit technique** according to:

  ![Diagram of switched-capacitor (SC) technique](image)

- **CMOS** technology options
- Circuit sensitivity against process, supply and temperature (PVT)
- **IC operation** conditions (calibration, testability...)
- **External** components available
Full-Custom Schematic Design

- **Splitting** system design problem into independent **blocks**:

  - Modeling **second order** effects due to limited block performance
  - Electrical simulation of each **block** is feasible
  - Transistor-level **final** simulation of overall system is still required!

  ![Opamp schematic diagram]

  **NAME_TABLE**:
  - Spice_Model_Name: opamp
  - C_Function_Name: cm_opamp
  - Description: "OpAmp macro"

  **PORT_TABLE**:
  - Port_Name: inp inn out
  - Description: "pos. input" "neg. input" "output"
  - Direction: in in out
  - Default_Type: v v v

  **PARAMETER_TABLE**:
  - Parameter_Name: G GBW SR
  - Description: "DC OL gain" "GBW" "slew-rate"
  - Data_Type: real real real
  - Default_Value: 1000 1e6 1e6
  - Limits: 

  - Parameter_Name: out_min out_max
  - Description: "lower out limit" "upper out limit"
  - Data_Type: real real
  - Default_Value: 0 5.0
  - Limits: 

  e.g. limited \{G,GBW,SR\} **Opamp** macro model
Full-Custom Schematic Design

Choosing the particular **circuit topology** for each system block:

- Several topologies can be easily investigated
- **Target specs** from previous step e.g. \{G, GBW, SR\}
- Fast and accurate **electrical simulations**
- **Separated** block tests
- **Several** topologies can be easily investigated
- Inter-block **coupled** effects not covered!
**Full-Custom Schematic Design**

- **Device size optimization** at block level:
  - e.g. OpAmp automatic optimization

```plaintext
optimize
  parameter 0 @m1:xopamp[w] low 6u high 120u initial 32u
  parameter 1 @m6:xopamp[m] low 1 high 10 initial 8
  parameter 3 @comp:xopamp[w] low 25u high 250u

... analysis 25 ac dec 50 10 1e6
  analysis 26 let gmag=20*log10(mag(v(vout)))
  analysis 27 let gph=phase(v(vout))
  analysis 28 cursor c right gmag 0
  analysis 29 let gbw=abs(frequency[%c])/1e6
  analysis 30 let pm=180+gph[%c]

... analysis 46 tran ln 5u
  analysis 47 cursor c right vout 2.1
  analysis 48 let t1=time[%c]
  analysis 49 cursor c right vout 2.9
  analysis 50 let t2=time[%c]
  analysis 51 let srpos=0.8/(t2-t1)*1e-6

... implicit 0 op2.pd lt 1.5
  implicit 1 op2.area lt 0.025
  implicit 4 ac2.pm gt 60
  implicit 5 tran2.srpos gt 12

... cost 1/tran2.srneg+1/tran2.srpos+abs(60-ac2.pm)
  method genetic elitism yes maxgen 1000
```
MOSFET Sizing Analog Guidelines

- **Transistor (also other devices) matching ratios:**
  - Multiplicity (M) design for a common channel aspect ratio (W/L)
  - Non-minimum channel length (L) above design rules for a given W/L

- **Device output impedance:**
  - \( \lambda \propto \frac{1}{L} \)

- **MOS transconductance:**
  - \( M \frac{W}{L} \uparrow \quad g_{m,g,s} \uparrow \)

- **Bandwidth, technology mismatching and flicker noise:**
  - \( C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} MWL \)
  - \( \sigma(\Delta P) \approx \frac{A_P}{\sqrt{MWL}} \)
  - \( \frac{dv_n f_k^2}{df} = \frac{K_{f_k}}{MWL f} \)

- **Physical layout considerations:**
  - M integer design for an overall MW/L
  - M even values for common centroid layout techniques
1. Device Sizing

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6. DFM Techniques
Process Simulation

- **Global** deviations of model parameters:
  - Same change in **all** devices
  - Worse case **corner** analysis: (t)yp, (f)ast, (s)low...

\[ p(\text{param}) \]

\[ \text{all pass!} \]

- **Montecarlo** statistical analysis:

\[ p(\text{param}) \]

\[ \text{yield!} \]
Mismatching Simulation

- **Local** deviations of model parameters:
  - Different change for **each device**
  - **Pelgrom Law**
  - **Montecarlo** statistical analysis:

```
..param avto=30e-9
.param rauo=5e-8
.param rac=7.3e-8

.subckt cnm25modn d g s b param: w=3u l=3u
  + ad=0 as=0 pd=0 ps=0 m=1
.param vton=.942+rndgauss(avto/sqrt(m*w*l))
.param uon=648*(1+rndgauss(rauo/sqrt(m*w*l)))
.model modnlocal nmos level=2 vto={vton} uo={uon} tox=...
  mn d g s b modnlocal w={w} l={l}
  + ad={ad} as={as} pd={pd} ps={ps} m={m}
.ends

.subckt cnm25cpoly t b param: w=30u l=30u m=1
  .param cj=4.227E-4*(1+rndgauss(rac/sqrt(m*w*l)))
  .model cpolylocal c cj={cj} cjsw=0.0
  c pip t b cpolylocal w={w} l={l} m={m}
.ends
```
1. Device Sizing

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6. DFM Techniques
General Matching Rules

- **Unitary** elements

  e.g. $1 : 2$ ratio

- Play with **multiplicity** only

- Same ratio for **second order** effects also (e.g. area and perimeter ratio in caps)

- **Larger area** for the overall array
General Matching Rules

- **Unitary** elements

- Large **area** devices

- Technology local **granularity**
  (e.g. distribution of dopants)

- **Pelgrom Law** \( \propto \frac{1}{\sqrt{WL}} \)
General Matching Rules

- **Unitary** elements
  - e.g. $1 : 1$ ratio

- Large **area** devices

- Minimum **distance**

- Technology global **drifts**
  - (e.g. gate oxide thickness slope)

- **Design rule** spacing limits
General Matching Rules

- **Unitary** elements
- **Large area** devices
- **Minimum distance**
- **Same orientation**

- **Anisotropic** materials
  (e.g. wafer crystal lattice orientation)

- Longer **routing** may be required...
General Matching Rules

- **Unitary** elements
- Large **area** devices
- Minimum **distance**
- Same **orientation**
- Same **surround**

- **Inter-device** second order effects (e.g. parasitic RLC)
- **Larger area** for the overall array
General Matching Rules

- **Unitary** elements
- Large **area** devices
- Minimum **distance**
- Same **orientation**
- Same **surround**
- Same **symmetry**

- **Differential** circuits (common mode interference)
- Complex **floorplan**

Interference source (thermal drift, radio coupling, power ripple, mechanical stress)
General Matching Rules

- **Unitary** elements
- Large **area** devices
- Minimum **distance**
- Same **orientation**
- Same **surround**
- Same **symmetry**

- Compensation of **linear** gradients (and non-linear at short distance)
- **Longer routing** is usually required...
Common Centroid Arrays

▼ Difficult to achieve for large and multiple groups of unitary elements

e.g. A : B : C : D ratios

8  4  2  2

Diagram showing a common centroid array with unitary device elements (M=1).
Common Centroid Arrays

▼ Difficult to achieve for **large** and **multiple groups** of unitary elements

► Centroid as a **center-of-mass** concept, but with area weights...

\[
\sum_{i=1}^{M} A_i (C_i - C_0) = 0
\]

 centroid coordinates

\[
C_0 = \frac{\sum_{i=1}^{M} A_i C_i}{\sum_{i=1}^{M} A_i}
\]

If all elements are of **same area**:

\[
C_0 \equiv \frac{1}{M} \sum_{i=1}^{M} C_i
\]
Common Centroid Arrays

\(\nabla\) Difficult to achieve for large and multiple groups of unitary elements

\(\nabla\) Centroid as a center-of-mass concept, but with area weights...

Each element area center-of-mass coordinates

\[
\sum_{i=1}^{M} A_i (C_i - C_0) = 0
\]

Centroid coordinates:

\[
C_0 = \frac{\sum_{i=1}^{M} A_i C_i}{\sum_{i=1}^{M} A_i}
\]

If all elements are of same area:

\[
C_0 \equiv \frac{1}{M} \sum_{i=1}^{M} C_i
\]

Center-of-area is the average of elements positions...
Common Centroid Arrays

- Difficult to achieve for large and multiple groups of unitary elements

- Centroid as a center-of-mass concept, but with area weights...

- Centroid-based golden rules:
  - Coincidence of all centroids

Not a common centroid arrangement!
Common Centroid Arrays

- Difficult to achieve for large and multiple groups of unitary elements

Centroid as a center-of-mass concept, but with area weights...

Centroid-based golden rules:
- Coincidence of all centroids
- Symmetry for X and Y axes
Common Centroid Arrays

▼ Difficult to achieve for **large** and **multiple groups** of unitary elements

► Centroid as a **center-of-mass** concept, but with area weights...

▲ **Centroid**-based golden rules:

- **Coincidence** of all centroids
- **Symmetry** for X and Y axes
- **Dispersion** of groups as uniformly as possible

```
A A B C D B A A
A A B D C B A A
A B A C A D A B
B A D A C A B A
```

**e.g.** $A : B : C : D$ ratios

```
8 4 2 2
```
Common Centroid Arrays

▼ Difficult to achieve for large and multiple groups of unitary elements

► Centroid as a center-of-mass concept, but with area weights...

▲ Centroid-based golden rules:

- **Coincidence** of all centroids
- **Symmetry** for X and Y axes
- **Dispersion** of groups as uniformly as possible
- **Compactness** of overall array to ideal square shape

\[
\text{e.g. } A : B : C : D \text{ ratios } 8 \quad 4 \quad 2 \quad 2
\]
PCell-Based Layout

▲ Unitary elements
▲ Regular geometry
▲ Design rule compliant

For all $w=28$ $l=6$ $mx=4$ $my=2$

common_{d,g,s}={1,0,0}  common_{d,g,s}={0,0,0}  common_{d,g,s}={0,0,1}

common_{d,g,s}={1,1,0}  common_{d,g,s}={0,1,0}  common_{d,g,s}={0,1,1}

common_{d,g,s}={1,1,1}  common_{d,g,s}={1,0,1}

e.g. CNM25 NMOSFET parameterized cell (PCell)
Decoupling Guidelines

- **Signal integrity** between analog, digital, RF... domains
Decoupling Guidelines

- **Signal integrity** between analog, digital, RF... domains

- Avoiding signal coupling through **power rails**

  - **Guard rings** against substrate noise
Decoupling Guidelines

- **Signal integrity** between analog, digital, RF... domains

- Avoiding signal coupling through **power rails**

- Investing peripheral free area for on-chip **decoupling capacitors**
OpAmp Layout Examples

Let's evaluate other students work....
OpAmp Layout Examples

Let's evaluate other students work....
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Geometrical Rules

- **Basic 2D concepts**

  - e.g. MOSFET gate
  - e.g. MiM capacitor
  - e.g. signal routing
  - e.g. serpentine resistor
Geometrical Rules

Technology rules set

e.g. 2.5um 2P2M CMOS (CNM25)

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>0.0</td>
<td>Design grid is 0.25um x 0.25um</td>
</tr>
<tr>
<td>1.1</td>
<td>N-well width &gt;= 8um</td>
</tr>
<tr>
<td>1.2</td>
<td>N-well spacing and notch &gt;= 8um</td>
</tr>
<tr>
<td>2.1</td>
<td>GASAD width &gt;= 2um</td>
</tr>
<tr>
<td>2.2</td>
<td>GASAD spacing and notch &gt;= 4um</td>
</tr>
<tr>
<td>2.3</td>
<td>N-well enclosure of P-plus active &gt;= 5um</td>
</tr>
<tr>
<td>2.4</td>
<td>N-well spacing to N-plus active &gt;= 5um</td>
</tr>
<tr>
<td>3.1</td>
<td>Poly0 width &gt;= 2.5um</td>
</tr>
<tr>
<td>3.2</td>
<td>Poly0 spacing and notch &gt;= 6um</td>
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<td>Poly0 spacing to GASAD &gt;= 6um</td>
</tr>
<tr>
<td>4.1.a</td>
<td>Poly1 width inside GASAD &gt;= 3um</td>
</tr>
<tr>
<td>4.1.b</td>
<td>Poly1 width outside GASAD &gt;= 2.5um</td>
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<td>Exact contact size = 2.5um x 2.5um</td>
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<td>Poly0 enclosure of Contact &gt;= 4um</td>
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<td>10.1</td>
<td>Exact passivation window size = 100um x 100um</td>
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Geometrical Rules

- **Technology rules set**

Front end of line (FEOL)

Back end of line (BEOL)

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<td>N-plus extension of Poly1 inside N-plus active &gt;= 1.5um</td>
</tr>
<tr>
<td>5.5</td>
<td>N-plus width &gt;= 2.5um</td>
</tr>
<tr>
<td>5.6</td>
<td>N-plus spacing and notch &gt;= 2.5um</td>
</tr>
<tr>
<td>6.1</td>
<td>Exact contact size = 2.5um x 2.5um</td>
</tr>
<tr>
<td>6.2</td>
<td>Contact spacing &gt;= 3um</td>
</tr>
<tr>
<td>6.3</td>
<td>GASAD enclosure of Contact &gt;= 1um</td>
</tr>
<tr>
<td>6.4</td>
<td>Poly1 enclosure of Contact &gt;= 1.25um</td>
</tr>
<tr>
<td>6.5</td>
<td>Poly1 Contact spacing to GASAD &gt;= 2.5um</td>
</tr>
<tr>
<td>6.6</td>
<td>Contact spacing to Poly1 inside GASAD &gt;= 2um</td>
</tr>
<tr>
<td>6.9</td>
<td>Poly0 enclosure of Contact &gt;= 4um</td>
</tr>
<tr>
<td>6.10</td>
<td>Contact spacing to Poly1 &amp; Poly0 &gt;= 4um</td>
</tr>
<tr>
<td>7.1</td>
<td>Metal1 width &gt;= 2.5um</td>
</tr>
<tr>
<td>7.2</td>
<td>Metal1 spacing and notch &gt;= 3um</td>
</tr>
<tr>
<td>7.3</td>
<td>Metal1 enclosure of Contact &gt;= 1.25um</td>
</tr>
<tr>
<td>8.1</td>
<td>Exact via size = 3um x 3um</td>
</tr>
<tr>
<td>8.2</td>
<td>Via spacing &gt;= 3.5um</td>
</tr>
<tr>
<td>8.3</td>
<td>Metal1 enclosure of Via &gt;= 1.25um</td>
</tr>
<tr>
<td>8.4</td>
<td>Via spacing to Contact &gt;= 2.5um</td>
</tr>
<tr>
<td>8.5</td>
<td>Via spacing to Poly1 &gt;= 2.5um</td>
</tr>
<tr>
<td>9.1</td>
<td>Metal2 width &gt;= 3.5um</td>
</tr>
<tr>
<td>9.2</td>
<td>Metal2 spacing and notch &gt;= 3.5um</td>
</tr>
<tr>
<td>9.3</td>
<td>Metal2 enclosure of Via &gt;= 1.25um</td>
</tr>
<tr>
<td>10.1</td>
<td>Exact passivation window size = 100um x 100um</td>
</tr>
</tbody>
</table>
Design Rule Checker

- **Programming** a rules set...

```python
... 
active = geomGetShapes("GASAD", "drawing")
polygate = geomGetShapes("POLY1", "drawing")
polycap = geomGetShapes("POLY0", "drawing")
gate = geomAnd(polygate, active)
cpoly = geomAnd(polygate, polycap)
geomOffGrid(polygate, 0.25, 1, "0.0. Design grid is ...
geomWidth(gate, 3, "4.1.a. Poly1 width inside GASAD >= ... 
geomSpace(polygate, 3, diffnet, "4.2. Poly1 spacing... 
geomNotch(polygate, 3, "4.2. Poly1 notch >= 3um")
geomExtension(polygate, active, 2.5, "4.4. Poly1 ext... 
geomEnclose(polycap, cpoly, 3, "4.6. Poly0 enclosure... 
... 

e.g. 2.5um 2P2M CMOS (**CNM25**) 
```
Design Rule Checker

- Using assisted DRC tools

- e.g. glade and CNM25

Report on total DRC error count
1 Device Sizing

2 Process and Mismatching Simulation

3 The Art of Analog Layout

4 Physical Verification

5 Parasitics Extraction

6 DFM Techniques
Motivation

- **Planar** technology parasitics

(2D layout view)

\[ R_{shunt} = 13.5 \rho \]

\[ \rho [\Omega/\square] \]
Motivation

- **Planar** technology parasitics

(2D layout view)

(2D cross section view)
Motivation

- **Planar** technology parasitics

- **R** and **L** require node **splitting**!

(2D layout view)

(2D cross section view)

(3D view)

<table>
<thead>
<tr>
<th>Circuit Component</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{shunt}$</td>
<td>$13.5\rho$</td>
</tr>
<tr>
<td>$\rho[\Omega/\square]$</td>
<td></td>
</tr>
<tr>
<td>$C_{fringe}$</td>
<td></td>
</tr>
<tr>
<td>$C_{overlap}$</td>
<td></td>
</tr>
<tr>
<td>$C_{sidewall}$</td>
<td></td>
</tr>
<tr>
<td>$L_{shunt}$</td>
<td></td>
</tr>
<tr>
<td>$K_{coup}$</td>
<td></td>
</tr>
</tbody>
</table>
Extraction Tools

Programm
g a simple rules set for parasitic overlap capacitance only...

cnm25xtr.py

... geomLabel(polygate, "POLY1", "pin", 1) geomLabel(polygate, "POLY1", "net", 0) geomConnect([ [cont, ndiff, pdiff, polygate, polycap, metal1], [via12, metal1, metal2]... ] ) extractMOS("cnm25modn", ngate, polygate, ndiff, pwell) extractParasitic3(pdiff, metal2, cmetal2diff, 0, [metal1, polygate, polycap]) ...

e.g. 2.5um 2P2M CMOS (CNM25)
4. Full-Custom Analog Design Methodology

Extraction Tools

► Programming a simple rules set for parasitic overlap capacitance only...

► Using assisted extraction tools...

.eSUBCKT opamp vinn vinp vout vdd vss ibias
MM0 vdd ibias vdd vdd cnm25modp w=1.2e-05 l=6e-06 as=...
MM1 vdd ibias vout vdd cnm25modp w=1.2e-05 l=6e-06 as=...
Cc0 vinter vout cnm25cpoly w=6.42928e-05 l=0.000156207
MM8 vout ibias vdd vdd cnm25modp w=1.2e-05 l=6e-06 as=...

... CP1 vinter vss C=3.8582e-13
CP2 vout ibias C=3.33692e-15
CP3 vinp vss C=3.85938e-15
CP4 vout vcomm C=2.0918e-15
... .ENDS

.eSUBCKT opamp_par.sub

Using assisted extraction tools...

e.g. glade and CNM25
1. Device Sizing

2. Process and Mismatching Simulation

3. The Art of Analog Layout

4. Physical Verification

5. Parasitics Extraction

6. DFM Techniques
Going Into Production

- From few IC prototypes to small and medium series

- Design for manufacturing (DFM) layout rules to increase manufacturing yield

- Some examples:
  - Dummy filling
Going Into Production

- From few IC **prototypes** to small and medium **series**
- Design for manufacturing (DFM) layout rules to increase manufacturing **yield**
- Some **examples**:
  - Dummy **filling**

Using few shapes also simplifies optical proximity correction (**OPC**)

**non-uniform**
layer area = **etching**
issues

**floating**
dummy
structures

**automatic**
filling for
a target
% coverage
Going Into Production

- From few IC prototypes to small and medium series
- Design for manufacturing (DFM) layout rules to increase manufacturing yield

Some examples:
- Dummy filling
- Antenna reduction

Charge stored during metal patterning can break thin gate oxide:

\[
\frac{A_{\text{met}}}{A_{\text{gate}}} < \text{max}
\]
Going Into Production

- From few IC **prototypes** to small and medium **series**

- Design for manufacturing (DFM) layout rules to increase manufacturing **yield**

- Some **examples**:
  - Dummy **filling**
  - **Antenna** reduction
  - Metal **slotting**
  - **Multiple** contacts
  - Extra **guard rings**