Class-AB Single-Stage OpAmp
for Low-Power Switched-Capacitor Circuits

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1 Introduction

2 Class-AB Architecture

3 Process-Independent Circuits

4 Practical Design

5 Experimental Results

6 Conclusions
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Low-Power Switched-Capacitor Design

Low-Voltage Approach

- Bulk-driven OpAmps
- Internal supply multipliers
- Inverter-based OpAmps
- Switched OpAmps

▲ Nominal-voltage downscaling
▼ Moderate power savings

Low-Current Approach

- Telescopic diff. pairs with LCMFB
- Dynamic biasing by RC bias tees
- Hybrid-Class-A/AB
- Adaptive biasing

▲ Higher power savings
▼ Parameter-variation sensitivity
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Single-Stage Class-AB OpAmp

- Two complementary diff. pairs
- Dynamic current mirrors
- Separate Class-AB control
- Partial positive feedback
- CMFB control through the NMOS-pair tail

- Gain improvement by the output cascode transistors
- No need for the Miller compensation capacitors
- High-peak Class-AB currents only in the output transistors
Supposing all boxed devices operating in strong inversion:

\[ D = \frac{AB}{A + B} \]

\[ \sqrt{\frac{I_{onp}}{D}} = \sqrt{\frac{I_{inp}}{A}} + \sqrt{\frac{n\beta}{2}} V_{cp} \]

Desired Class-AB behavior:

\[ \begin{align*}
& I_{outp} \equiv 0 & V_{cp} \equiv V_{xp} & I_{onp} \equiv I_{inp} \\
& I_{outp} \neq 0 & V_{cp} \neq V_{xp} \begin{cases} 
I_{onp} \ll I_{inp} \\
I_{onp} \gg I_{inp}
\end{cases}
\end{align*} \]
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Type I

\[ I_{\text{inp}} = B \left( 2 \sqrt{\frac{I_{\text{onn}}}{D}} - \sqrt{\frac{I_{\text{onp}}}{D}} + \sqrt{\frac{I_{\text{inp}}}{A}} \right) \left( \sqrt{\frac{I_{\text{onp}}}{D}} - \sqrt{\frac{I_{\text{inp}}}{A}} \right) \]

\[ + C \left( \sqrt{2 \frac{I_{\text{tail}}}{D}} - \sqrt{\frac{I_{\text{onp}}}{D}} - \sqrt{\frac{I_{\text{onn}}}{D}} + \sqrt{\frac{I_{\text{inp}}}{A}} + \sqrt{\frac{I_{\text{inn}}}{A}} \right) \]

\[ \left( \sqrt{\frac{I_{\text{onp}}}{D}} - \sqrt{\frac{I_{\text{onn}}}{D}} - \sqrt{\frac{I_{\text{inp}}}{A}} + \sqrt{\frac{I_{\text{inn}}}{A}} \right) \]

- **Cross-coupled** pair for the Class-AB operation
- **Crossing** transistor as a Class-AB limiter
- **Independence** from the technology parameters
- **Need for an extra bias** reference
Type I with Class-AB Smoother

- Low-level common-mode current injection
- Instability prevention under a high Class-AB modulation
- Need for extra current sources
Type II

\[ I_{\text{inp}} = \left[ 2 \left( B \sqrt{\frac{I_{\text{onn}}}{D}} + C \sqrt{\frac{I_{\text{onp}}}{D}} \right) - (B+C) \left( \sqrt{\frac{I_{\text{onp}}}{D}} - \sqrt{\frac{I_{\text{inp}}}{A}} \right) \right] \left( \sqrt{\frac{I_{\text{onp}}}{D}} - \sqrt{\frac{I_{\text{inp}}}{A}} \right) \]

\[ D = \frac{A(B+C)}{A+B+C} \]

\[ I_{\text{max}} \approx \frac{1+A}{1+B+C} I_{\text{tail}} > I_{\text{tail}} \]

- **Independence** from the technology parameters
- **Auto-biased** Class-AB limiter
- **Self-latch prevention**
- **Simple sizing** procedure
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Type-II OpAmp Using a 0.18-µm CMOS Technology

- Circuit design based on the inversion-coefficient
- Reduced set of transistor matching groups
- Minimum-channel-length devices can be used
- Bias for cascode transistors optimized for maximum output full scale
- 1.8-V nominal voltage supply of the CMOS technology
Simulation Results

- DC transfer curve
- Analytical versus numerical behavior
- Class-AB achieves about $\times 4$ bias current
Simulation Results

- Frequency response
- 200-pF load capacitance

![Simulation Results Graph]

- Differential Gain [dB]
- Frequency [Hz]
- Phase [°]

- 72 dB
- 50 °
Simulation Results

- Step response for several load conditions

![Graph showing step response for different load conditions.](image)

- Stability robustness
Integration

- **Standard**
  0.18-\(\mu\)m 1P6M CMOS technology

- 0.07-mm\(^2\) area

- Additional **CMFB** averaging capacitors for SC applications
Integration

- **Standard**
  0.18-µm 1P6M CMOS technology

- **0.07-mm² area**

- **Additional CMFB averaging capacitors for SC applications**
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Step Response

Diff. Output Voltage [V]

Simulated
Measured

Current [mA]

$I_{\text{supply}}$
$I_{\text{opp}}$
$I_{\text{opn}}$

Time [ms]

Current [mA] Diff. Output Voltage [V]
Full-Scale Evaluation

\[ 3.3V_{pp} \text{ differential full scale at } 1.8\text{-V voltage supply} \]
## Figure-of-Merit Comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[5]</th>
<th>This work</th>
<th>Units</th>
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<tbody>
<tr>
<td>Technology</td>
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<td>0.5</td>
<td>0.25</td>
<td>0.13</td>
<td>0.18</td>
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<td>µm</td>
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<tr>
<td>Supply</td>
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<td>2</td>
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<td>0.8</td>
<td>1.8</td>
<td>V</td>
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<tr>
<td>DC gain</td>
<td>43</td>
<td>45</td>
<td>69</td>
<td>70</td>
<td>51</td>
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<td>dB</td>
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<tr>
<td>$C_{\text{load}}$</td>
<td>80</td>
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<td>4</td>
<td>5.5</td>
<td>8</td>
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<td>pF</td>
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<td>GBW</td>
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<td>165</td>
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<td>86.5</td>
<td>MHz</td>
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<td>Phase margin</td>
<td>89.5</td>
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<td>65</td>
<td>45</td>
<td>60</td>
<td>50</td>
<td>°</td>
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<td>Slew rate, SR</td>
<td>89</td>
<td>20</td>
<td>329</td>
<td>19.5</td>
<td>0.14</td>
<td>74.1</td>
<td>V/µs</td>
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<td>Static power, $P$</td>
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<td>0.04</td>
<td>5.8</td>
<td>0.11</td>
<td>0.0012</td>
<td>11.9</td>
<td>mW</td>
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<tr>
<td>Area</td>
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<td>0.012</td>
<td>N/A</td>
<td>0.012</td>
<td>0.057</td>
<td>0.07</td>
<td>mm²</td>
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<td>FOM</td>
<td>59.33</td>
<td>12.50</td>
<td>0.28</td>
<td>0.98</td>
<td>0.93</td>
<td>1.25</td>
<td>V/µs pF/µW</td>
</tr>
</tbody>
</table>

$$FOM = \frac{\text{SR} \cdot C_{\text{load}}}{P} \left[ \frac{V}{\mu s} \frac{\text{pF}}{\mu W} \right]$$
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Conclusions

- New family of **Class-AB OpAmps**
- **Single-stage** topology
- **No** need for an internal frequency **compensation**
- Class-AB current **peaks in the output transistors only**
- **Low sensitivity** to the technology parameter variations
- **Simple** analytical design flow
- **Successfully used** in a 16-bit 100-kS/s $\Delta \Sigma$ ADC

Thank you!
References


Normalized Current Transfer Curve for Different B/C Ratios
Normalized Current Transfer Curve Under Corners for B/C=3

\[ \frac{2I_{\text{on}}}{I_{\text{tail}}} \]

- typical at 20 °C
- fast at -40 °C
- slow at 80 °C

\[ \frac{2I_{\text{onp}}}{I_{\text{tail}}} \]

\[ \frac{(I_{\text{inp}} - I_{\text{inn}})}{I_{\text{tail}}} \]