A 0.18\(\mu\)m CMOS Low-Power Charge-Integration DPS for X-Ray Imaging

Roger Figueras\(^1\), Justo Sabadell\(^2\), Josep Maria Margarit\(^1\), Elena Martín\(^1\), Lluís Terés\(^1\) and Francisco Serra-Graells\(^1\)

paco.serra@imb-cnm.csic.es

\(^1\)Integrated Circuits and Systems (ICAS)
Instituto de Microelectrónica de Barcelona, IMB-CNM(CSIC)

\(^2\)X-Ray Imatek S.L.

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2 Lossless A/D Conversion

3 Dark Current Cancellation

4 Gain Programmability and Built-in Test

5 Local Bias Generation

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Introduction

- **Hybrid X-ray digital** imagers
- Low-energy (<20keV) medical applications: **mammography**

- DPS circuits for **visible** spectrum:
  - $e^-/h^+$ collection
  - Pulsed X-ray input current (typ. 15ke$^-$/hit@10$\mu$s)
  - Dark current + gain FPN
  - Built-in test

- Few DPS for **X-ray** based on **photon-counting**:
  - Saturation due to pile-up
  - Losses from charge sharing with neighbors
Introduction

- **Hybrid X-ray digital** imagers
- **Low-energy (<20keV)** medical applications: **mammography**

- **Novel X-ray DPS proposal** based on **charge-integration** to solve all plus:
  - ✔ Self-biasing
  - ✔ Lossless A/D conversion

... **subthreshold** operation and circuit **reuse** for a **low-power** and **compact** DPS!

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Lossless A/D Conversion

**Predictive scheme:**

- Pulse density modulator
- Low-pass digital filter

\[
q_{adc} = \left\lfloor n_{adcideal} \right\rfloor
\]

\[
n_{adcideal} = \frac{T_{frame}}{T_{pulseideal}} = \frac{T_{frame}}{C_{int} V_{th}} I_{adc}
\]

\[
e.g. \ 10\text{bit and } T_{frame}=10\text{ms require } T_{res}<5\text{ns!}
\]

**Under real low-power operation:**

\[
n_{adcreal} = \frac{n_{adcideal}}{1 + \frac{T_{res}}{T_{frame}} n_{adcideal}}
\]

\[
T_{res} < \frac{T_{frame}}{2 q_{fullscale}^2} \text{ for } <0.5\text{LSB error}
\]
Lossless A/D Conversion

**Predictive** scheme:

- Pulse density modulator
- Low-pass digital filter

\[ I_{\text{adc}} \rightarrow \int V_{\text{int}} - V_{\text{ref}} \rightarrow V_{\text{pulse}} \rightarrow \sum q_{\text{adc}} \rightarrow V_{\text{int}} \rightarrow b_{\text{init}} \]

\[ V_{\text{int}} \rightarrow V_{\text{pulse}} - V_{\text{ref}} \rightarrow V_{\text{ref}} \]

Under real low-power operation:

- \( n_{\text{adcreal}} \equiv n_{\text{adcideal}} \)
- \( T_{\text{res}} \) independent
- \( \min(T_{\text{res}}) \) for charge redistribution
- \( \max(f_{\text{pulse}}) = \frac{1}{2T_{\text{res}}} \)
Lossless A/D Conversion

CMOS proposal:

Capacitive TransImpedance Amplifier (CTIA) = M1-4 + $C_{int}$

Non-overlapped reset by M6-7

$b_{h/\bar{e}}$ for controlling collection polarity

Inherent Correlated Double Sampling (CDS)
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Dark Current Cancellation

- Current copiers based $I_{dark}$ auto-calibration
- Coarse + fine for charge injection compensation
- Composite switches for long retention time (up to 1s)
- Dual operation for $b_{h/e}$
- ADC PDM parts reused
- CTIA offset independent

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Gain Programmability

- FPN compensation via individual \( V_{th} \) control:

\[
V_{prog} = V_{DD} \sum_{i=0}^{B-1} \frac{q_{dac}(i)}{2^{B-i}} \geq 0
\]

- SC DAC based
  - Serial **program-in** during read-out (no speed losses), for \( C_{samp} = C_{mem} \):

\[
V_{prog} = V_{DD} \sum_{i=0}^{B-1} \frac{q_{dac}(i)}{2^{B-i}} \geq 0
\]

- **Polarity** + storage:

\[
V_{th} = \frac{C_{mem}}{C_{int}} \frac{V_{DD}}{2} \sum_{i=0}^{B-1} \frac{q_{dac}(i)}{2^{B-i}}
\]

- **ADC PDM reused**
- **Built-in test** through charge injection...
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Local Bias Generation

- $I_{bias}$ and $V_{ref}$ DPS generator
- PTAT core M1-M4 in weak inversion saturation:

$$V_{bias} = U_t \ln P$$

- M8 and M9 in strong inversion saturation and conduction:

$$I_{bias} = Q I_{S9} \quad I_{S9} = 2n/\beta_9 U_t^2$$

$$Q = \left[ \frac{\ln P}{2(M+1)} \left( \sqrt{\frac{M}{N}} + \sqrt{\frac{M}{N}} + M + 1 \right) \right]^2$$

- M12 in strong inversion saturation:

$$V_{ref} = 2n \sqrt{\frac{QX}{Y}} U_t + V_{TO}$$

- $I_S$-based $I_{bias}$ for low dependence on technology
- $V_{ref}$ thermal compensation
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CMOS Integration

- **DPS cell layout:**

  - Dark current cancellation
  - X-ray sensor bumping pad
  - Local bias generation
  - A/D conversion (PDM-CTIA)
  - Gain programming and built-in test
  - A/D conversion (PDM-comparator)
  - A/D conversion (PDM-control)
  - A/D conversion (filter-counter) and digital I/O

- \( I_{bias} = 250 \text{nA} \)
- \( V_{ref} = 670 \text{mV} \)
- \( C_{int}, C_{reset/CDS}, C_{mem}, \) and \( C_{samp} = 100 \text{fF} \)
- \( B = (10+1) \text{bit} \)
- \( 40 \text{mV} < V_{th} < 400 \text{mV} \)
CMOS Integration

- **DPS test** oriented circuit:

  - $I_{bias} = 250\text{nA}$
  - $V_{ref} = 670\text{mV}$
  - $C_{int}$, $C_{reset/CDS}$, $C_{mem}$ and $C_{samp} = 100\text{fF}$
  - $B = (10+1)\text{bit}$
  - $40\text{mV} < V_{th} < 400\text{mV}$
  - Single transistor $I_{sens}$ emulators
  - $0.18\mu\text{m}$ 1P 6M triple-well CMOS technology

DPS matrix for crosstalk studies

DPS single experiments

500\mu m
Experimental Results

- **PDM transfer function:**

- **DPS performance:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td>Dark current range</td>
<td>0.01 to 20</td>
<td>nA</td>
</tr>
<tr>
<td>Transfer gain</td>
<td>&lt;1/50</td>
<td>LSB/ke−</td>
</tr>
<tr>
<td>Equivalent noise charge</td>
<td>1.5 to 18</td>
<td>ke−rms</td>
</tr>
<tr>
<td>Integration time</td>
<td>10 to 1000</td>
<td>ms</td>
</tr>
<tr>
<td>Output dynamic range</td>
<td>10</td>
<td>bit</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>&lt;0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>Program-in/read-out speed</td>
<td>50</td>
<td>Mbps</td>
</tr>
<tr>
<td>Static power consumption</td>
<td>5</td>
<td>μW</td>
</tr>
<tr>
<td>Bias mismatching (±σ)</td>
<td>&lt;10</td>
<td>%</td>
</tr>
<tr>
<td>Silicon area</td>
<td>100×100</td>
<td>μm²</td>
</tr>
</tbody>
</table>

...for $V_{th}=0.4V$ ('00010010110').
Experimental Results

▶ Overall transfer function:

\[ N_{pulse} \left[ \text{LSB} \right] \]
\[ I_{sens} \left[ \text{A} \right] \]

...for \( V_{th}=0.4\text{V} \) (‘00010010110’).

▶ DPS performance:

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<td>Integration time</td>
<td>10 ms</td>
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</tr>
<tr>
<td>Output dynamic range</td>
<td>10 bit</td>
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Conclusions

- Novel charge-integration DPS for X-ray digital imaging
- In-pixel lossless A/D conversion
- Dark current automatic compensation
- FPN cancellation through digital gain programmability
- Built-in test capabilities
- Local analog bias and references for low crosstalk
- Very low-power CMOS circuits
- Preliminary test results in 0.18\(\mu\)m 1P 6M triple-well CMOS technology
Future Work

- **Scaling, scaling and scaling!**

... thanks for your attention.