A Novel DPS Integrator for Fast CMOS Imagers

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2 Reset Issues in Spike Counting

3 Novel PDM Scheme

4 Compact CMOS Realization

5 Simulation Results

6 Conclusions
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In-pixel ADC

- Architecture?
  - X Direct (flash)
  - X Algorithmic (success. approx.)
  - ✓ Predictive ($\Sigma\Delta$)

- Feedback = relaxed analog specs

- Pulse modulator + digital filter
  - PWM $\equiv$ time-to-first spike
  - PDM $\equiv$ spike counting
  - ✓ No external clocks
  - ✓ Switching power $\propto$ signal
  - X Signal loss due to reset times
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PDM for Fast Imaging

- Classic topology:
- CTIA to cancel input parasitics
- Correlated double sampling (CDS) for noise cancellation

- Ideally:

\[ q_{adc} = \left\lfloor n_{adc\text{ideal}} \right\rfloor \]

\[ n_{adc\text{ideal}} = \frac{T_{frame}}{T_{pulse\text{ideal}}} = \frac{T_{frame}}{C_{int} V_{th}} I_{sens} \]
Real Scenario

- Loss due to reset time:
  \[ n_{\text{adc real}} = \frac{T_{\text{frame}}}{T_{\text{pulse ideal}} + T_{\text{res}}} \]
  \[ n_{\text{adc real}} = \frac{n_{\text{adc ideal}}}{1 + \frac{T_{\text{res}}}{T_{\text{frame}}} n_{\text{adc ideal}}} \]

- Non-linearity error:
  \[ n_{\text{error}} = |n_{\text{adc real}} - n_{\text{adc ideal}}| \]

- Maximum at full-scale:
  \[ \max(n_{\text{error}}) = q_{\text{fullscale}} - \frac{q_{\text{fullscale}}}{1 + \frac{T_{\text{res}}}{T_{\text{frame}}} q_{\text{fullscale}}} < 0.5\text{LSB} = \frac{1}{2} \]
  \[ T_{\text{res}} < \frac{T_{\text{frame}}}{2 q_{\text{fullscale}}^2} \text{ for } q_{\text{fullscale}} \gg 1 \]
  e.g. \( q_{\text{fullscale}} = 1023 \) (10bit) \( T_{\text{frame}} = 10\text{ms} \) \( \Rightarrow T_{\text{res}} < 5\text{ns} \)

Not compatible with low-power nor low-voltage!
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Reset-Insensitive Topology

- **Charge controlled** reset of the PDM integrator
- **Continuous-time** integration (like APS!)
- **Built-in CDS** mechanism
- **Switch charge** injection similar to classic topology
Real Scenario

- During reset, charge from \( I_{sens} \) and \( C_{reset}/CDS \) is combined and integrated in \( C_{int} \).

- Almost ideal, even for \( T_{pulsereal} \sim T_{res} \).

- Minimum \( T_{res} \) required for redistribution...

- ...but \( T_{res} \) value not relevant (technology independence).

True low-power and low-voltage compatible!
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CMOS Proposal

- **3-stage compact** PDM circuit

- **Single** transistor CTIA stage M1

- **Local** reference M2

- Built-in **threshold** comparator M3 (all in weak inversion):

  \[ V_{th} = nU_t \ln \left( \frac{W}{L} \right)_1 \frac{(W/L)_3}{(W/L)_3} \]

- **Technology mismatching**
  \( C_{int} \leftrightarrow C_{reset/CDS}, M1 \leftrightarrow M2 \) and \( M1 \leftrightarrow M3 \)

  are equivalent to \( \Delta V_{th} \)

- **\( \Delta V_{th} \) reduction through DPS area increase**
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Quasi-Static (QS) Stimulus

- **0.18μm 1-poly 6-metal CMOS technology**

- **Design parameters:**
  \[ C_{int,reset/CDS} = 100fF, \quad V_{ref} = 1V, \]
  \[ \left(\frac{W}{L}\right)_1 = 20\left(\frac{W}{L}\right)_3 \quad \text{so} \quad V_{th} = 0.1V \]
  and \[ T_{frame} = 2\text{ms} \]
Non Quasi-Static (NQS) Stimulus

- **Non systematic loss**
  - even at low amplitudes for classic PDM
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Conclusions

- Novel pulse density modulator (PDM) for high-speed DPS.
- Reset-insensitive analog integrator proposal.
- Low non-linearity for low-power and low-voltage operation.
- Compact CMOS circuit realization.
- Comparative study in 0.18µm 1-poly 6-metal technology.
- Robust simulation results for both QS and NQS signals.