1V Compact Class-AB CMOS Log Filters

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1 Introduction

2 Basic Class-A Operation

3 New Class-AB Proposal

4 Design Example

5 Conclusions
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Companding filtering scenario

MOS log-mapping

log-domain: \( F(x) = e^x \)

✓ Low-voltage

? Low-current vs dynamic range

? Low-area vs auxiliary circuitry

...the answer is **compact Class-AB**!
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Compressor and expander

\[ I = F(V) = I_{ref} e^{\frac{V - V_{ref}}{nU_t}} \quad I > 0 \]

Note: presented by same authors in ISCAS’00

✓ \( V_{ref} \) used to optimize low-voltage: M3,12 do not need saturation!

✓ \( K \) allows simple frequency compensation

\[ \zeta = \frac{1}{2} \sqrt{\frac{KC_{comp}}{C_{in}}} \]

\[ K \geq 2 \frac{C_{in}}{C_{comp}} \]

✗ \( I_{ref} \) limits the full-scale due to log-mapping:

\[ I_{max} = \frac{I_{ref}}{2} \]

with thermal noise:

\[ \Delta SNR = +3\text{dB/oct}(I_{ref}) \]

... poor improvement!
Integrator

- ODE in the lineal $I$-domain:
  \[
  \frac{dI_{out}}{dt} = \pm \frac{1}{\tau} I_{in}
  \]

- ODE in the compressed $V$-domain:
  \[
  \frac{dV_{out}}{dt} = \pm \frac{nU_t}{\tau} e^{\frac{V_{in} - V_{out}}{nU_t}}
  \]

- ODE in the circuit $Q$-domain:
  \[
  \frac{dQ_{out}}{dt} = C \frac{dV_{out}}{dt} = \pm I_{tun} e^{\frac{V_{in} - V_{out}}{nU_t}}
  \]

- Tunable time constant
- Single dis/charge due to log mapping ($I_{in} > 0$), op ensured at filter level
- Half integrator shared
- $SNR$ issues ($I_{tun} \geq I_{ref}$) cause high-value $C$!
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Input Splitter and Compressor

- **Differential signaling:**
  \[ I_{in} = I_{inp} - I_{inn} \]
  \[ I_{inp,n} > 0 \]

- **Constant geometric mean splitting:**
  \[ I_{inp} I_{inn} = I_{ref}^2 \]

- **Same low-voltage capability as Class-A**
- **Full-scale** \( I_{max} \leftrightarrow I_{ref} \)
- **Optimization:** \( I_{ref} \downarrow \)
  \[ \Delta SNR \approx +6 \text{dB/oct} \left( I_{max} \right) \]

- **Current multiplier M1-M4**
- **Feedback** \( \frac{I_{ref}}{I_{inp}} \) M6-M8
- **M2 shared by TL+compressors**
Differential Integrator with CMFB (1)

ODE in the linear $I$-domain for multiple-inputs:

\[
\frac{dI_{out}}{dt} = \frac{1}{\tau} \sum_{K} \pm I_{inK} \quad \text{(even different } \tau_K)\]

High-gain **CMFB** to ensure geometric-mean common-mode:

\[
\frac{dI_{outp}}{dt} = \frac{1}{\tau} \left[ \sum_{K} \pm I_{inpK} - \frac{I_{outp}I_{outn}}{I_{ref}} + I_{ref} \right] \quad \checkmark \text{ Does not affect } I_{out} \]

\[
\frac{dI_{outn}}{dt} = \frac{1}{\tau} \left[ \sum_{K} \pm I_{innK} - \frac{I_{outp}I_{outn}}{I_{ref}} + I_{ref} \right] \quad \checkmark \text{ CMFB overhead} \]

\[\propto \text{ filter order} \]

\[\leftrightarrow \text{ filter complexity} \]
Differential Integrator with CMFB (2)

- ODE in the compressed $V$-domain:

\[
\frac{dV_{\text{out}p}}{dt} = \frac{nUt}{\tau} \left[ \sum_{K} \frac{I_{\text{inp}K}}{I_{\text{out}p}} - \frac{I_{\text{out}n}}{I_{\text{ref}}} + \frac{I_{\text{ref}}}{I_{\text{out}p}} \right]
\]

\[
\frac{dV_{\text{out}n}}{dt} = \frac{nUt}{\tau} \left[ \sum_{K} \frac{I_{\text{inn}K}}{I_{\text{out}n}} - \frac{I_{\text{out}p}}{I_{\text{ref}}} + \frac{I_{\text{ref}}}{I_{\text{out}n}} \right]
\]

- Finally, ODE in the circuit $Q$-domain:

\[
\frac{dQ_{\text{out}p}}{dt} = I_{\text{tun}} \left[ \sum_{K} \pm e \frac{V_{\text{inp}K} - V_{\text{out}p}}{nUt} - e \frac{V_{\text{out}n} - V_{\text{ref}}}{nUt} + e \frac{V_{\text{ref}} - V_{\text{out}p}}{nUt} \right]
\]

\[
\frac{dQ_{\text{out}n}}{dt} = I_{\text{tun}} \left[ \sum_{K} \pm e \frac{V_{\text{inn}K} - V_{\text{out}n}}{nUt} - e \frac{V_{\text{out}p} - V_{\text{ref}}}{nUt} + e \frac{V_{\text{ref}} - V_{\text{out}n}}{nUt} \right]
\]

\text{cross} \uparrow\text{coupled}
Differential Integrator with CMFB (and 3)

Realization:

\[
\frac{dQ_{\text{outp}}}{dt} = I_{\text{tun}} \left[ \sum_{K} \pm e \frac{V_{\text{inp}K} - V_{\text{outp}}}{nUt} \right. \\
\left. - e \frac{V_{\text{outn}} - V_{\text{ref}}}{nUt} + e \frac{V_{\text{ref}} - V_{\text{outp}}}{nUt} \right]
\]

\[
\frac{dQ_{\text{outn}}}{dt} = I_{\text{tun}} \left[ \sum_{K} \pm e \frac{V_{\text{inn}K} - V_{\text{outn}}}{nUt} \right. \\
\left. - e \frac{V_{\text{outp}} - V_{\text{ref}}}{nUt} + e \frac{V_{\text{ref}} - V_{\text{outn}}}{nUt} \right]
\]

✓ Low-voltage capability
✓ Most CMFB shared by 1...K
✓ Half CMFB shared by all \(C\)'s
✓ \(I_{\text{ref}}\) \(\downarrow\) allows \(I_{\text{tun}}\) \(\downarrow\), so downscaling \(C\) (Si area)
Differential Integrator with CMFB (and 3)

Realization:

\[
\frac{dQ_{outp}}{dt} = I_{tun} \left[ \sum_{K} \pm e \frac{V_{inpK} - V_{outp}}{nUt} + e \frac{V_{ref} - V_{outp}}{nUt} \right]
\]

\[
\frac{dQ_{outn}}{dt} = I_{tun} \left[ \sum_{K} \pm e \frac{V_{innK} - V_{outn}}{nUt} + e \frac{V_{ref} - V_{outn}}{nUt} \right]
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\[
\frac{dQ_{outn}}{dt} = I_{\text{tun}} \left[ \sum \pm e \frac{V_{\text{innK}} - V_{outn}}{nUt} \right]
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- Realization:

\[
\frac{dQ_{outp}}{dt} = I_{tun} \left[ \sum K \pm e \frac{V_{inpK} - V_{outp}}{nUt} \right] \\
- e \frac{V_{outn} - V_{ref}}{nUt} + e \frac{V_{ref} - V_{outp}}{nUt}
\]

\[
\frac{dQ_{outn}}{dt} = I_{tun} \left[ \sum K \pm e \frac{V_{innK} - V_{outn}}{nUt} \right] \\
- e \frac{V_{outp} - V_{ref}}{nUt} + e \frac{V_{ref} - V_{outn}}{nUt}
\]

- Low-voltage capability
- Most CMFB shared by 1…K
- Half CMFB shared by all C’s
- \( I_{ref} \downarrow \) allows \( I_{tun} \downarrow \), so downscaling \( C \) (Si area)
Output Expanders

- Differential to single-ended:

\[
I_{out} = I_{outp} - I_{outn}
\]

\[
I_{out} = I_{ref} \left[ e^{\frac{V_{outp} - V_{ref}}{nU_t}} - e^{\frac{V_{outn} - V_{ref}}{nU_t}} \right]
\]

✓ Low-voltage capability like Class-A
✓ Same \( I_{ref} \downarrow \) as compressors
✓ M1,2 expanders share half circuitry
✓ For multiple outputs, all expanders can share this part...
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Second-Order Band-Pass Log-Filter

- $f_{center} = 42\text{KHz}$
- $Q = 1$
Class-A versus New Class-AB

- 0.35\(\mu\)m CMOS technology
- Designed for the same full-scale
- IMD analysis through periodic steady-state (PSS) simulations:

\[ f_{in1} = 40\text{KHz} \]
\[ f_{in2} = 44\text{KHz} \]
Class-A versus New Class-AB

- 0.35μm CMOS technology
- Designed for the same full-scale
- IMD analysis through periodic steady-state (PSS) simulations:

\[ f_{in1} = 40 \text{KHz} \]
\[ f_{in2} = 44 \text{KHz} \]
## Overall Results

<table>
<thead>
<tr>
<th></th>
<th>Class-A</th>
<th>Class-AB</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1 V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{TON} +</td>
<td>V_{TOP}</td>
<td>$</td>
<td>1.2 V</td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>0.5 V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{ref}$ (and $I_{tun}$)</td>
<td>10 µA</td>
<td>2.5 µA</td>
<td>µA</td>
</tr>
<tr>
<td>$C$</td>
<td>1000 pF</td>
<td>250 pF</td>
<td>pF</td>
</tr>
<tr>
<td>Boxed-MOSFET ratios</td>
<td>$50 \times \frac{40}{1.5} \mu\text{m}$</td>
<td>$21 \times \frac{40}{1.5} \mu\text{m}$</td>
<td>µm/µm</td>
</tr>
<tr>
<td>Signal full-scale</td>
<td>$\sim 10 \mu\text{A}_p$</td>
<td></td>
<td>µA_p</td>
</tr>
<tr>
<td>IMD @ half full-scale</td>
<td>0.15 %</td>
<td>0.3 %</td>
<td>%</td>
</tr>
<tr>
<td>$DR$ (10KHz-100KHz)</td>
<td>68 dB</td>
<td>$&gt; 68$ dB</td>
<td>dB</td>
</tr>
<tr>
<td>Quiescent power</td>
<td>150 µW</td>
<td>85 µW</td>
<td>µW</td>
</tr>
<tr>
<td>Total capacitance</td>
<td>2000 pF</td>
<td>1000 pF</td>
<td>pF</td>
</tr>
<tr>
<td>Total boxed-MOS area</td>
<td>0.033 mm$^2$</td>
<td>0.037 mm$^2$</td>
<td>mm$^2$</td>
</tr>
</tbody>
</table>

✓ -40% overall power  
✓ -50% capacitance area
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Conclusions

- Very low-voltage Class-AB CMOS log filters
- Complete set of basic building blocks: splitting, compression, expansion, integration and CMFB
- Quiescent low-power consumption
- Compact area with reduced circuit overhead
- 0.35 µm CMOS Class-A/AB comparative example