IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS & SYSTEMS
ISCAS·2017
BALTIMORE, MD, USA | MAY 28-31, 2017
from Dreams to Innovation

An Academic EDA Suite for the Full-Custom Design of Mixed-Mode Integrated Circuits

J. Pallarès[1], K. Sabine[2], L. Terés[1,3] and F. Serra-Graells[1,3]

[1]Institut de Microelectrònica de Barcelona, IMB-CNM(CSIC) [2]Peardrop Design Systems Ltd. [3]Universitat Autònoma de Barcelona

Centro Nacional de Microelectrónica IMB

Universitat Autònoma de Barcelona

http://www.cnm.es/~pserra/apdk

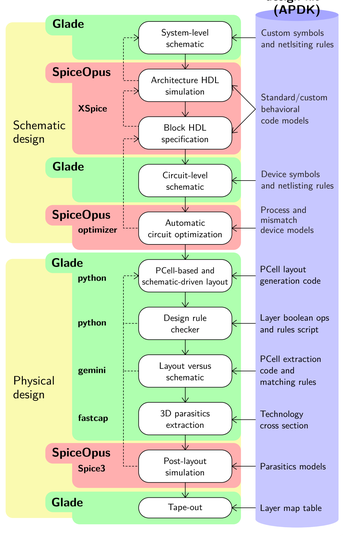
1 Introduction

▼ Expensive commercial EDA tools of complex installation, maintenance and learning

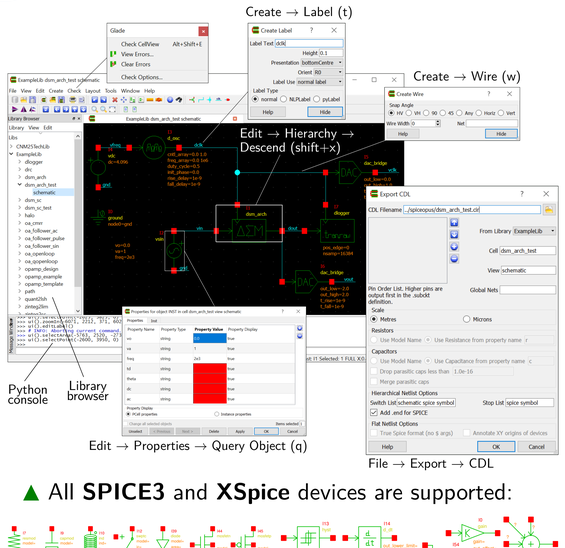
▲ **Free** framework for full-custom IC design:
- + **Schematic** and **layout** edition
- + **Mixed** A/D, event/electrical simulation
- + Automatic circuit **optimzation**
- + All **physical** verification steps

▲ Physical design kit (**PDK**) for target CMOS technology

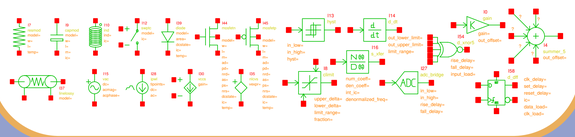
▲ Available for:



2 Schematic Edition

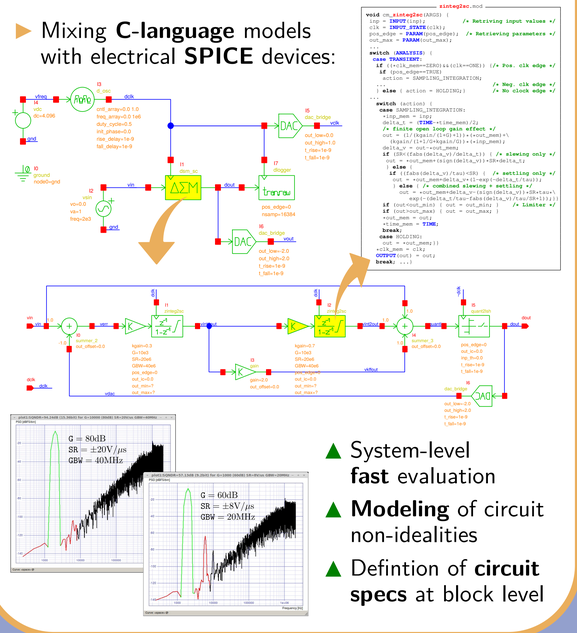


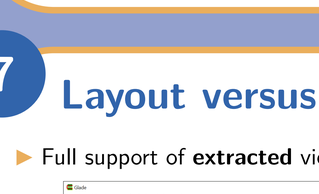
▲ All **SPICE3** and **XSpice** devices are supported:



3 XSpice HDL Simulation

▲ Mixing **C-language** models with electrical **SPICE** devices:





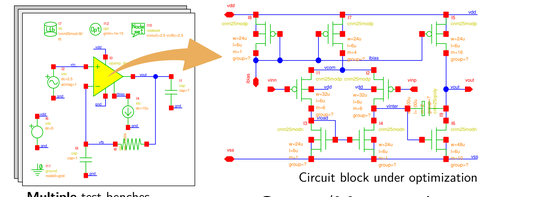
▲ System-level **fast** evaluation

▲ **Modeling** of circuit non-idealities

▲ Defintion of **circuit specs** at block level

4 Circuit Optimization

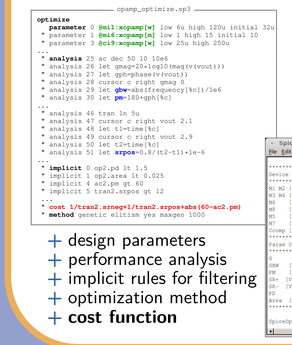
▶ Usage of SpiceOpus `optimize` command:



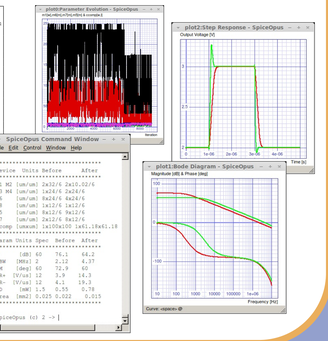
Multiple test benches

Circuit block under optimization

▲ **Custom** control:



▲ Corner/Montecarlo CMOS **process**/**mismatch**



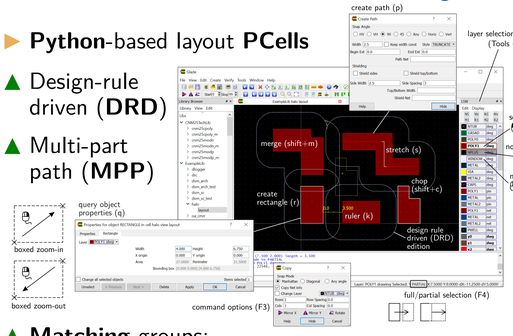
+ design parameters
+ performance analysis
+ implicit rules for filtering
+ optimization method
+ **cost function**

5 Schematic-Driven Layout

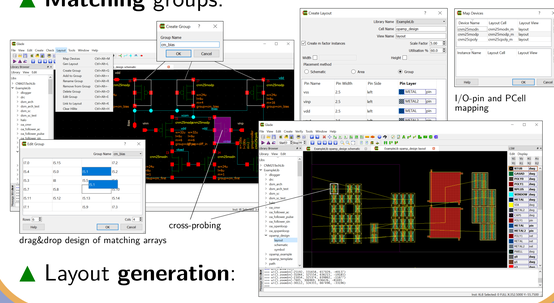
▶ **Python**-based layout **PCells**

▲ Design-rule driven (**DRD**)

▲ Multi-part path (**MPP**)



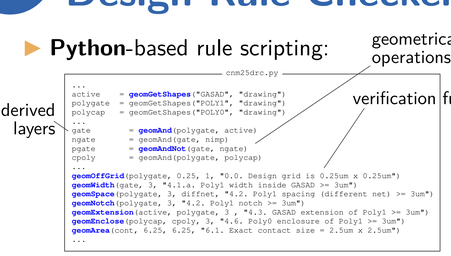
▲ **Matching** groups:



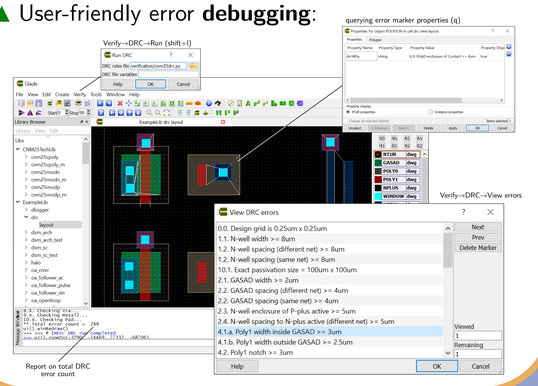
▲ Layout **generation**:

6 Design Rule Checker

▶ **Python**-based rule scripting:

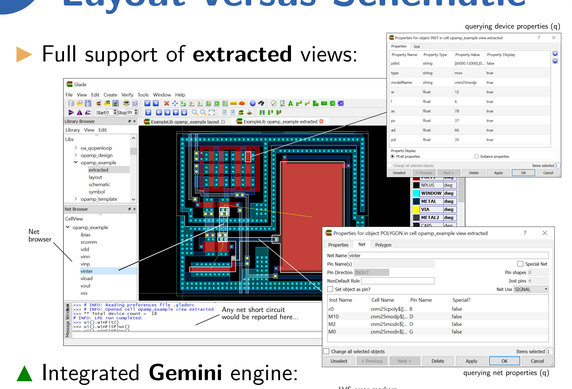


▲ User-friendly error **debugging**:

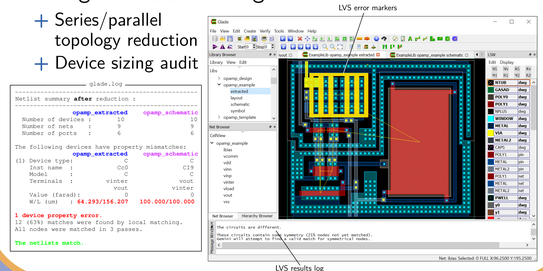


7 Layout versus Schematic

▶ Full support of **extracted** views:

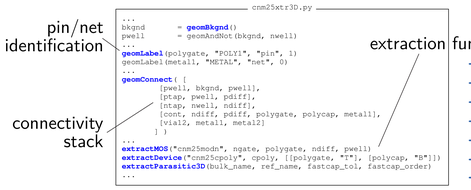


▲ Integrated **Gemini** engine:
- + Series/parallel topology reduction
- + Device sizing audit



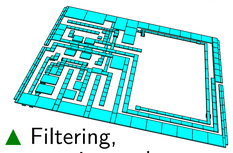
8 3D Parasitics Extraction

▶ **Python**-based rule scripting:



▲ Integrated **Fastcap** finite-element engine

▲ Automatic **mesh** generation



▲ Filtering, merging and **backannotation**