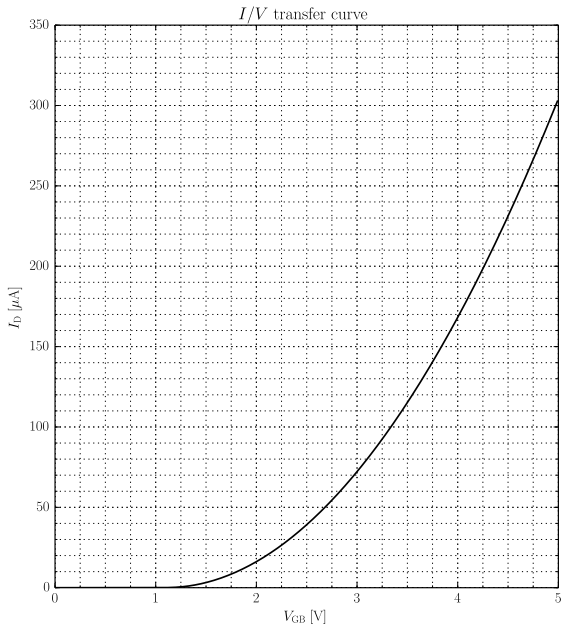
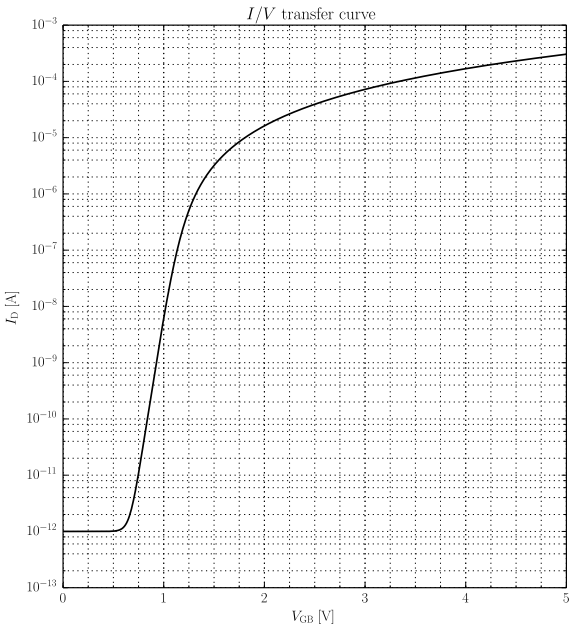
# 42838
# Integrated Heterogeneous Systems Design
## Theory Exercises

Francesc Serra Graells
http://www.cnm.es/users/pserra/uab/ihsd
paco.serra@imb-cnm.csic.es

## 1 Introduction to Integrated Heterogeneous Systems

**1.1** The characterization engineer of a CMOS foundry has measured the following $I/V$ transfer curve for a 10$\mu$m/10$\mu$m NMOSFET operating in saturation ($V_{\mathrm{DB}}$>$V_{\mathrm{Dsat}}$) and room temperature (27°C). Can you extract the equivalent subthreshold slope ($n$), current factor ($\beta$) and threshold voltage ($V_{\mathrm{TH}}$) of its EKV analytical model?

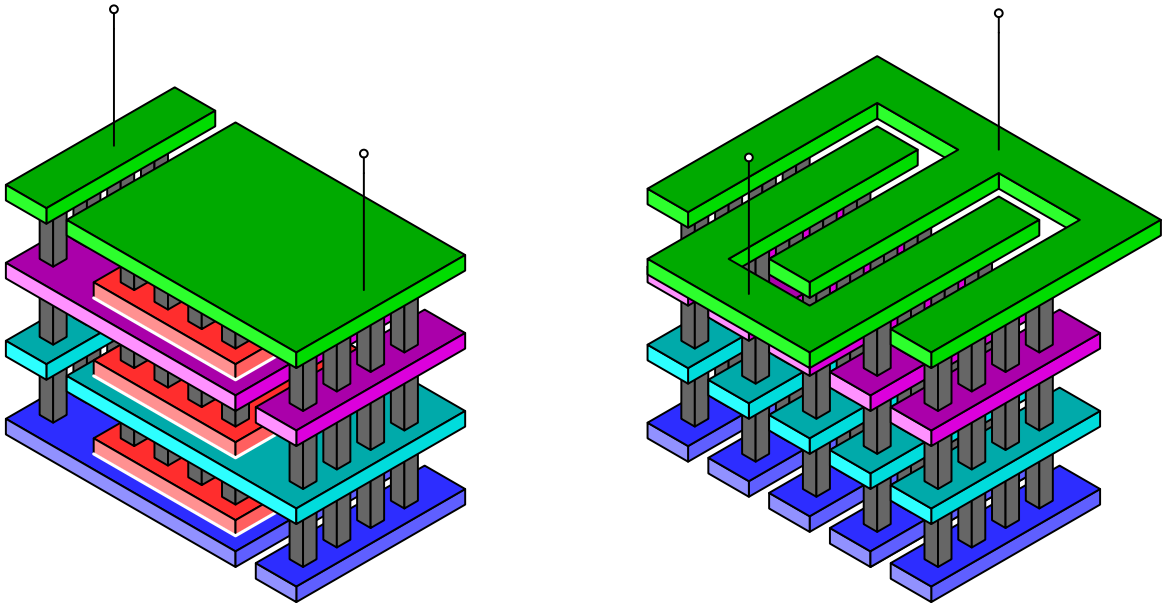


**1.2** Assuming a CMOS technology with the design rules and process parameters given below, estimate the required area to integrate a 50k$\Omega$ serpentine-type resistor for each of the available design layers.

| Layer | Width [$\mu$m] | Spacing [$\mu$m] | Res. [$\Omega/\square$] |
|---|---|---|---|
| N-well | >5 | >4 | 1k |
| P-Diff | >0.5 | >0.5 | 100 |
| HiPo | >1 | >1 | 1k |
| Metal | >0.3 | >0.3 | 10m |

**1.3** Compare the area efficiency of triple MIM versus lateral metal capacitors for a CMOS technology with the following characteristics: $SiO_2$ oxide ($\epsilon_r$=3.9), 35nm MIM oxide thickness, 0.2$\mu$m metal spacing and width, 1$\mu$m metal thickness (drawing not to scale). Vias contribution to fringing capacitance can be neglected.



**1.4** For a switched-capacitor circuit, two matched MIM devices of $C_1$=10pF and $C_2$=50pF are required.

- **a** Taking into account the maximum allowed size for a single MIM structure is 900$\mu$m$^2$, and the area and perimeter density is 1fF/$\mu$m$^2$ and 200aF/$\mu$m respectively, choose the suitable unitary capacitor element size.
- **b** How many of the above unitary capacitors would be required to implement $C_1$ and $C_2$? Draw the overall array of unitary elements and choose their distribution to optimize technology matching between the two capacitors.
- **c** Supposing a Pelgrom's Law parameter of $A_C$=0.4%$\mu$m, what would be the maximum relative mismatching between $C_1$ and $C_2$ for the 99.7% of IC samples?

**1.5** Consider a mono audio ADC with 22kHz bandwidth and $1V_{pp}$ input full scale, which delivers a digital output in agreement with CD quality (i.e. 16-bit dynamic range and 44kHz sampling rate):

- **a** What is the $\mathrm{SQNR}_{\max}$ and maximum noise allowed at the input electret microphone?
- **b** What is the minimum capacitor value for the ADC input sampler?
- **c** Specify the maximum jitter of the clock signal controlling the ADC input sampler.
- **d** In case of increasing the sampling frequency up to 5.632MHz, what would be the improvement in $\mathrm{SQNR}_{\max}$?

**1.6** Same as exercise **1.5** but for two different scenarios:

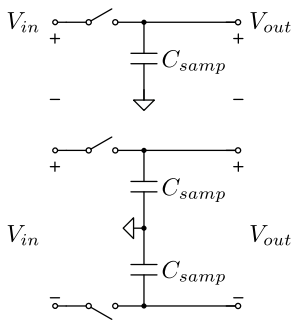
- **a** Increasing 2-bit in dynamic range.
- **b** Doubling signal bandwidth.

**1.7** Imagine you are designing the input sampling stage of an ADC circuit for a $1V_{pp}$ full-scale and 100kHz bandwidth sensor:

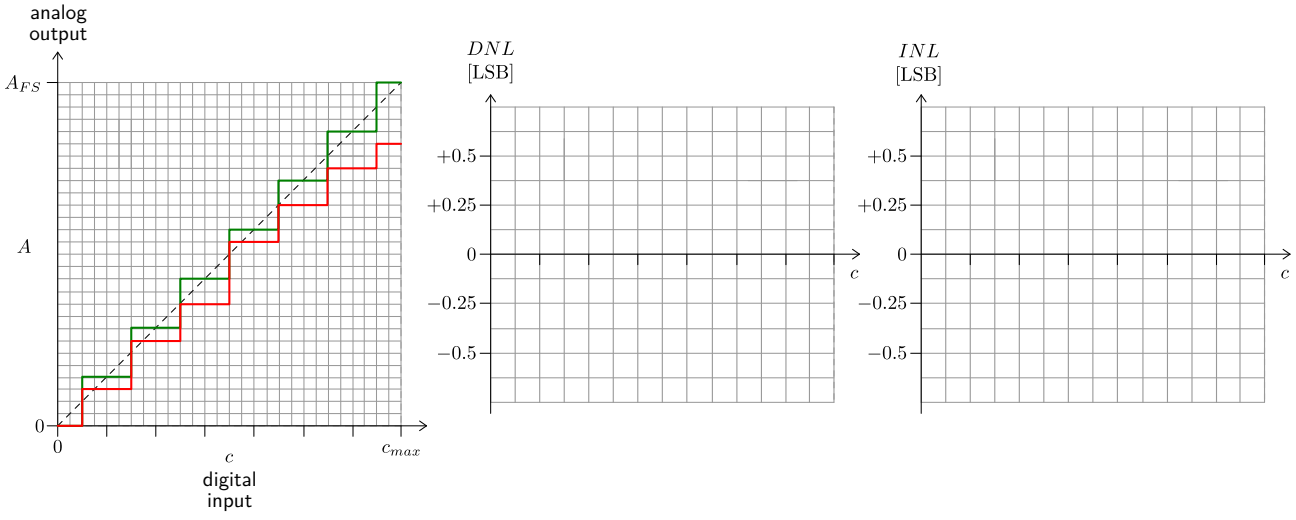
- **a** Complete the following table for a CMOS technology with $C_{\mathrm{ua}}$=1fF/$\mu$m$^2$:

| Max. $V_{\mathrm{sampn}}$ [$V_{\mathrm{rms}}$] | Min. $C_{\mathrm{samp}}$ [pF] | Min. $C_{\mathrm{samp}}$ [$\mu$m $\times$ $\mu$m] | Max. $\sigma_{\mathrm{jit}}$ [$\mathrm{ps}_{\mathrm{rms}}$] |
|---|---|---|---|
| 1m | | | |
| 100$\mu$ | | | |
| 10$\mu$ | | | |
| 1$\mu$ | | | |

- **b** How are these values being modified if a fully differential input sampler is used instead of single-ended one?




**1.8** Draw the differential and integral non-linearity of the following DAC static transfer curve, and explain the results in terms of gain/offset errors, monotonicity, missing codes and maximum errors:



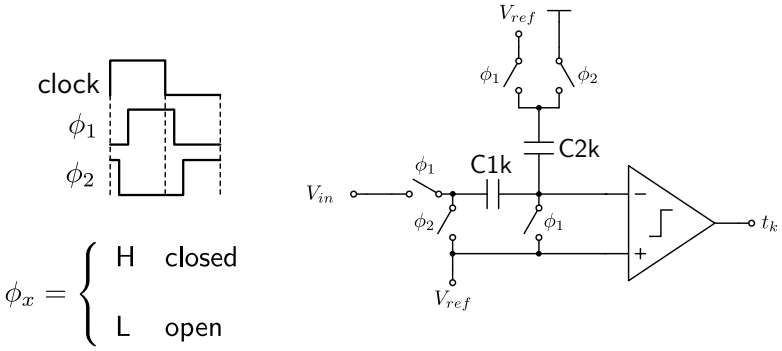
# 2 ADC Architectures and CMOS Circuits

**2.1** Given the following integrated data converter circuits: a flash ADC with 8-bit dynamic range at 1GS/s consuming 10mW (ADC1), a 12-bit SAR ADC at 12MHz clock frequency draining 50$\mu$A from 1.8V supply (ADC2), and a $\Delta\Sigma$ modulator based ADC performing 100dB $SNDR_{max}$ for 50kHz bandwidth and 10mW power consumption (ADC3),

**a** Which of them are performing best according to Schreier and Walden figures of merit?

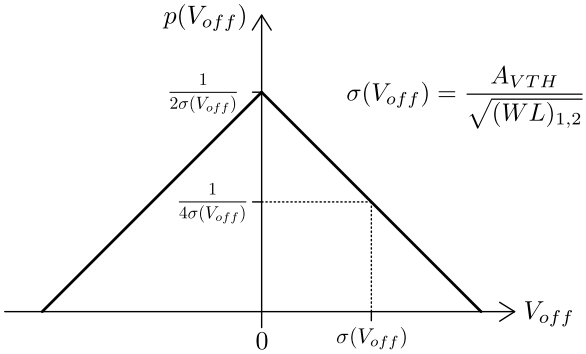
**b** Can any of them be considered as a state-of-art A/D converter?

**2.2** For a single-ended 3-bit flash ADC with ideal input full scale (i.e. from ground to $V_{DD}$), design each of the 7 capacitor coefficients ($C_{2k}/C_{1k}$ for $k = 0 \ldots 7$) of the corresponding level shifters in order to ensure all comparators latch at the signal baseline level $V_{ref} = V_{DD}/2$:




**2.3** A flash ADC with 1V$_{pp}$ input full-scale and 8-bit resolution is being designed for its integration in CNM25 CMOS technology with process parameters $A_{VTH}$=30mV$\mu$m, $\epsilon_{ox}$=3.9$\epsilon_o$ and $t_{ox}$=38nm:

**a** Estimate the minimum area ($WL$) of the comparators input MOS transistors, so bubble can not occur at $\pm$2 thermometer code distance. For simplification purposes, use the following triangular probability distribution and assume uncorrelated stochastic processes:




**b** For the above case, what is the probability of having bubbles? What is the total ADC input capacitance?

**c** Accepting bubble can only occur at $\pm$1 thermometer code distance, design the bubble error correction (BEC) logic at gate level and verify its behavior with `0` and `1` bubble examples.

**2.4** For the general scheme of a 12-bit sub-range flash ADC with coarse and fine sub-conversion stages, create a table calculating the number of comparator elements according to all possible ENOB splitting cases, as follows:

| Coarse ENOB | Fine ENOB | Coarse ADC elements | Fine ADC elements | Total elements |
|---|---|---|---|---|
| 11 | 1 | ... | ... | ... |
| 10 | 2 | ... | ... | ... |
| ... | ... | ... | ... | ... |

**a** Which is the optimum ENOB splitting between coarse and fine stages?

**b** Expand the same table to include the number of circuit elements of the coarse flash DAC block, which follows the same rule. Does the optimum ENOB splitting remain the same?

**2.5** Consider a 3-stage 1-bit/stage pipeline ADC implemented using the SC circuit seen in theory sessions. For the following case of technology mismatching between sampling and feedback capacitors:

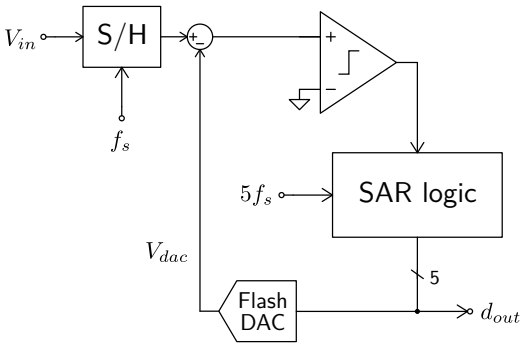
| Stage | #1 | #2 | #3 |
|---|---|---|---|
| $C_s/C_f$ | 0.9 | 1.1 | 1.0 |

**a** Represent the static voltage-to-code transfer function.

**b** Calculate the resulting DNL curve and maximum deviation.

**c** Calculate the resulting INL curve and maximum deviation.

**2.6** Taking the general block scheme of a 5-bit SAR ADC:

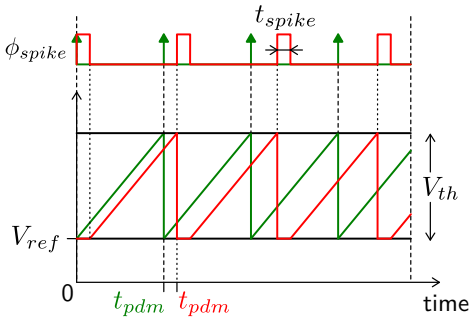



**a** Represent the equivalent state machine diagram for the digital SAR block.

**b** Following the above graph, plot the waveform of DAC feedback $V_{dac}$ for $V_{in}$=0.34375$V_{FS}$.

**c** What is the resulting output code $d_{out}$?

**2.7** For a 10-bit integrate-and-fire ADC operating at 1kS/s sampling rate:




**a** Calculate the maximum INL for a spike reset time of $t_{spike}$=10$\mu$s.

**b** Which is the maximum spike reset time allowed to keep INL below 0.5LSB?

**2.8** Consider the design of a 15-bit delta-sigma ADC with 2nd-order 1-bit single-loop architecture:

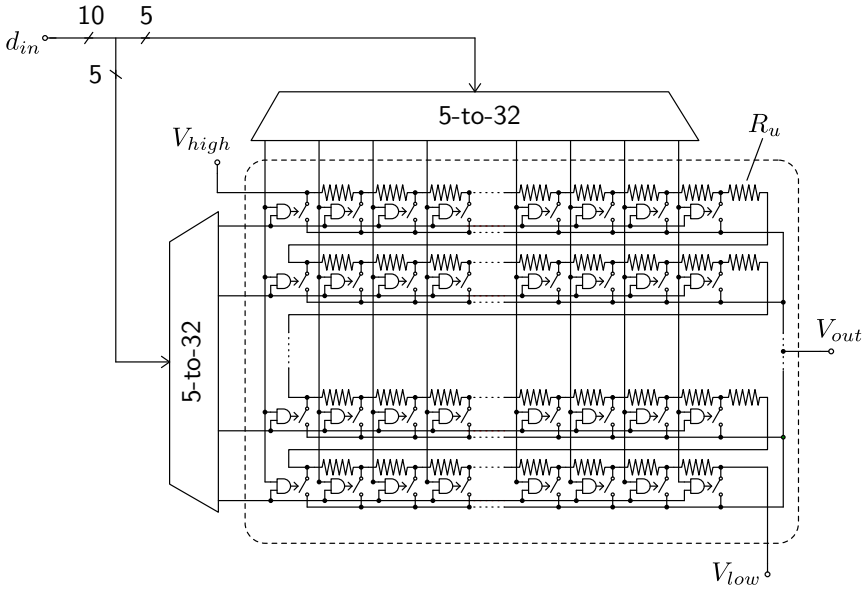
**a** Compute the minimum OSR required.

**b** What will be the improvement in dynamic range if sampling frequency is doubled?

**c** How many levels will require the quantizer to compensate for halving the sampling frequency?

# 3 DAC Architectures and CMOS Circuits

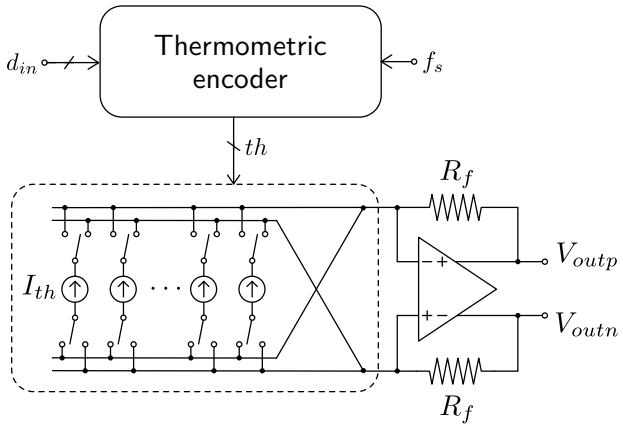
**3.1** For the following 10-bit 10MS/s segmented $R$-element flash DAC with $V_{high}$=3V and $V_{low}$=1V:




**a** Calculate the maximum value for unitary resistive elements $R_u$.

**b** What is the maximum and minimum output impedance?

**3.2** Given a 12-bit 100kHz 2V$_{FS}$ fully-differential SI flash DAC as below:



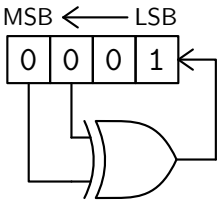

**a** Obtain the maximum value for the feedback resistors $R_f$ for room temperature (300K) operation.

**b** Choose a realistic $R_f$ and calculate the required cell reference current $I_{th}$.

**3.3** For a 4-bit PWM DAC, draw the generated waveform $V_{pdm}$ for $d_{in}$=1000 and the following non-monotonic counter cases:

**a** 4-bit linear feedback shift-register (LFSR) of polynomial $x^4+x^3+1$ and initial seed 0001.

**b** Same as in previous case but flipping counter value from MSB to LSB before comparison at ALU.




**3.4** Calculate the number of full-width logic registers required to implement a 5th-order MASH DAC based on single-bit quantizers.

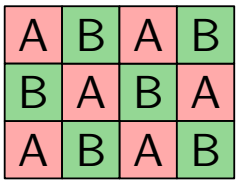
# 4 Full-Custom IC Design Methodology

**4.1** Based on the XSpice code examples given in class and supplied with the lab manual, write the corresponding interface file specification (IFS) and code model (CM) for the following functional blocks:

- **a** A digital AND logic gate with parameters: rise and fall delays and input capacitance.
- **b** An analog slew-rate limiter with parameters: maximum positive and negative slopes.

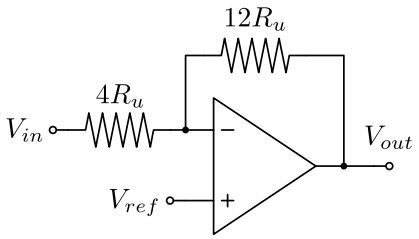
**4.2** An expert layout designer proposes the following physical array structure for a differential pair, whose two transistors (A and B) are segmented in 6 unitary and squared elements:

- **a** Demonstrate that this array structure does not exhibit a common centroid.
- **b** Propose an alternative arrangement compliant with common centroid guidelines.



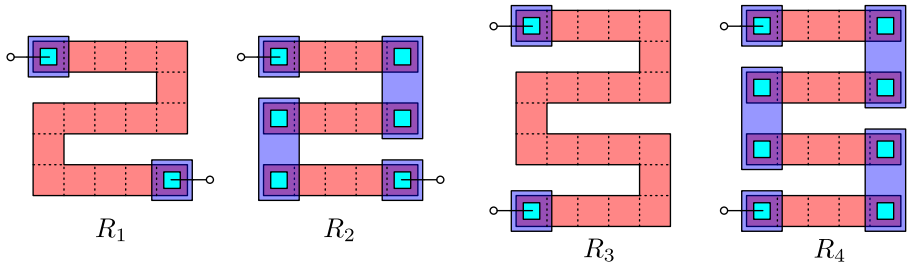

**4.3** Find the best common centroid array for a multiple current mirror with scaling ratios 1:2:4:4 and squared-shape unitary transistor elements. Also, consider the use of dummy elements.

**4.4** For the following inverter amplifier with linear gain $\times 3$:



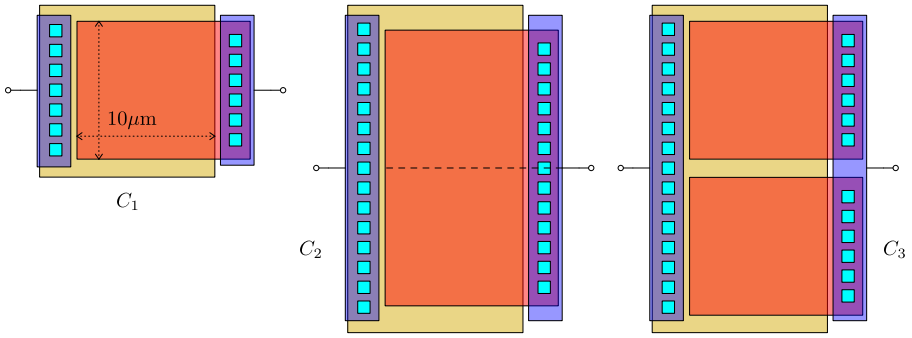

- **a** Draw a common-centroid array for both resistors in case of squared unitary elements, i.e. $(L/W)_u$=1.
- **b** Same as in previous point but for $(L/W)_u$=4.

**4.5** Given the 3-to-4 times scaled resistors shown below, where metal resistivity can be neglected:




- **a** Compute matching ratios $R_3/R_1$ and $R_4/R_2$.
- **b** Which layout style ensures more accurate scaling?

**4.6** A switched-capacitor circuit requires a 2:1 PiP capacitors for a CMOS technology with overlap and fringing capacitances $C_{ua}$=0.42fF/$\mu$m$^2$ and $C_{up}$=0.041fF/$\mu$m, respectively.




**a** What are the real matching ratios $C_2/C_1$ and $C_3/C_1$?

**b** Propose a $2C_1$ single shape element.

# 5 CMOS Operational Amplifiers

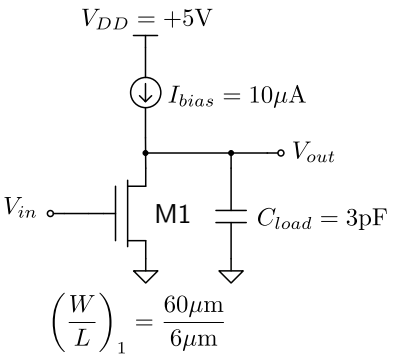
**5.1** The following single-transistor Opamp is being integrated in CNM25 CMOS technology (i.e. $\beta = 59\frac{W}{L}\mu$A/V$^2$ and $n = 1.5$, while $\lambda = 0.2$V$^{-1}$ for $L = 3\mu$m):

**a** Is M1 working in strong inversion (above threshold)?

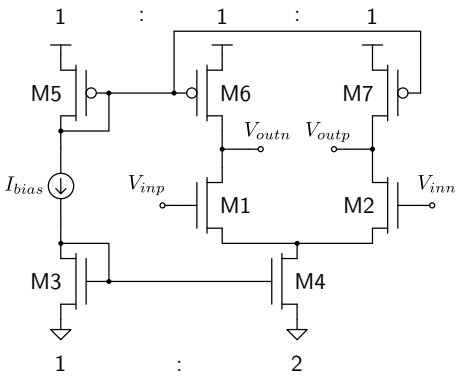
**b** Calculate $G(DC)$. How will this value change in case $I_{bias}$ and (W/L)$_1$ are doubled?

**c** Draw the equivalent Bode plot indicating values for $BW$ and $GBW$. What would happen under same changes as in **b**?

**d** Considering thermal noise only and ideal full scale, find the equivalent number of bits (ENOB) required by the ADC at the output of the OpAmp.




**5.2** Given the fully-differential single-stage OpAmp shown below to be integrated in CNM25 technology (i.e. $\beta = 59\frac{W}{L}\mu$A/V$^2$ and $n = 1.5$, while $\lambda = 0.2$V$^{-1}$ for $L = 3\mu$m):




**a** If we want to achieve

$$CMRR = \frac{g_{mg1,2}}{2\Delta g_{mg1,2}}\left(\frac{2ng_{mg1,2}}{g_{md4}} + 1\right) > 80\text{dB},$$

what is the maximum mismatching in % of the input pair transconductance acceptable for $I_{bias} = 10\mu$A, $(W/L)_{all} = 15$ and $L_{all} = 6\mu$m?

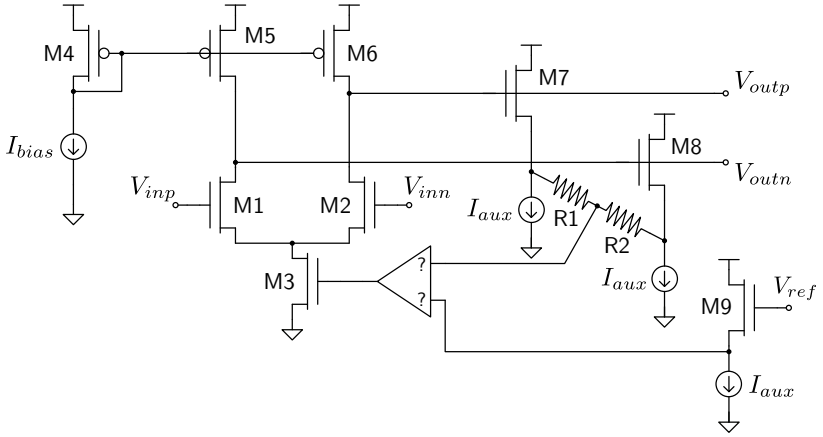
**b** In the event of dealing with 5% mismatching due to area restrictions, how would you compensate it by design in order to reach the target $CMRR$?

**5.3** Taking the OpAmp of previous exercise, a CMFB loop based on resistive dividers is added to stabilize the output common-mode level at $V_{ref} = V_{DD}/2$:

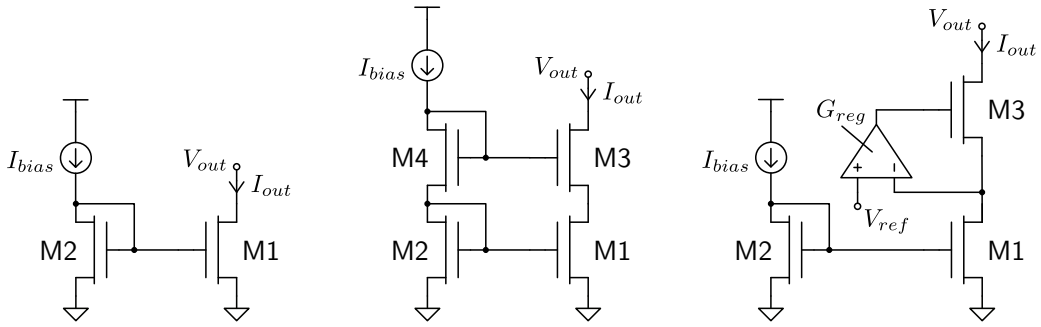
**a** Choose the correct sign of the feedback OpAmp to ensure CMFB stability.

**b** Compare the expression of OpAmp differential output range with and without this control loop.

**c** Find the design constraint to avoid any losses in the output range due to CMFB.




**5.4** Classic, cascode and regulated cascode current sources with $I_{bias}$=10$\mu$A, $(W/L)$=$\frac{30\mu m}{3\mu m}$ and $G_{reg}$=50 are designed for CNM25 technology ($V_{TH}$=1V, $\beta = 59\frac{W}{L}\mu$A/V$^2$, $n = 1.5$ and $\lambda|_{L\equiv 3\mu m} = 0.2$V$^{-1}$):

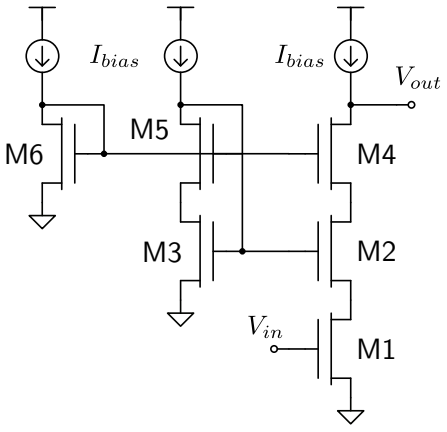



**a** Calculate the output resistance of each current source.

**b** Obtain the minimum output voltage to operate them and find the optimum value for $V_{ref}$.

**c** Draw a comparative plot of their output $I/V$ curves.

**5.5** Imagine you are designing a single-stage single-ended double-cascode OpAmp as shown here:



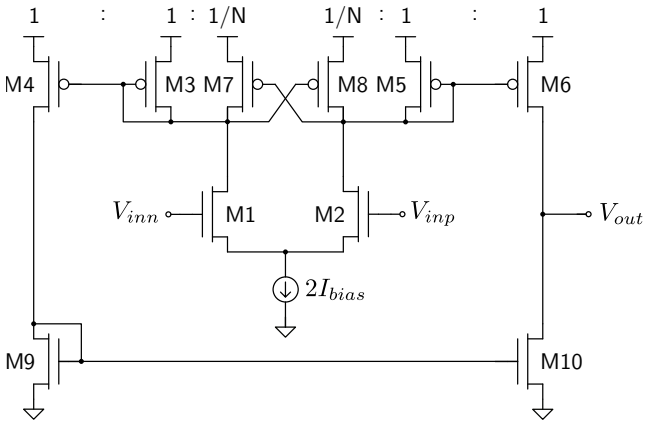

**a** Find the optimal matching ratios between transistors in order to maximize the voltage output range. Can you generalize the matching rule for $N$-cascode topologies?

**b** What is the expression of the output resistance and DC voltage gain compared to the single-transistor OpAmp?

**5.6** Consider the following folded OpAmp with cross-coupled transconductance boosting to be integrated in CNM25 technology (i.e. $A_{VTH}$=30mV$\mu$m). If all transistors are sized at $(W/L)$=10 and $I_{bias}$=10$\mu$A:

**a** Build a table with the required $N$ ratios for +6dB, +12dB and +18dB gain improvements.

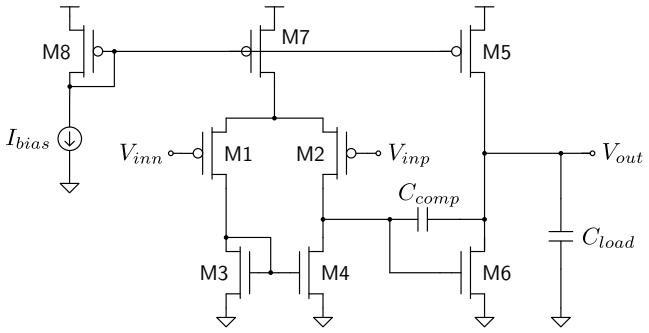
**b** What is the minimum device area to ensure technology mismatching causes $\sigma(\Delta G) \leq$ 3dB?




**5.7** For the following differential to single ended two-stage Miller Opamp to be optimized for CNM25 technology (i.e. $\beta_{N,P} = \{59, 20\}\frac{W}{L}\mu$A/V$^2$, $n = 1.5$, $\lambda|_{L\equiv 3\mu\text{m}} = 0.2\text{V}^{-1}$):

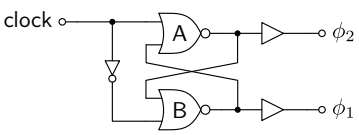
**a** Define the minimum set of design variables for device sizing and biasing.

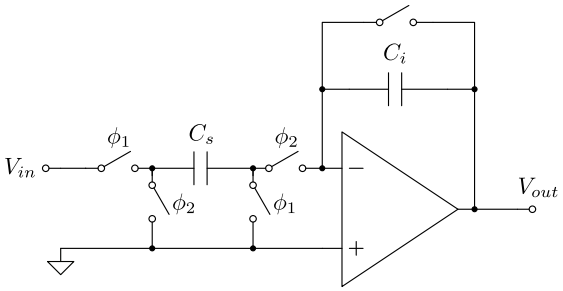
**b** Find a complete solution to verify $G(DC)\geq$60dB, $GBW\geq$1MHz, $SR\pm\geq$1.5V/$\mu$s and $m\phi\geq$60° for $C_{load}$=10pF.




# 6 Delta-Sigma Modulators for ADC

**6.1** Consider the following logic circuit as a clock splitter to generate the phase signals needed by the typical switched-capacitor integrator used in discrete-time DSMs:




**a** Analyze the operation of the clock splitter and draw the equivalent chronogram to demonstrate it generates the correct non-overlapping sequence of phase signaling.

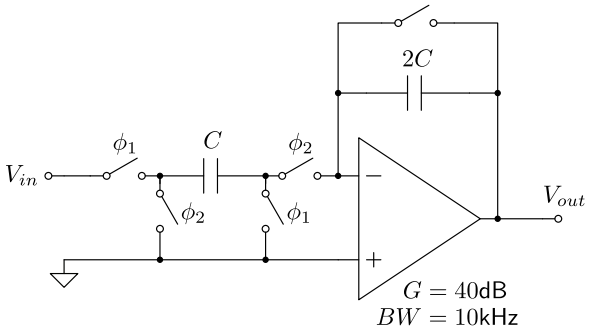
**b** What are the non-overlapping times in terms of gate delays $t_{dA}$ and $t_{dB}$?

**6.2** For the following switched-capacitor basic building block of a 1MS/s DSM ADC:

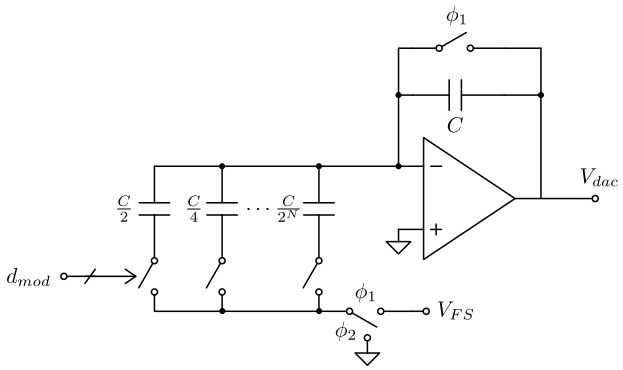
**a** Draw the equivalent model in terms of $Z$-domain blocks for the ideal case (i.e. $G \to \infty$ and $BW \to \infty$).

**b** Same as previous point, but incorporating now the second-order effects due to the limited-performance OpAmp.

**c** Is the resulting SC integrator still linear?




**6.3** A multi-bit single-loop DSM for ADC is built using the switched-capacitor feedback DAC shown below:




**a** Analyze the circuit from the charge viewpoint to find the expression of $V_{dac}$ as a function of $d_{mod}$.

**b** What is the maximum DAC output compared to full-scale $V_{FS}$?

**c** What modification would you recommend to ensure $V_{dac}$ can reach $V_{FS}$?