7. Application Specific ROICs for Smart Sensors

Francesc Serra Graells

francesc.serra.graells@uab.cat
Departament de Microelectrònica i Sistemes Electrònics
Universitat Autònoma de Barcelona

paco.serra@imb-cnm.csic.es
Integrated Circuits and Systems
IMB-CNM(CSIC)

1. High-Resolution SC Delta-Sigma ADC for Space Applications
2. Compact Pixel Integrating ADC for X-Ray Imagers
3. Low-Power Potentiostatic CT Delta-Sigma ADC for Electrochemical Integrated Sensors

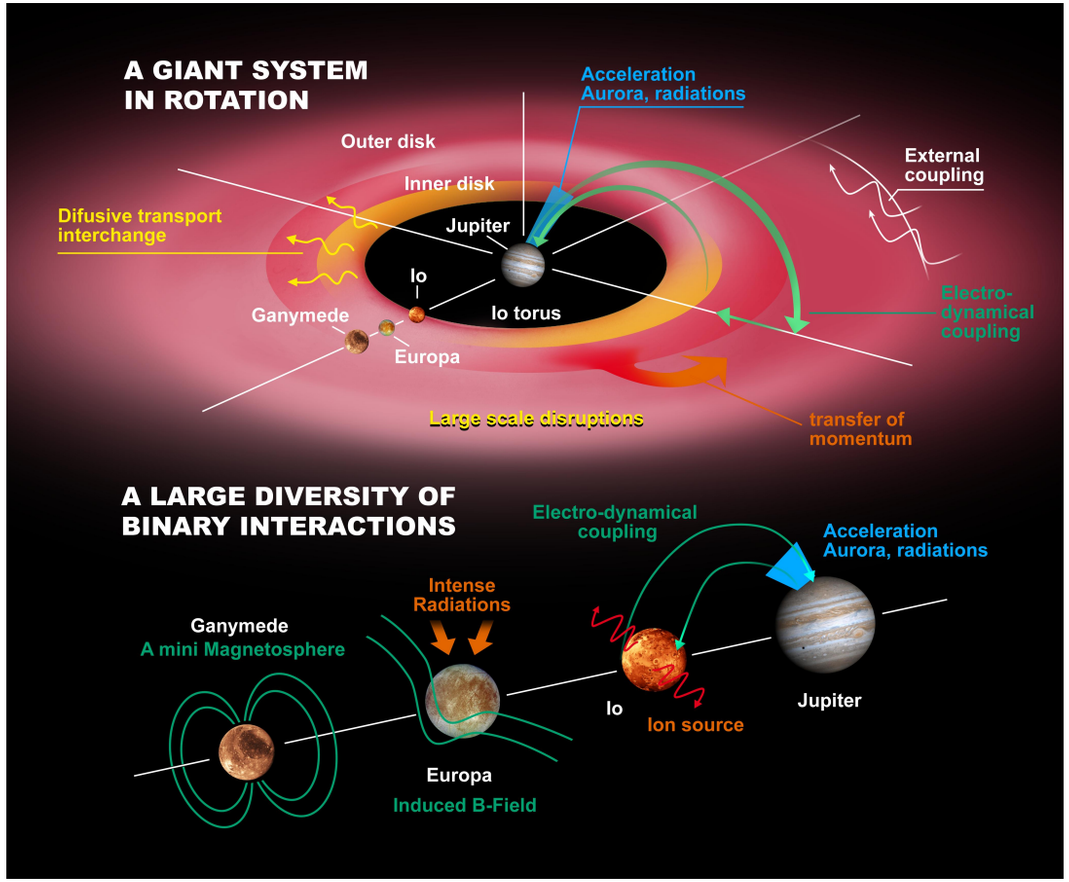
1 High-Resolution SC Delta-Sigma ADC for Space Applications

2 Compact Pixel Integrating ADC for X-Ray Imagers

3 Low-Power Potentiostatic CT Delta-Sigma ADC for Electrochemical Integrated Sensors

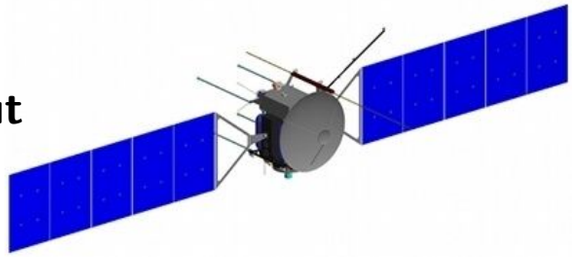
ESA Cosmic Vision JUICE

- **Cosmic Vision** is ESA 2015-2025 planning for space science missions
- Jupiter Icy Moons Explorer (**JUICE**) L-class mission launched in 2023 (7.6y cruise & 3.5y in the Jovian system)
- Primary mission themes:
  - Emergence of **habitable worlds** around gas giants
  - **Jupiter** system as an archetype for gas giants
- Science instrument payload:
  - **JANUS** - Optical camera system
  - **MAJIS** - Moons and Jupiter Imaging Spectrometer
  - **GALA** - GAnymede Laser Altimeter
  - **RIME** - Radar for Icy Moons Exploration
  - **J-MAG** - A magnetometer for JUICE
  - **RPWI** - Radio & Plasma Wave Investigation
  - **PRIDE** - Planetary Radio Interferometer & Doppler Experiment
  - ...



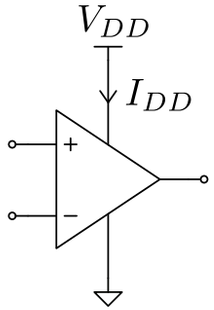
↗ sci.esa.int/web/juice

▼ Next generation of **read-out electronics** is needed!



Low-Power High-Res ADC

- Low-voltage vs **low-current** design?



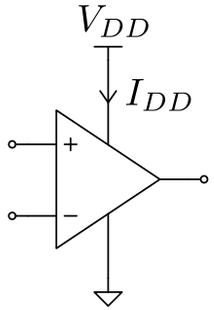
$$P_{DD} = V_{DD} \times I_{DD}$$

- Alternative supply **sources** (battery, solar cell, scavenging)
- **Poor** power scaling
- Limited by **technology**
- **Circuit techniques**: rail-to-rail, inverter-base, supply multipliers, back gate...

- **Strong** power savings
- Limited by **noise** and **bandwidth**
- **Circuit techniques**: subthreshold operation, Class-AB, dynamic biasing, low duty cycle...

Low-Power High-Res ADC

- Low-voltage vs **low-current** design?



$$P_{DD} = V_{DD} \times I_{DD}$$

- Alternative supply **sources** (battery, solar cell, scavenging)
- **Poor** power scaling
- Limited by **technology**
- **Circuit techniques**: rail-to-rail, inverter-base, supply multipliers, back gate...

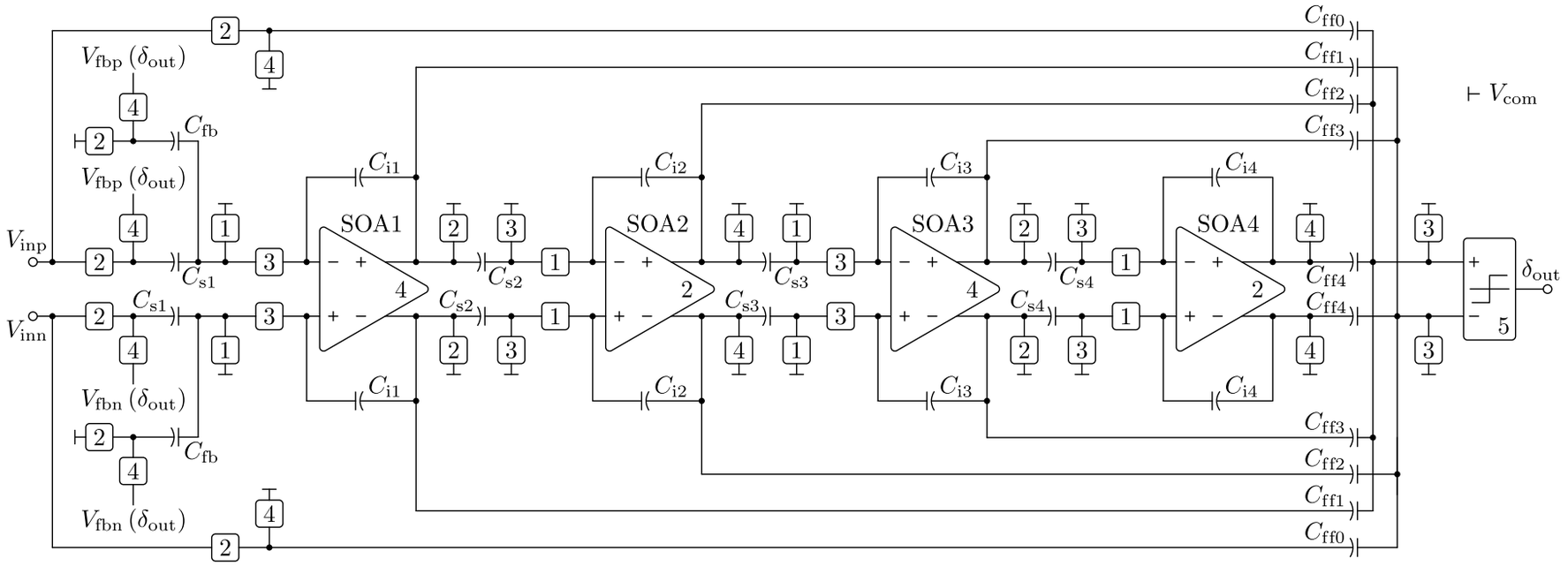
- **Strong** power savings
- Limited by **noise** and **bandwidth**
- **Circuit techniques**: subthreshold operation, Class-AB, dynamic biasing, low duty cycle...

- State-of-art **extended-DR** SC circuits for DSM ADCs [1-6]:
  - **Clock bootstrapping** to reduce switch non-linearity [3-5]
  - **High-voltage devices** at input sampler to increase signal full scale [1,6]
  - **Multi-bit quantization** with analog calibration or digital post-processing due to mismatching [6]

- **Rad-Hard** 1.8V 0.18µm 1P6M CMOS technology

DSM Architecture

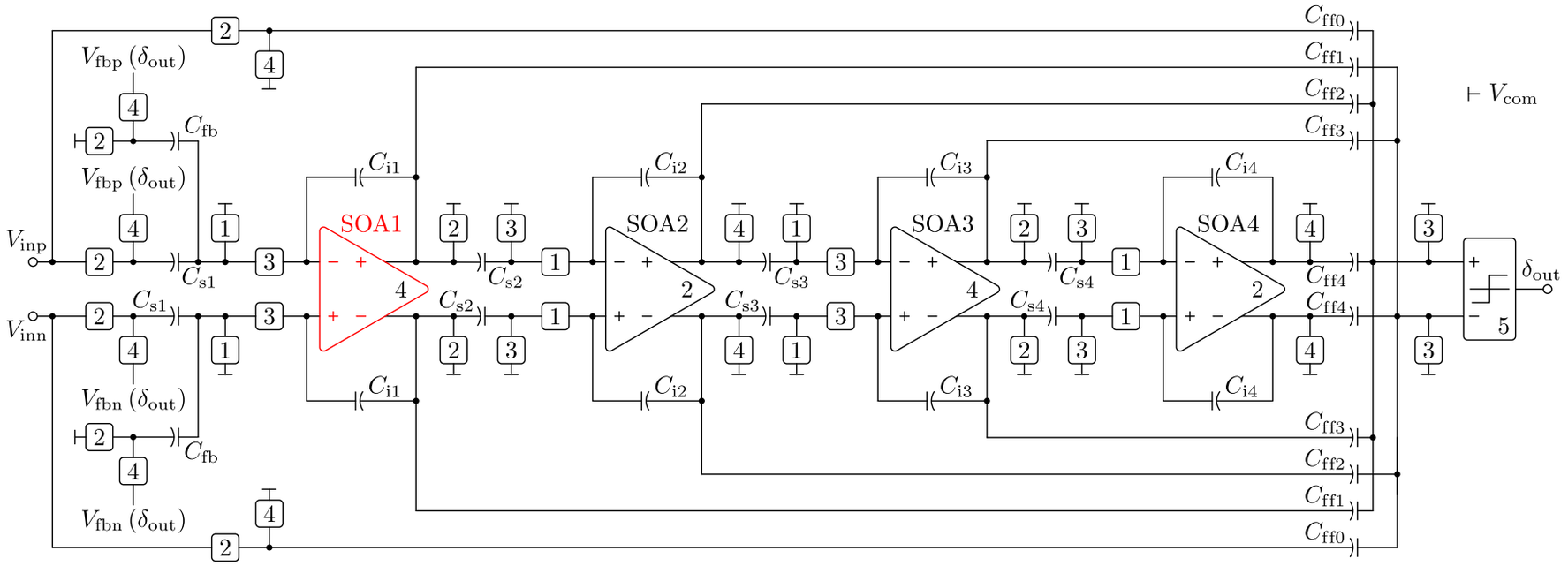
- **4th-order** single-loop 1-bit topology for >**90dB**-SNDR and **50kHz**-bandwidth:



- **Multiple feedforward paths** to relax signal headroom at OpAmps output [7]
- **Two-level quantization** is intrinsically linear and allows passive adder [5]
- High shaping order to compensate **oversampling**: $OSR = 136 \quad f_s = 13.6\text{MS/s}$

DSM Architecture

- **4th-order** single-loop 1-bit topology for >**90dB**-SNDR and **50kHz**-bandwidth:

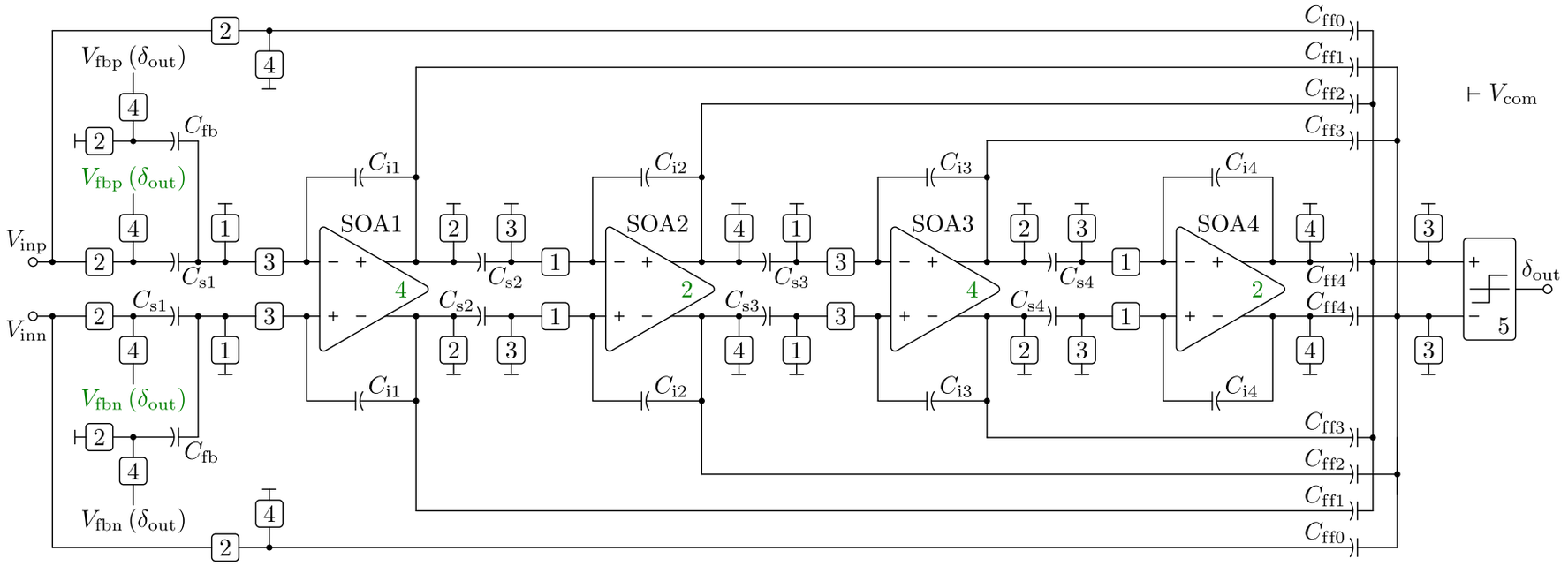


- **Large capacitor sizing** [pF] according to kT/C specs and optimal coefficients [8]:

Capacitance	Value	Capacitance	Value	Capacitance	Value
C_{ff0}	0.92	C_{fb}	21.16		
C_{ff1}	0.92	C_{s1}	42.32	C_{i1}	211.6
C_{ff2}	0.92	C_{s2}	3.68	C_{i2}	9.2
C_{ff3}	0.92	C_{s3}	0.92	C_{i3}	9.2
C_{ff4}	1.84	C_{s4}	0.92	C_{i4}	9.2

DSM Architecture

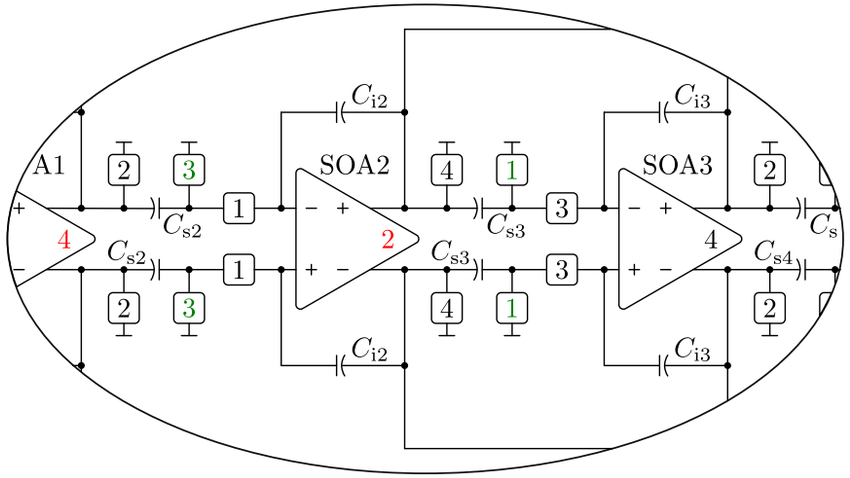
- **4th-order** single-loop 1-bit topology for >**90dB**-SNDR and **50kHz**-bandwidth:

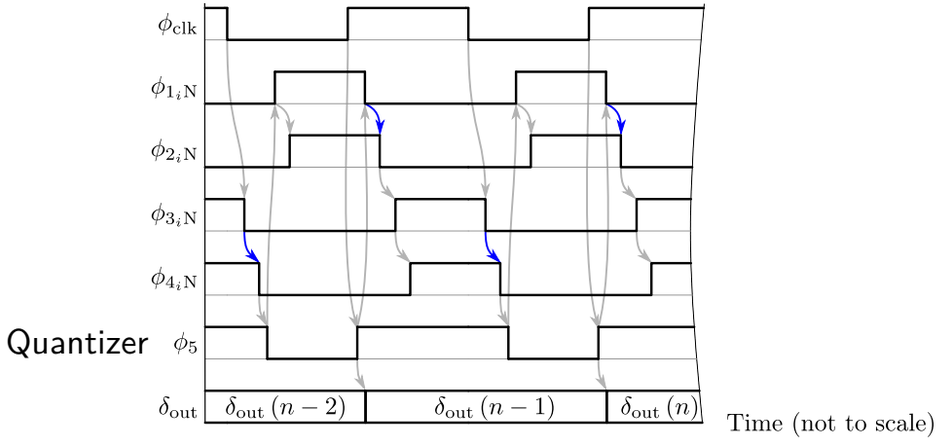


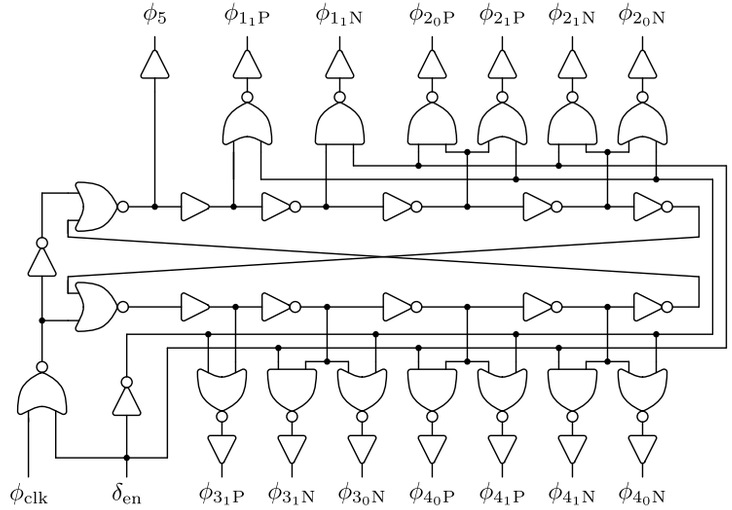
- Feedback DAC **shares** capacitor with input sampler to reduce overall area
- **Switched-OpAmp** (SOA) for replacing critical switches and 50% duty cycle [9]

DSM Architecture

- **4th-order** single-loop 1-bit topology for >**90dB**-SNDR and **50kHz**-bandwidth:



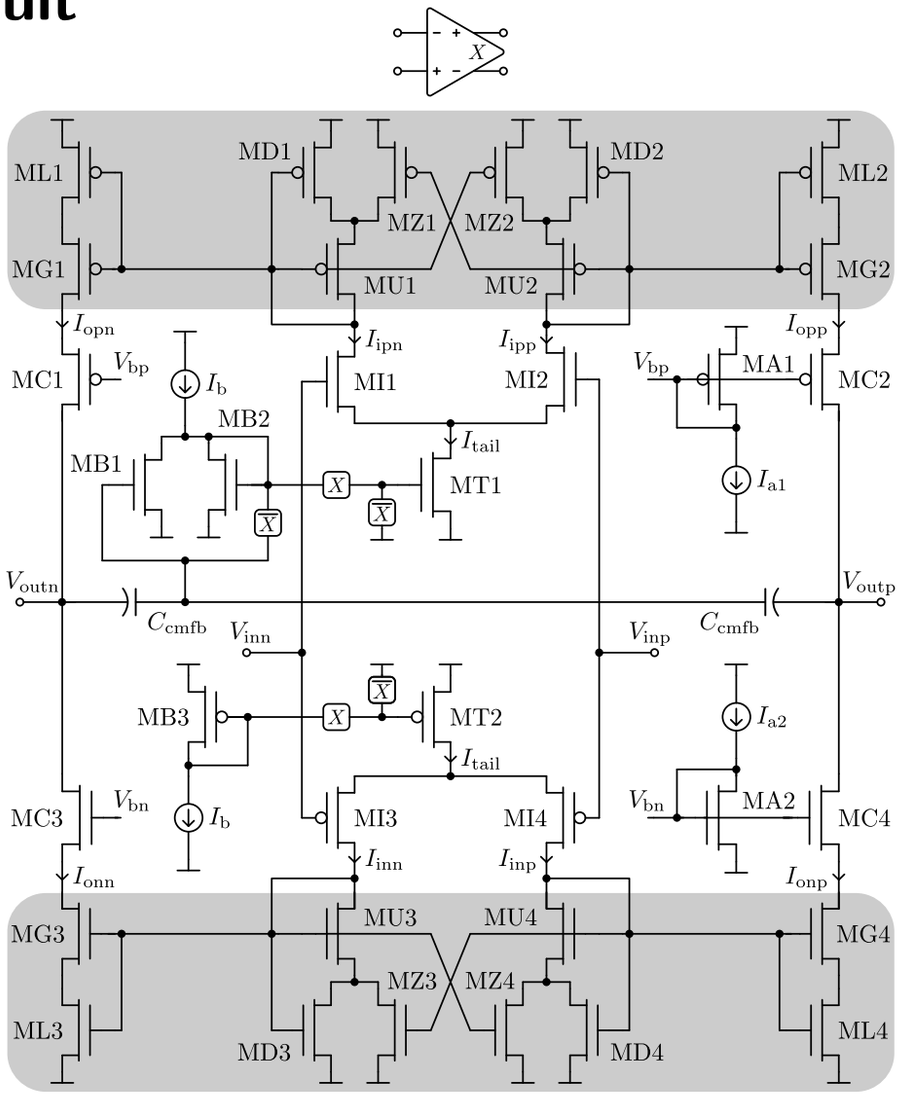




- **(4+1)-phase** switching scheme to avoid signal-dependent charge injections that would cause distortion [8]

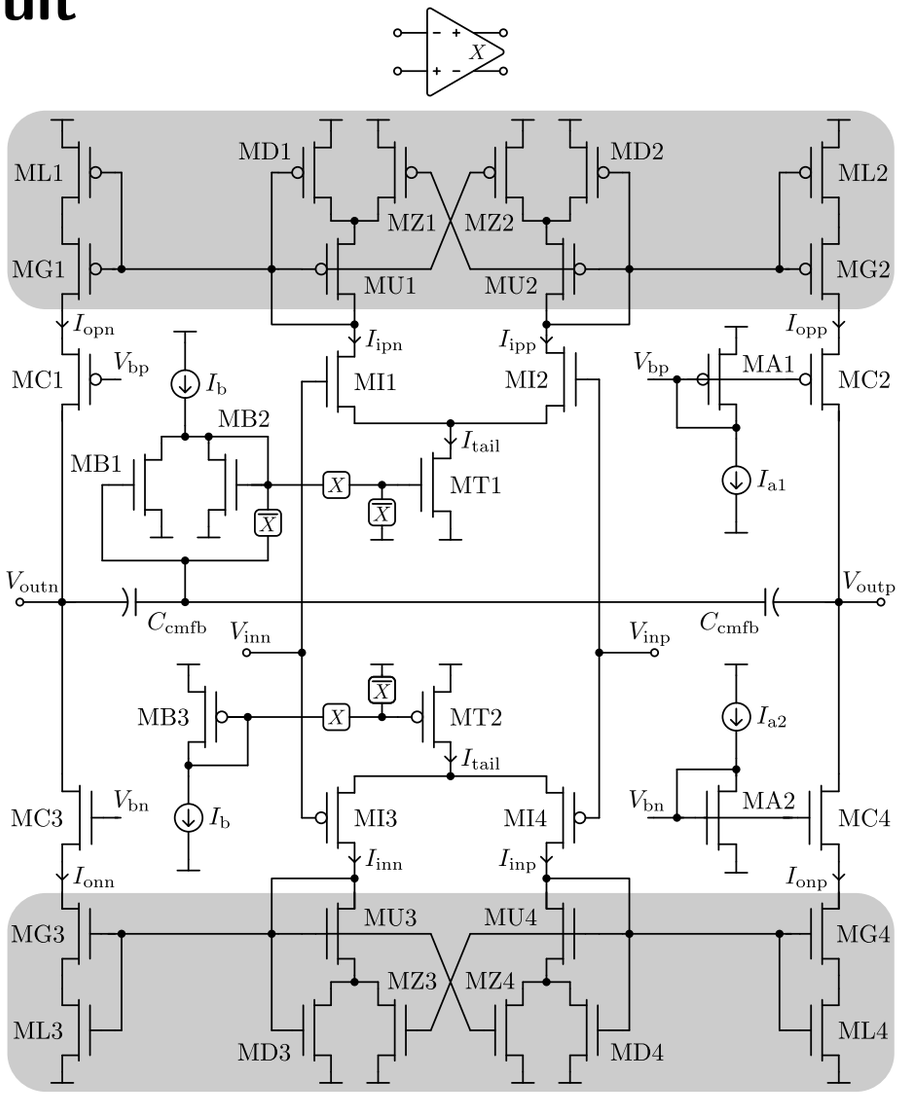
Switched-OpAmp Circuit

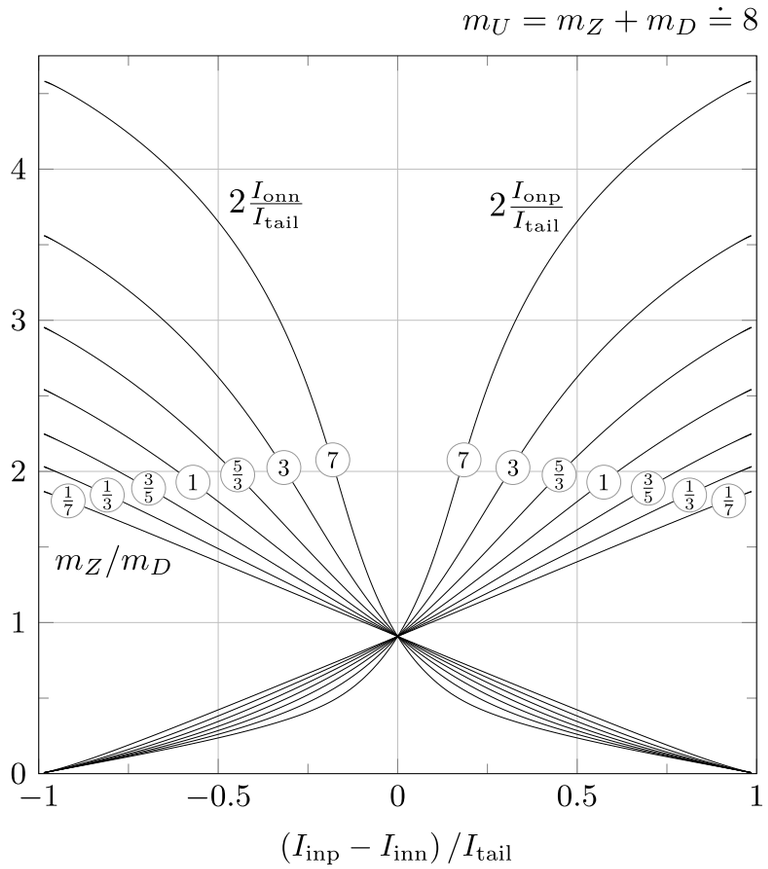
- Low-power **Class-AB** single-stage design
- Complementary non-linear current mirrors with **partial positive** feedback
- Class-AB current in output transistors **only**
- No-need for Miller **compensation** capacitor
- Fast switched-OpAmp **on/off-power** operation



Switched-OpAmp Circuit

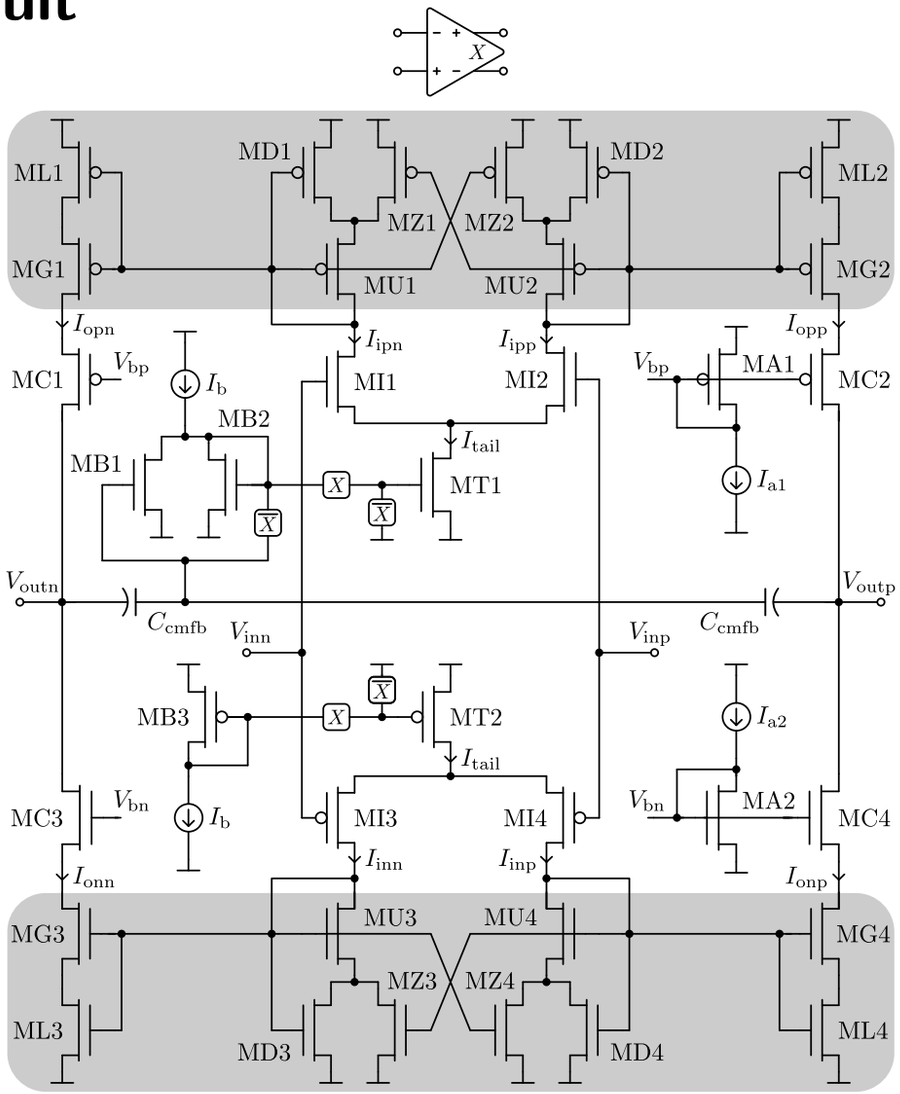
- Low-power **Class-AB** single-stage design
- Complementary non-linear current mirrors with **partial positive** feedback
- Class-AB current in output transistors **only**
- No-need for Miller **compensation** capacitor
- Fast switched-OpAmp **on/off-power** operation
- Simple analytic design based on **matching ratios**

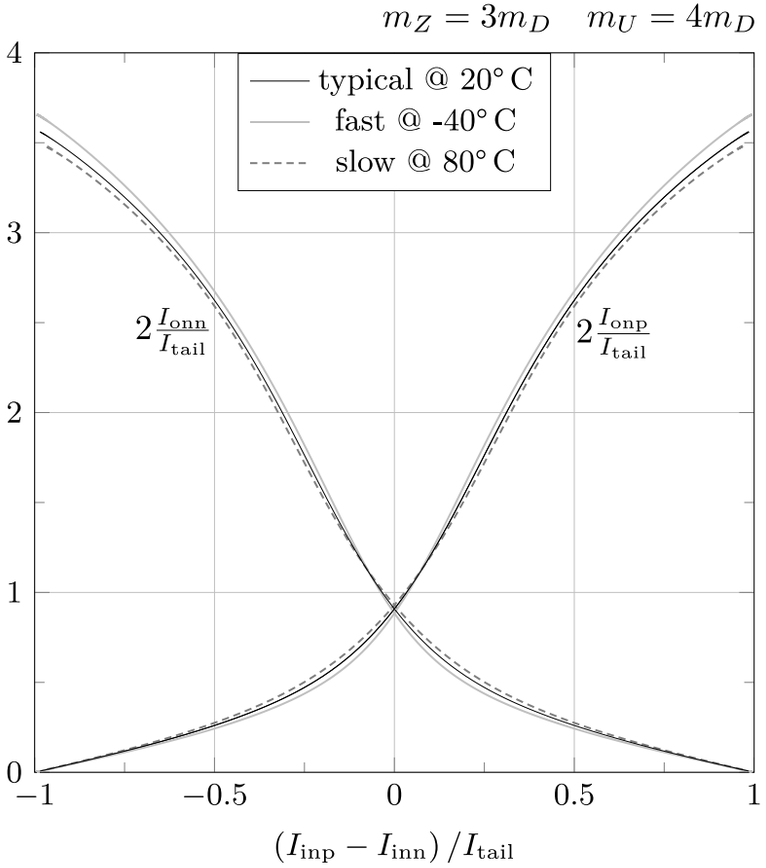




Switched-OpAmp Circuit

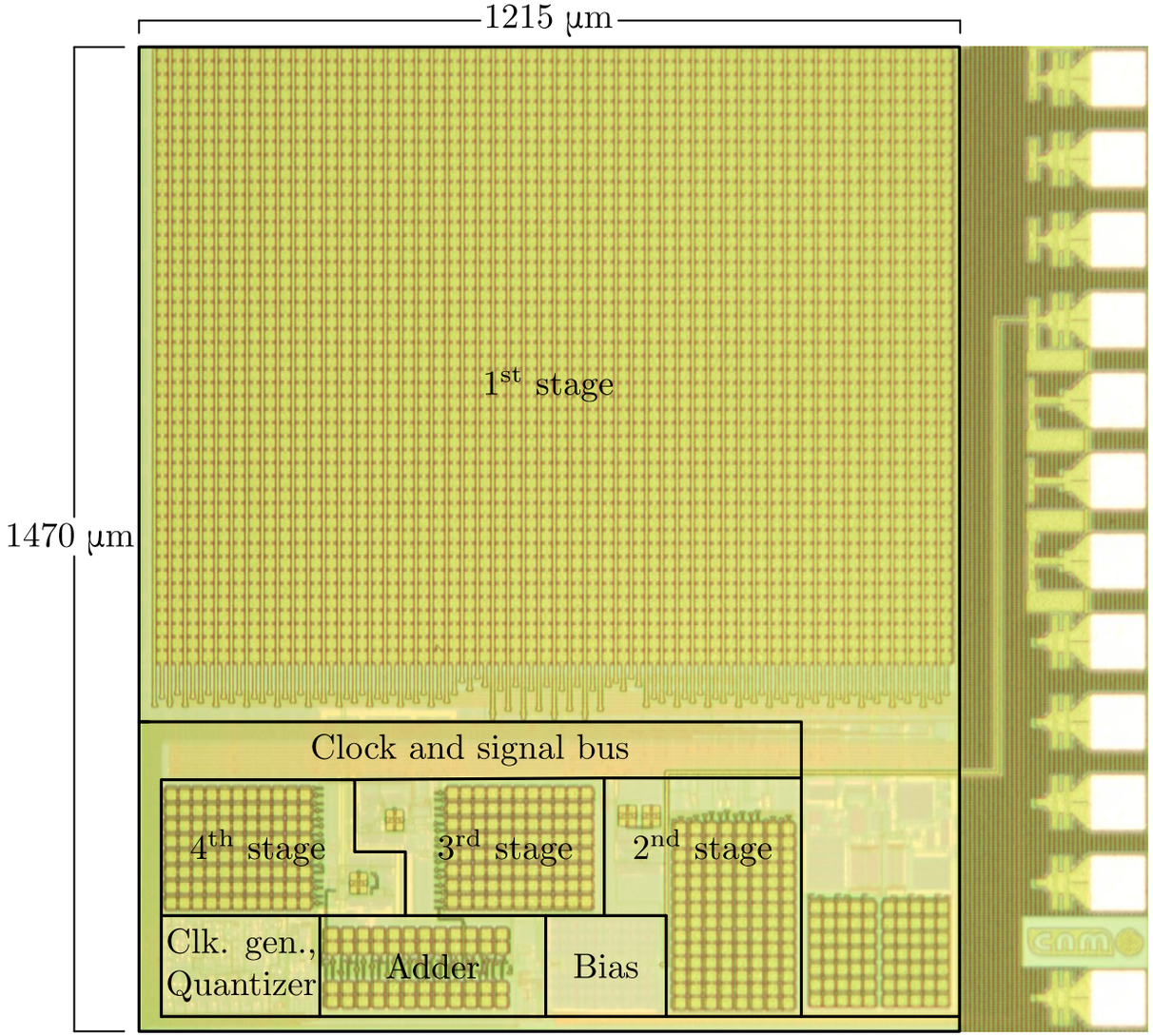
- Low-power **Class-AB** single-stage design
- Complementary non-linear current mirrors with **partial positive** feedback
- Class-AB current in output transistors **only**
- No-need for Miller **compensation** capacitor
- Fast switched-OpAmp **on/off-power** operation
- Simple analytic design based on **matching ratios**
- **Low sensitivity** to CMOS technology deviations





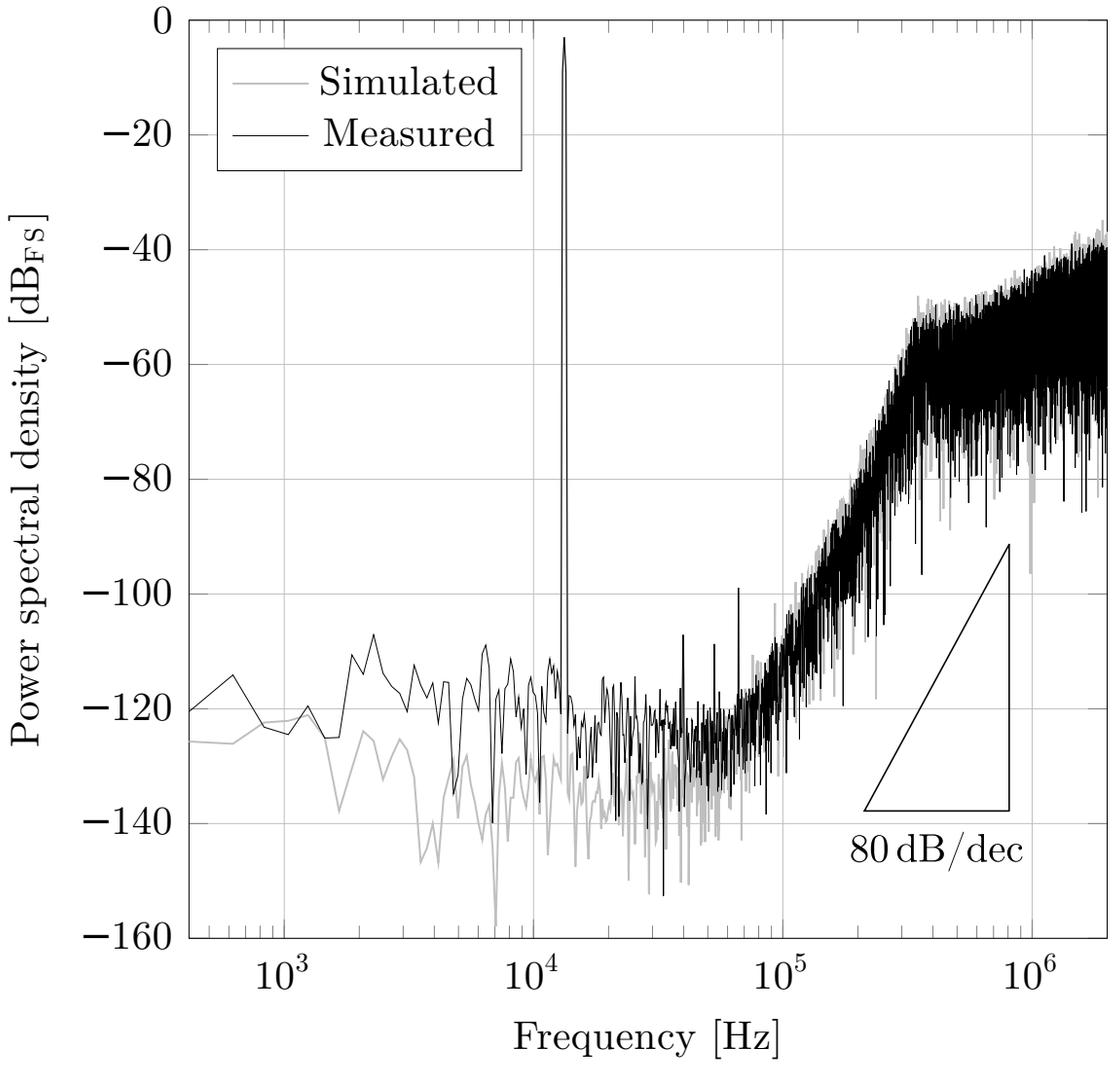
DSM CMOS Integration

- **Rad-Hard** 1.8V 0.18µm 1P6M CMOS technology
- Metal-insulator-metal (**MIM**) capacitors
- **1.8mm²** overall area



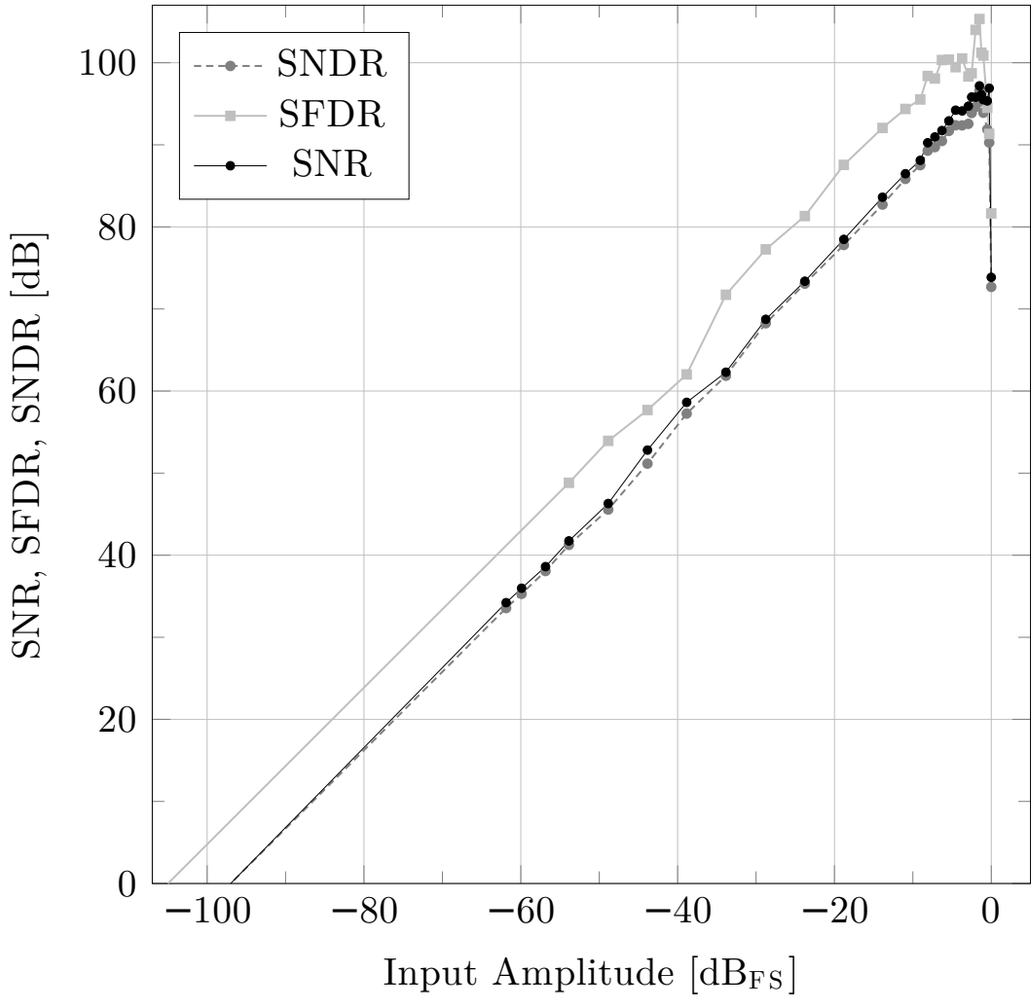
Experimental Results

- Power spectral density at -**2dB** full scale



Experimental Results

- Power spectral density at -**2dB** full scale
- **$SNDR_{max}$=96.6dB**, $SFDR_{max}$=105.3dB, and DR=97dB at 13.28kHz
- **$2.4V_{pp}$** input full-scale
- **7.9mW** at 1.8V
- **Non-bootstrapped** supply to avoide device stress
- **Calibration-free** operation to increase ADC robustness



Comparison with High-Res ADCs

- Schreier **FOM** comparison: $FOM_S[\text{dB}] \doteq SNDR[\text{dB}] + 10\log(BW/P)$

	[1]	[2]	[3]	[4]	[5]	[6]	**This work**	
Architecture	$\Delta\Sigma$ SC	$\Delta\Sigma$ CT+SC	$\Delta\Sigma$ SC	$\Delta\Sigma$ SC	$\Delta\Sigma$ SC	Pipe+ SAR	$\Delta\Sigma$ SC	
Technology	0.25	0.18	0.18	0.18	0.35	0.18	0.18	μm
Supply voltage		3.3	1.8	0.7	1.5	5, 1.8	1.8	V
Diff. full scale	6.6	5.7				10	2.4	V_{pp}
Sampling rate	20	6.14	45.2	5	2.4	5	13.6	MS/s
Bandwidth	1000	20	500	25	20	2500	50	kHz
Supply power	475	37	38	0.87	0.14	30.5	7.9	mW
Area	20.2	0.65	3.5	2.16	0.21	5.74	1.8	mm^2
DR	103	102	90.1	100	92.6	100.2	97	dB
$SFDR_{max}$			97				105.3	dB
$SNDR_{max}$		95	86.3	95	87.9	98.6	96.6	dB
FOM	(166.2)	152.3	157.5	169.6	169.5	177.7	164.6	dB
Bootstrap-free	Yes	Yes	No	No	No	Yes	Yes	
Calibration-free	Yes	Yes	Yes	Yes	Yes	No	Yes	

↗ S. Sutula, et al.
A Calibration-Free 96.6-dB-SNDR Non-Bootstrapped 1.8-V 7.9-mW Delta-Sigma Modulator with Class-AB Single-Stage Switched VMAs
IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, May 2016
doi.org/10.1109/ISCAS.2016.7527170

References

[1] R. Brewer, J. Gorbold, P. Hurrell, C. Lyden, R. Maurino, and M. Vickery, "A 100dB SNR 2.5MS/s Output Data Rate ΔΣ ADC," in Proceedings of the IEEE International Solid-State Circuits Conference, 2005, pp. 172–173.

[2] P. Morrow, M. Chamarro, C. Lyden, P. Ventura, A. Abo, A. Matamura, M. Keane, R. O'Brien, P. Minogue, J. Mansson, N. McGuinness, M. McGranaghan, and I. Ryan, "A 0.18µm 102dB-SNR Mixed CT SC Audio-Band ΔΣ ADC," in Proceedings of the IEEE International Solid-State Circuits Conference, 2005, pp. 178–592.

[3] A. Agah, K. Vleugels, P. Griffin, M. Ronaghi, J. Plummer, and B. Wooley, "A High-Resolution Low-Power Oversampling ADC with Extended-Range for Bio-Sensor Arrays," in Symposium on VLSI Circuits Digest of Technical Papers, 2007, pp. 244–245.

[4] H. Park, K. Nam, D. K. Su, K. Vleugels, and B. A. Wooley, "A 0.7-V 100-dB 870-µW Digital Audio ΔΣ Modulator," in Symposium on VLSI Circuits Digest of Technical Papers, 2008, pp. 178–179.

[5] T. Christen, "A 15bit 140 µ W Scalable-Bandwidth Inverter-Based Audio ΔΣ Modulator with >78dB PSRR," in Proceedings of the European Solid-State Circuits Conference, 2012, pp. 209–212.

[6] A. Bannon, C. Hurrell, D. Hummerston, and C. Lyden, "An 18 b 5 MS/s SAR ADC with 100.2 dB Dynamic Range," in Symposium on VLSI Circuits Digest of Technical Papers, 2014, pp. 1–2.

[7] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "A wideband low-distortion Delta-Sigma ADC topology," IEEE Electronics Letters, vol. 37, pp. 737–738, 2001.

[8] L. Yao, M. Steyaert, and W. Sansen, "A 1-V, 1-MSs, 88-dB Sigma-Delta Modulator in 0.13-µm Digital CMOS Technology," in Symposium on VLSI Circuits Digest of Technical Papers, 2005, pp. 180–183.

[9] J. Crols and M. Steyaert, "Switched-OpAmp: An Approaach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages," IEEE J. Solid-State Circuits, vol. 29, no. 8, pp. 936–942, Aug 1994.

[10] P. Aguirre and F. Silveira, "Bias Circuit Design for Low-Voltage Cascode Transistors," in Proceedings of the 19th Annual Symposium on Integrated Circuits and Systems Design, 2006, pp. 94–97.

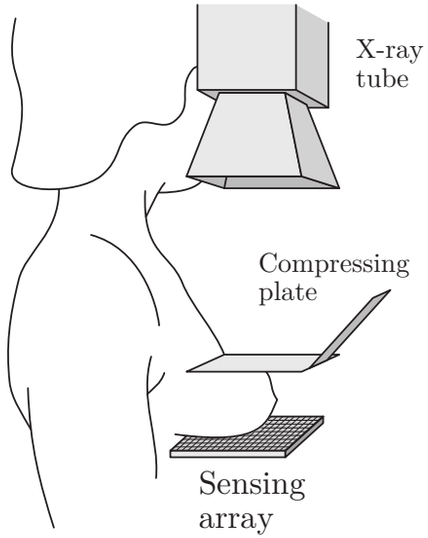
1 High-Resolution SC Delta-Sigma ADC for Space Applications

2 Compact Pixel Integrating ADC for X-Ray Imagers

3 Low-Power Potentiostatic CT Delta-Sigma ADC for Electrochemical Integrated Sensors

Direct X-Ray Digital Imagers

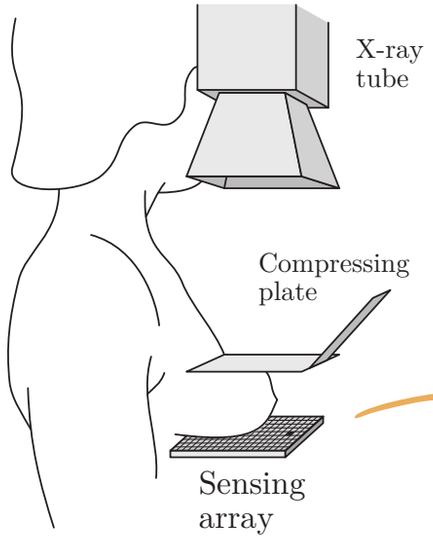
- Low-energy (<20keV) medical applications: e.g. **Mammography**



  - High **dynamic range** (e.g. 10-bit) and high **spatial resolution** (e.g. 50µm-pitch) to identify microcalcifications
  - **High-speed** A/D conversion for low-dose X-ray exposure
  - **Low-power** circuit consumption to prevent heating X-ray detector

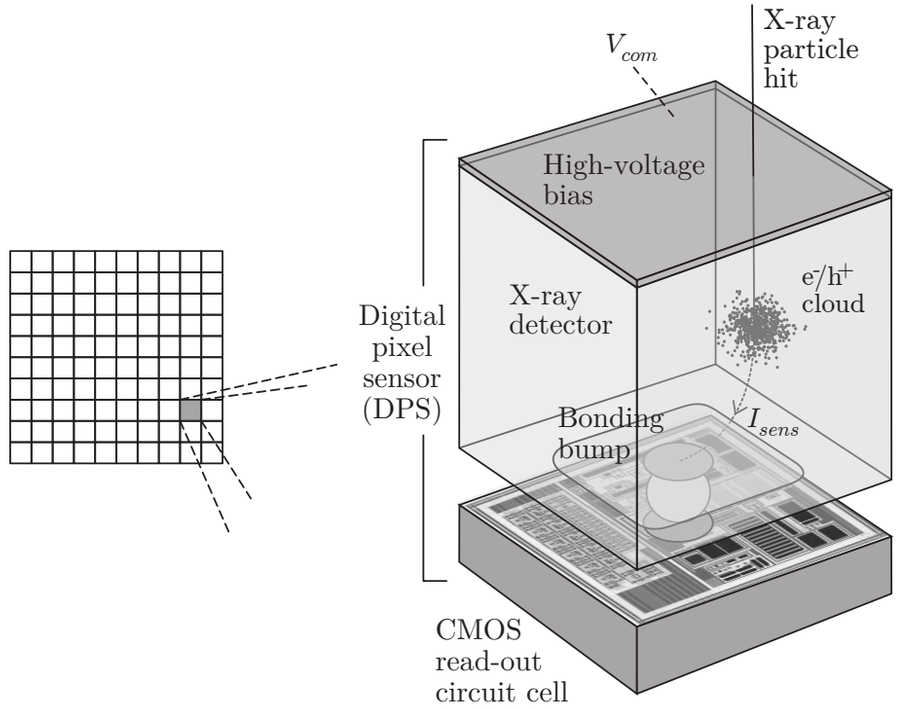
Direct X-Ray Digital Imagers

- Low-energy (<20keV) medical applications: e.g. **Mammography**



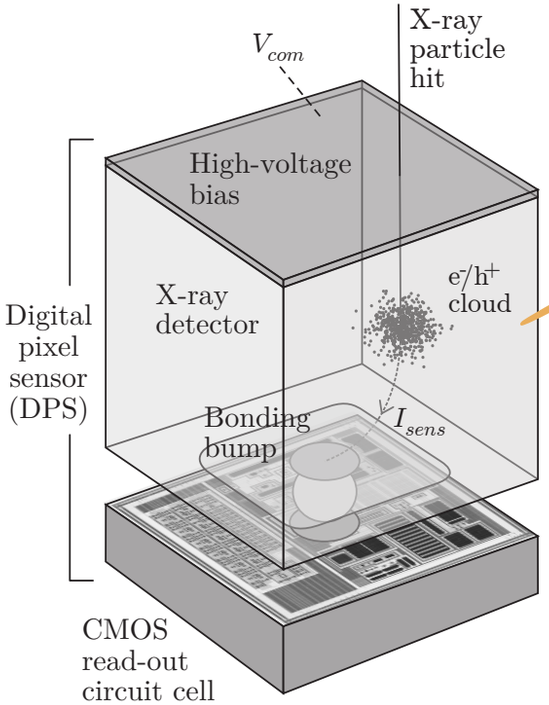
- High **dynamic range** (e.g. 10-bit) and high **spatial resolution** (e.g. 50µm-pitch) to identify microcalcifications
- **High-speed** A/D conversion for low-dose X-ray exposure
- **Low-power** circuit consumption to prevent heating X-ray detector

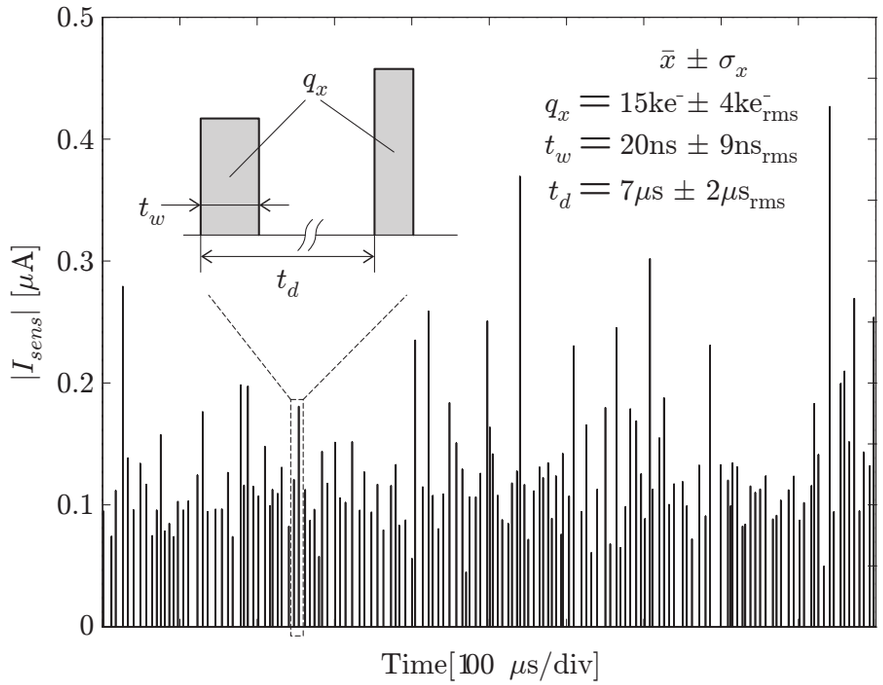
- **Digital pixel sensor** (DPS) = X-ray detector (e.g. CdTe or Si) + CMOS read-out circuit



- Pixel-by-pixel **bump-bonding** (bump-growing + flip-chip):
  - High **filling** factors
  - **Expensive** packaging

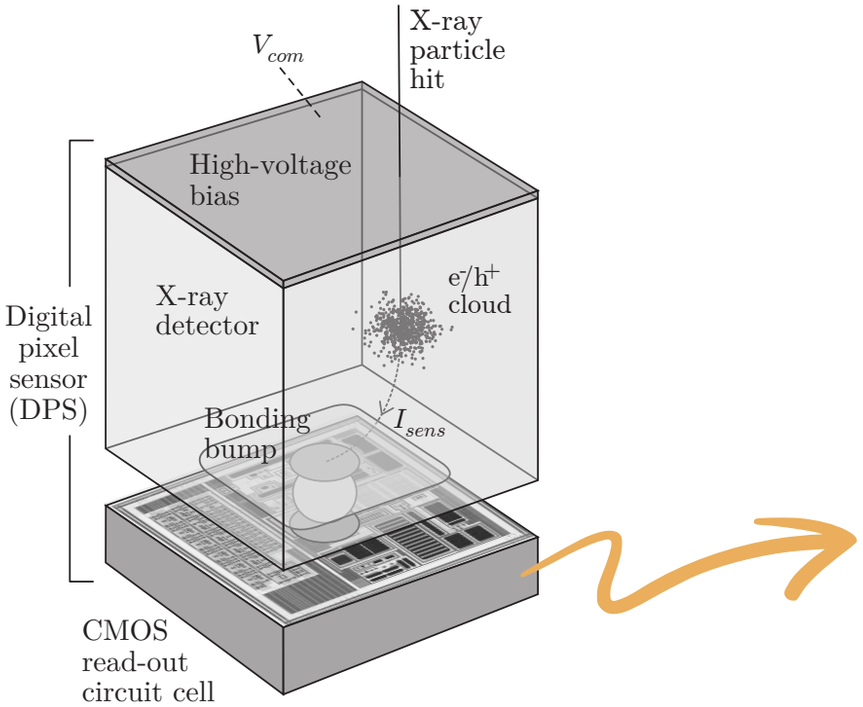
Photon Counting vs Charge Integration

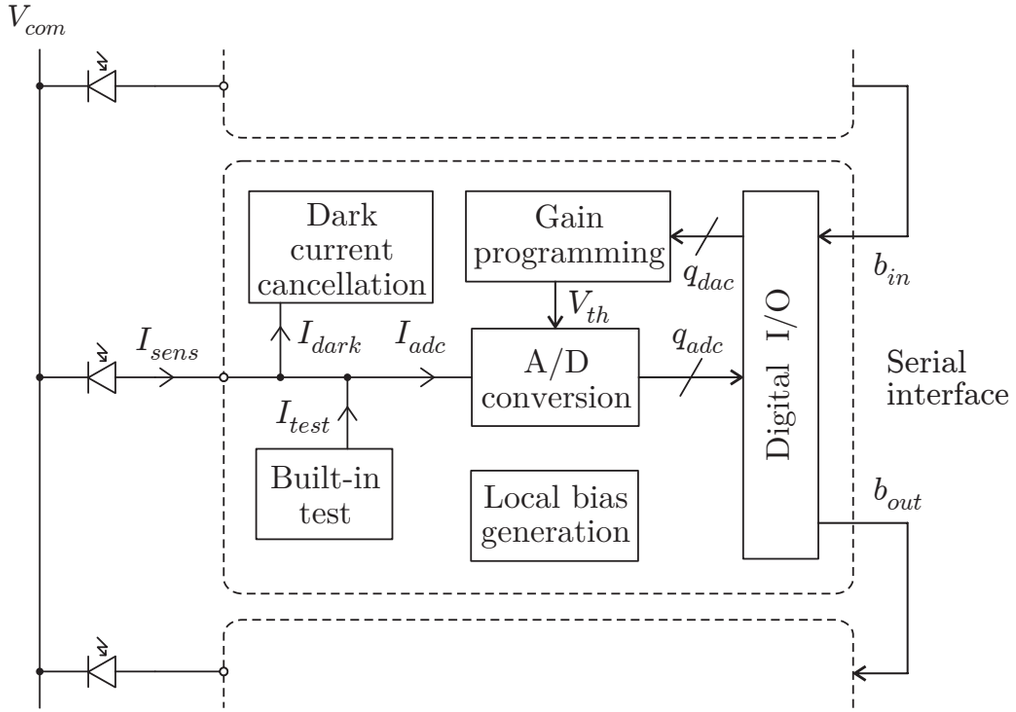




- **Single particle** detection:
  - Less sensitive to circuit **noise**
  - Possibility of photon **classification**
  - Transient **pile-up** effects
  - **Charge-sharing** between pixels
- Overall **charge integration**:
  - Less sensitive to **pile-up** effects
  - **Charge-sharing** can be compensated by digital post-processing
  - Circuit **noise** can corrupt data

Proposed DPS Architecture

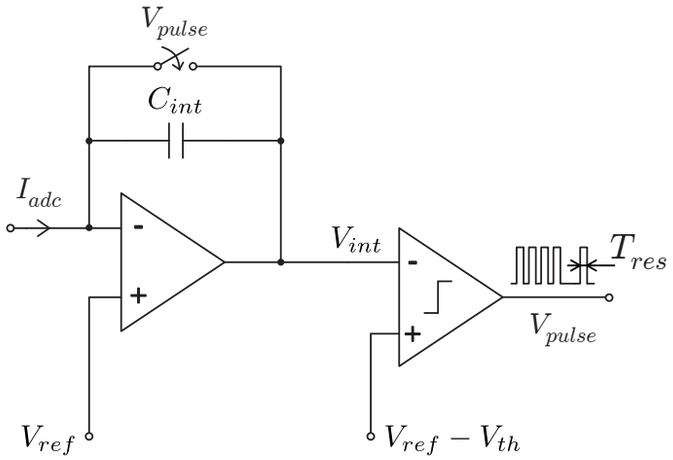


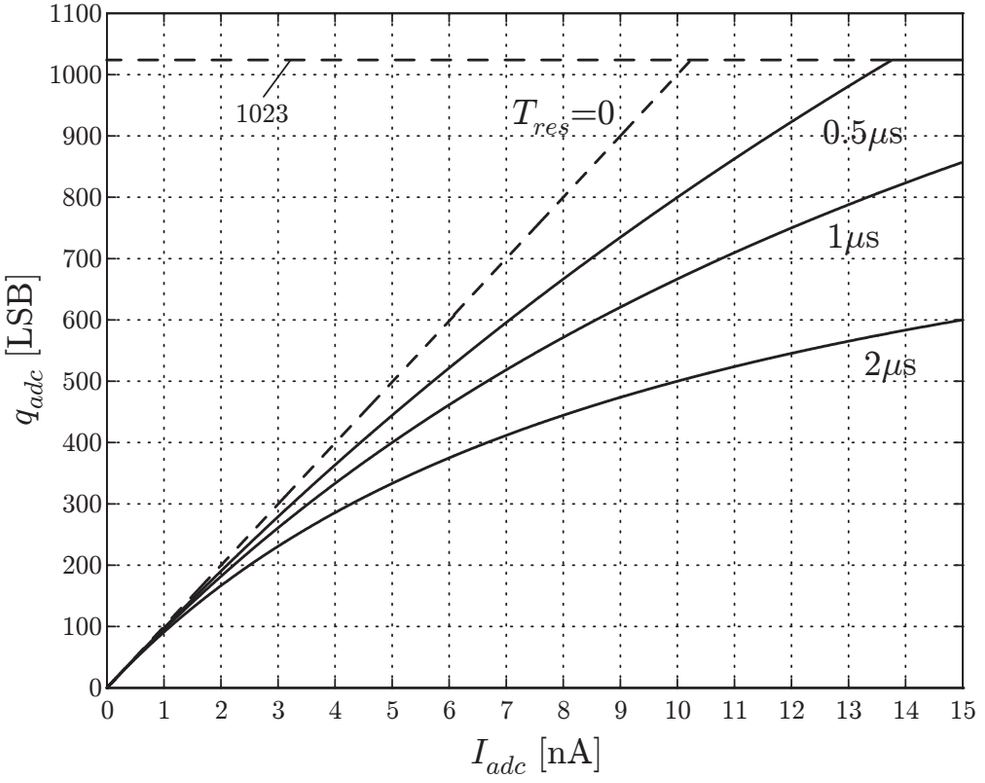


- **Charge integration** method
- Self-biasing for **digital-only I/O** and inter-pixel **low crosstalk**
- **Linear ADC** for high-flux X-rays
- Fixed-pattern noise (**FPN**) cancellation for image equalization
- **Built-in test** for pre-packaging screening
- All with **reduced pitch** and **low power**

Loss-Less A/D Conversion

- **Classic** asynchronous integrate-and-fire (IAF) modulator:



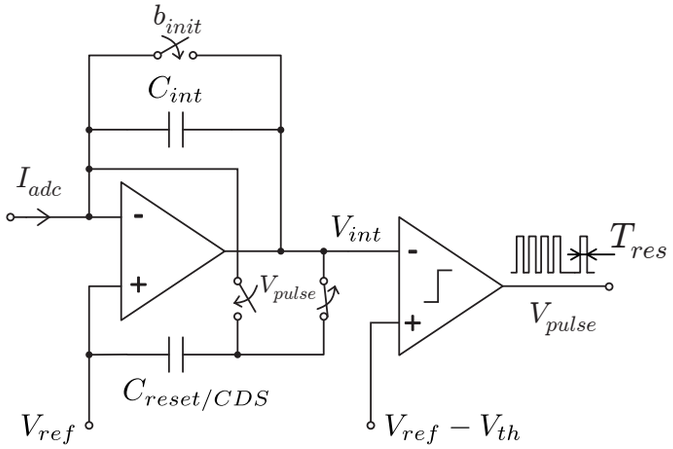


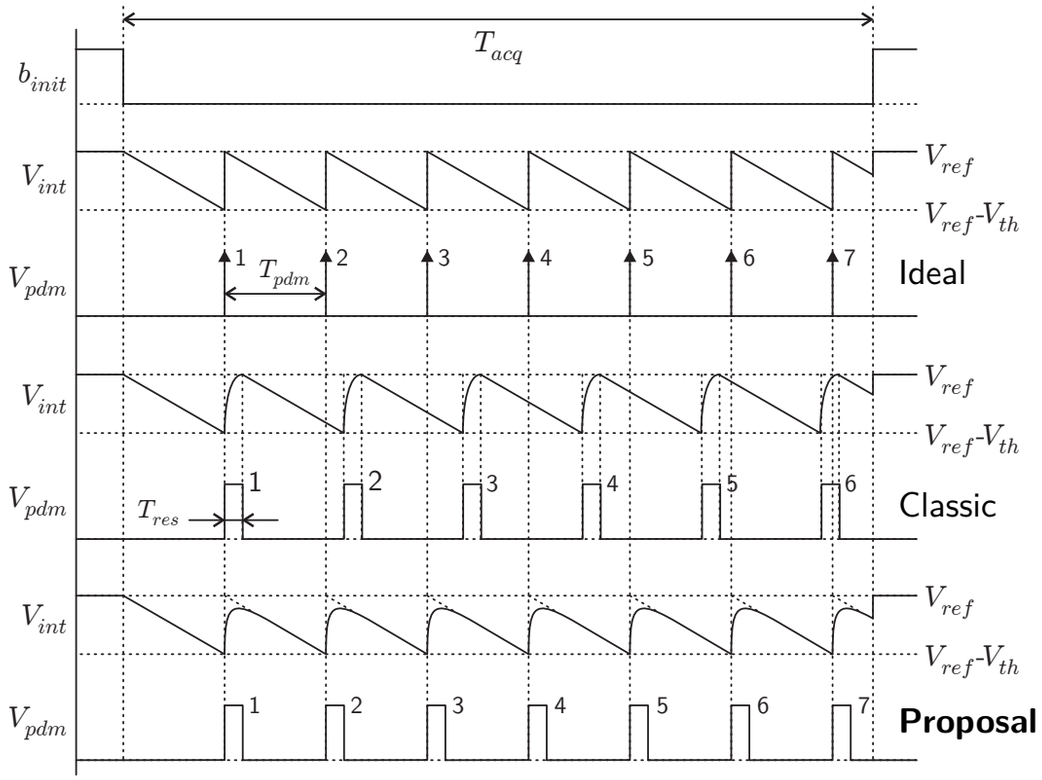
- **Saturation** due to event reset time!

e.g. C_{int}=100fF, V_{th}=200mV, T_{caq}=2ms and 10bit output

Loss-Less A/D Conversion

- **Classic** asynchronous integrate-and-fire (IAF) modulator:

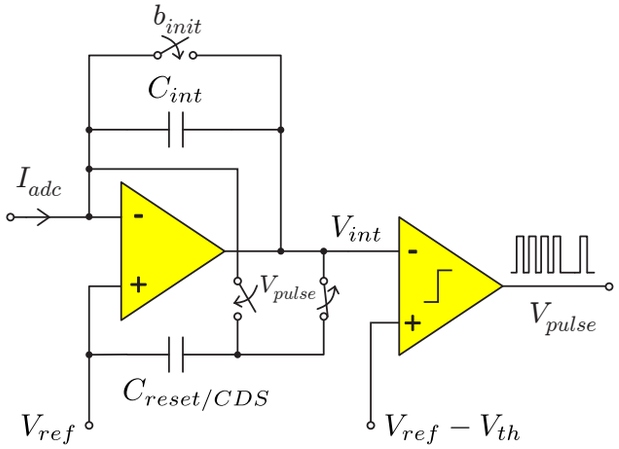


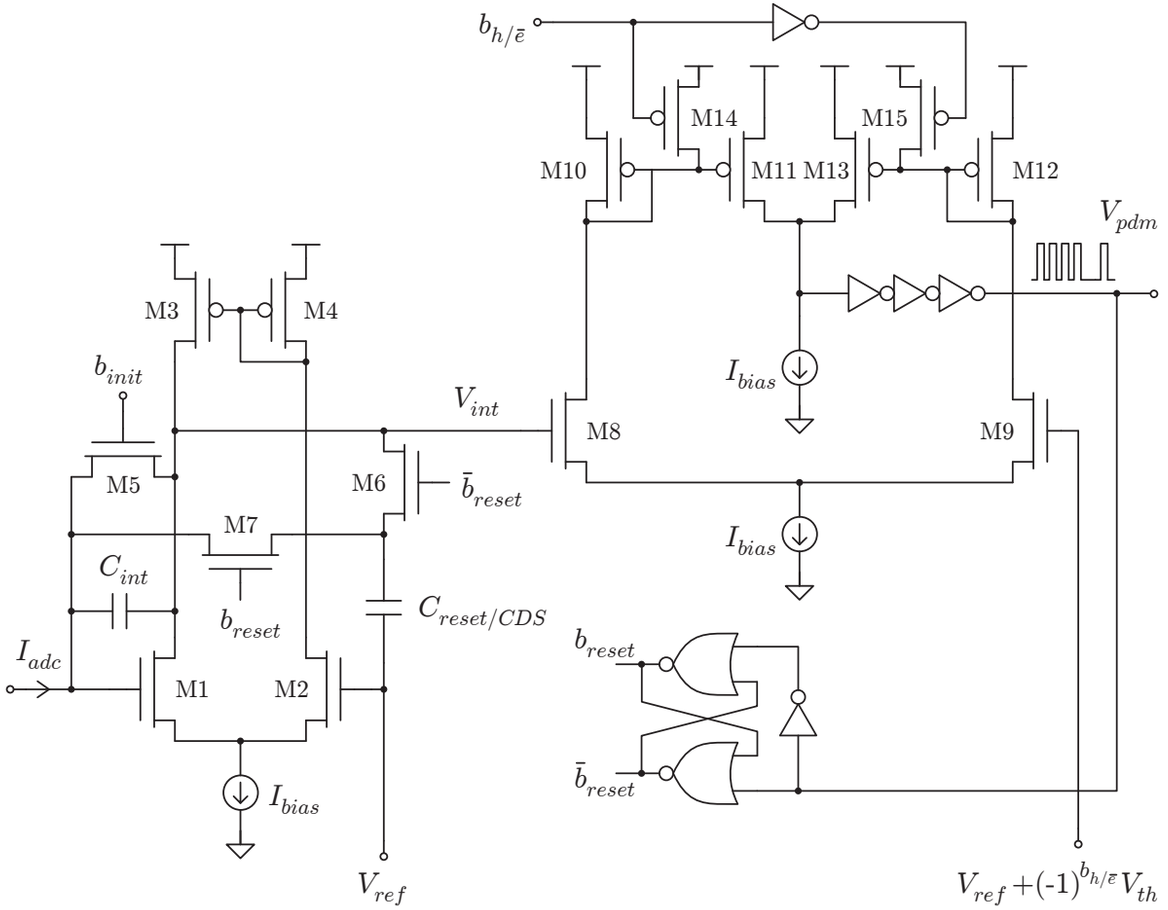


- ▲ Reset-time **independent**
- ▲ **Max f_{pdm}** close to $1/T_{res}$
- ▼ **Double**-capacitor area

Loss-Less A/D Conversion

- **Compact** CMOS circuit implementation:

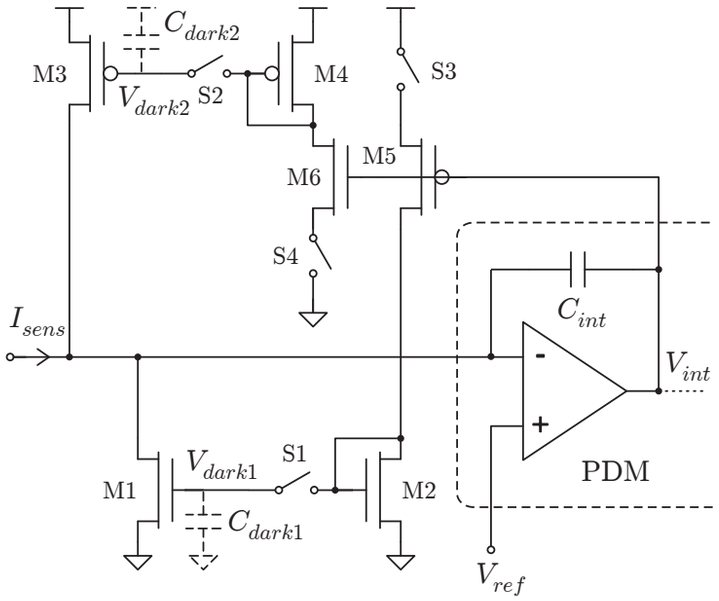




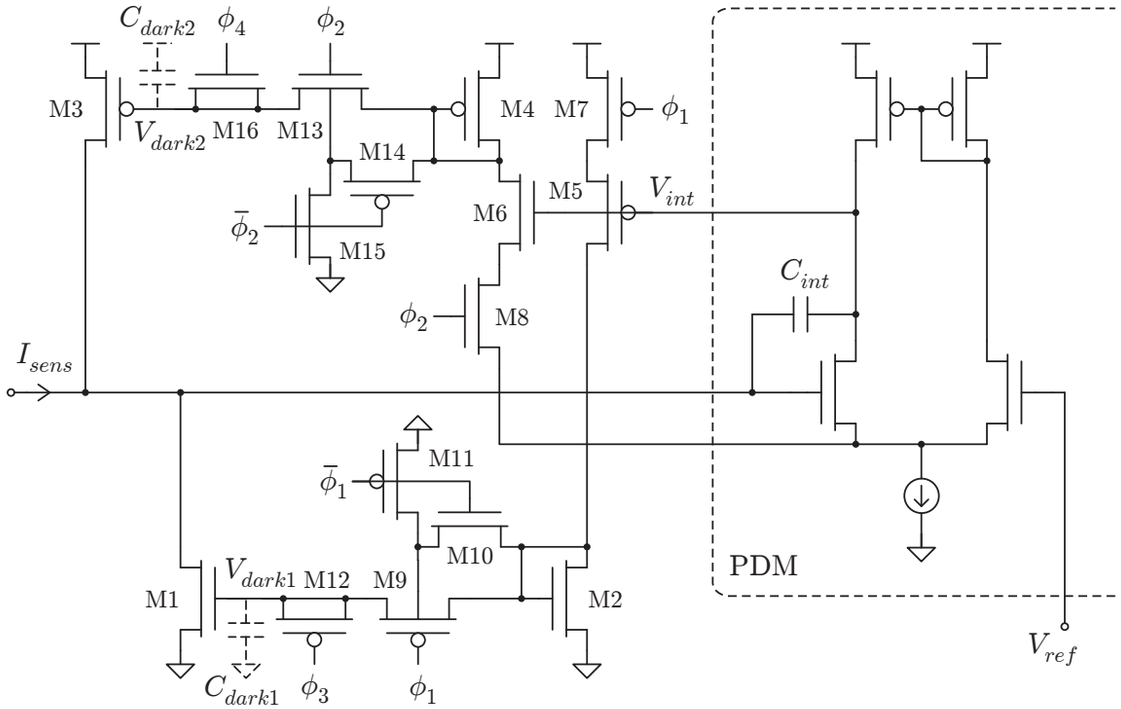
- **Bidirectional** e^-/h^+ charge collection

Dark-Current Cancellation

- Based on **current-copiers**:



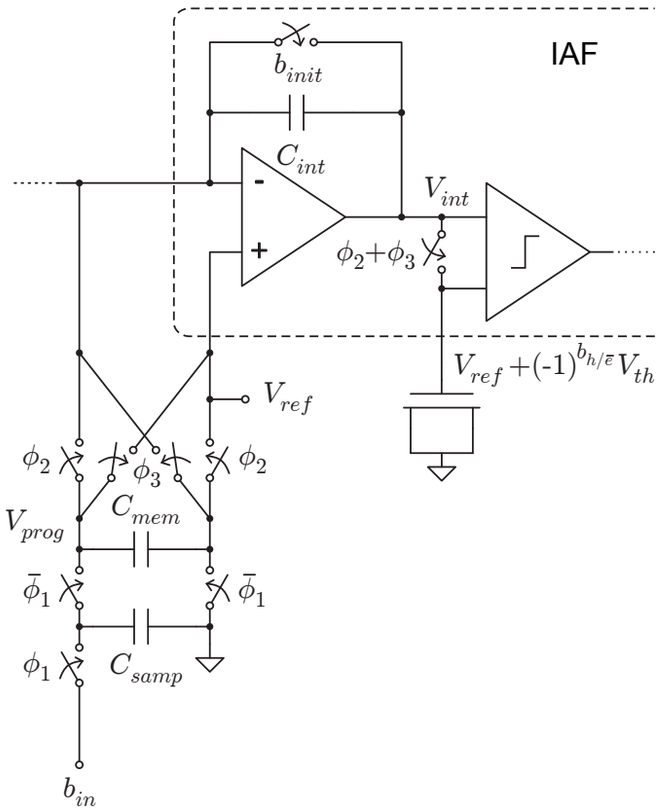
- **Reuse** of ADC CMOS circuit for compact area



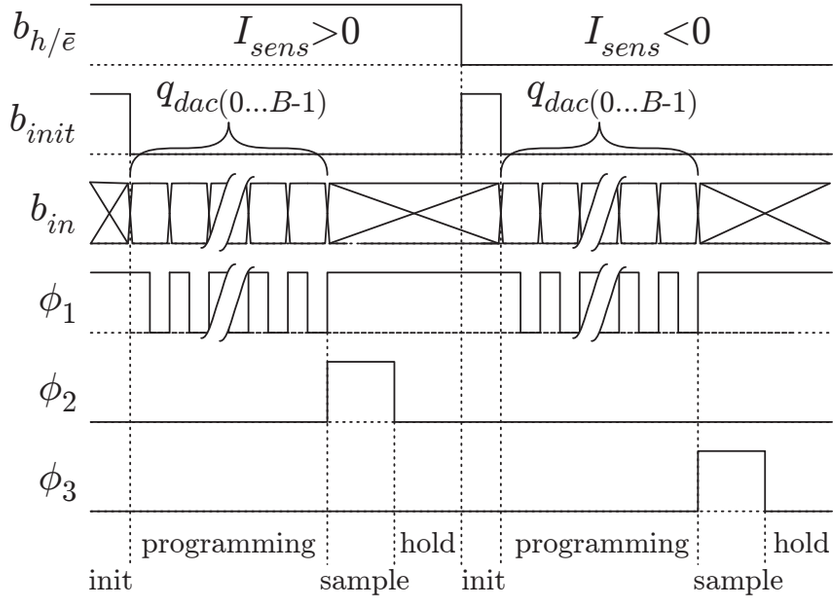
- **Auto-calibration**
- **Coarse** + **fine** for charge-injection compensation
- Composite switches for **long retention** times

Individual-Pixel Gain Programmability

- In-pixel SC **DAC** circuit:



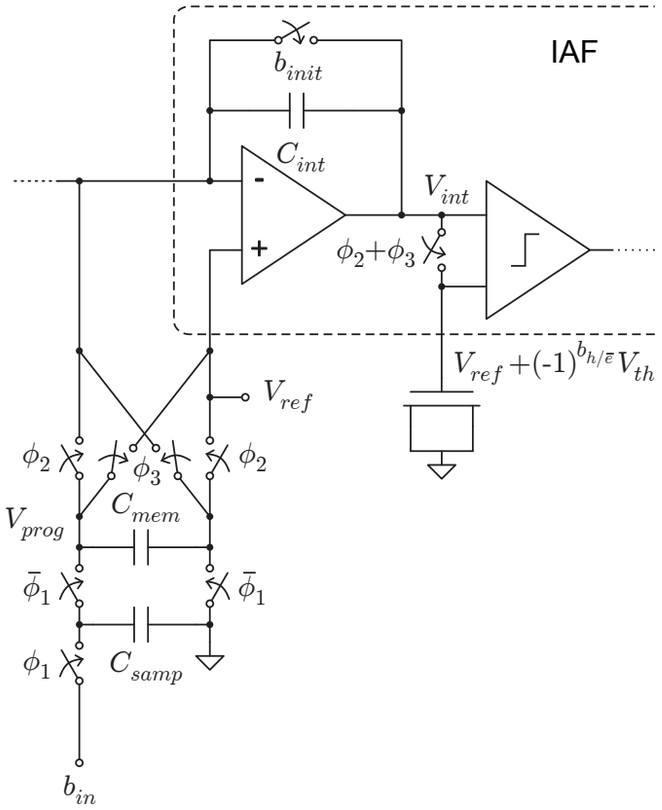
- **Reuse** of ADC CMOS circuit for compact area

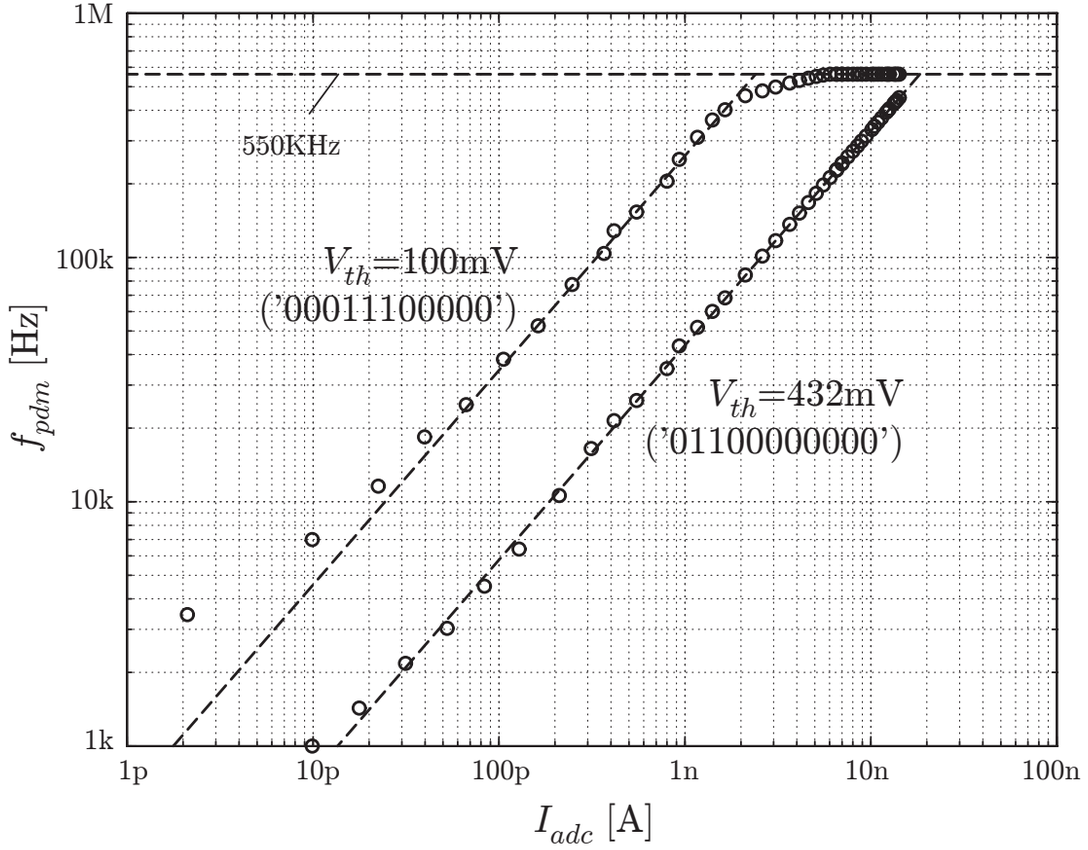


- Serially **program-in** during read-out (no speed reduction)
- Gain **FPN** compensation
- Also for **built-in test** through input charge injection...

Individual-Pixel Gain Programmability

- In-pixel SC **DAC** circuit:

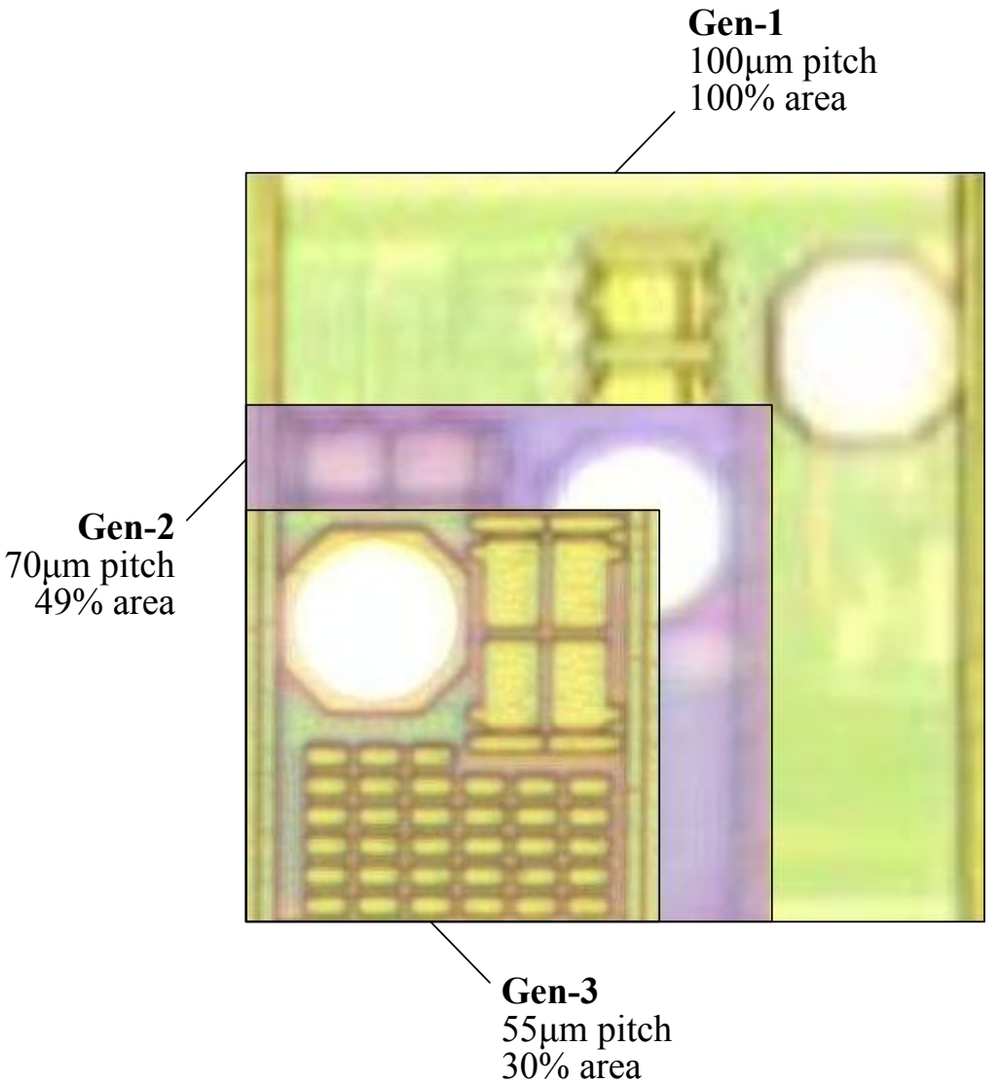




DPS CMOS Integration

- 1.8V 0.18µm 1P6M CMOS technology
- **Pitch** evolution:
  100µm (Gen-1),
  70µm (Gen-2)
  and 55µm(Gen-3)

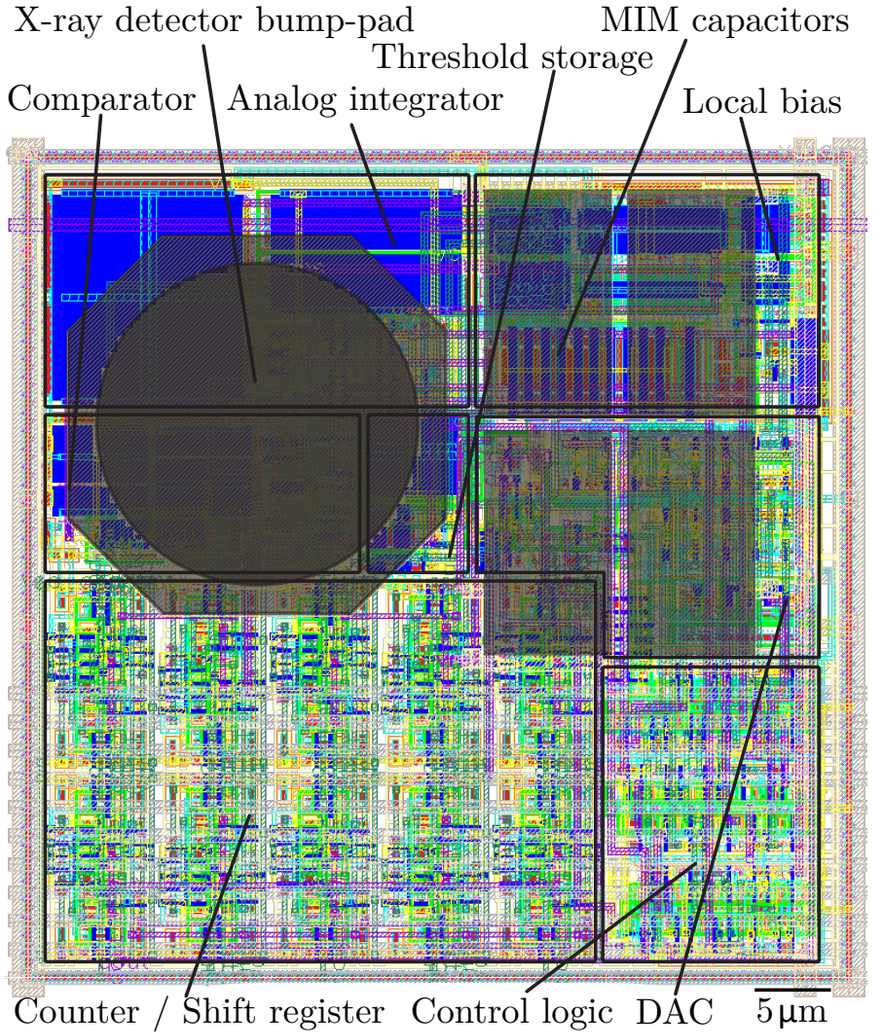
Parameter	Value	Units
I_{bias}	450	nA
V_{ref}	760	mV
C_{int}	85	fF
$C_{reset/CDS}$	85	fF
C_{mem}	85	fF
C_{samp}	85	fF
V_{th}	40 to 400	mV
T_{reset}	0.5	μs
N	10 to 12	bit



DPS CMOS Integration

- 1.8V 0.18µm 1P6M CMOS technology
- **Pitch** evolution:
  100µm (Gen-1),
  70µm (Gen-2)
  and 55µm(Gen-3)

Parameter	Value	Units
I_{bias}	450	nA
V_{ref}	760	mV
C_{int}	85	fF
$C_{reset/CDS}$	85	fF
C_{mem}	85	fF
C_{samp}	85	fF
V_{th}	40 to 400	mV
T_{reset}	0.5	μs
N	10 to 12	bit



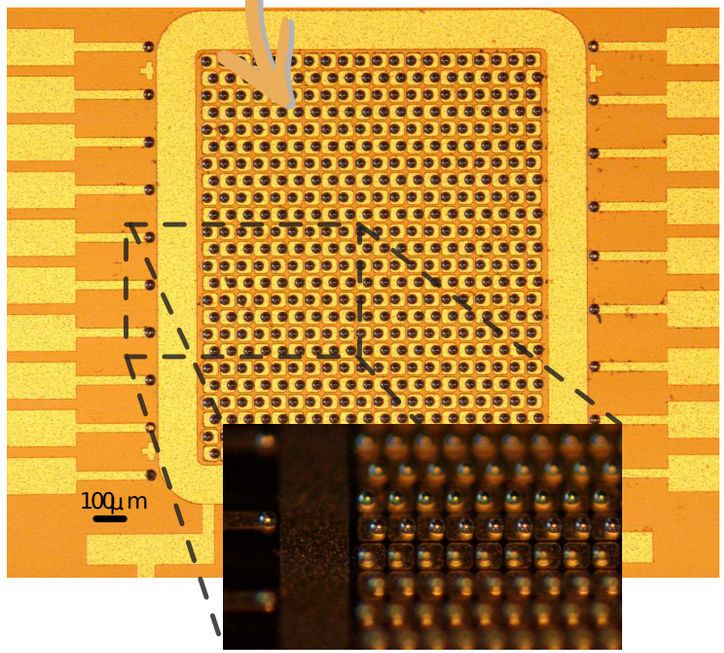
DPS CMOS Integration

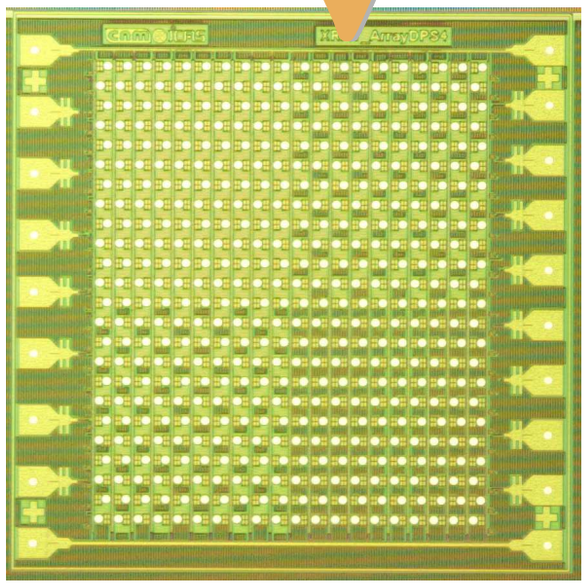
- 1.8V 0.18µm 1P6M CMOS technology
- **Pitch** evolution:
  100µm (Gen-1),
  70µm (Gen-2)
  and 55µm(Gen-3)

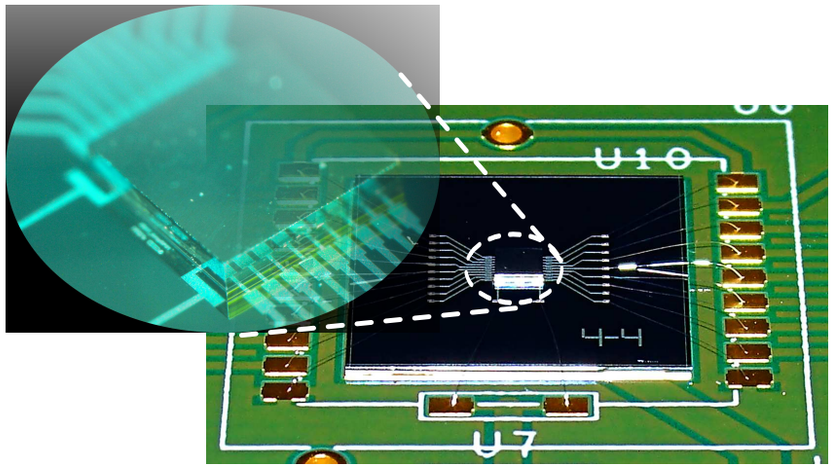
Parameter	**Gen-1**	**Gen-2**	**Gen-3**	**Units**
Supply voltage	1.8	1.8	1.8	V
Reference voltage	650	815	830	mV
Biasing current	270	550	500	nA
Bias mismatching	< 10	< 10	< 15	%
Typical transfer gain	1/50	1/50	1/50	LSB/ke$^-$
Full scale	> 10	> 10	> 10	nA
Integration time	1 to 1000	1 to 1000	1 to 1000	ms
Output dynamic range	10	10	12	bit
Digital I/O speed	> 50	> 60	100	Mbps
PDM pulses frequency	600	600	800	kHz
Dark current range	up to 20	up to 20	N.A.	nA
Compensated dark current	95	95	N.A.	%
Equivalent noise charge	< 2	< 2	< 2	ke$^-_{rms}$
Crosstalk	no	no	no	
Static power consumption	5	8	6	μW
Integrating capacitor	100	100	100	fF
Silicon area	100×100	70×70	55×55	μm$\times\mu$m

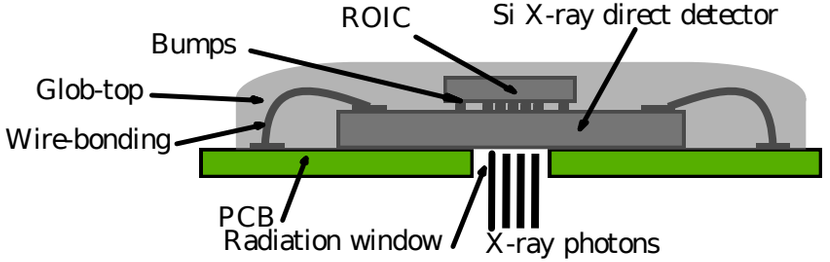
X-Ray Test ICs

- **Small arrays** of DPS cells in standard UMC 0.18µm 1P6M MIM CMOS technology
- **Si pixelated detectors** in inexpensive IMB-CNM(CSIC) 2.5µm 2P1M PIP CMOS technology



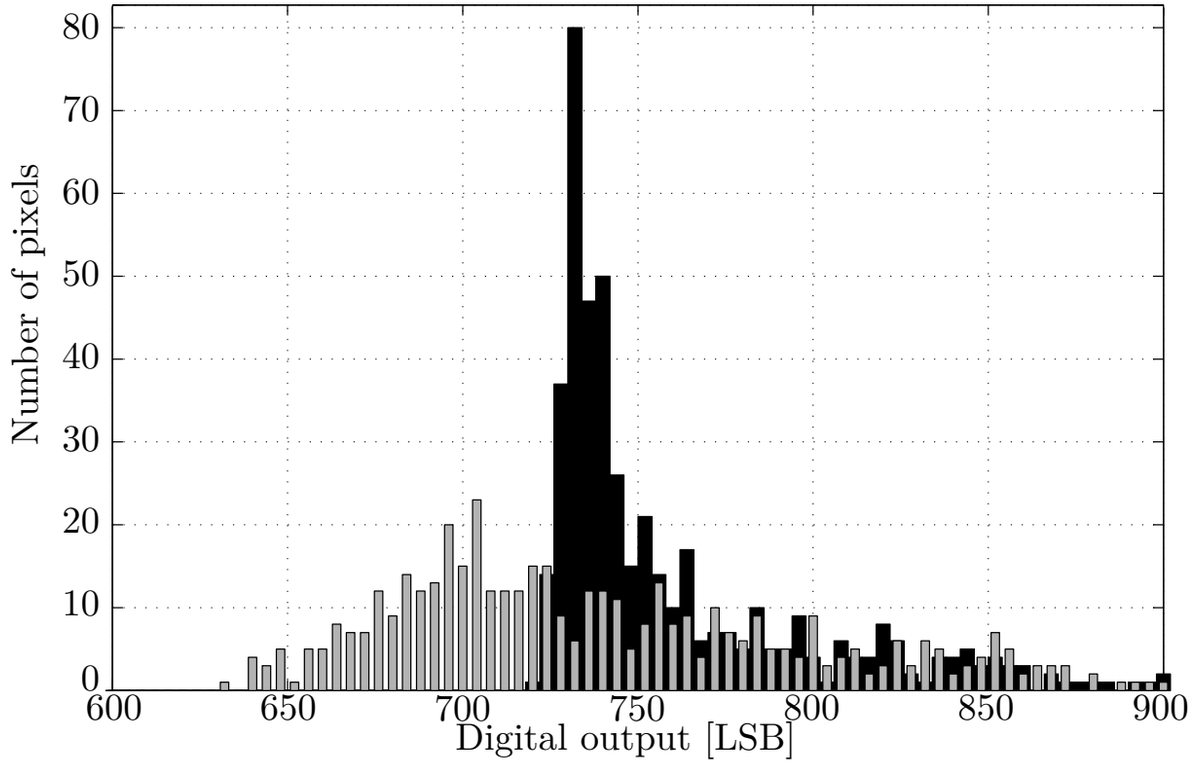


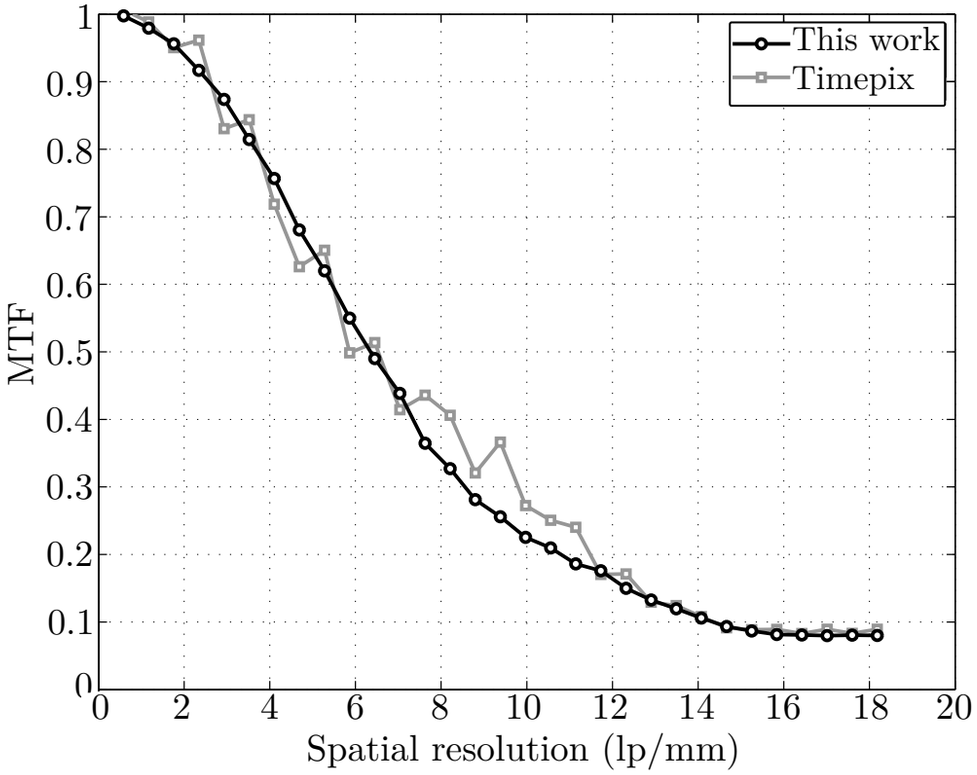




X-Ray Test ICs

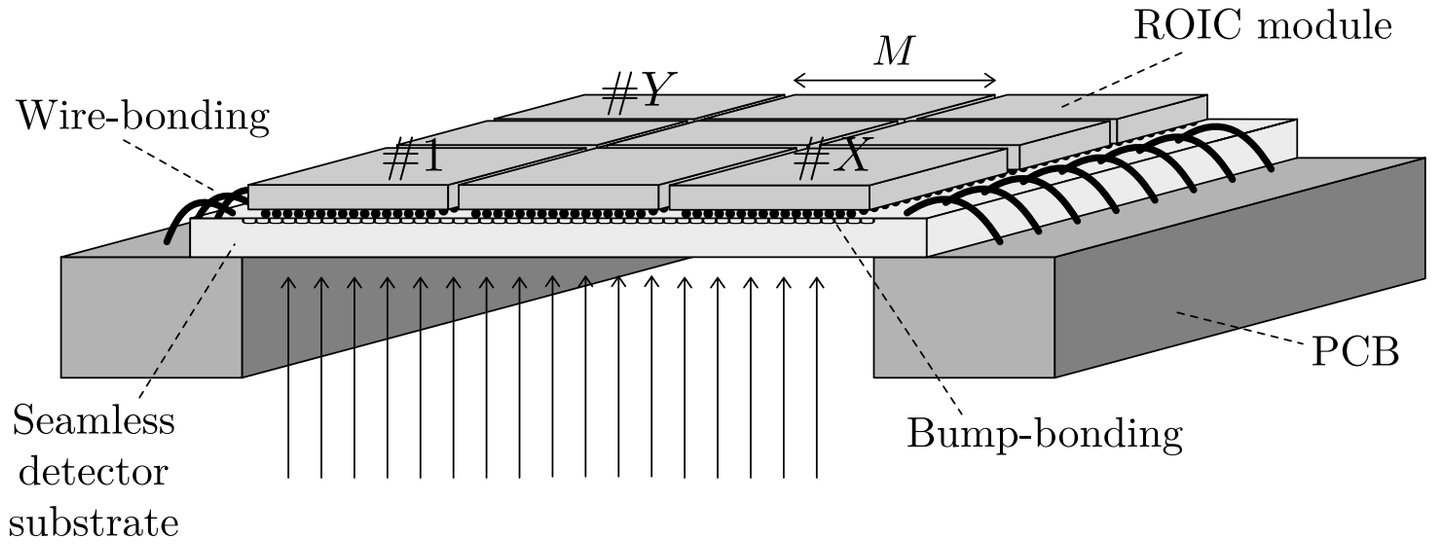
- **Good DPS** results in terms of maximum SNDR, FPN reduction, spatial resolution, crosstalk...





True 2D Modular X-Ray Imagers

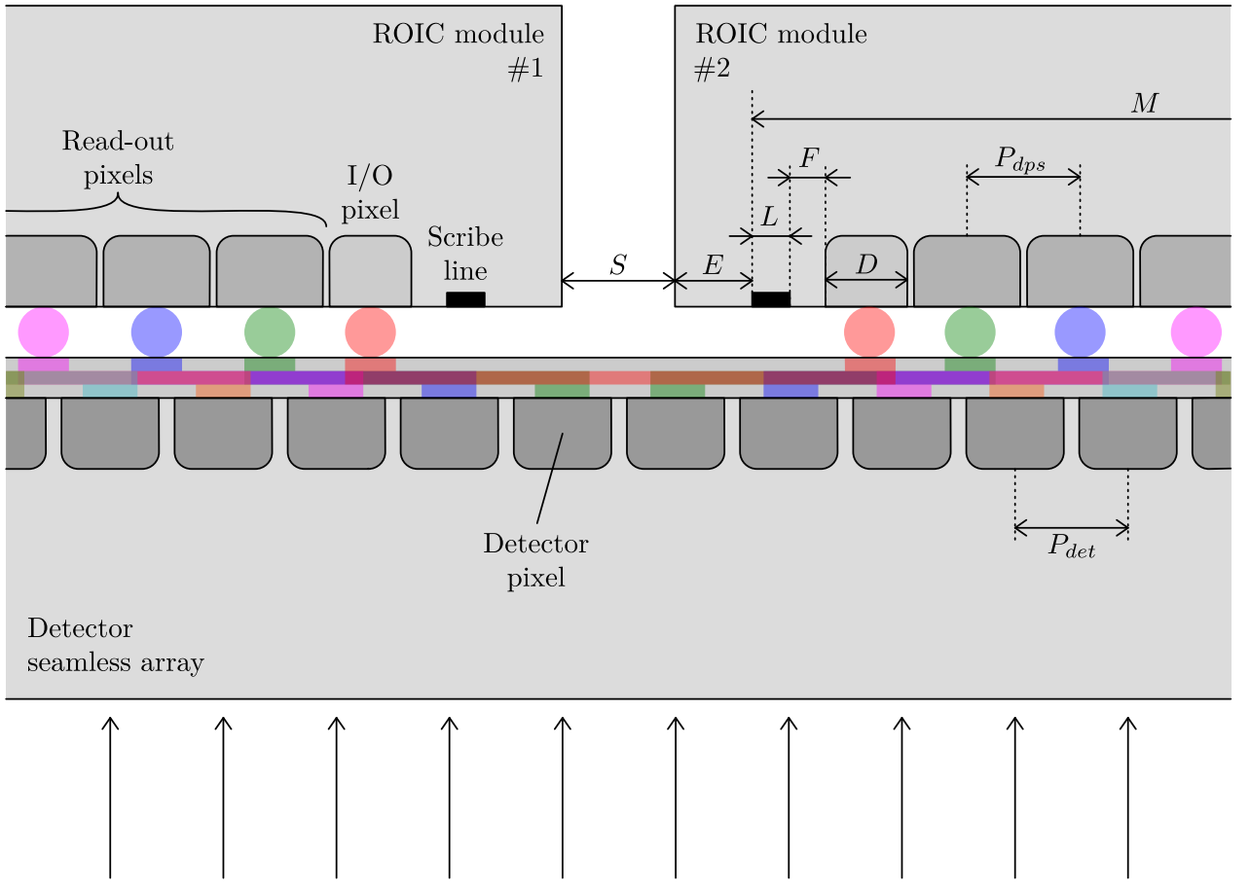
- Array of read-out ICs attached to **seamless** pixelated detector substrate:

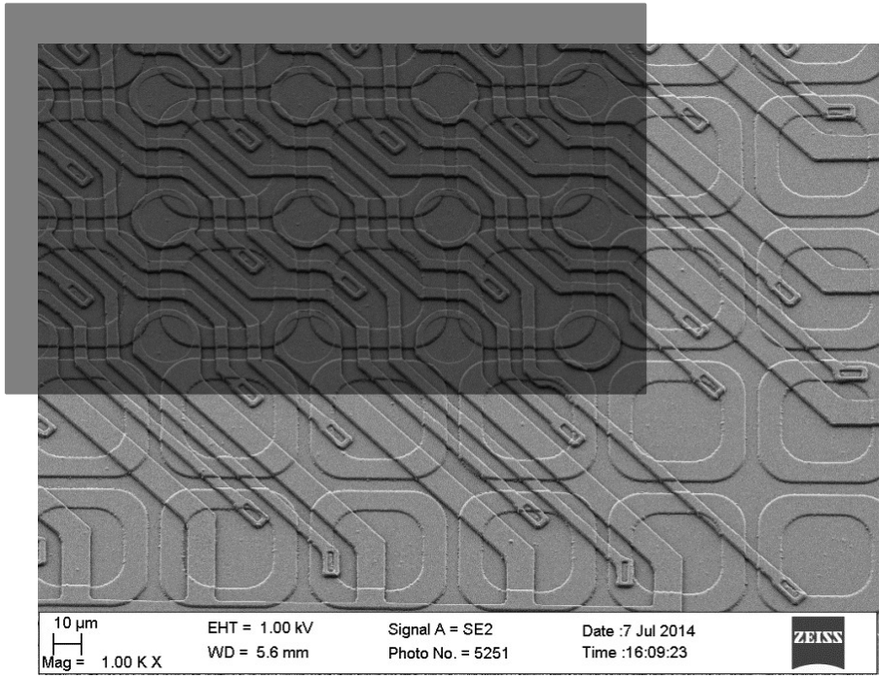


- Final goal is to reduce **CMOS costs** for large area imagers...

True 2D Modular X-Ray Imagers

- Array of read-out ICs attached to **seamless** pixelated detector substrate:

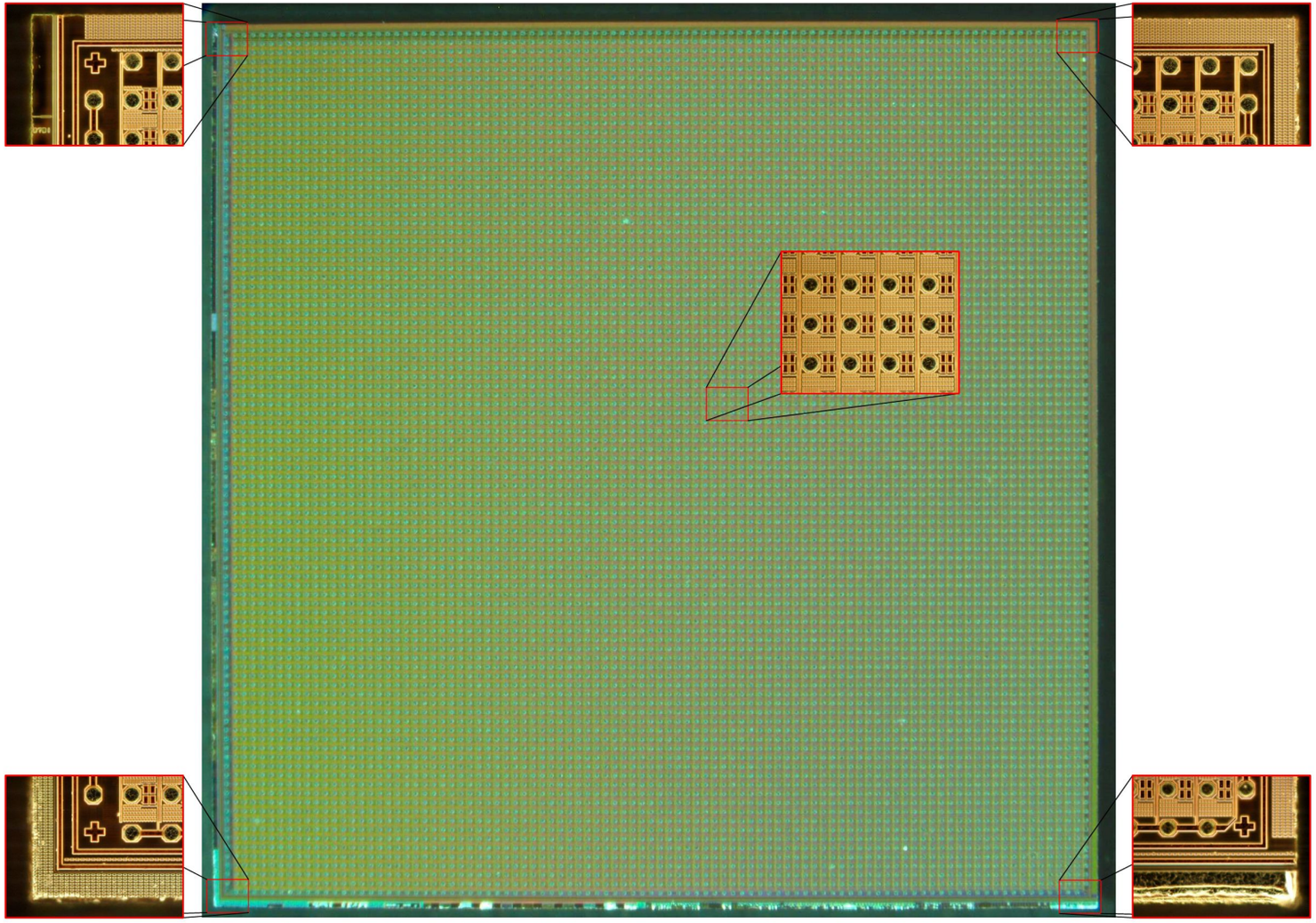




- ▲ Pixel detector-to-circuit **rerouting**
- ▼ Inter-pixel **crosstalk**?

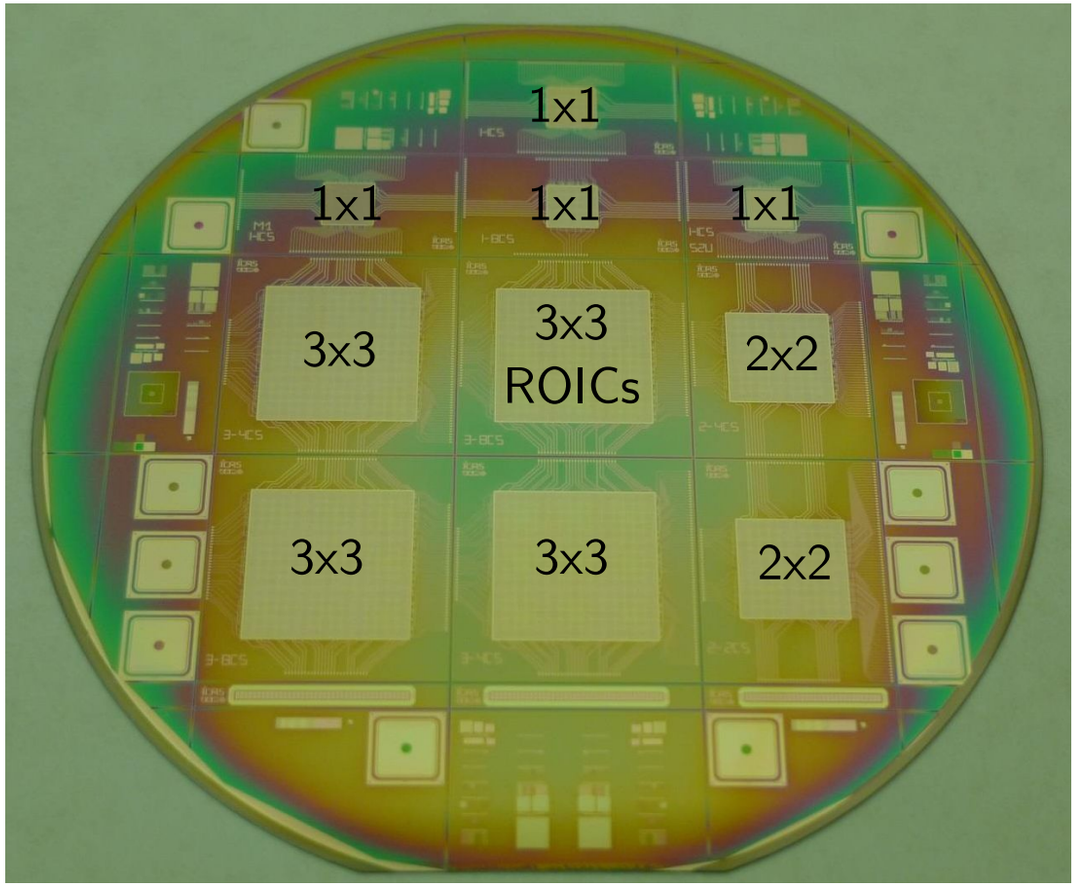
True 2D Modular X-Ray Imagers

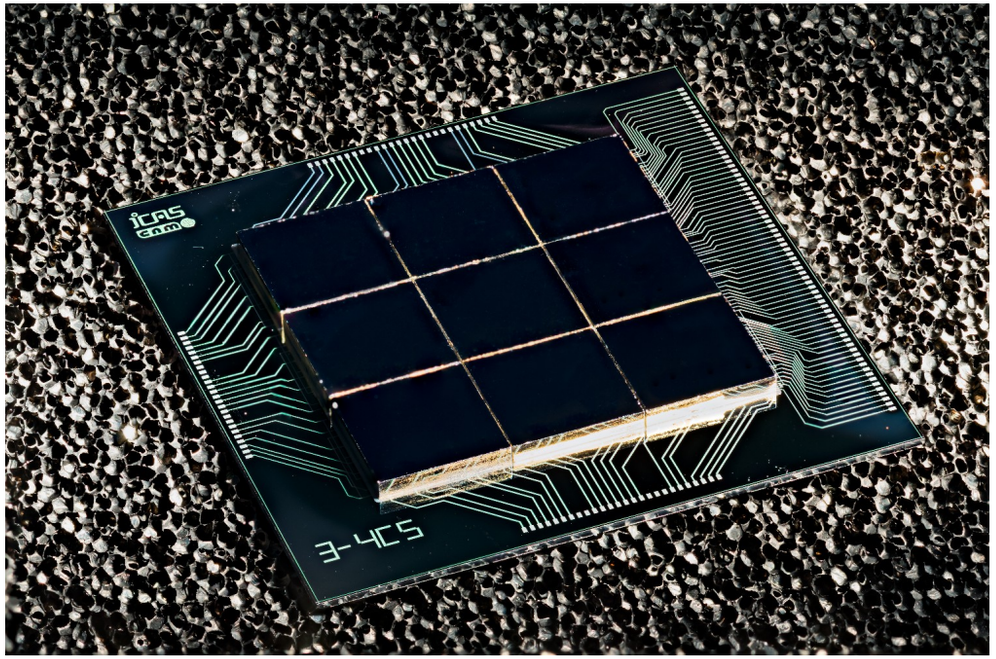
- CMOS **ROIC module**
  - 94x94 pixel (5mmx 5mm)
  - 52µm-pitch
  - 6µW/pix at 1.8V



True 2D Modular X-Ray Imagers

- 55µm-pitch **seamless arrays** of pixelated Si detectors in 4-inch wafers:





↗ R. Figueras et al.
A 70-um Pitch 8-uW Self-Biased Charge-Integration Active Pixel for Digital Mammography
IEEE Transactions on Biomedical Circuits and Systems, 5:5(481-489), Oct 2011
doi.org/10.1109/TBCAS.2011.2151192

↗ R. Figueras et al.
Experimental Characterization of a 10uW 55um-pitch FPN-Compensated CMOS Digital Pixel Sensor for X-ray Imagers, Elsevier Nuclear Instruments and Methods in Physics Research A, 761(19–27), Oct 2014
doi.org/10.1016/j.nima.2014.05.085

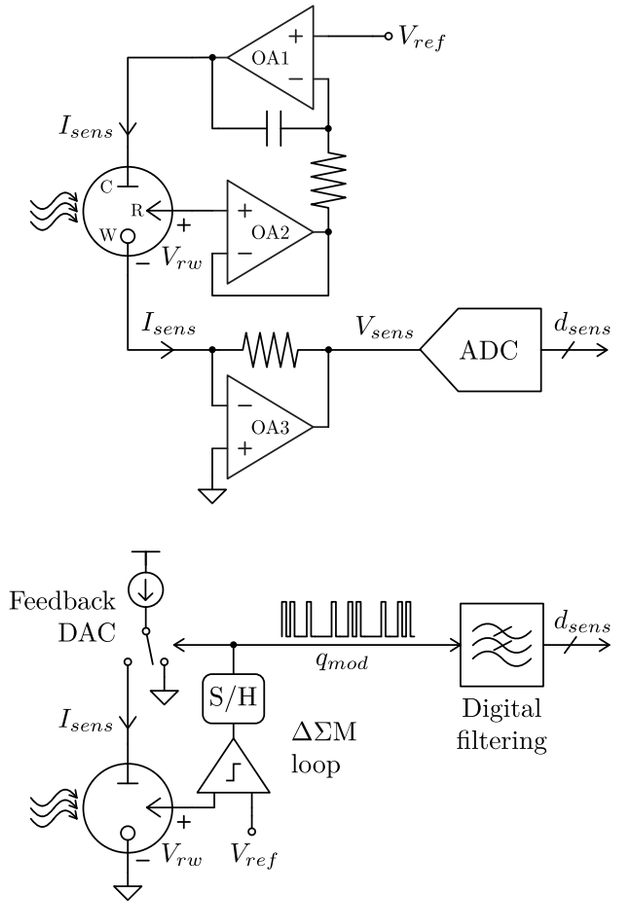
1 High-Resolution SC Delta-Sigma ADC for Space Applications

2 Compact Pixel Integrating ADC for X-Ray Imagers

3 Low-Power Potentiostatic CT Delta-Sigma ADC for Electrochemical Integrated Sensors

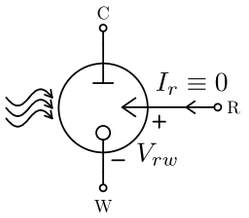
Smart Electrochemical Sensors

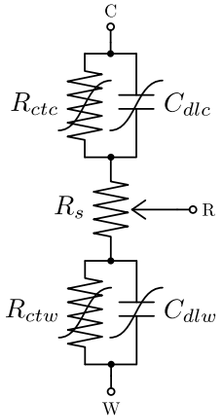
- **Integrated** chemical sensors:
  - Interaction with microorganisms
  - Selectivity by functionalization
  - Speed limitation
  - Reduced life time
  - Packaging costs
- **Electrochemical** family:
  - CMOS compatible
  - **Potentiostatic** biasing
  - **Amperometric** reading
- **Classic** circuit interfaces require multiple OpAmps + resistors + ADC
- **Low-power MOS-only** circuit proposal based on mixed electronic and chemical domain potentiostatic $\Delta\Sigma$ modulator

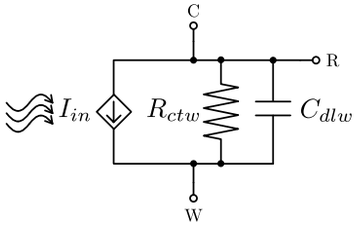


Sensor Modeling

- Reuse of **sensor dynamics** for circuit design needs accurate device modeling!
- **R**eference, **W**orking and **C**ounter planar microelectrodes
- Non-linear electrical impedance model under **potentiostatic** operation:
  - R_s = electrolyte solution resistance
  - R_{ctx} = charge-transfer resistance
  - C_{dlx} = double-layer capacitance
- **Solution resistance** smaller than electrode-solution counterparts ($10^2 k\Omega$)
- Similar impedance results with internal (micro) and external (macro) **counter microelectrodes**
- Simplified linear **dynamic model**

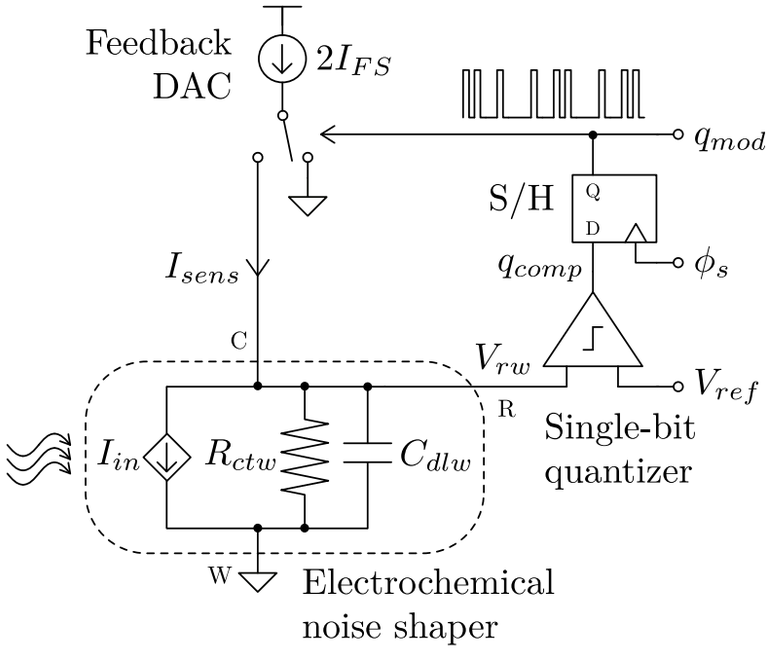






ΔΣ Modulator Architecture

- Behavior similar to **low-pass first-order single-bit CT** ΔΣ A/D modulator
- Error current is converted into voltage and shaped in frequency by the **electrochemical sensor** itself
- Quantization, S/H and DAC feedback in **electronic domain**
- **Amperometric** read-out through the ΔΣ modulation of output bit stream q_{mod} by chemical input I_{in}
- Overall negative feedback ensures **potentiostatic** operation by keeping V_{rw} biased closed to V_{ref} potential
- High oversampling ratios (**OSR>100**) can be easily obtained with kHz-range clock frequencies f_s

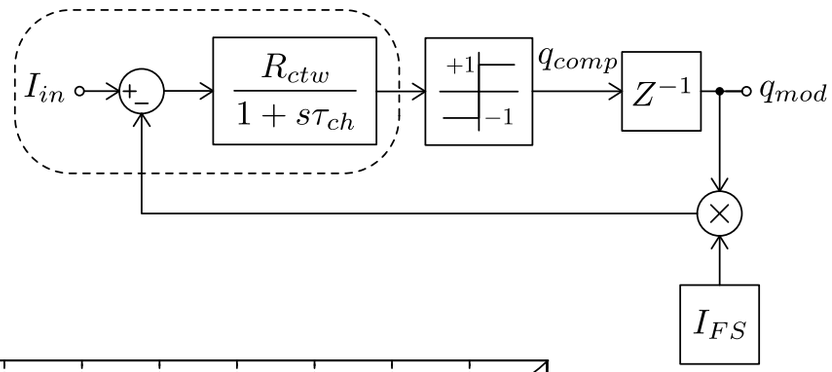


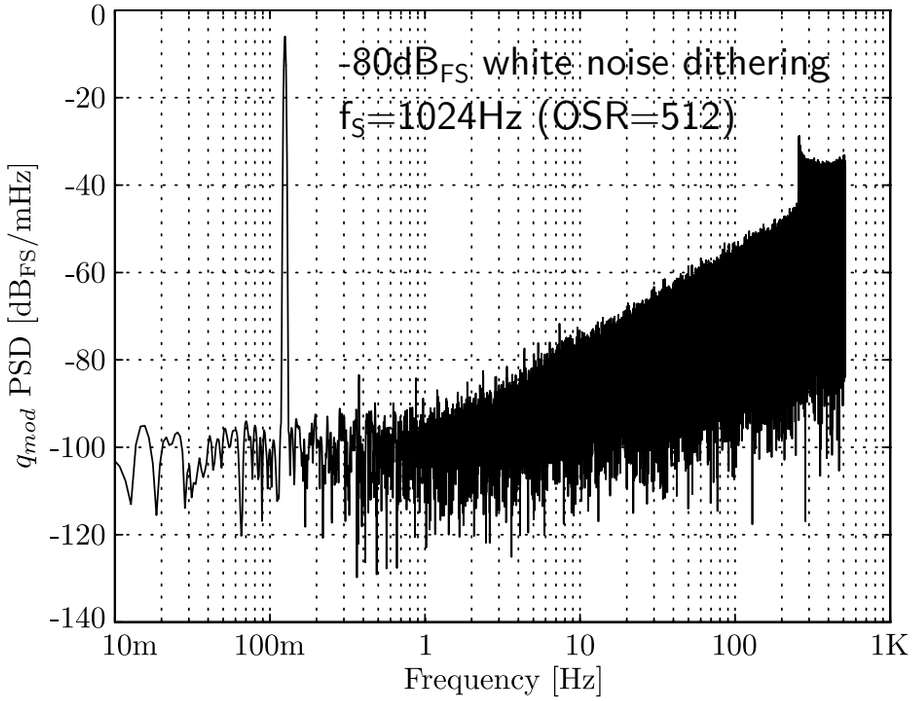
Class-A **full scale**: $I_{FS} = \frac{V_{ref}}{R_{ctw}}$

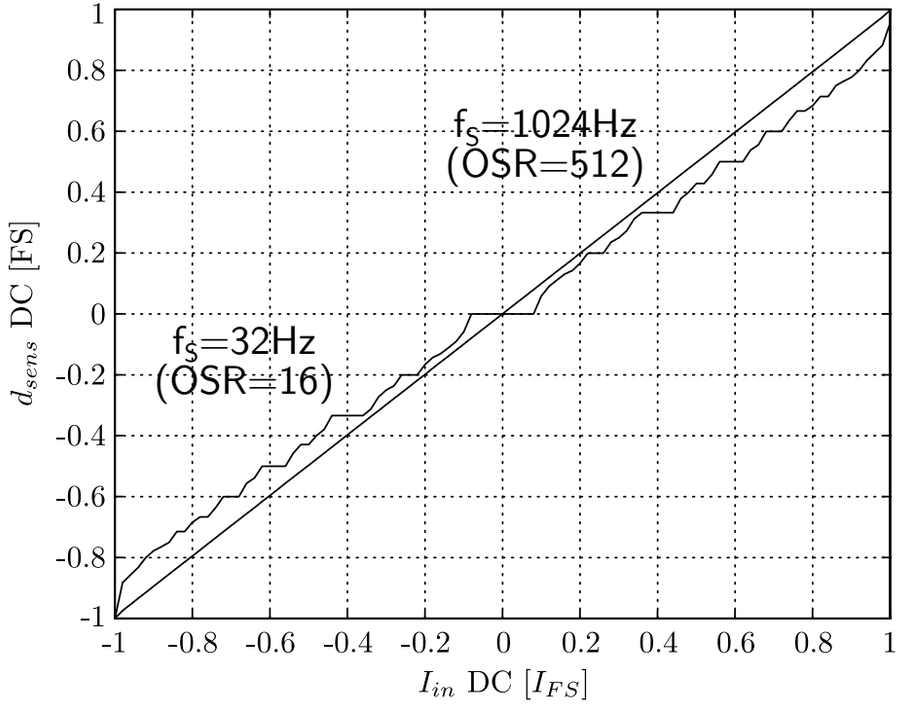
Electrochemical **time constant**: $\tau_{ch} = R_{ctw}C_{dlw} \sim 10^{-1}s$

ΔΣ Modulator Optimization

- Typical **tonal components** of first-order ΔΣ modulation are attenuated through **thermal noise dithering** at DAC
- Fractal **staircase** DC transfer function due to DT losses of CT electrochemical integrator is improved by **increasing OSR**





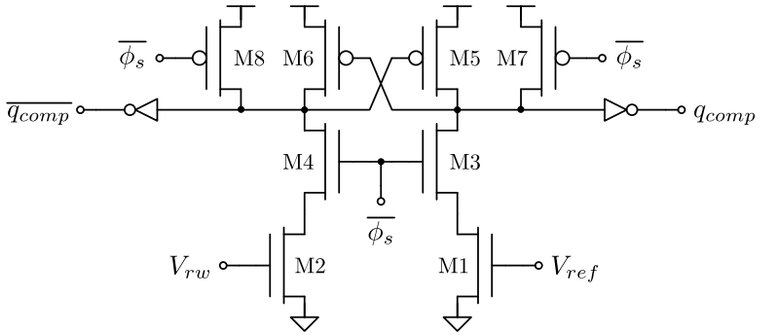


e.g. ΔΣM behavioral simulation for R_{ctw}=500kΩ, τ_{ch}=0.16s, V_{ref}=1V and I_{FS}=2μA

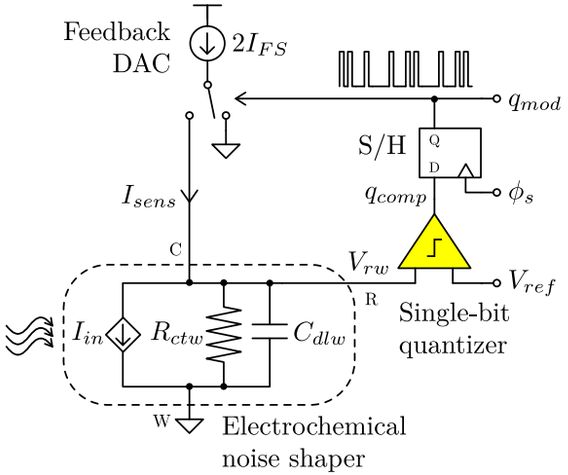
Low-Power MOS-Only Circuits

- Two **analog blocks** only

- **Latched comparator** for 1-bit quantization:

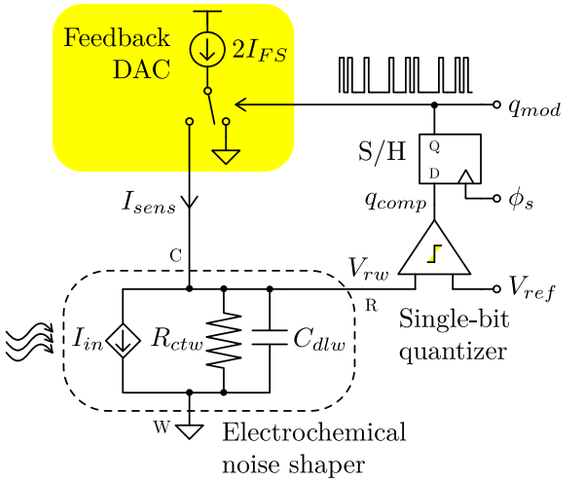


  - **Technology mismatching** does not cause distortion but DC offset at V_{rw}
  - If V_{ref} is chosen higher than redox potential, electrochemical signals can tolerate comparator **offsets** as large as ±10mV

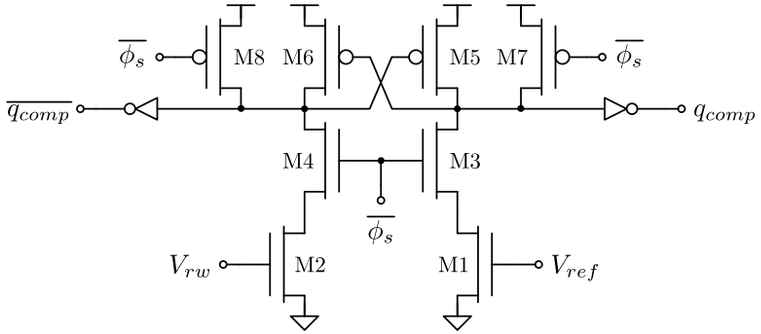


Low-Power MOS-Only Circuits

- Two **analog blocks** only

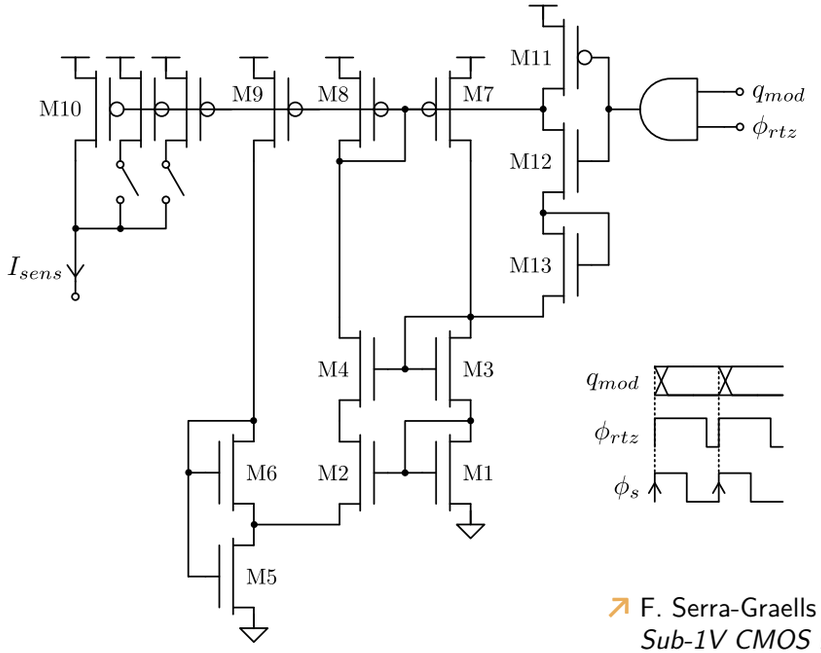


- **Latched comparator** for 1-bit quantization:



  - **Technology mismatching** does not cause distortion but DC offset at V_{rw}
  - If V_{ref} is chosen higher than redox potential, electrochemical signals can tolerate comparator **offsets** as large as ±10mV

- **Compact reference** generator for current DAC:



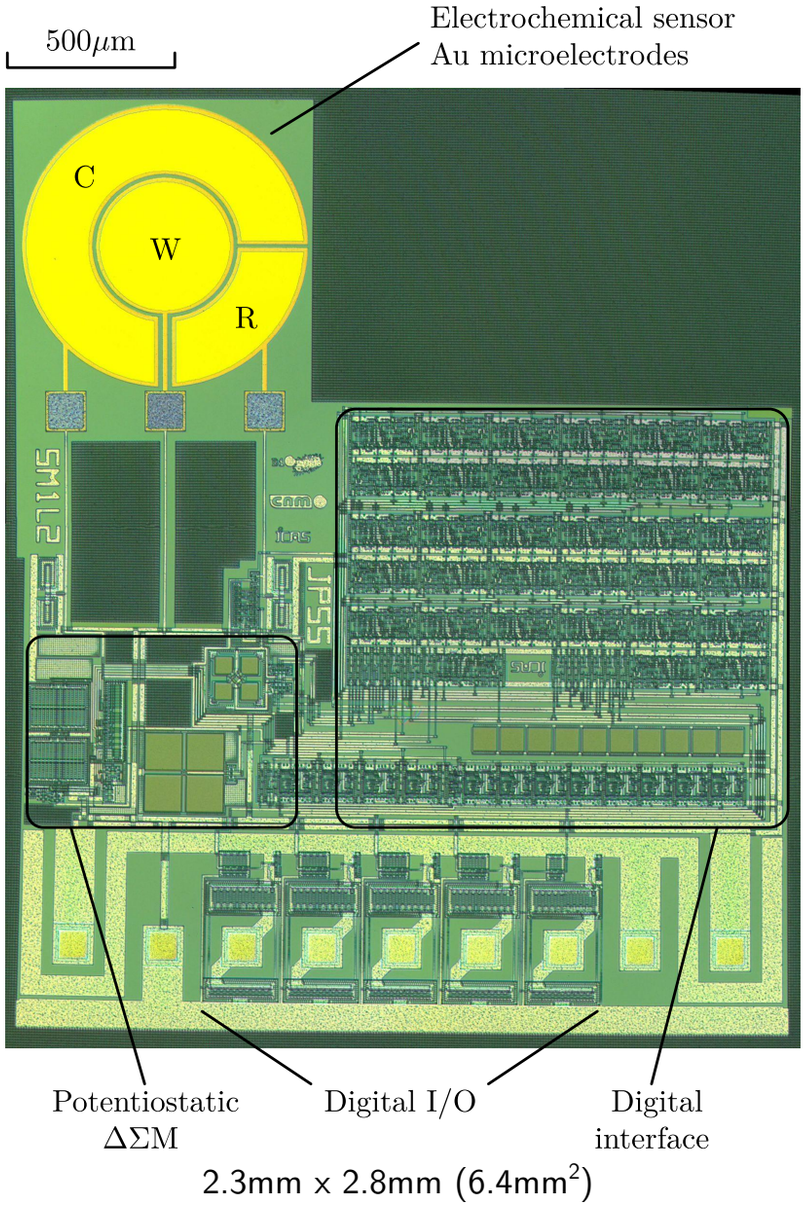
  - **Programmable full scale** for different integrated sensor designs
  - **Power in/off** instead of current steering operation to reset all MOSFETs and reduce **flicker noise**
  - **RTZ** signaling in order to avoid typical waveform asymmetries issues of CT ΔΣMs

↗ F. Serra-Graells and J. L. Huertas
Sub-1V CMOS Proportional-to-Absolute-Temperature References
IEEE J. Solid-State Circuits, 38:1(84-88), Jan 2003
doi.org/10.1109/JSSC.2002.806258

Monolithic CMOS Integration

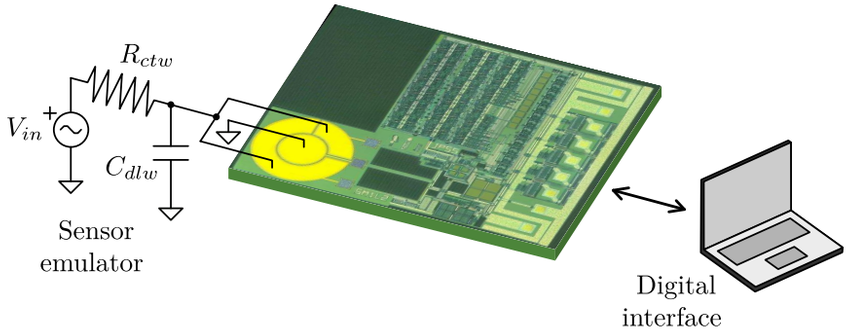
- Inexpensive 2.5µm 1M CMOS technology (**CNM25**)
- In-house **sensor post-processing** at wafer level consisting on sputtering of Ti(15nm)+Au(150nm) thin films and lithographic patterning by lift-off
- **Sensor layout** design: D_{in}=390µm, D_{out}=830µm and S=30µm
- **Sensor electrical** model: R_{ctw}=500kΩ and τ_{ch}=0.16s
- **ΔΣM** design parameters: V_{ref}=1V, I_{FS}=2µA and f_S=1024Hz (OSR=512)

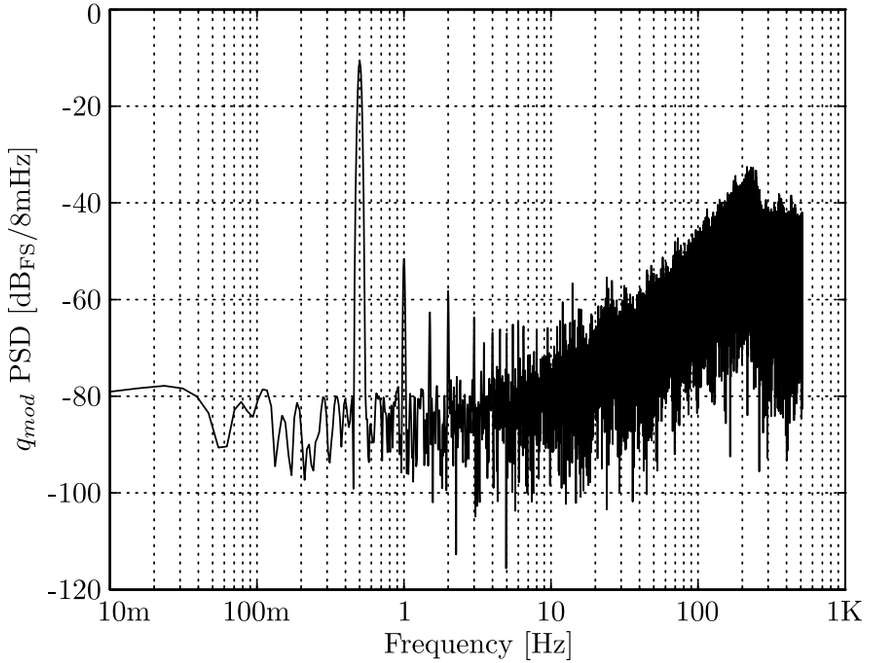
- **Low-area** overhead of proposed ΔΣM
- **Digital-only interface** for low-pass filtering + V_{ref} and I_{FS} programming



Electrical Tests

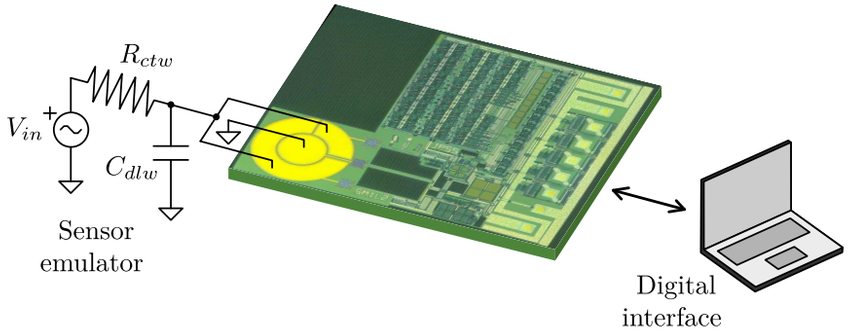
- **Sensor emulation** with external network (R_{ctw}=500kΩ, C_{dlw}=330nF) and SRS DS360 generator in equivalent Thévenin configuration
- Although dithering noise at DAC should be increased, PSD returns good **robustness** against tones



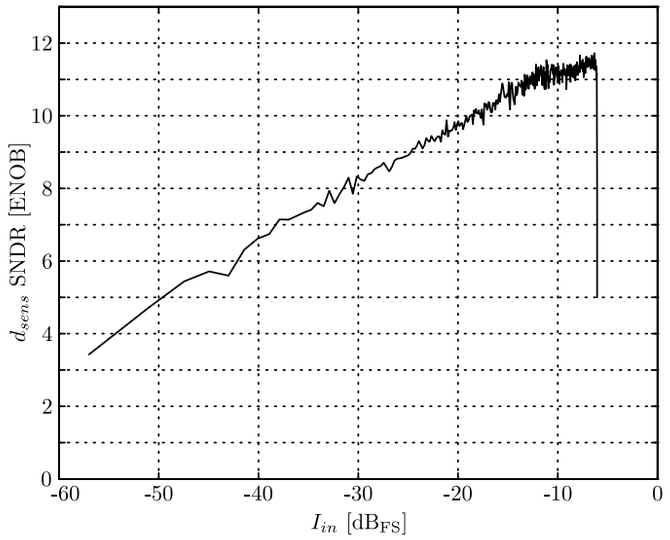


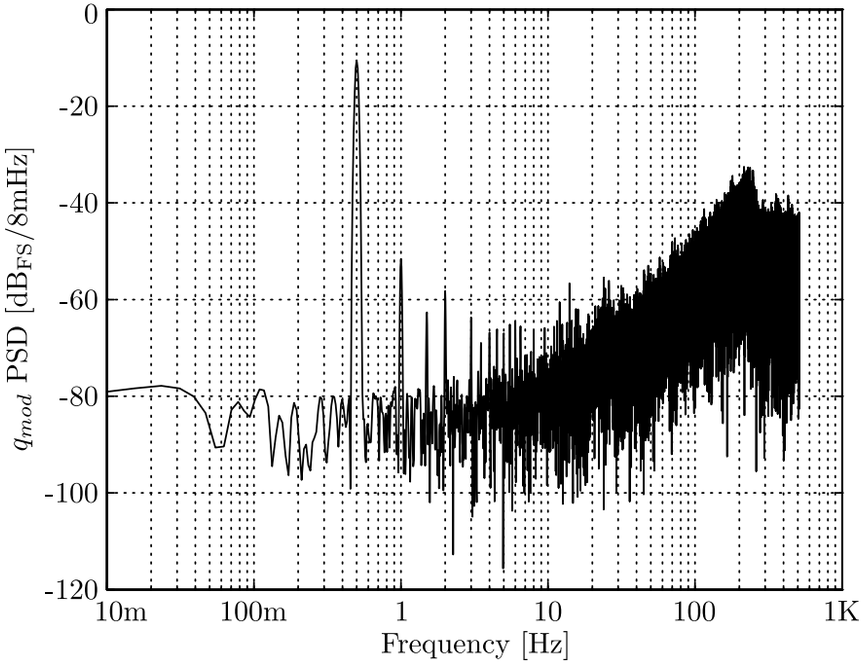
Electrical Tests

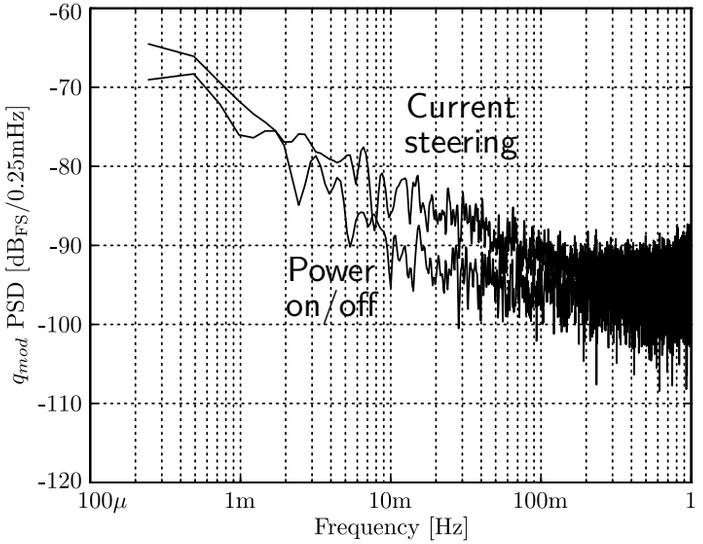
- **Sensor emulation** with external network (R_{ctw}=500kΩ, C_{dlw}=330nF) and SRS DS360 generator in equivalent Thévenin configuration
- Although dithering noise at DAC should be increased, PSD returns good **robustness** against tones
- Quasi-static response shows high enough **SNDR** to not limit electrochemical sensor resolution
- **Statistical analysis** on 9 samples returns DR deviations below ±0.5bit
- Experimental comparison between **power-on/off** and current steering DAC operation points to 3dB flicker noise reduction



2Hz noise bandwidth (OSR=256)



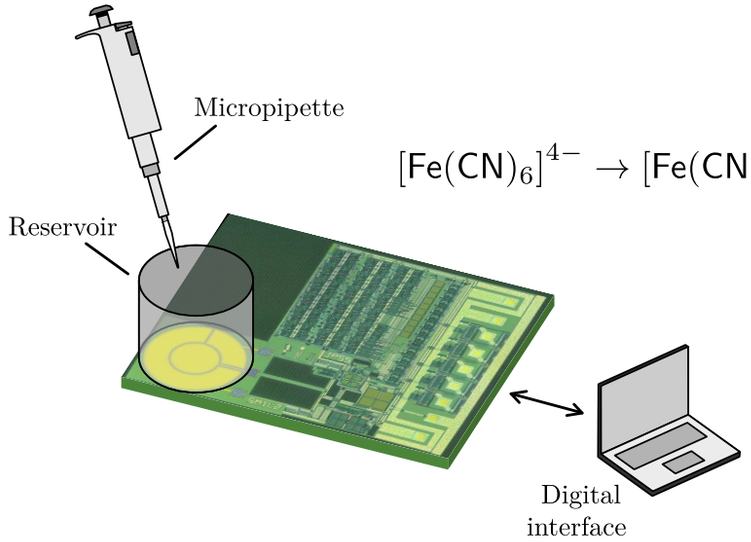




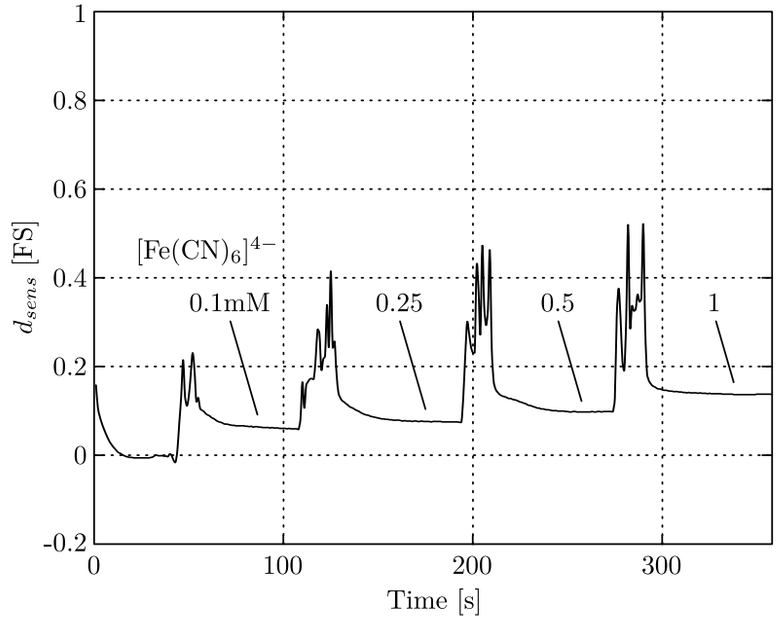
Electrochemical Tests

- **Standard experiment** based on ferrocyanide ion oxidation into ferricyanide:
- **10µL reservoir** with ferrocyanide dissolved in Phosphate buffer solution (PBS) at pH=7
- **Ion concentration** swept from 0.1mM to 1mM and **potentiostatic** V_{ref}=0.7V

▲ Electrochemical **time constant** as expected...



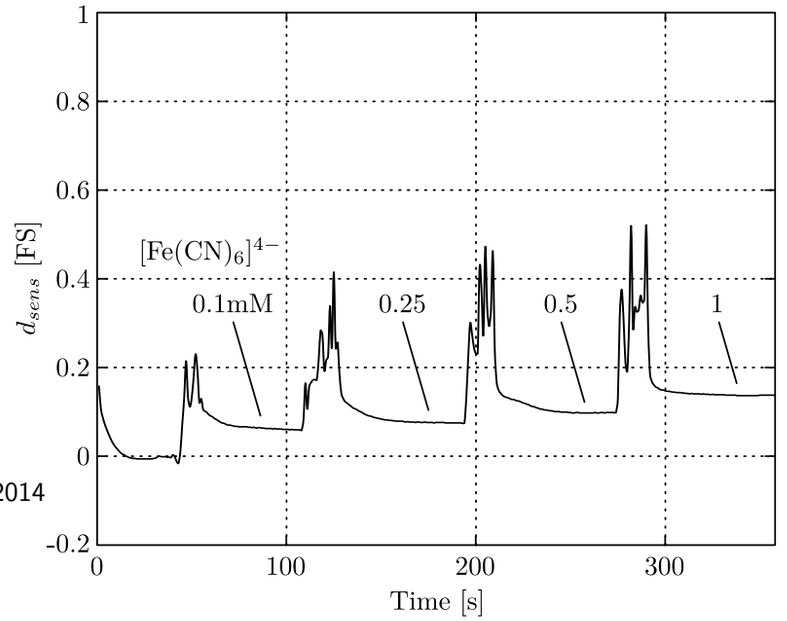
$$[Fe(CN)_6]^{4-} \rightarrow [Fe(CN)_6]^{3-} + 1e^-$$



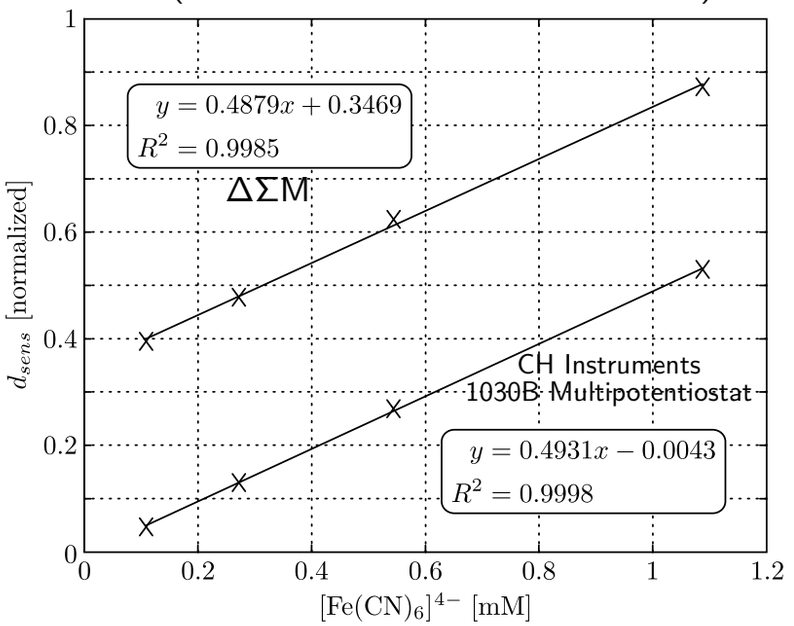
Electrochemical Tests

- Remarkable **linearity** below 1mM
- Comparable to lab **desktop equipment**
- Good **performance** for sensing applications
- Very **low-power** operation compared to sensor consumption itself (can improve with low-voltage CMOS technologies)

Parameter	Value	Units
Full scale range	2 to 32	μA
Potential range	0 to 5	V
Sampling frequency	1	kHz
Oversampling ratio	$\geq$256	
Electrical dynamic range	$>$10	ENOB
Residual standard deviation (n=6)	$<$15	%
Coefficient of determination (R^2)	0.9985	
Supply voltage	5	V
Power consumption at 2μA_{FS}	25	μW
Die size	2.3$\times$2.8	mm^2



(with same microelectrode structure)



↗ S. Sutula, et al.
A 25-μW All-MOS Potentiostatic Delta-Sigma ADC for Smart Electrochemical Sensors
IEEE Transactions on Circuits and Systems-I, 61:3(671-679), Mar 2014
doi.org/10.1109/TCSI.2013.2284179