# 6. Delta-Sigma Modulators for ADC

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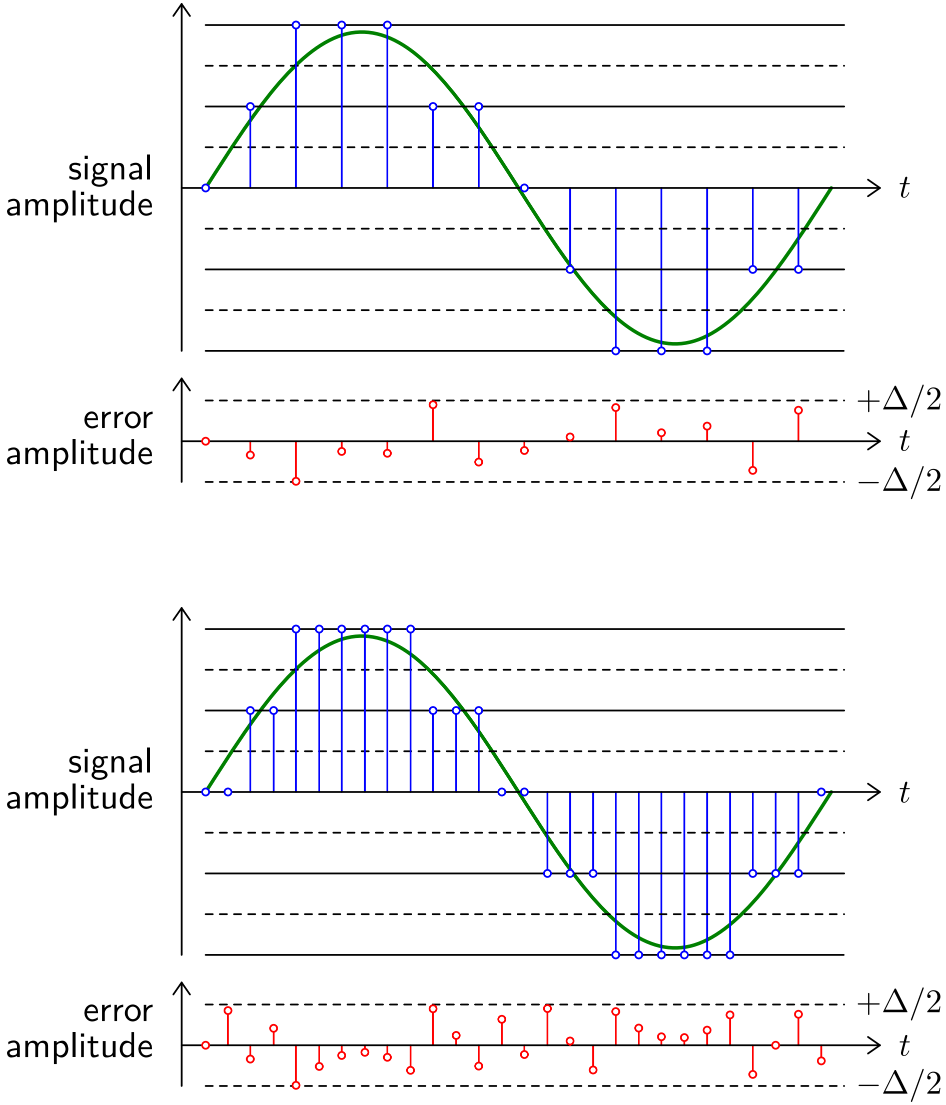
# Oversampling

- Flat (**white**) error spectrum profile

$$\Delta = \frac{V_{FS}}{2^N} \qquad QN = \frac{\Delta^2}{12}$$

e.g. 5-level quantization




2-times sampling rate

# Oversampling

- Flat (**white**) error spectrum profile:

$$QN(f) = \frac{1}{6}\frac{\Delta^2}{f_s} \quad \text{[W/Hz]}$$

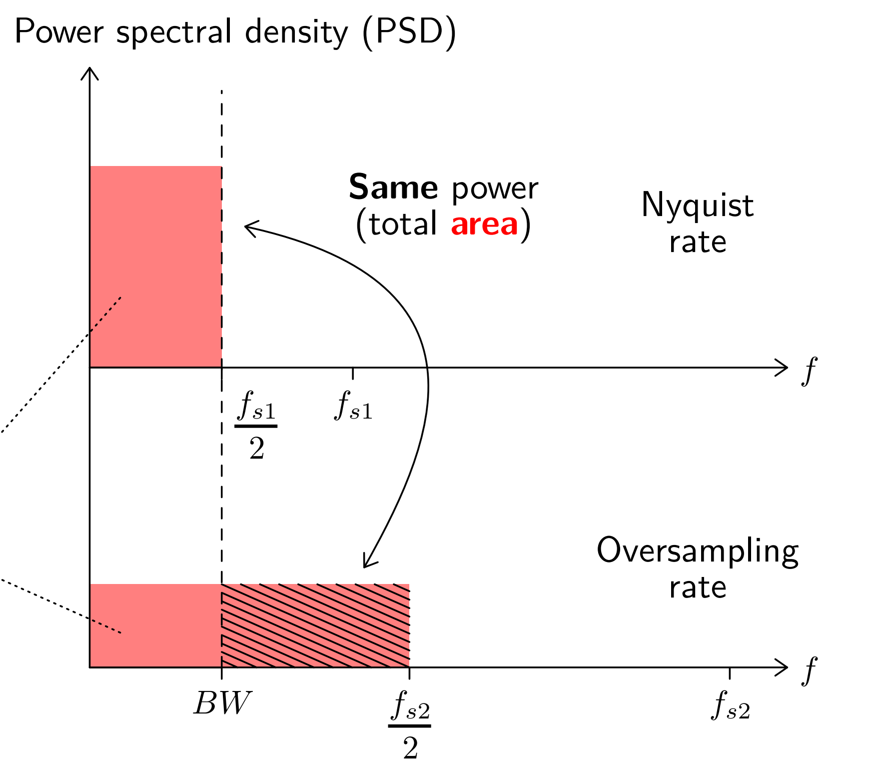
- **Spread** across spectrum (fs/2)

- **Oversampling** ratio:

$$OSR \doteq \frac{f_s}{f_{nyq}} \equiv \frac{f_s}{2BW}$$

**dependent** from sampling frequency

$$QN = \frac{1}{6}\frac{BW}{f_s}\Delta^2$$



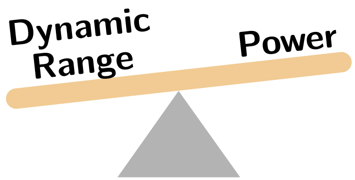

$$QN = \frac{\Delta^2}{12}\frac{1}{OSR} \qquad S_{max} = \left(\frac{V_{FS}}{2\sqrt{2}}\right)^2 \qquad SQNR_{max} \doteq \frac{S_{max}}{QN} = \left(2^N\sqrt{1.5}\right)^2 OSR$$

- ▲ Lower **in-band noise**

$$SQNR_{max} = 6.02N + 1.76 + 10\log OSR \quad \text{[dB]}$$

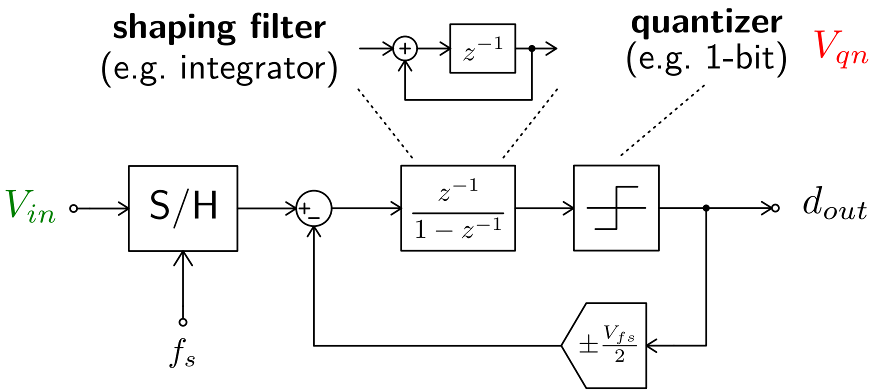
+3dB/oct
+0.5bit/oct

- ▼ Higher **clock frequencies**



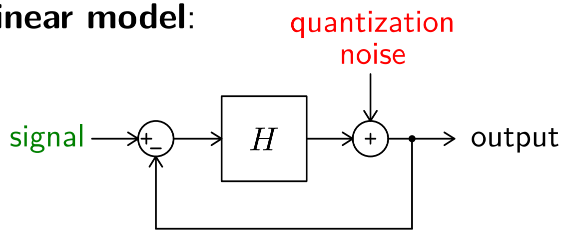
# Quantization Noise Shaping

- Basic single-loop Delta-Sigma modulator (**DSM**) for discrete time (**DT**) ADCs:

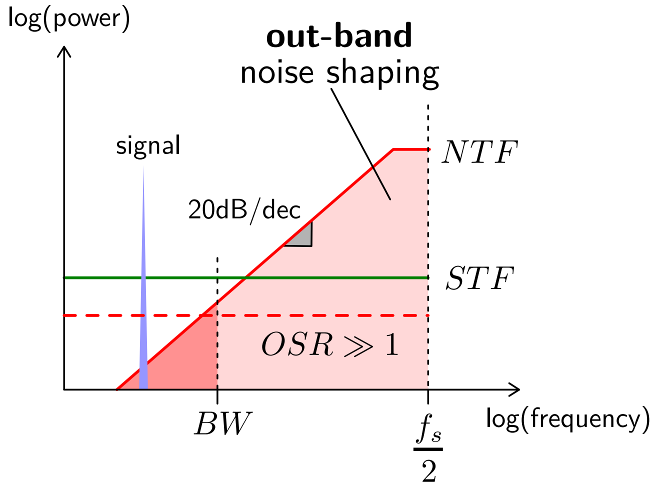



$$D_{out} = STF(z)V_{in} + NTF(z)V_{qn} \quad \begin{cases} STF = \dfrac{H}{1+H} & \rightarrow 1 \\ & H \rightarrow \infty \\ NTF = \dfrac{1}{1+H} & \rightarrow 0 \end{cases}$$

Equivalent **linear model**:

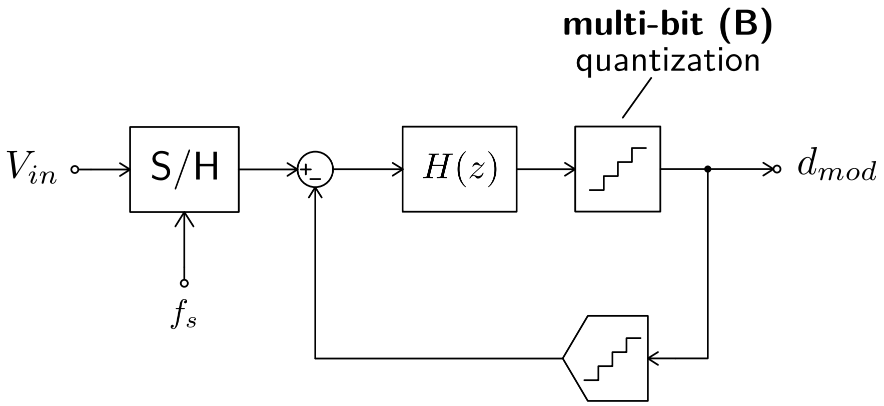



$$H(z) = \frac{z^{-1}}{1-z^{-1}} \quad \begin{cases} STF = \dfrac{H}{1+H} \equiv z^{-1} & \text{all-pass} \\ NTF = \dfrac{1}{1+H} \equiv 1 - z^{-1} & \textbf{high-pass}\text{ shaping} \end{cases}$$



# Quantization Noise Shaping

- N-order B-bit single loop architecture:




- **Multi-bit** quantization:
  - Resolution added to overall **DR**
  - **Internal full-scale** reduction
  - Feedback DAC **not intrinsically linear**

- **High-order** filtering:
  - **Sharper** noise shaping
  - **Stability** issues

- **Ideal** dynamic range:

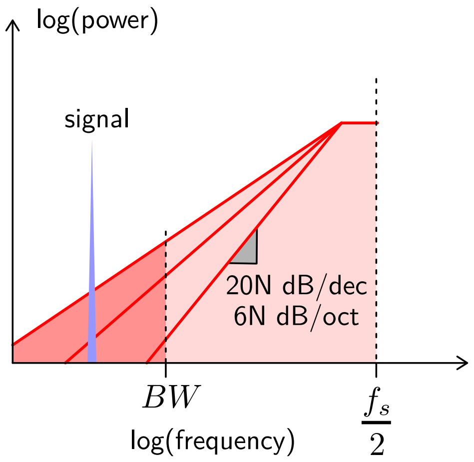
$$DR = \frac{3\pi}{2}\left(2^B - 1\right)^2 (2N+1)\left(\frac{OSR}{\pi}\right)^{2N+1}$$

**shaping** order — **oversampling** only

**(N+0.5)-bit/oct(OSR)**

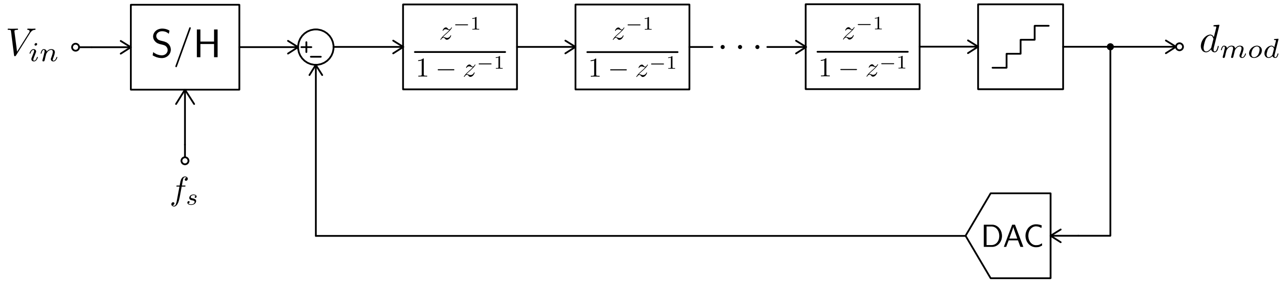
$$DR[\text{dB}] = 6.7 + 20\log\left(2^B - 1\right) + 10\log(2N+1) + 20(N+0.5)\log\frac{OSR}{\pi}$$

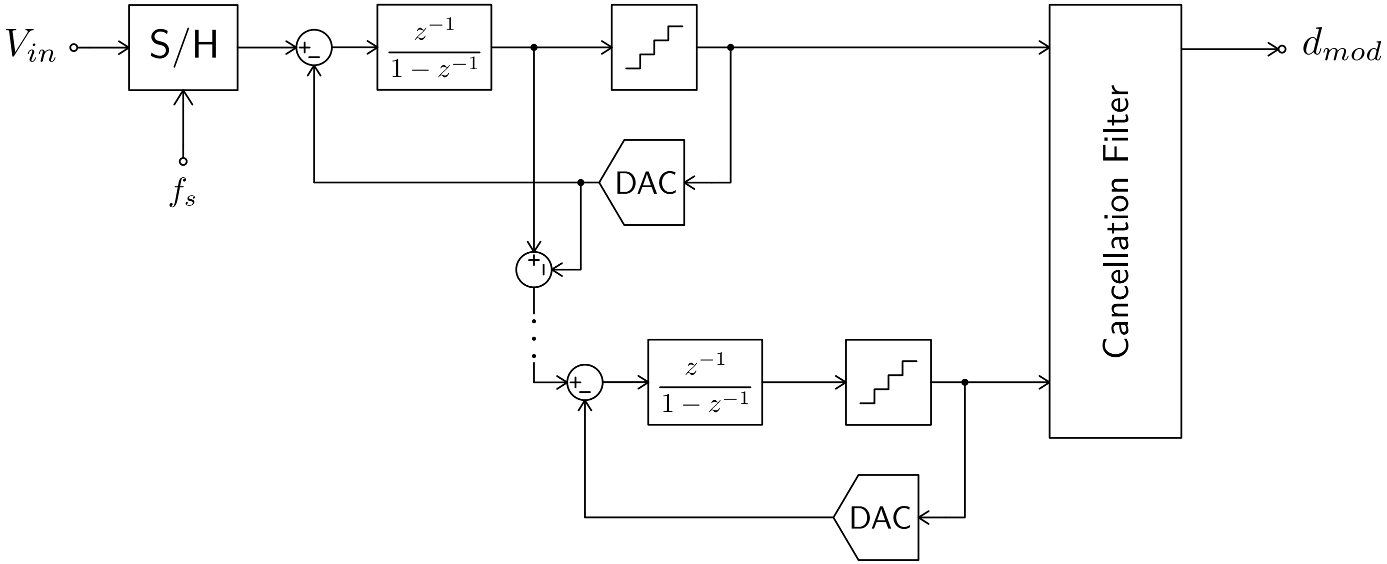
**direct** improvement



# Single-Loop vs MASH

- High-order **feedback** or **feedforward** DSM architectures:



# Single-Loop vs MASH

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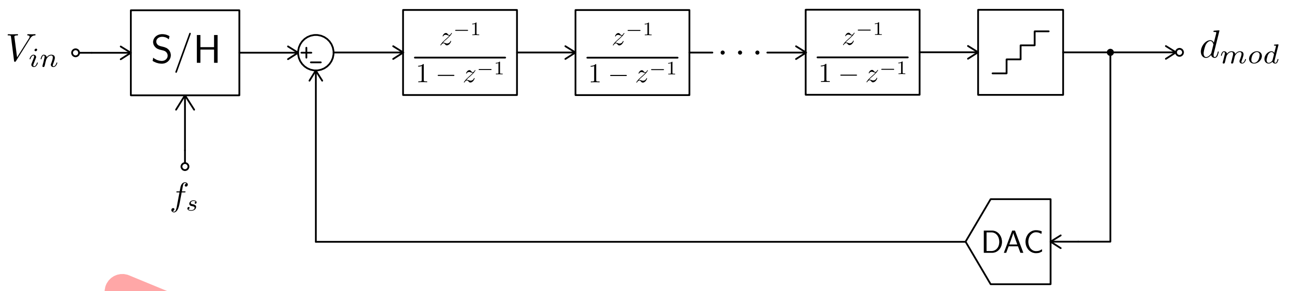
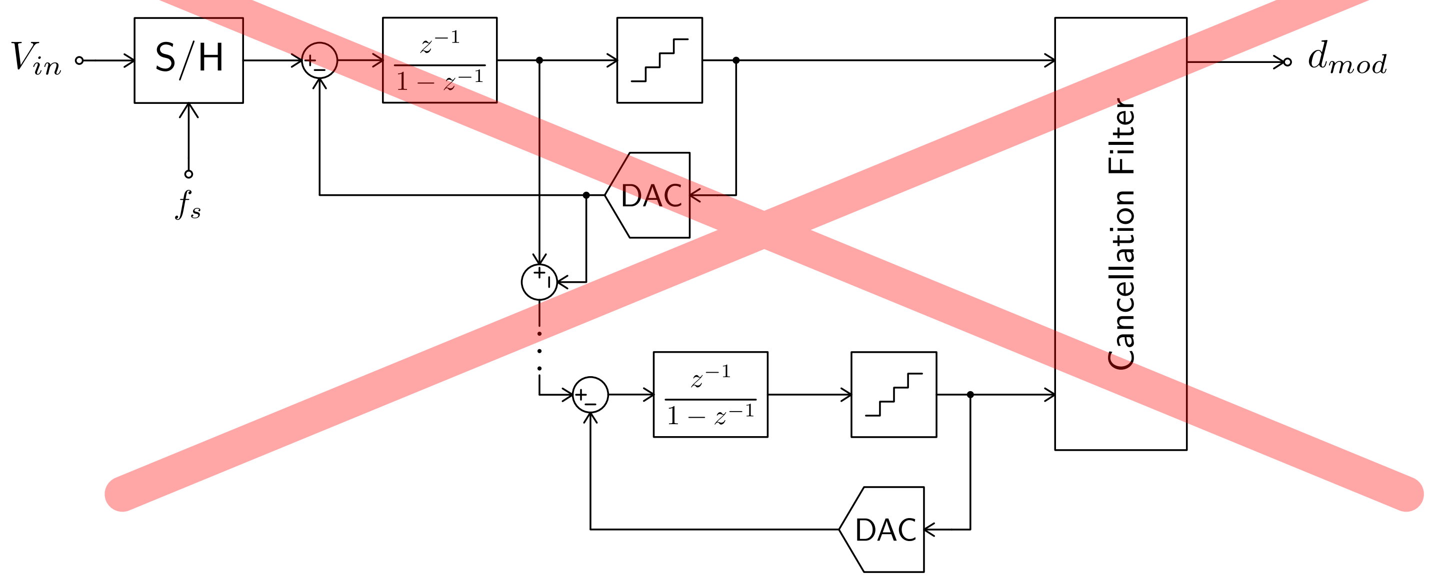
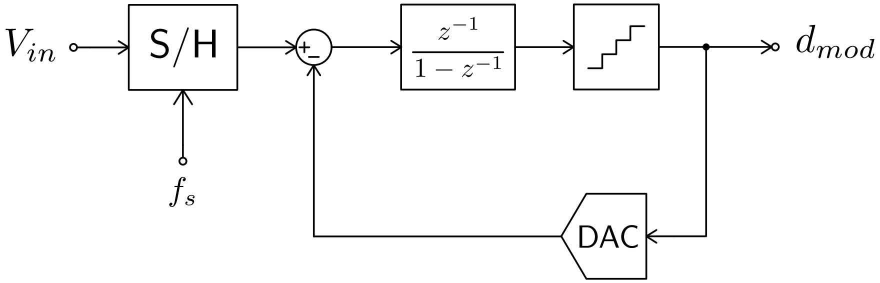



- **Unstability** issues
- **Mismatching** sensitivity
- More suitable for DSM **DACs**!

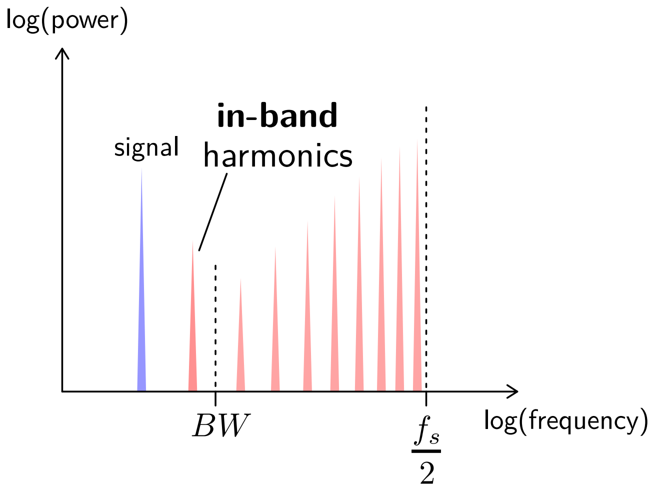
# Order Selection

- Simplest DSM architecture: **first order**



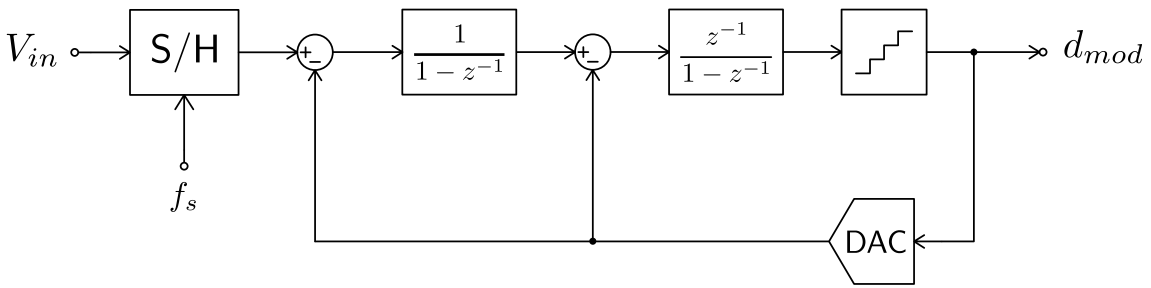

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \quad \begin{cases} STF = \dfrac{H}{1+H} \equiv z^{-1} \\ NTF = \dfrac{1}{1+H} \equiv 1 - z^{-1} \end{cases}$$

- ▲ Intrinsically **stable**
- ▼ **Large OSR** needed
- ▼ **Tonal** spectrum caused by signal to quantization noise correlation!



# Order Selection

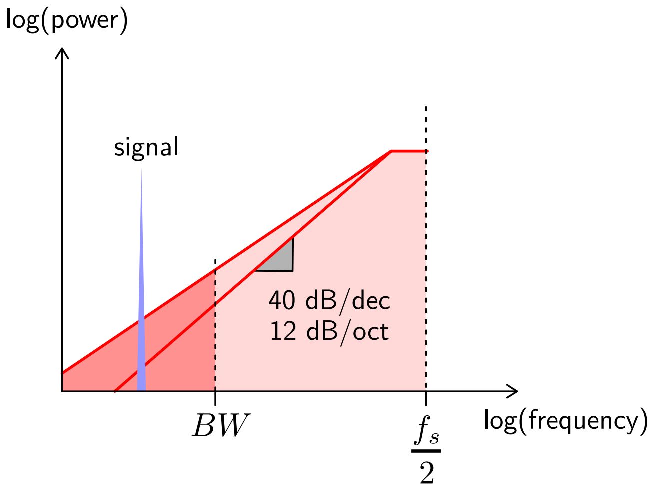
- Next architecture step: **second order**




$$
\begin{cases}
STF = \dfrac{1}{\left(\frac{1-z^{-1}}{z^{-1}}+1\right)(1-z^{-1})+1} \equiv z^{-1} \\
NTF = \dfrac{1}{1+\left(\frac{1}{1-z^{-1}}+1\right)\frac{z^{-1}}{1-z^{-1}}} \equiv (1-z^{-1})^2
\end{cases}
$$

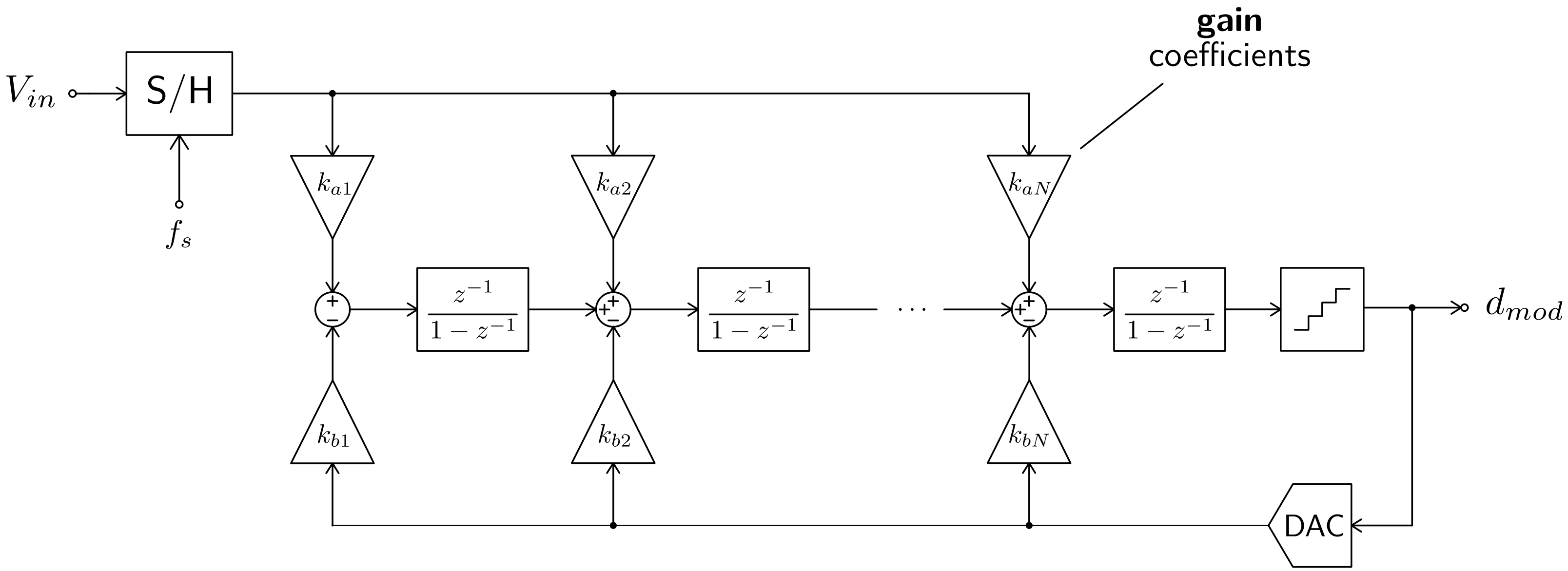
**second-order**
high-pass

- ▲ Intrinsically **stable** for limited input range
- ▲ Signal to quantization noise **uncorrelation** (continuous spectrum)
- Moderate **OSR** requirements



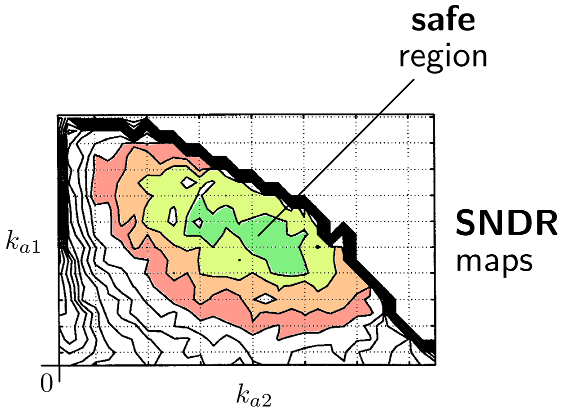
# Delta-Sigma Noise Shaping

- **Higher-order** general architecture:



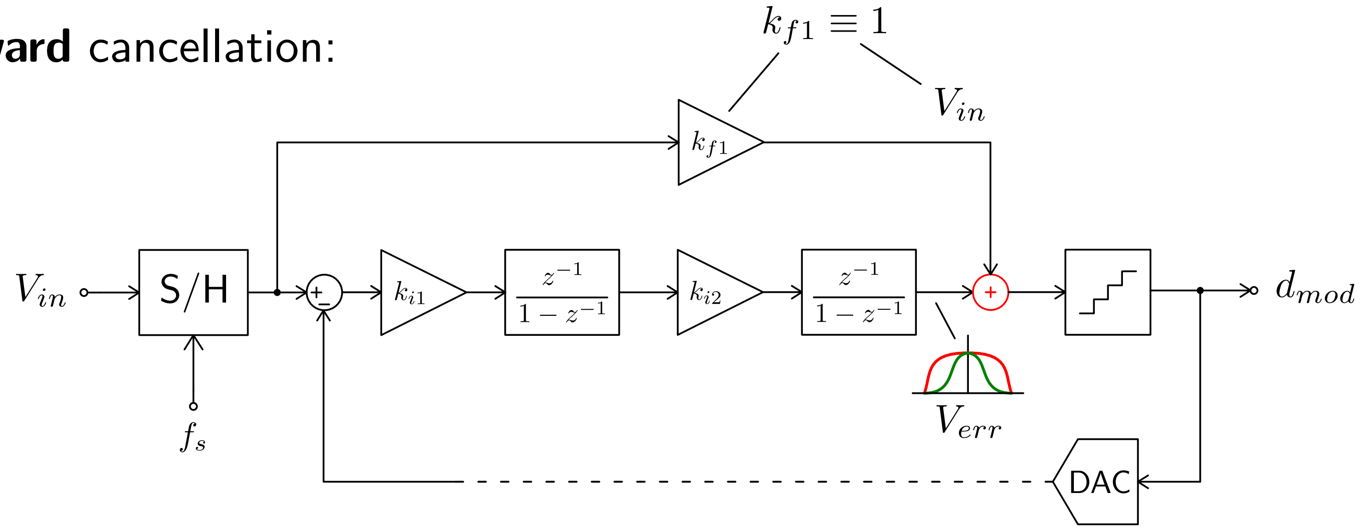

- ▲ **Sharper** noise shaping
- ▼ Possibility of loop **instability** for N>2

- **Coefficients** optimization against **mismatching**



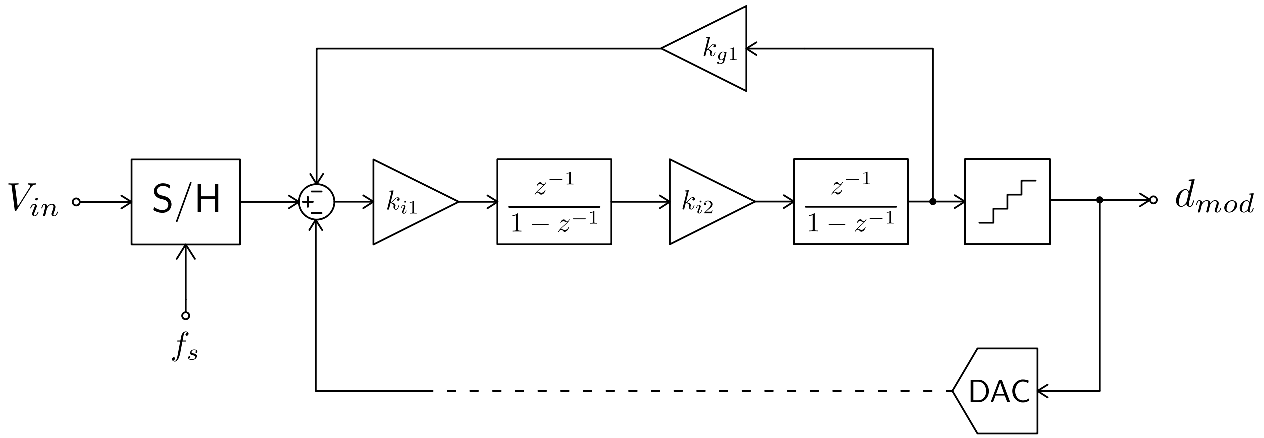
# Commonly Used Architectures

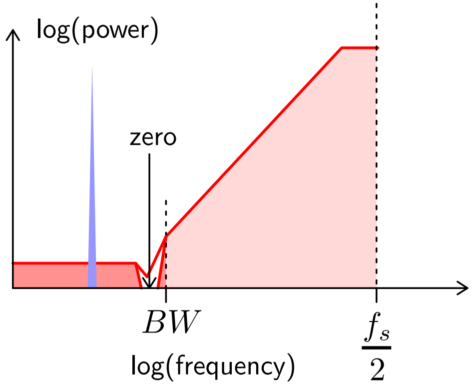
- **Feedfoward** cancellation:




- ▲ **Internal full scale** low occupancy
- ▼ Additional **adder stage** in front of quantizer

- **Resonator** attenuation:

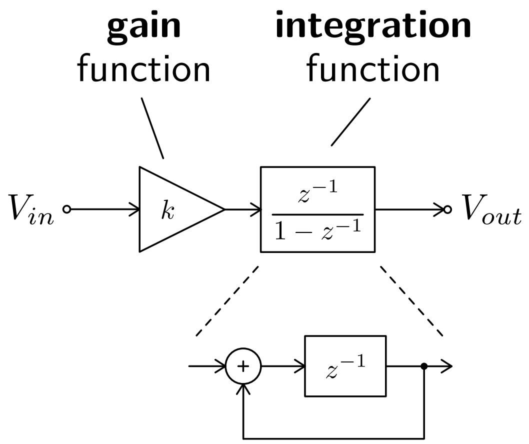



- ▲ Extra noise shaping at **band edge**
- ▼ Zero sensitivity to coefficient **matching**

# SC Integrator

- Shaping filter basic building **block**:




**Analog** circuit realization (ADC)

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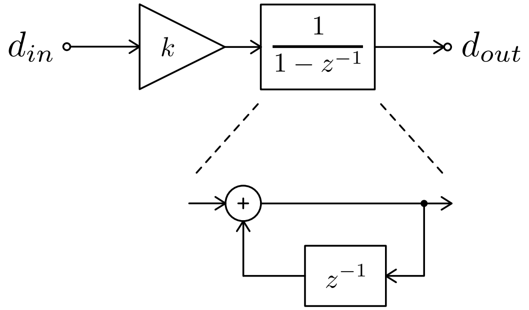
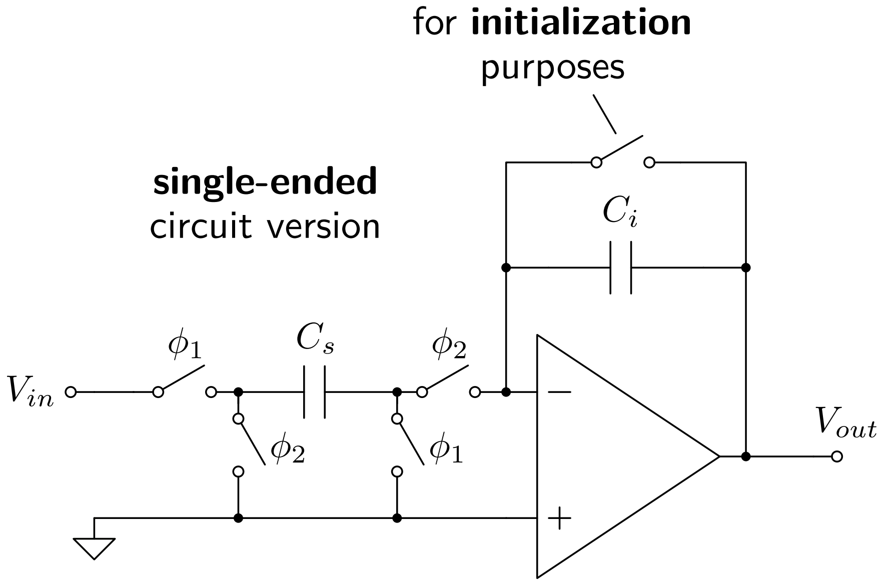
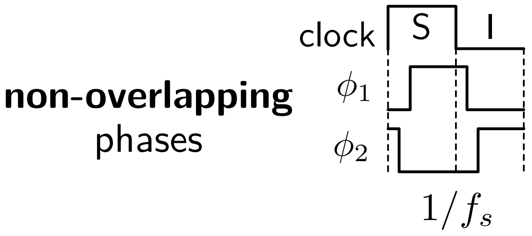
**Digital** circuit realization (DAC)




- SC-OpAmp **compact** implementation:




$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

# SC Integrator

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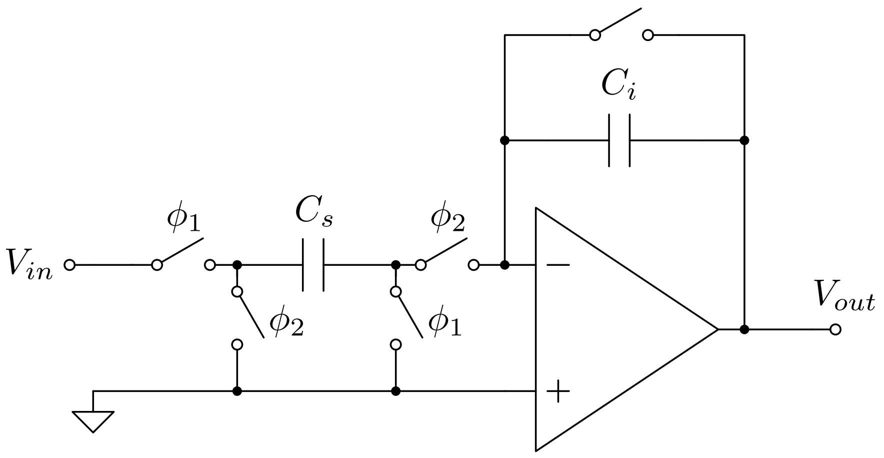


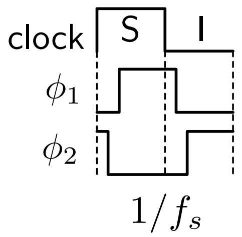


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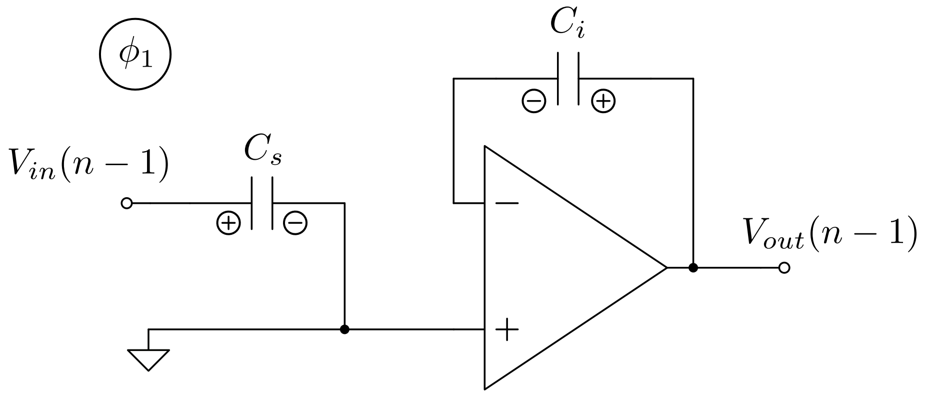

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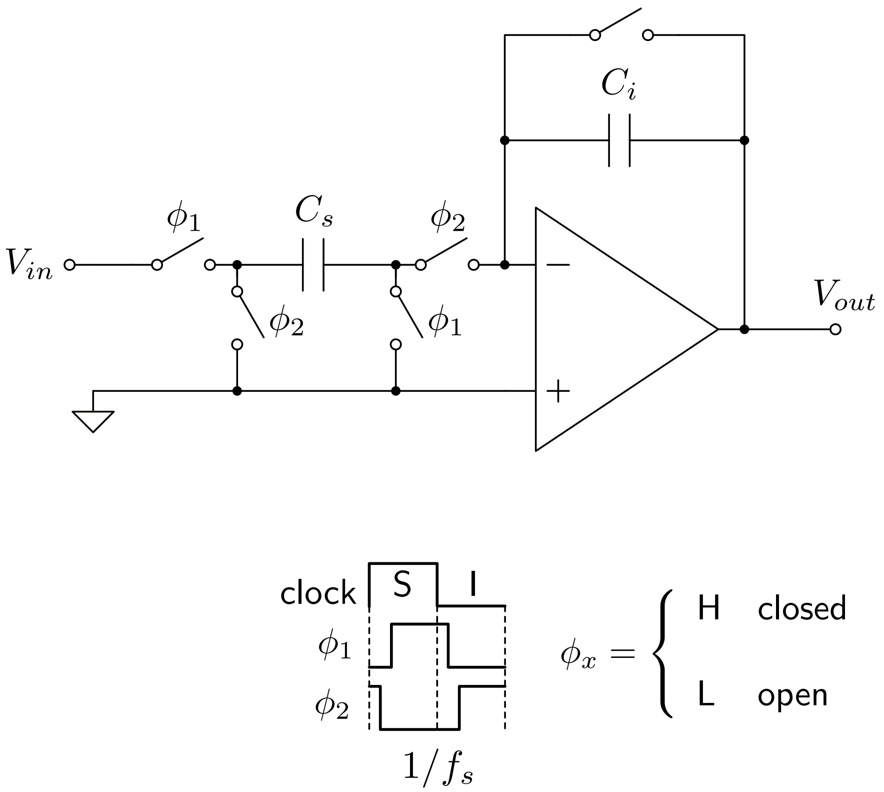


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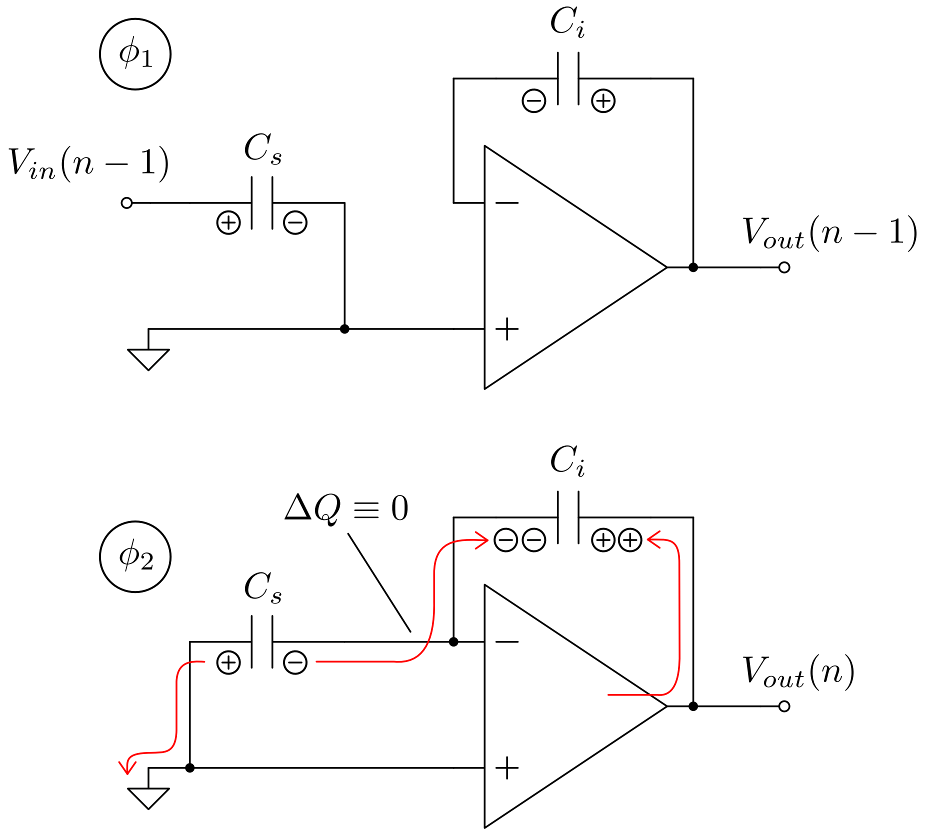


$$V_{out}(n) = V_{out}(n-1) + \frac{C_s}{C_i} V_{in}(n-1)$$

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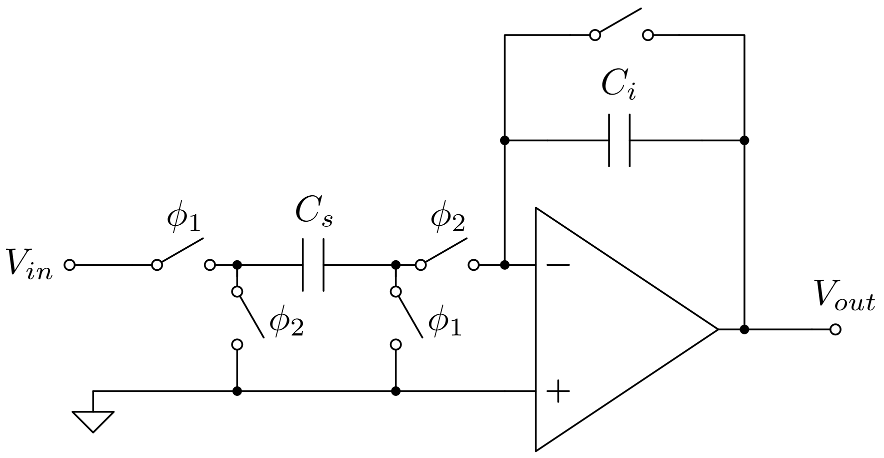
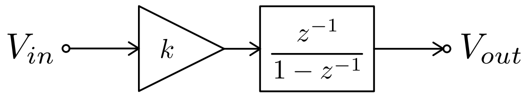
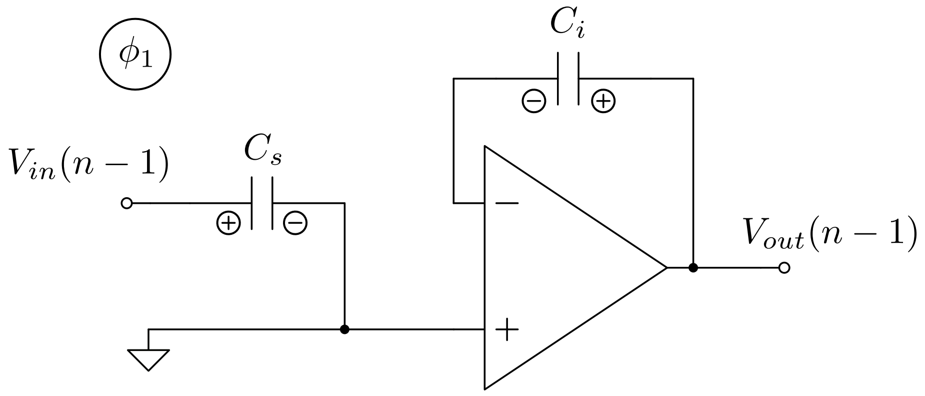
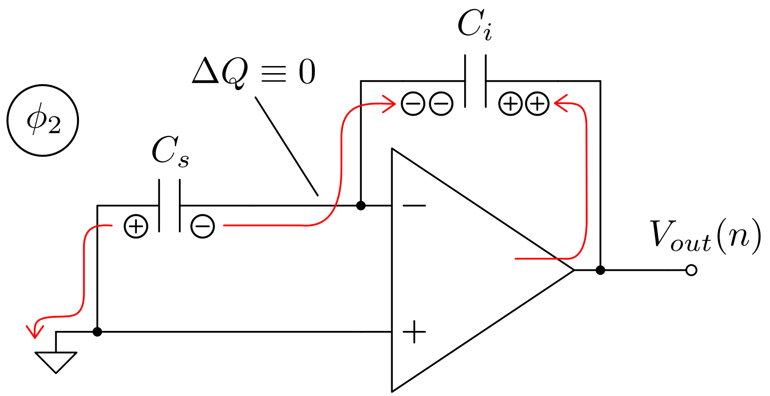



$$\frac{V_{out}(z)}{V_{in}(z)} = k\frac{z^{-1}}{1-z^{-1}} \qquad k \doteq \frac{C_s}{C_i}$$



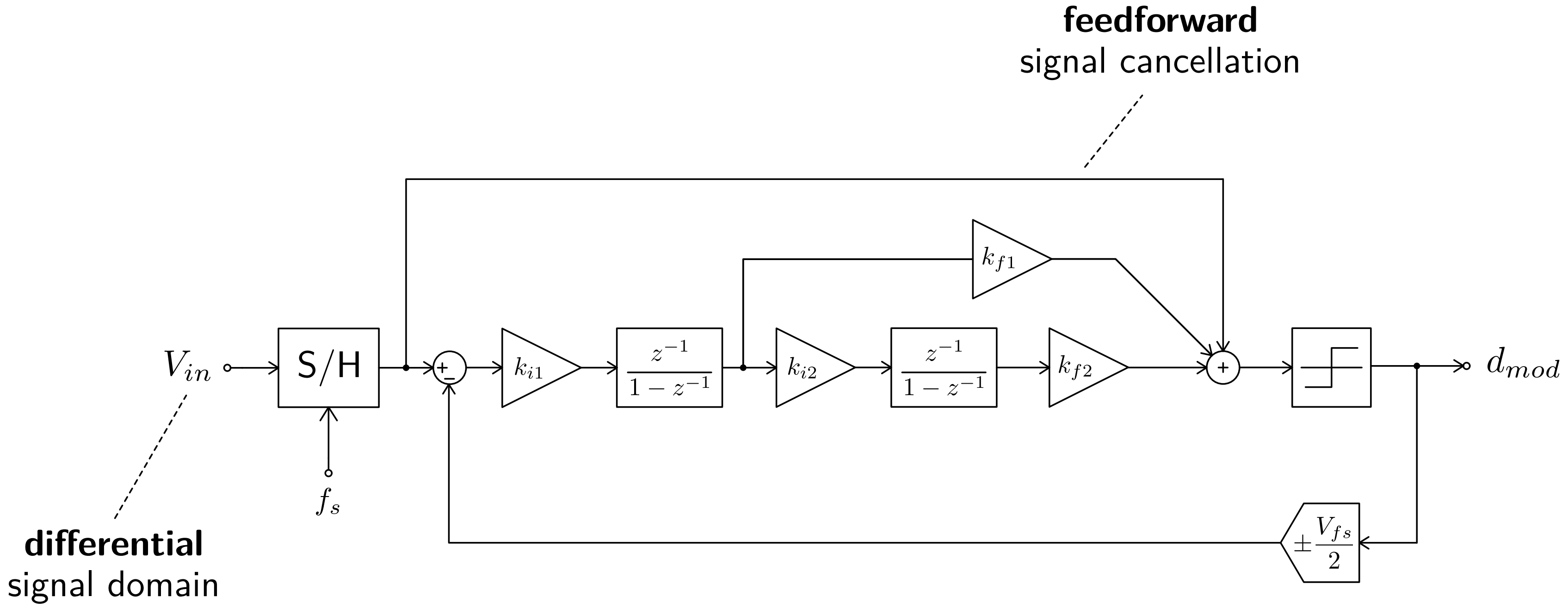




$$V_{out}(n) = V_{out}(n-1) + \frac{C_s}{C_i}V_{in}(n-1)$$

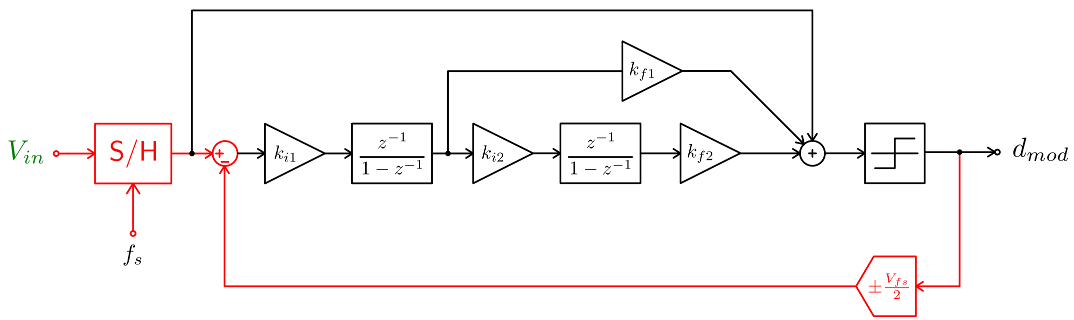
$$V_{out}(z) = z^{-1}V_{out}(z) + \frac{C_s}{C_i}z^{-1}V_{in}(z)$$

## SC Noise Shaper

- **Fully-differential** 2nd-order single-bit DSM example:



# SC Noise Shaper



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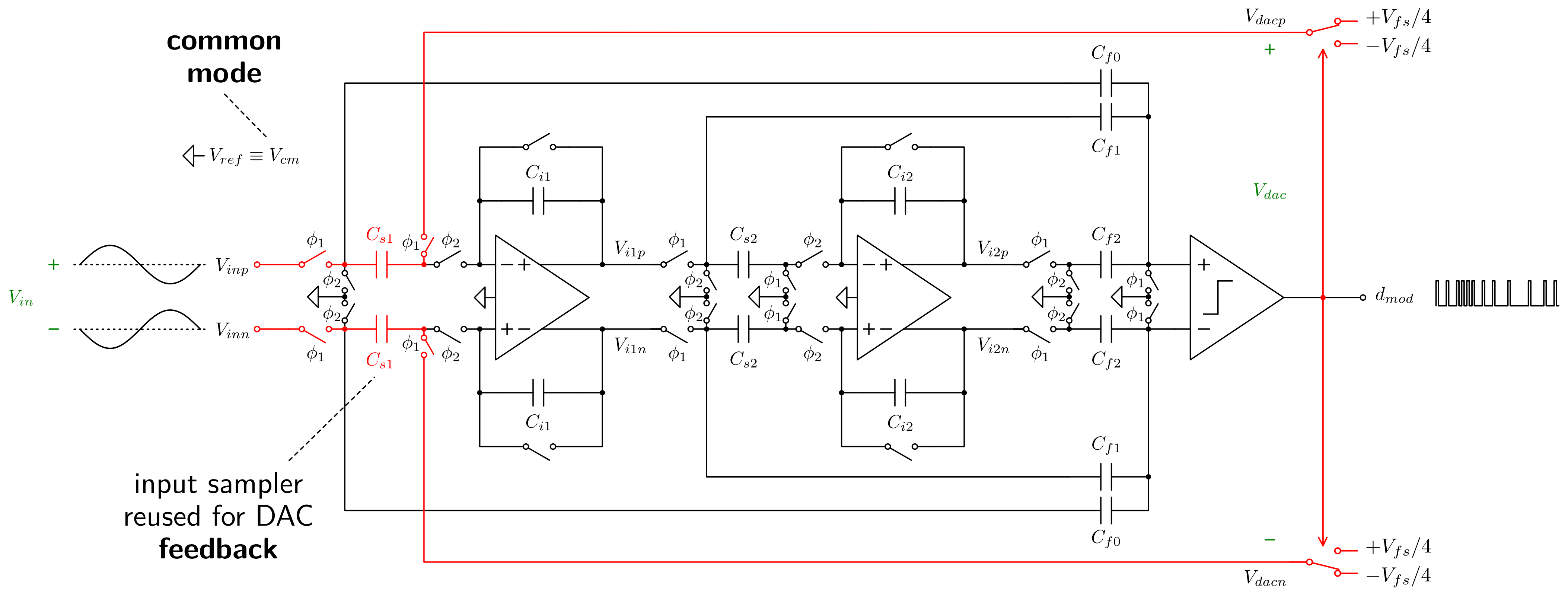
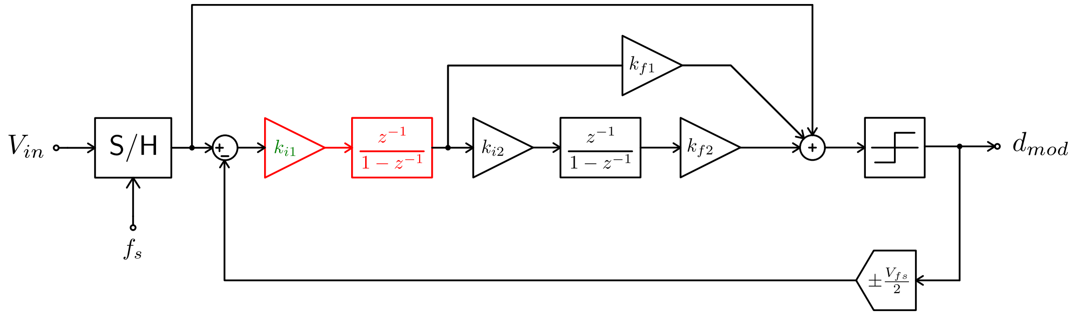



$\phi_1$ $Q_{s1}(n-1) = C_{s1}\left[V_{in}(n-1) - V_{dac}(n-1)\right]$

# SC Noise Shaper

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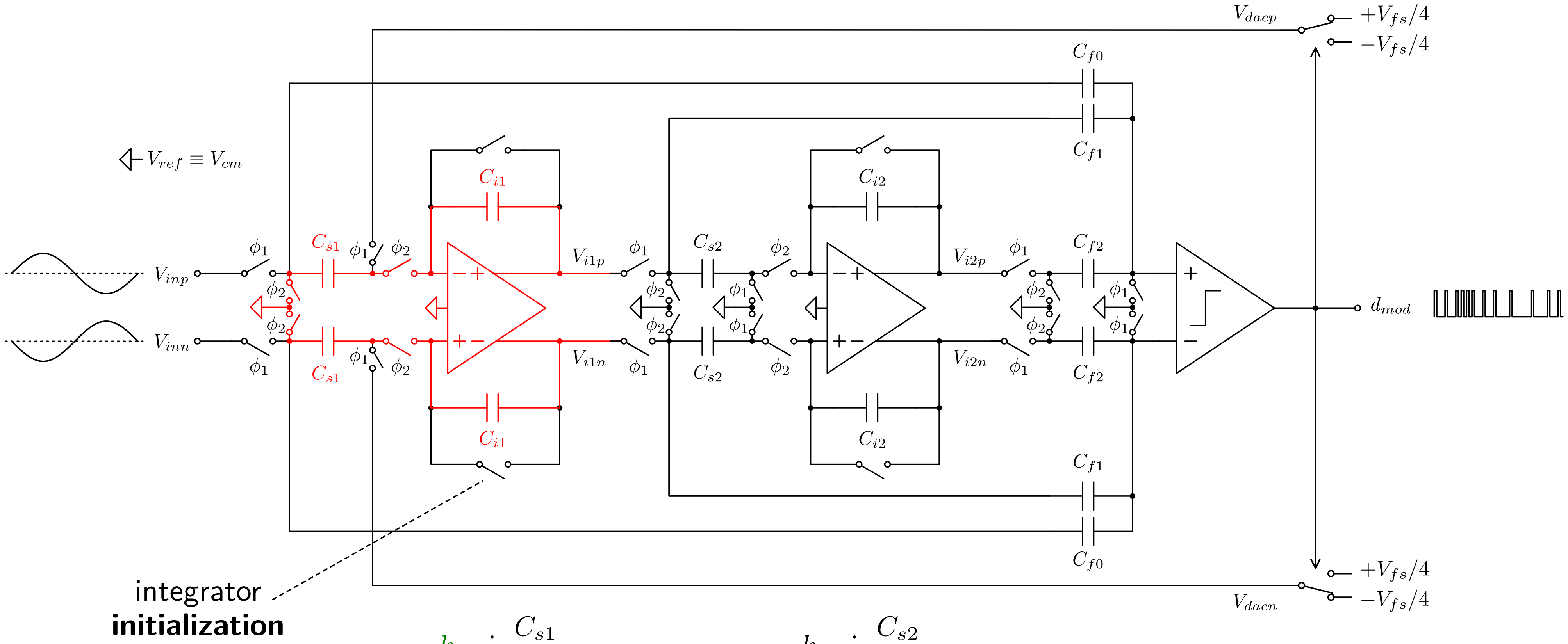


$$k_{i1} \doteq \frac{C_{s1}}{C_{i1}} \qquad k_{i2} \doteq \frac{C_{s2}}{C_{i2}}$$

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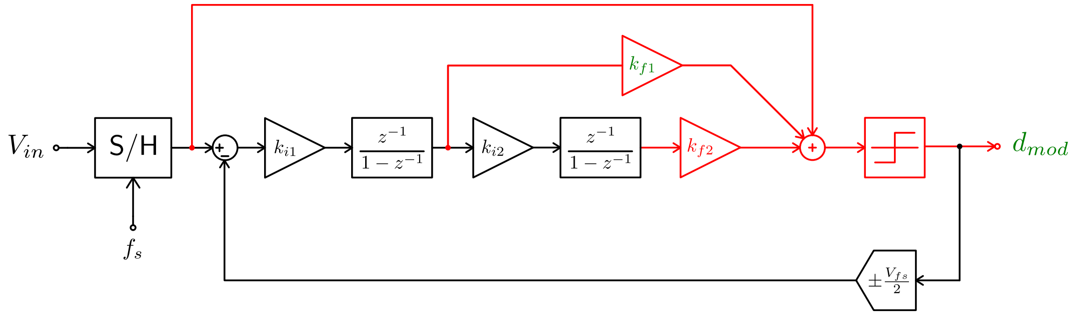
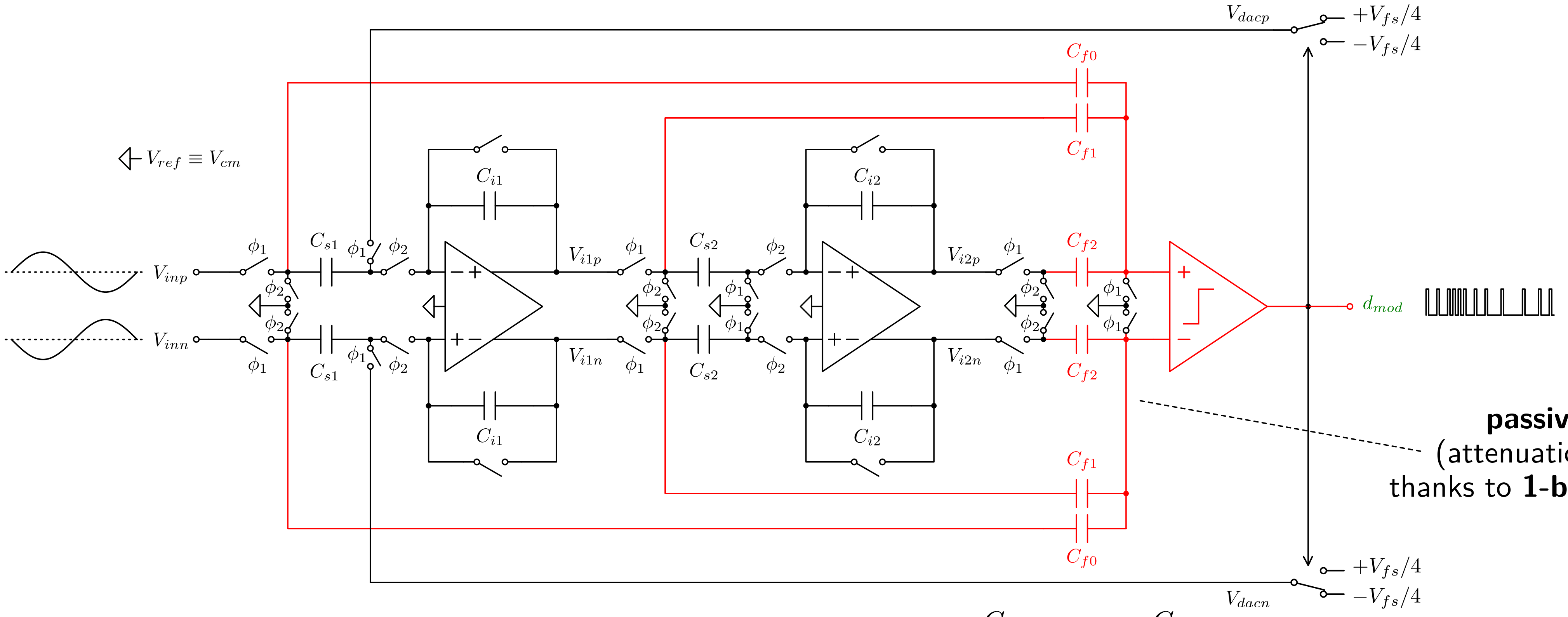


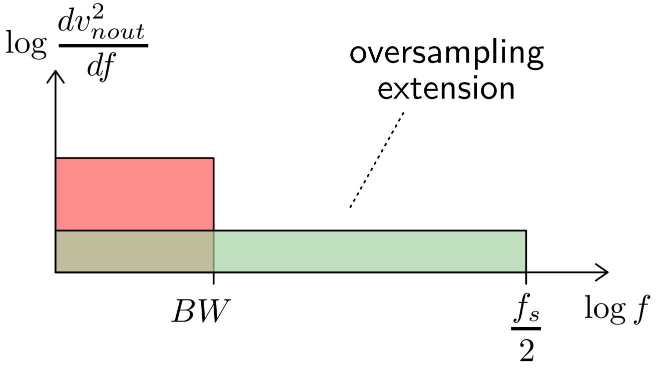



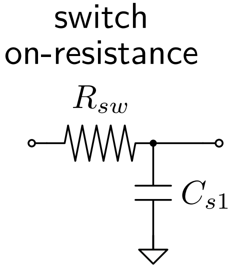

**passive adder**
(attenuation negligible
thanks to **1-bit** quantization)

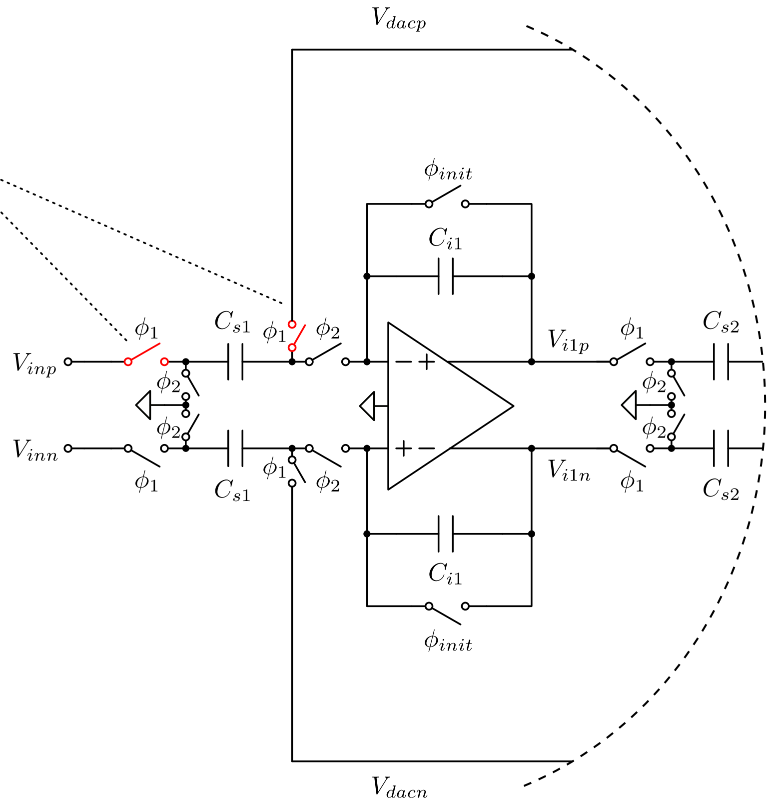
$$k_{f1} \doteq \frac{C_{f1}}{C_{f0}} \qquad k_{f2} \doteq \frac{C_{f2}}{C_{f0}}$$

# Switch Thermal Noise

- Added to signal at **input sampler**:




$$\frac{dv_{nout}^2}{df} = 4KTR_{sw}$$

$$v_{nsw}^2 \equiv \frac{KT}{C_{s1}} \frac{1}{OSR}$$

+0.5bit/oct

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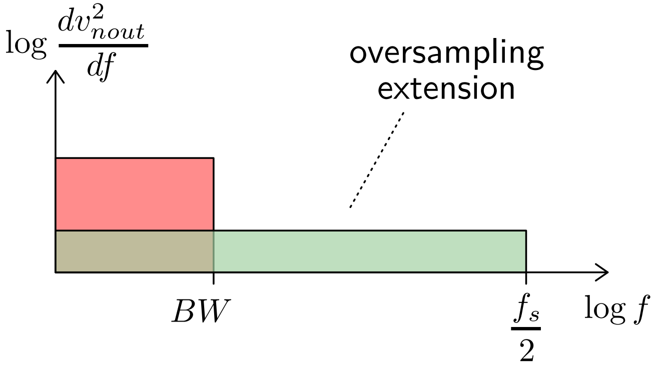
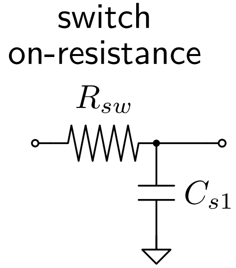


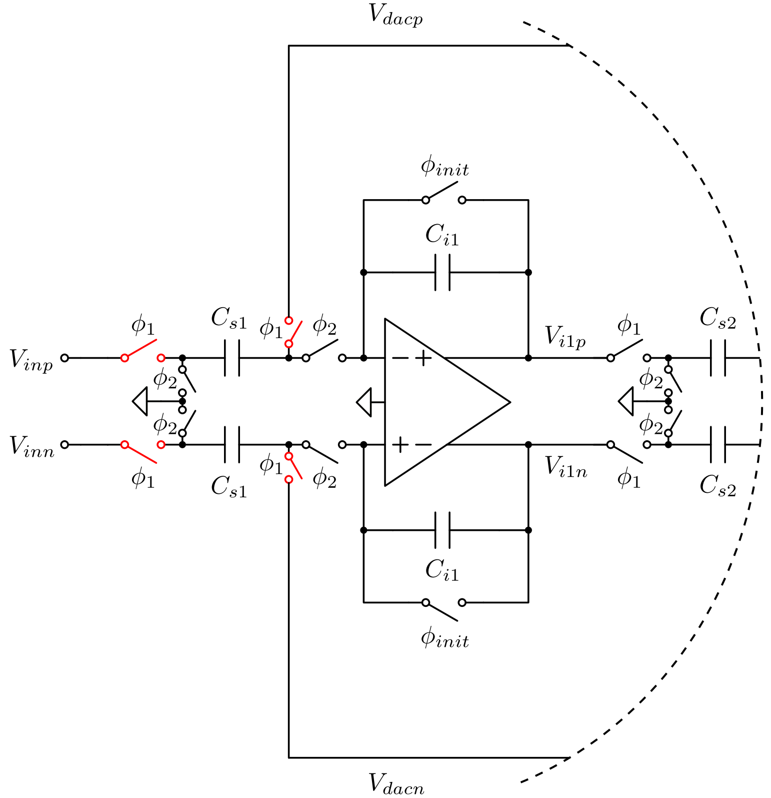



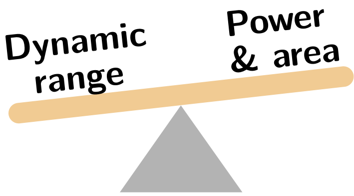

$$\frac{dv^2_{nout}}{df} = 4KTR_{sw} \qquad v^2_{nsw} \equiv \frac{KT}{C_{s1}} \frac{1}{OSR}$$

+0.5bit/oct

- **Fully differential** contributions: $v^2_{nswtot} \equiv 2\frac{KT}{C_{s1}}\frac{1}{OSR}$

$$DR_{diff} = DR_{sing} - \underbrace{3\text{dB}}_{\text{switches}\times 2} + \underbrace{6\text{dB}}_{\text{full-scale}\times 2} = DR_{sing} + 3\text{dB}(+0.5\text{bit})$$

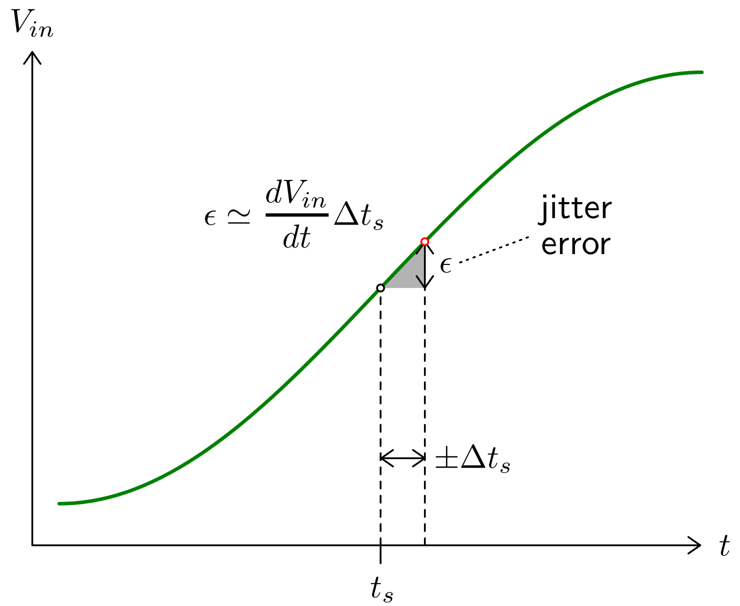


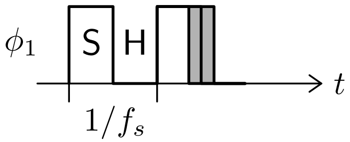



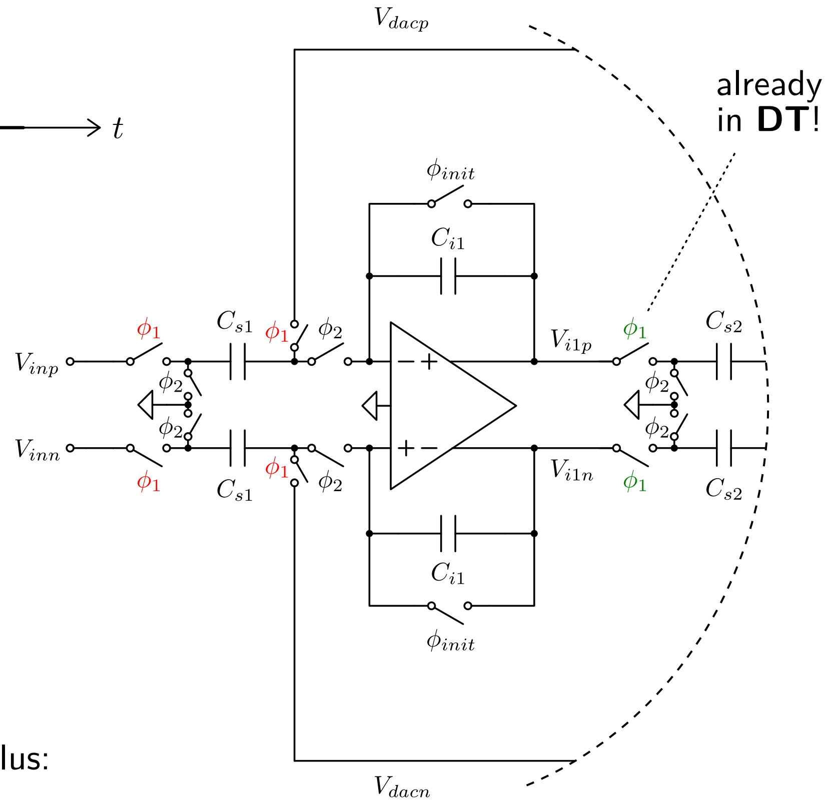

- Large **capacitor area** and low **input impedance** values!

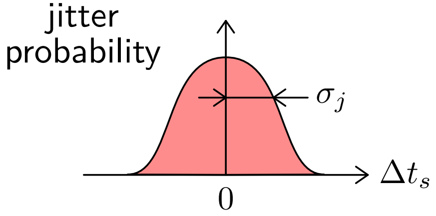
# Clock Jitter

- Critical at **input sampler** due to its continuous (**CT**) to discrete time (**DT**) conversion:



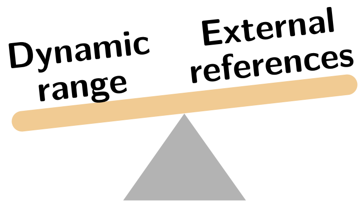



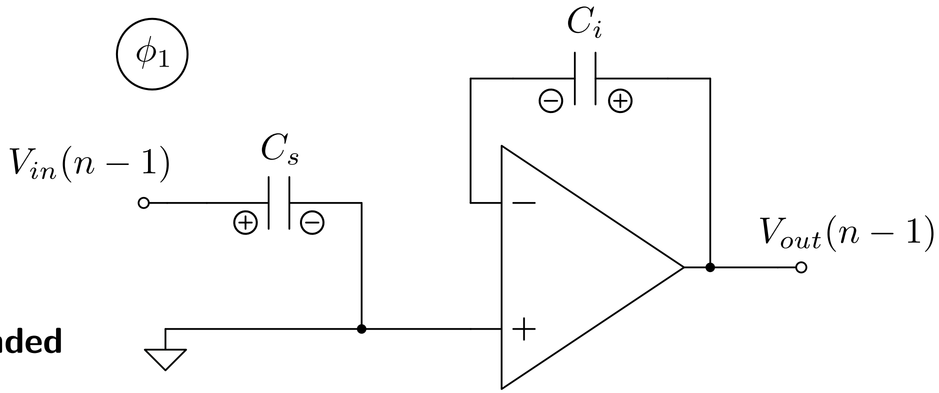

estimated power under **harmonic** stimulus:

$$JN = \frac{2(\sigma_j V_{FS}\pi BW)^2}{OSR}$$

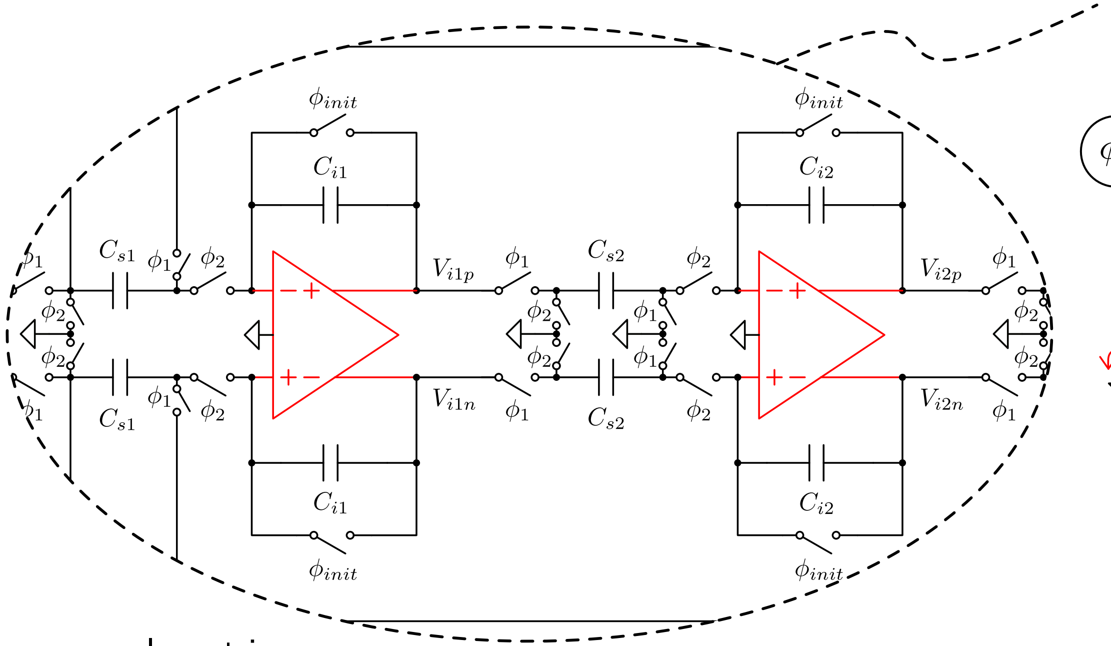


# OpAmp Finite Gain

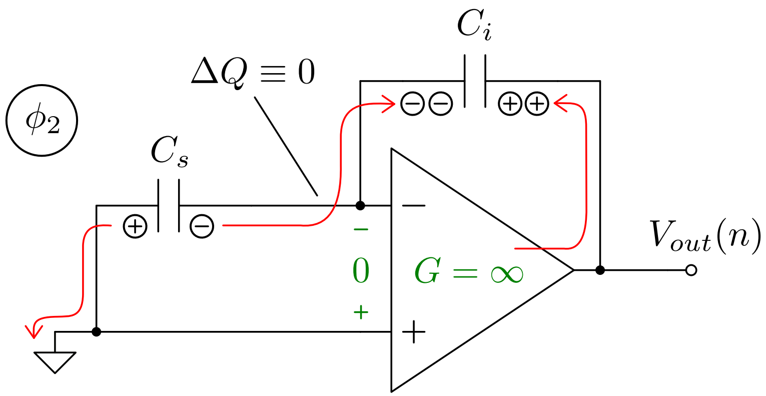
- SC **integrator** transfer function when OpAmp **open loop gain** is limited:




equivalent **single ended** half circuit




more relevant in **first stages**




$$V_{out}(n) = V_{out}(n-1) + \frac{C_s}{C_i} V_{in}(n-1)$$

$$\frac{V_{out}}{V_{in}}(z) = k\frac{z^{-1}}{1-z^{-1}} \qquad k \doteq \frac{C_s}{C_i}$$

# OpAmp Finite Gain

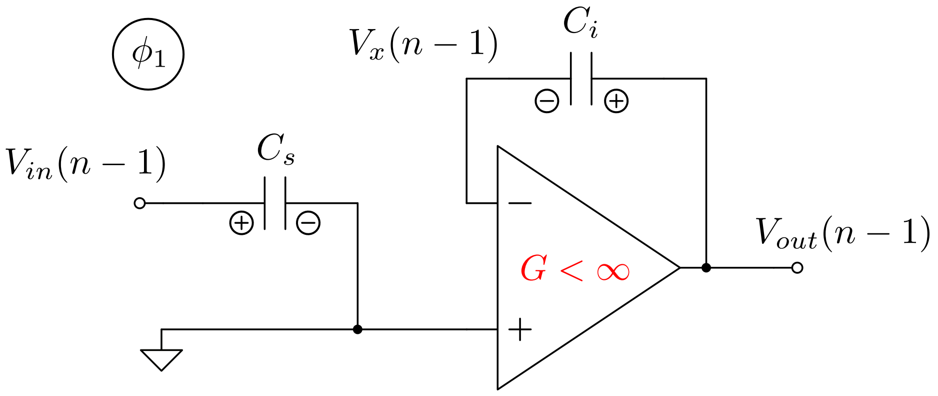
- SC **integrator** transfer function when OpAmp **open loop gain** is limited:

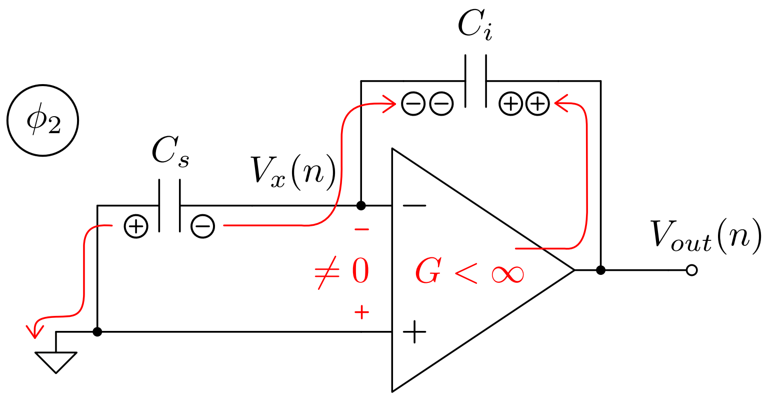
$$Q_x(n) \equiv Q_x(n-1)$$

$$C_s V_x(n) + C_i \left[ V_x(n) - V_{out}(n) \right] =$$
$$= -C_s V_{in}(n-1) + C_i \left[ V_x(n-1) - V_{out}(n-1) \right]$$

$$V_x \doteq -\frac{V_{out}}{G}$$

$$+C_s \frac{V_{out}(n)}{G} + C_i \left(1 + \frac{1}{G}\right) V_{out}(n) =$$
$$= +C_s V_{in}(n-1) + C_i \left(1 + \frac{1}{G}\right) V_{out}(n-1)$$




integration **leakage** gain **mismatch**

$$k \doteq \frac{C_s}{C_i} \qquad V_{out}(n) = \frac{V_{out}(n-1)}{1 + \frac{k}{1+G}} + \frac{k V_{in}(n-1)}{1 + \frac{1}{G}(k+1)}$$

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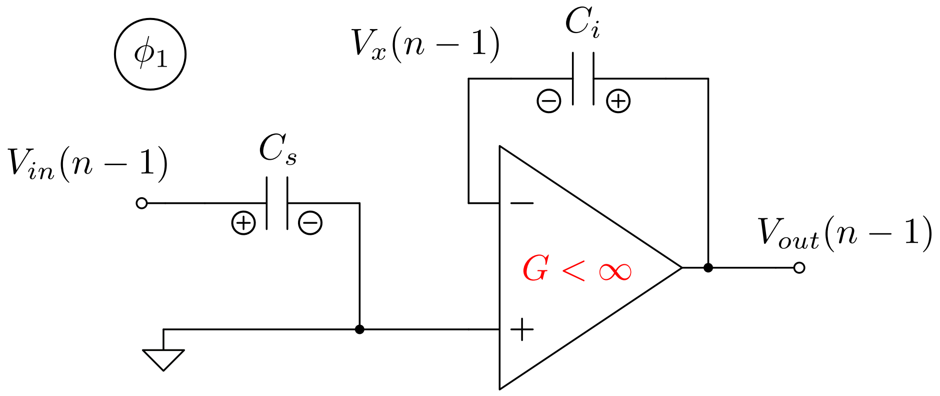


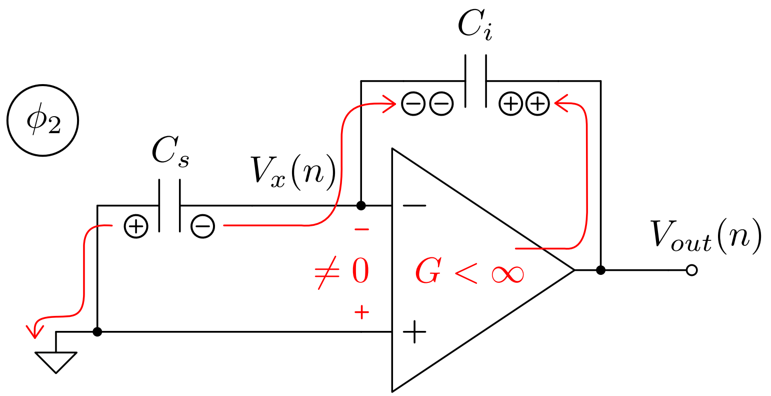


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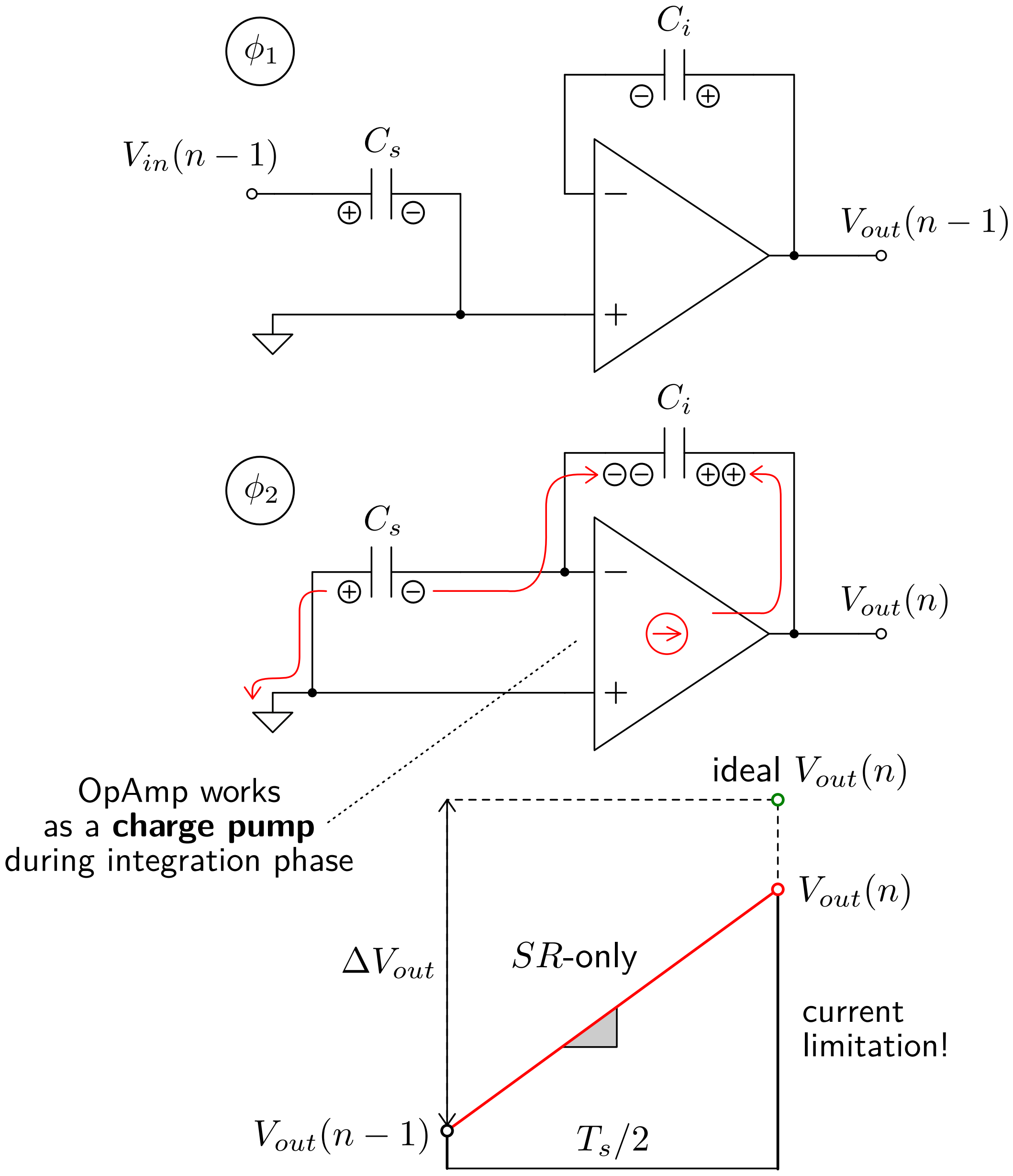
- **Signal dependent** gain generates output **distortion**

$$G \to \infty \qquad V_{out}(n) = V_{out}(n-1) + k V_{in}(n-1)$$

# OpAmp Slew-Rate and GBW

- Qualitative **case studies**:
  - if $SR < \dfrac{\Delta V_{out}}{T_s/2}$ : **slewing** only

$$V_{out}(n) = V_{out}(n-1) \pm SR\frac{T_s}{2}$$



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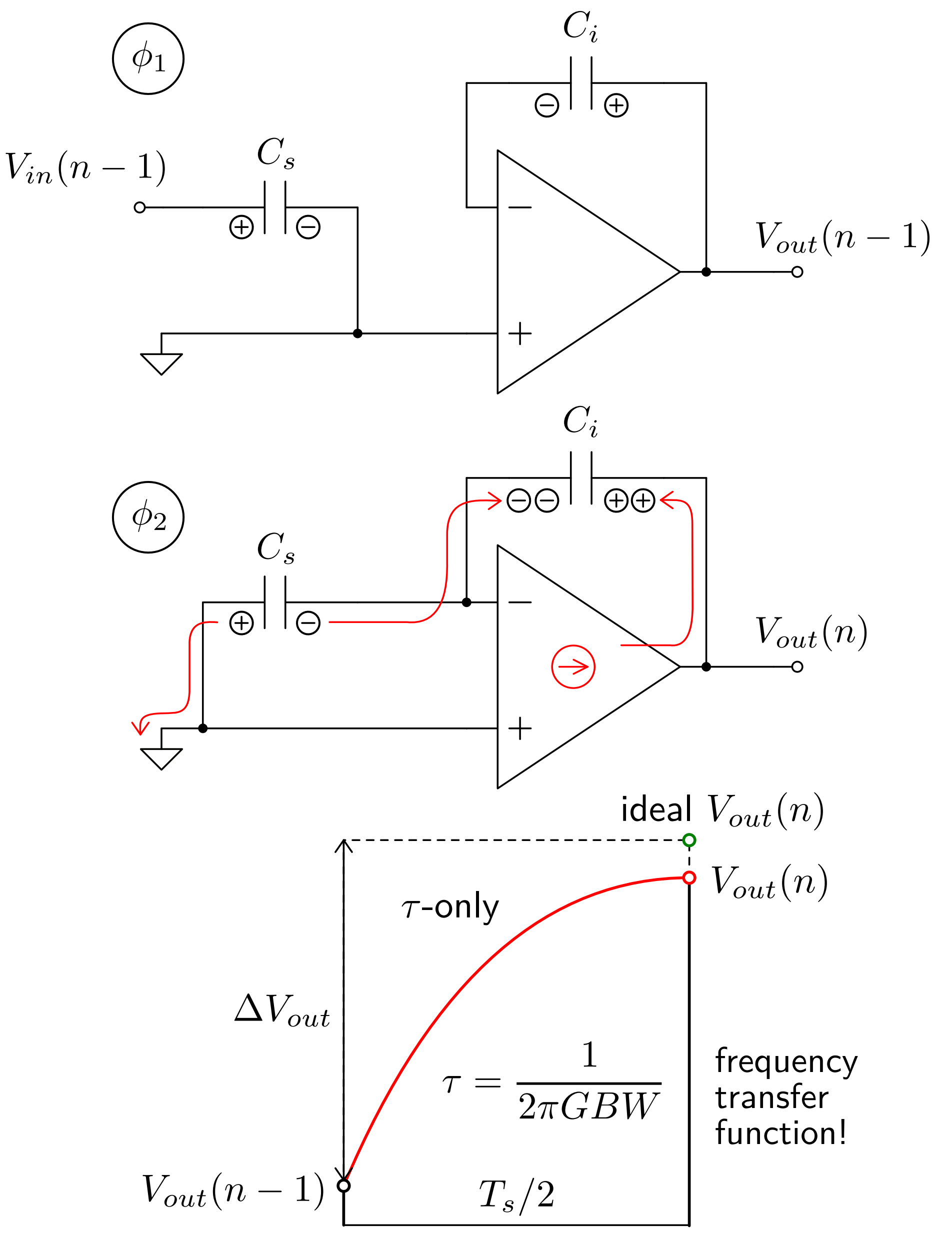
  - if $\left|\dfrac{\Delta V_{out}}{\tau}\right| < SR$ : **settling** only

    $$V_{out}(n) = V_{out}(n-1) + \Delta V_{out}\left(1 - e^{-\frac{T_s}{2\tau}}\right)$$



# OpAmp Slew-Rate and GBW

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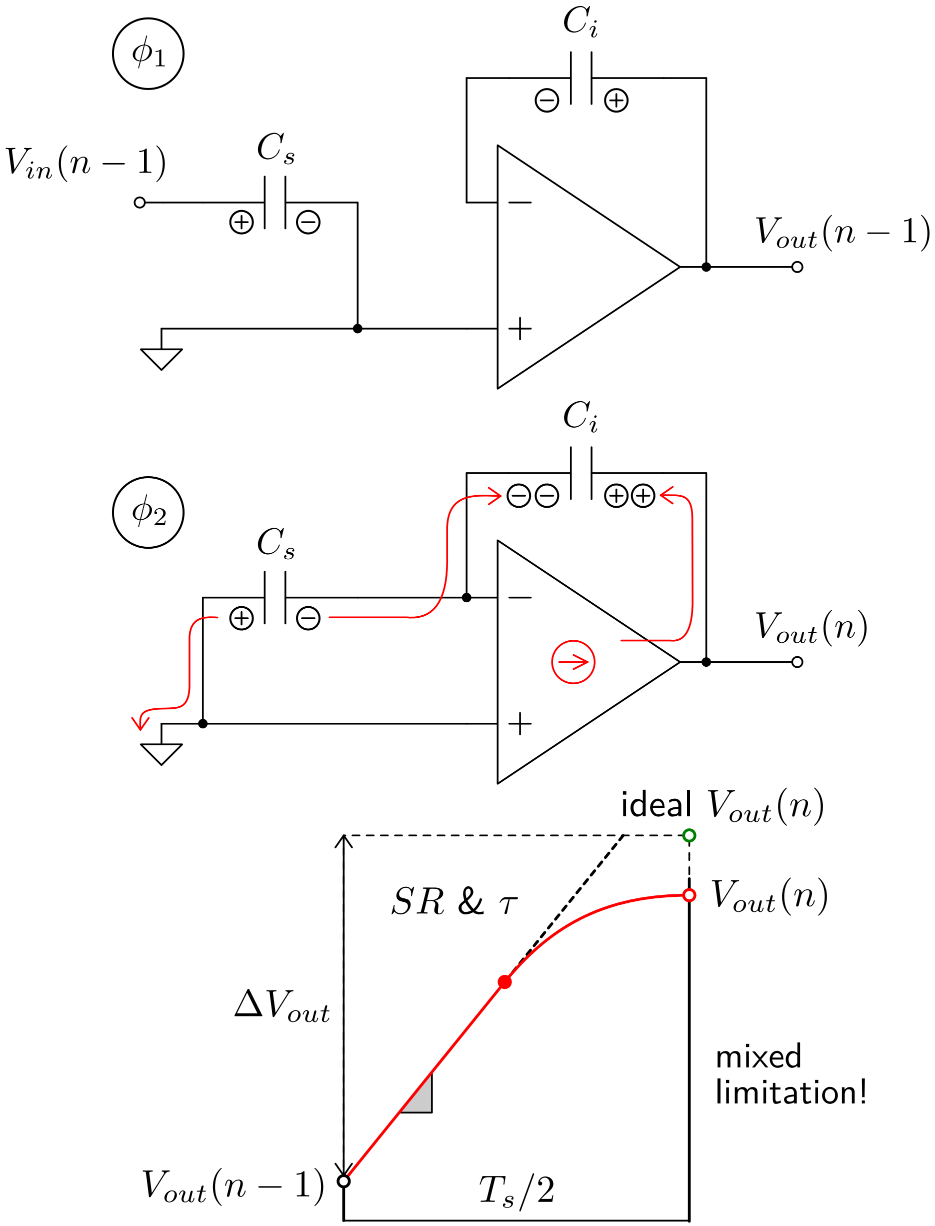
    $$V_{out}(n) = V_{out}(n-1) + \Delta V_{out}\left(1 - e^{-\frac{T_s}{2\tau}}\right)$$

  - else : **slewing+slettling**

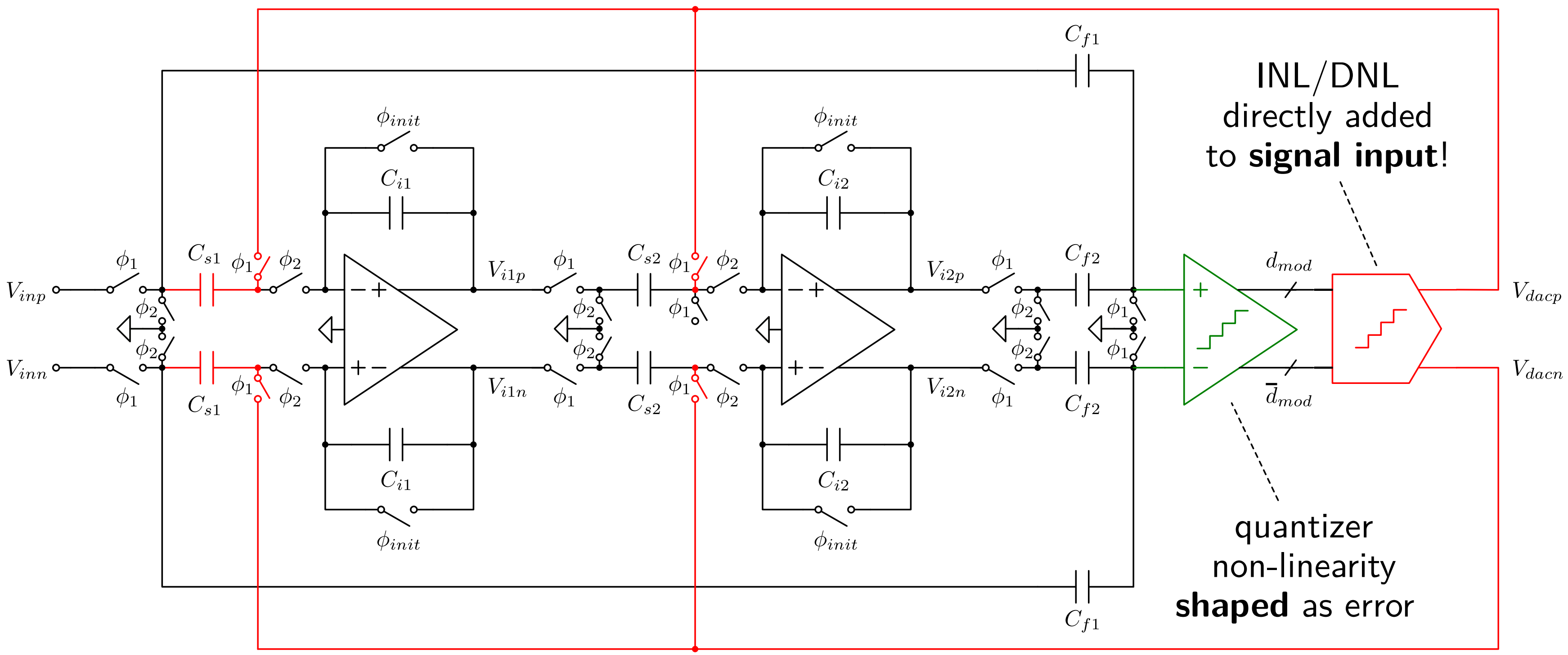
    $$V_{out}(n) = V_{out}(n-1) + \Delta V_{out} - SR\tau e^{-\left(\frac{T_s}{2\tau} - \frac{\Delta V_{out}}{\tau SR} + 1\right)}$$

- **Non-linear** errors = signal **distortion**



# Feedback DAC Non-Linearity

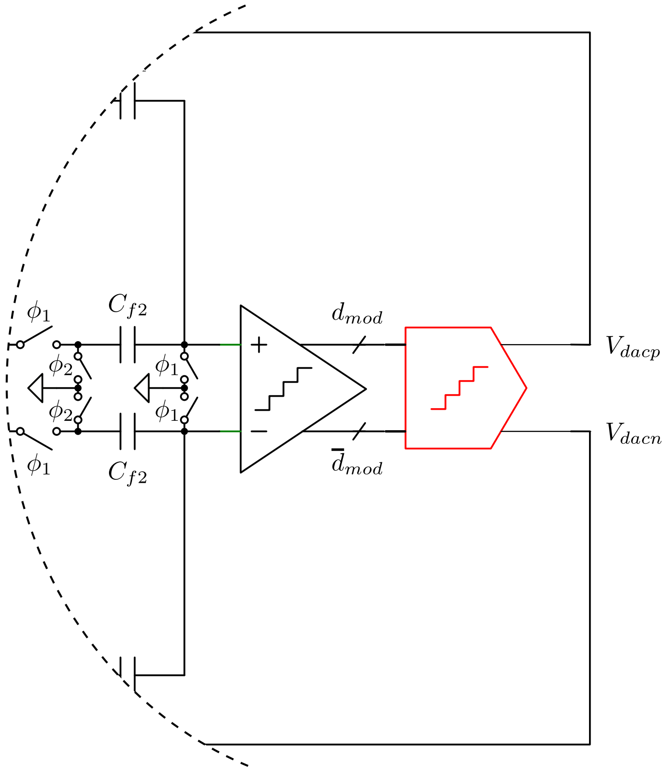
- Only for **multi-bit** DSM architectures:



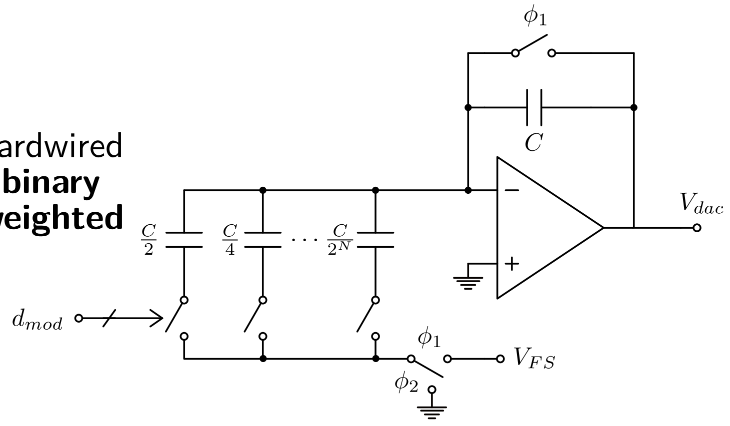

- How to get rid of feedback **flash DAC** non-linearity effects?

# Feedback DAC Mismatching

- Single-stage **multi-bit SC flash** architecture example:



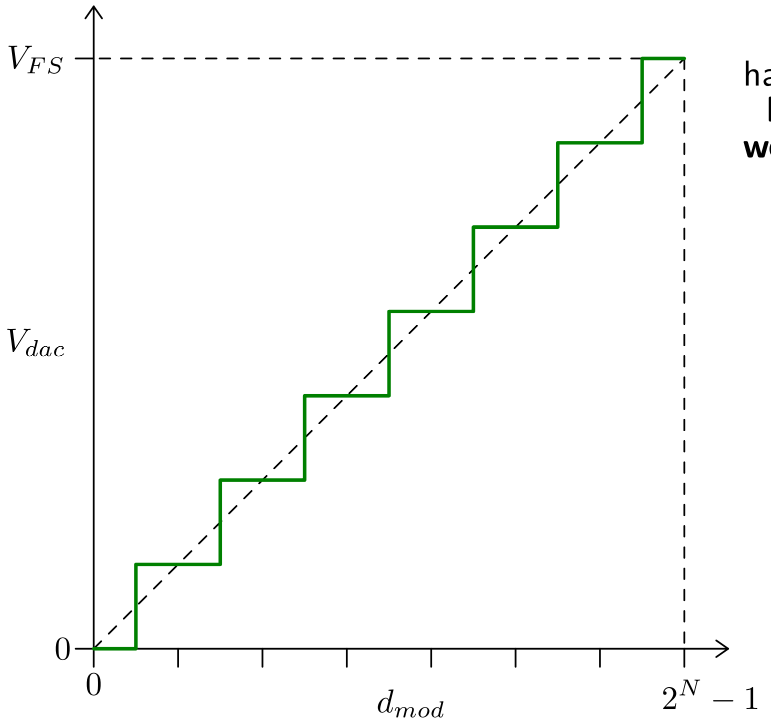

hardwired **binary weighted**

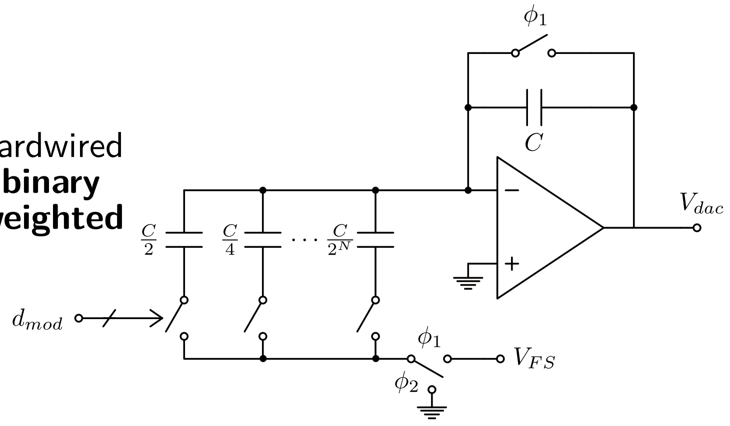



**single-ended** version

# Feedback DAC Mismatching

- Single-stage **multi-bit SC flash** architecture example:

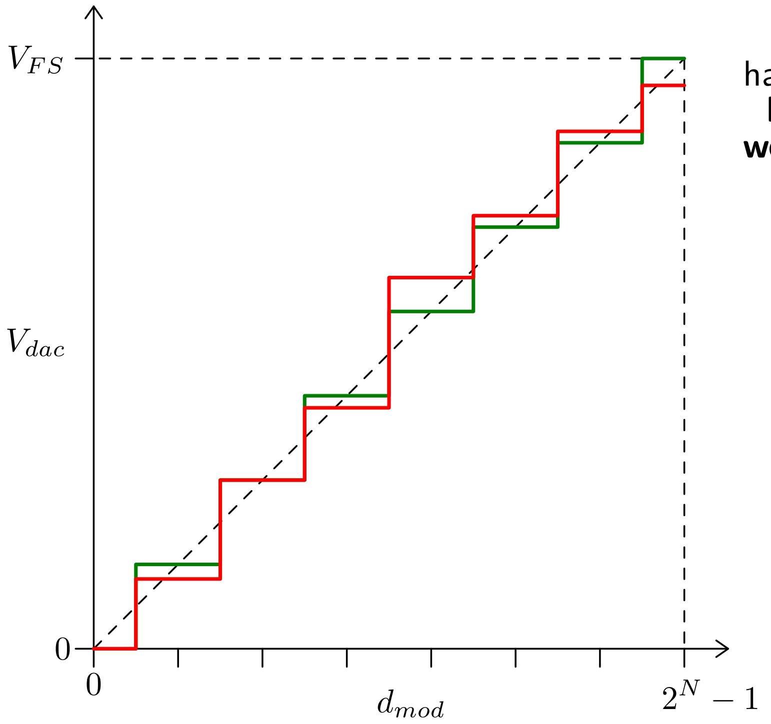


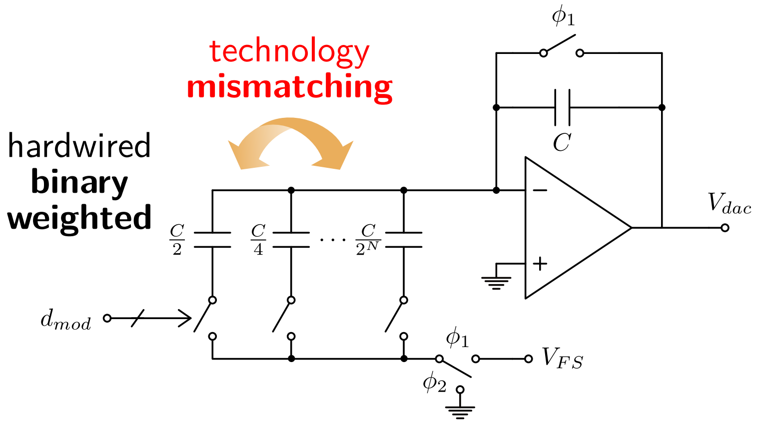



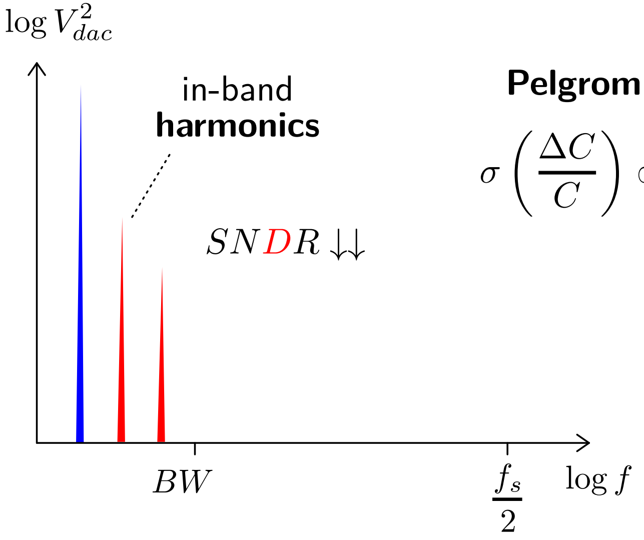

- **Simple** digital control

# Feedback DAC Mismatching

- Single-stage **multi-bit SC flash** architecture example:



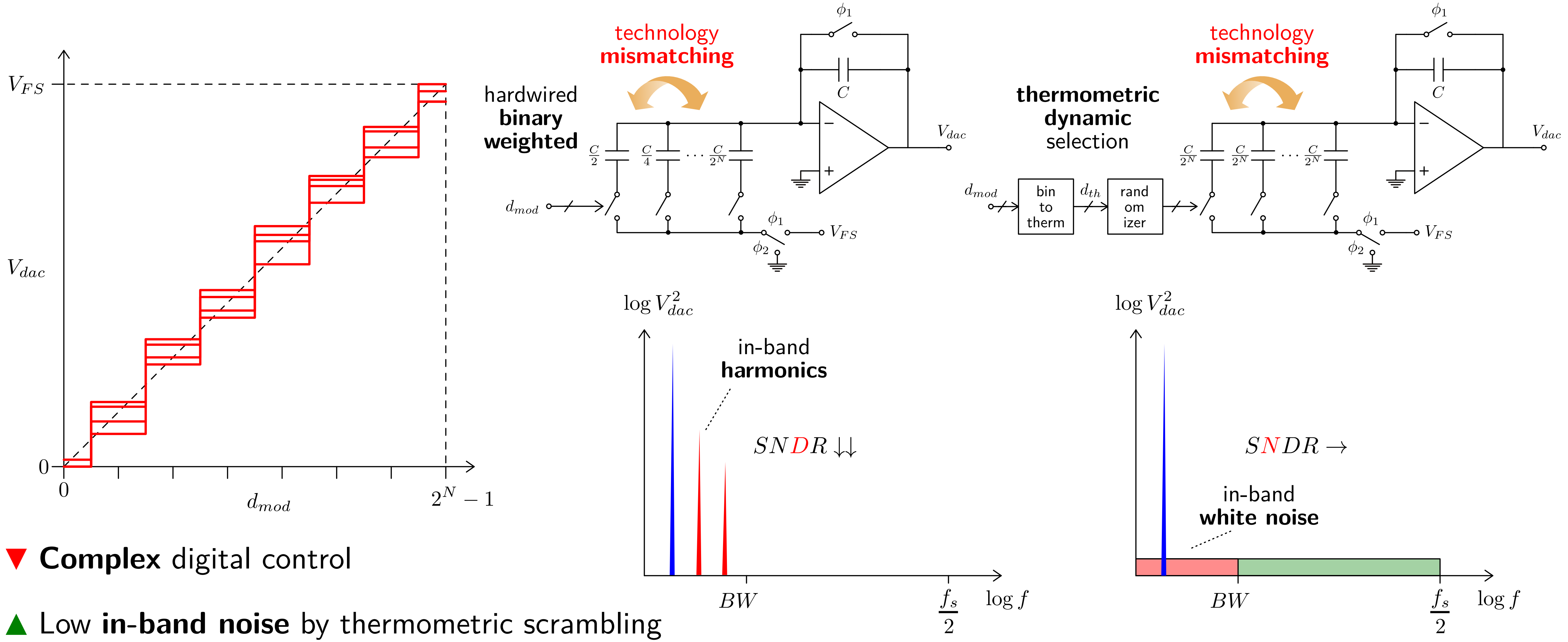

**Pelgrom's Law**

$$\sigma\left(\frac{\Delta C}{C}\right) \propto \frac{1}{\sqrt{WL}}$$

- ▲ **Simple** digital control
- ▼ **Distortion** caused by static mismatching

# Feedback DAC Mismatching

▶ Single-stage **multi-bit SC flash** architecture example:

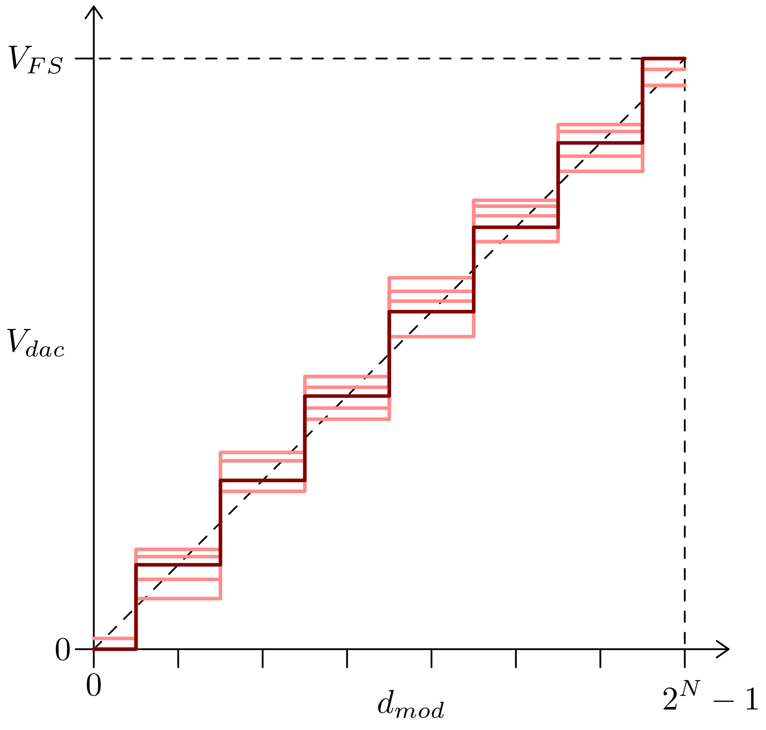


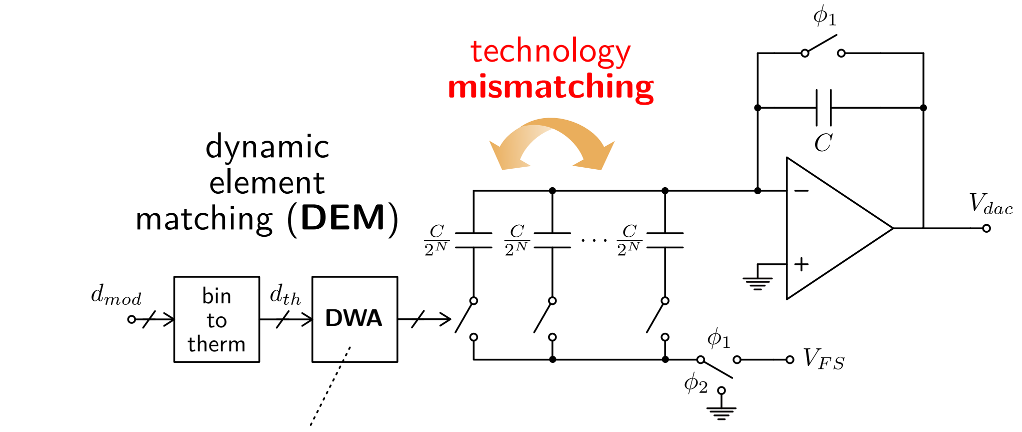

▼ **Complex** digital control

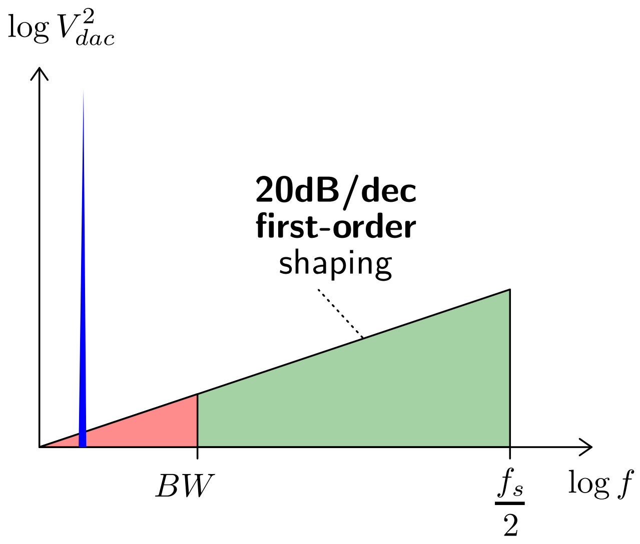
▲ Low **in-band noise** by thermometric scrambling

# Feedback DAC Mismatching

- Single-stage **multi-bit SC flash** architecture example:



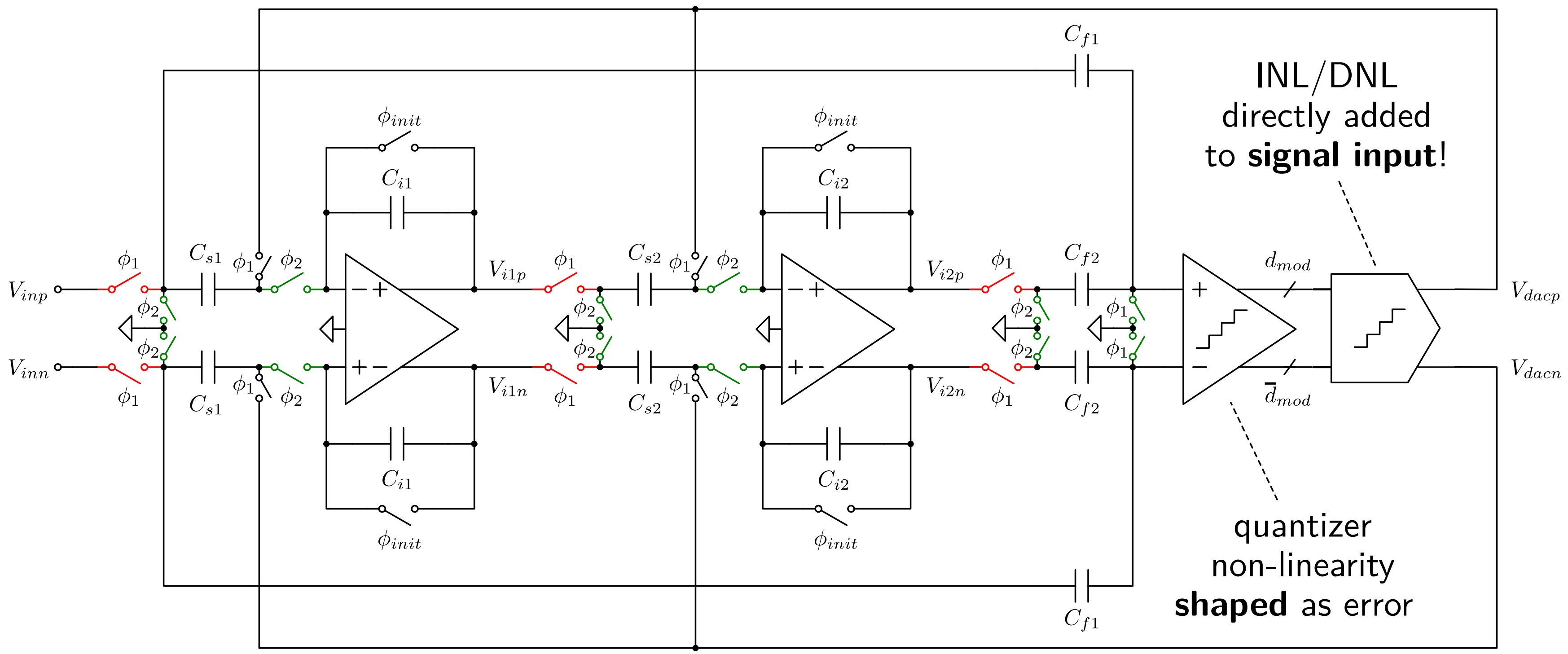




- **Complex** digital control
- **Mismatch shaping** by equalizing long-term element selection

# Switched OpAmp (SOA)

- **Distortion** caused by signal-dependent switch on-resistance:

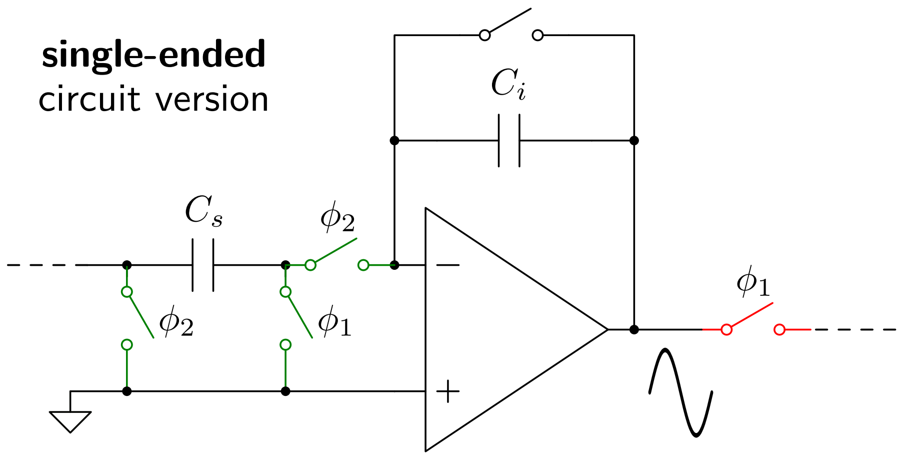



▼ How to make **on-resistance independent from signal** for these particular switches?

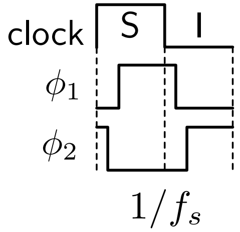
# Switched OpAmp (SOA)

- Moving output switches into **OpAmp** blocks:

**single-ended**
circuit version




$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$



# Switched OpAmp (SOA)

↗ J. Crols and M. Steyaert
*Switched-OpAmp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages*
IEEE Journal of Solid-State Circuits 29(8):936–942, Aug 1994
doi.org/10.1109/4.297698

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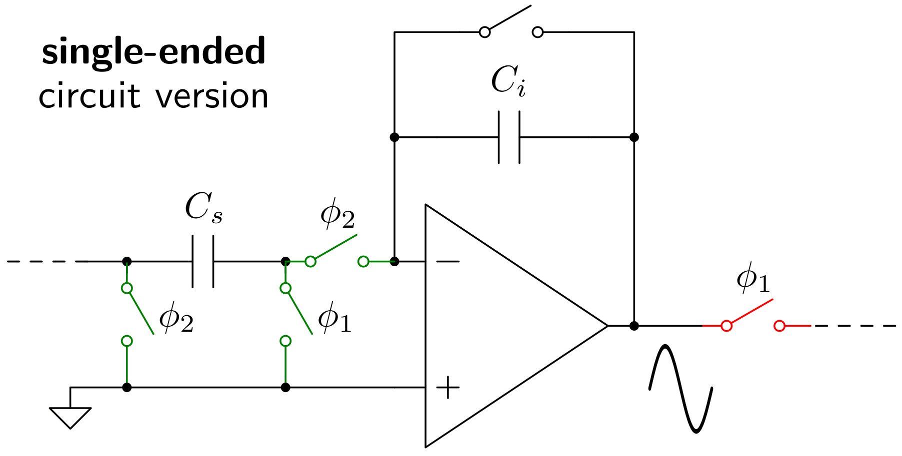


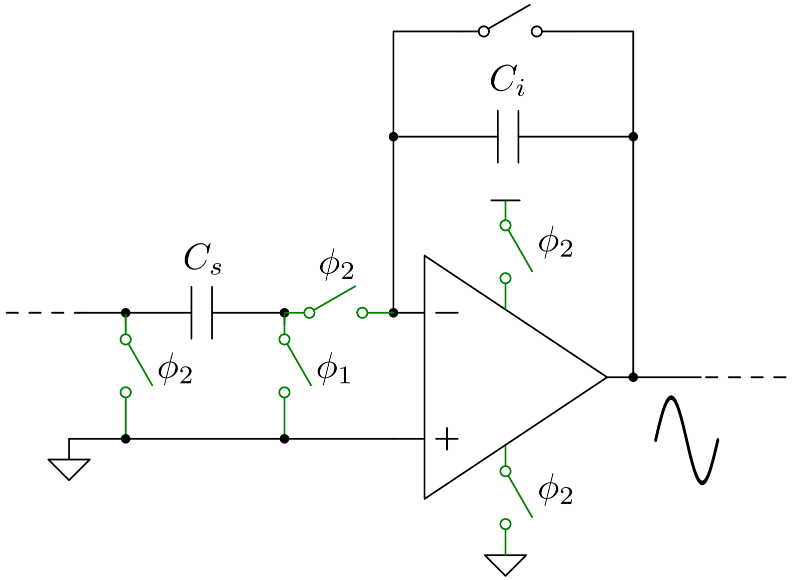


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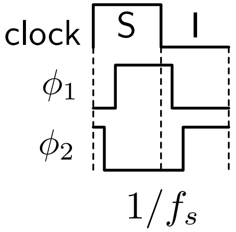


▲ **Constant** on-resistance for all switches

▲ Power savings due to 50% OpAmp **duty cycle**

▼ Each integrator stage operates in **alternative phases**

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J. Crols and M. Steyaert
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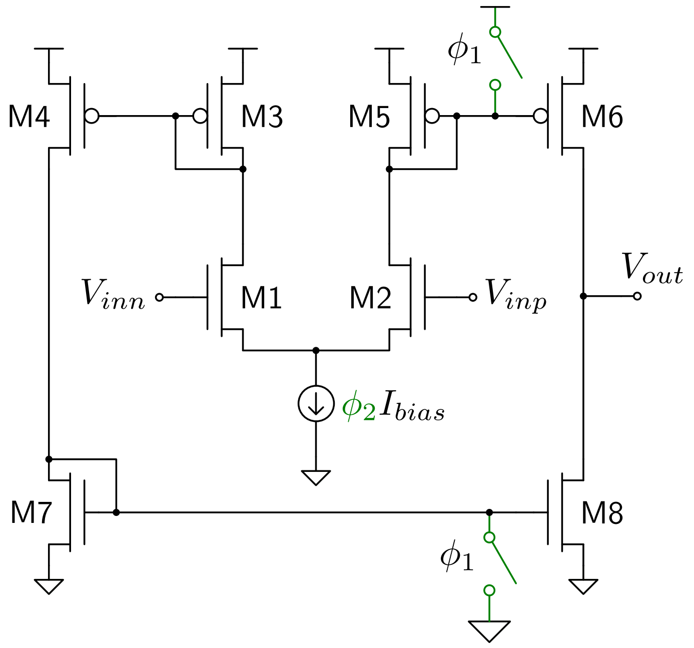
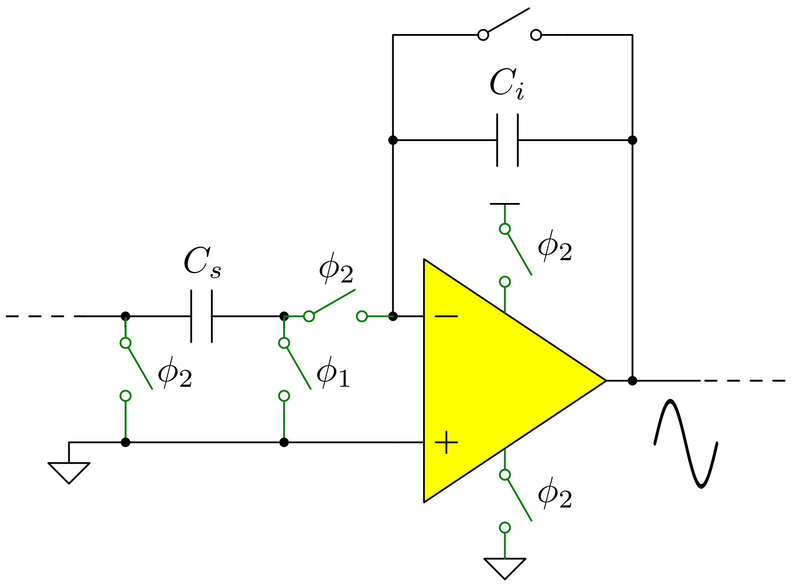



**Example:** single-ended single-stage folded OpAmp




- ▲ **Constant** on-resistance for all switches
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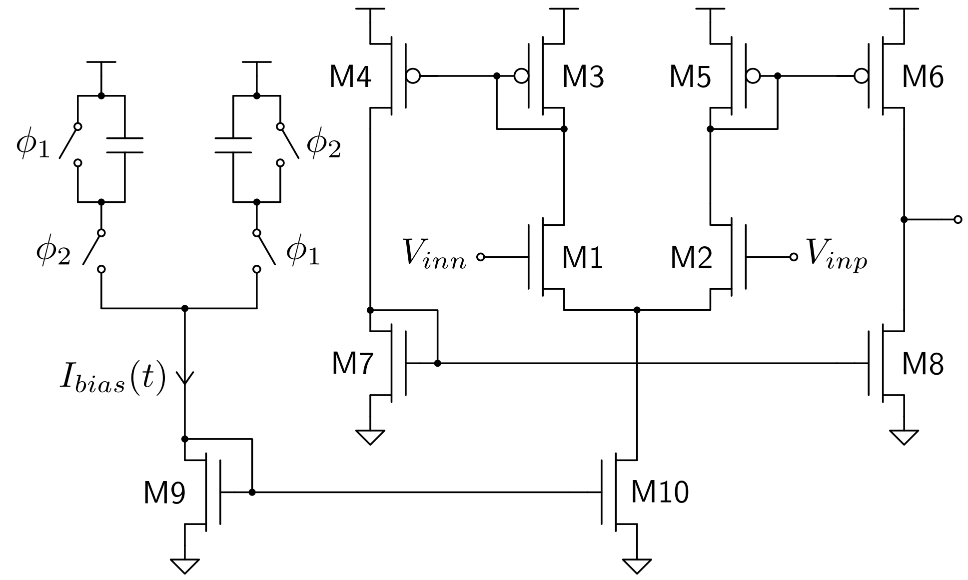
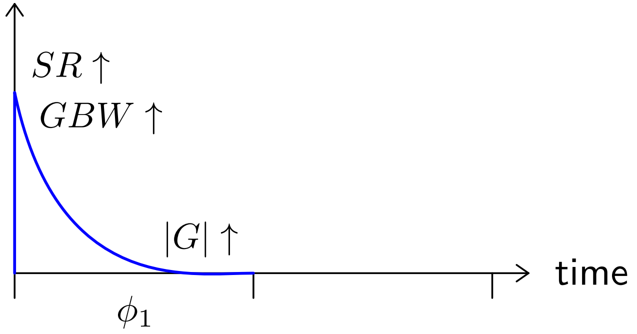
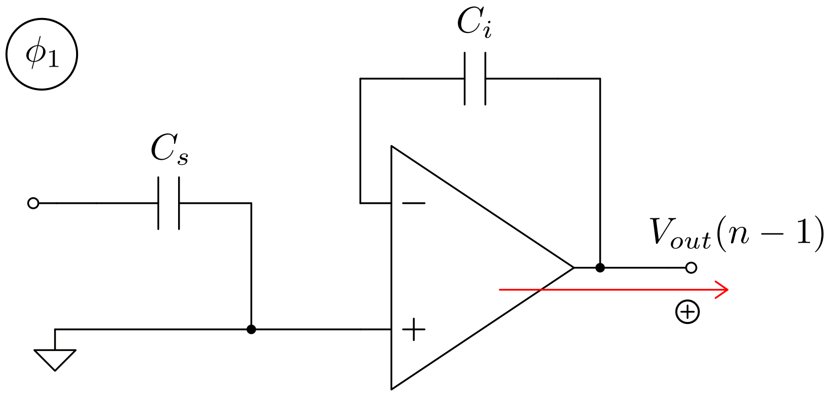
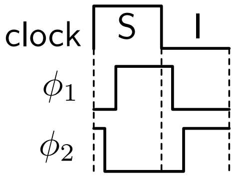
# OpAmp Dynamic Biasing

- Discrete time **dynamic biasing**:




$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$

B. J. Hosticka
*Dynamic CMOS amplifiers*
IEEE Journal of Solid-State Circuits 15(5):881–886, Oct 1980
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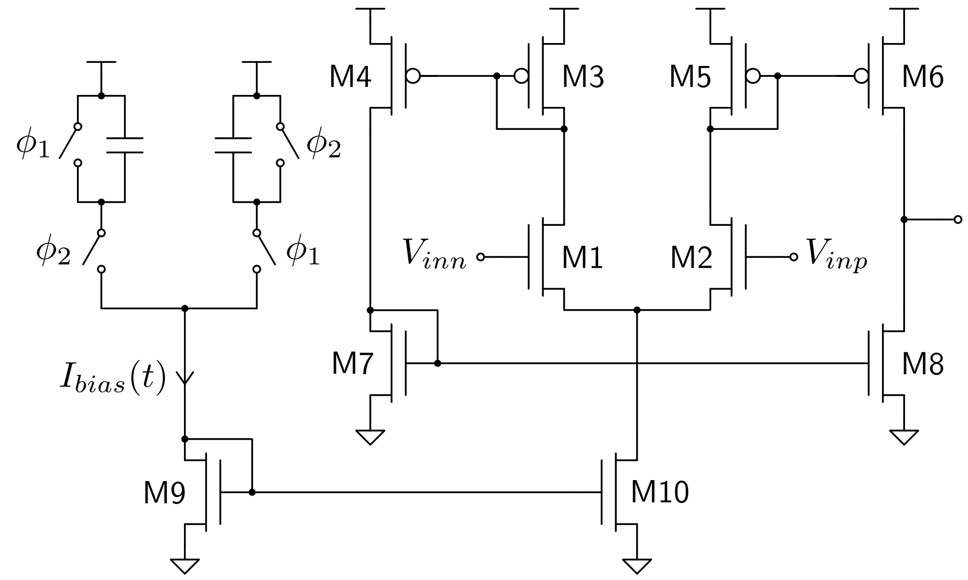


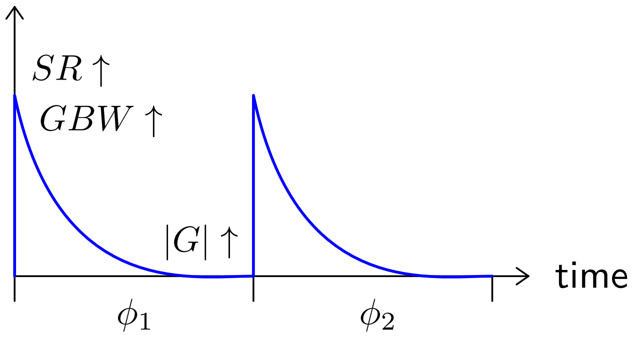


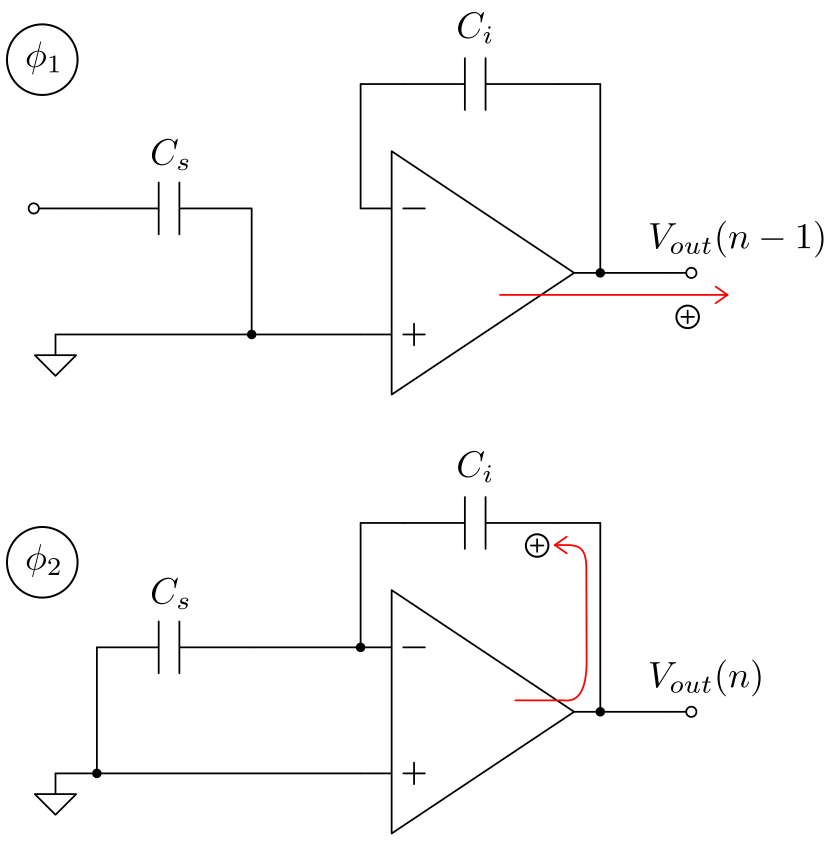


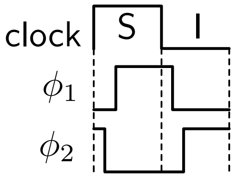


$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

- ▲ Synchronous **Class-AB** operation
- ▲ Static **power** savings
- ▼ OpAmp fast on/off **recovery** time required
- ▼ Biasing **peak** value is technology dependent
- ▼ **Ripple** induced in the power rails (digital-like)

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