5. CMOS Operational Amplifiers

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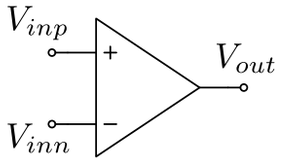
Universal Analog Building Block

- Operational voltage amplifier (**OpAmp**)



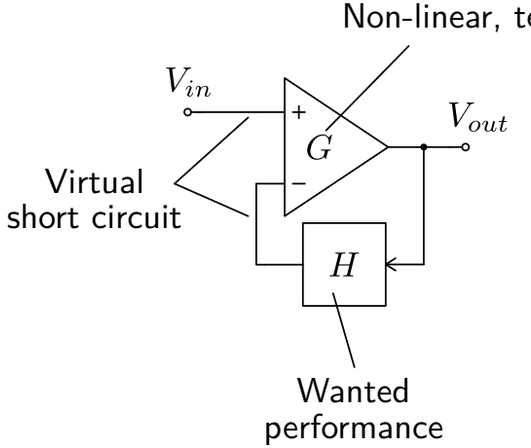
$$\begin{cases} V_{din} = V_{inp} - V_{inn} \\ V_{cm} = \dfrac{V_{inp} + V_{inn}}{2} \end{cases}$$

Single ended case study

$$V_{out} = GV_{din} + \cancel{G_{cm}V_{cm}}^{0}$$

with $G \to \infty$

- Analog computing **operations** in closed loop:



$$\frac{V_{out}}{V_{in}} = \frac{G}{1+GH} \simeq \frac{1}{H}$$

As far as OpAmp **gain** and **bandwidth** are large enough

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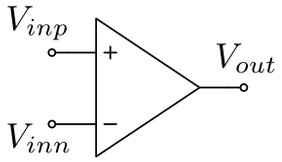

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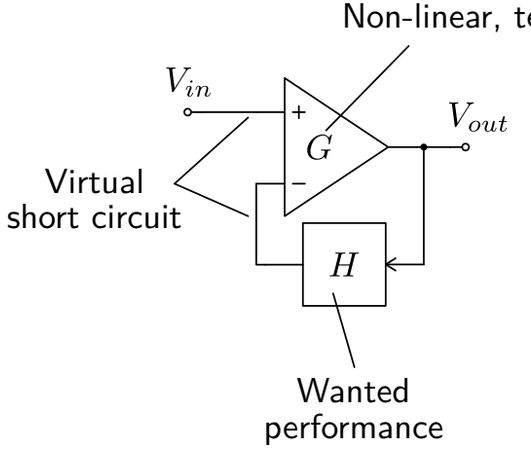
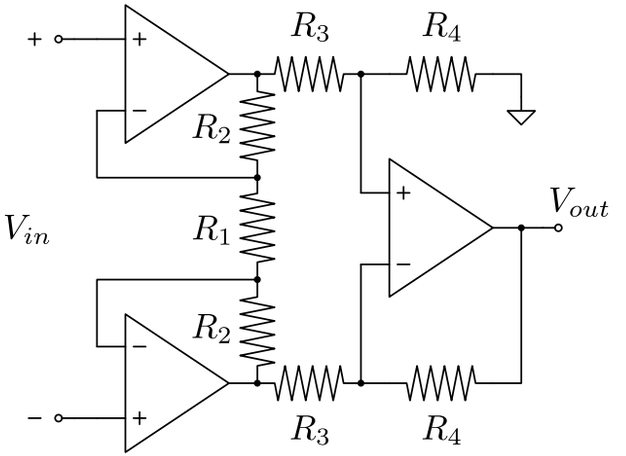


$$\frac{V_{out}}{V_{in}} = \frac{G}{1+GH} \simeq \frac{1}{H}$$

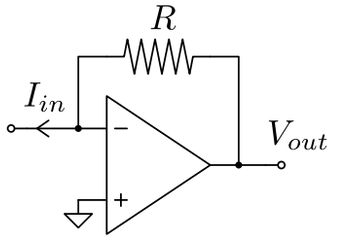
As far as OpAmp **gain** and **bandwidth** are large enough

e.g. Instrumentation amplifier



$$\frac{V_{out}}{V_{in}} = \left(1 + \frac{2R_2}{R_1}\right)\frac{R_4}{R_3}$$

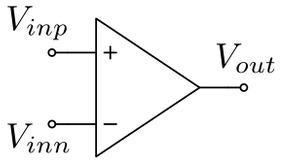
e.g. I/V converter



$$\frac{V_{out}}{I_{in}} = R$$

Universal Analog Building Block

- Operational voltage amplifier (**OpAmp**)



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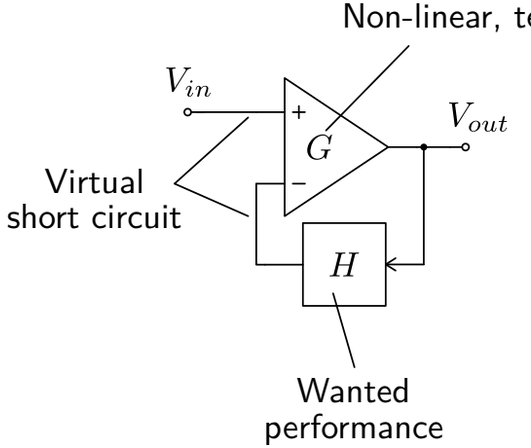
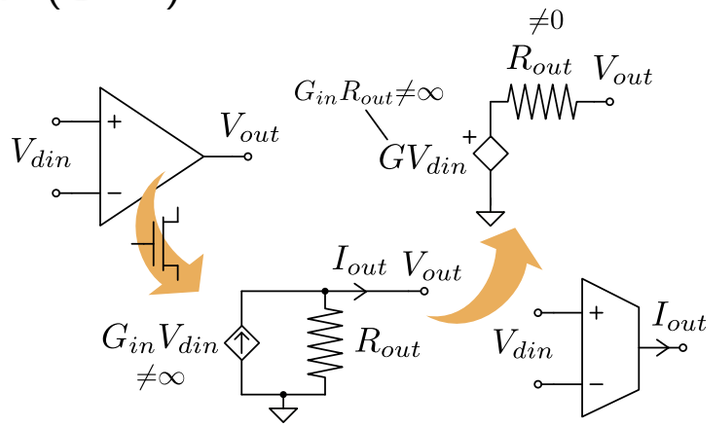


$$\frac{V_{out}}{V_{in}} = \frac{G}{1+GH} \simeq \frac{1}{H}$$

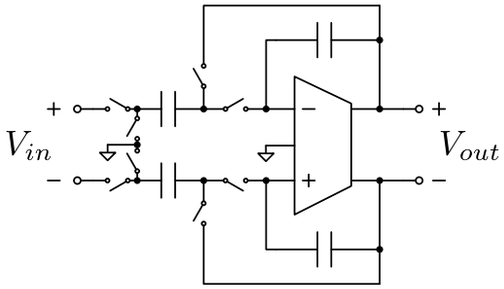
As far as OpAmp **gain** and **bandwidth** are large enough

- **CMOS** OpAmp known as operational transconductance amplifier (**OTA**)



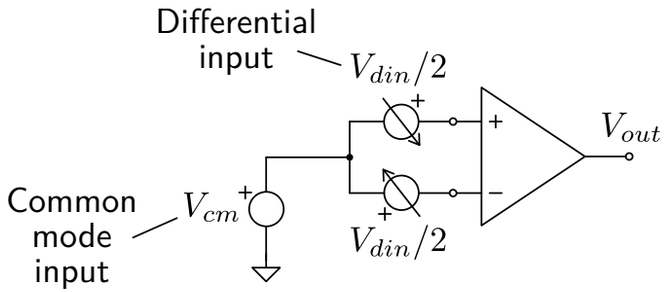
OpAmp or OTA naming depends on the load conditions...

e.g. switched capacitor (SC) filters

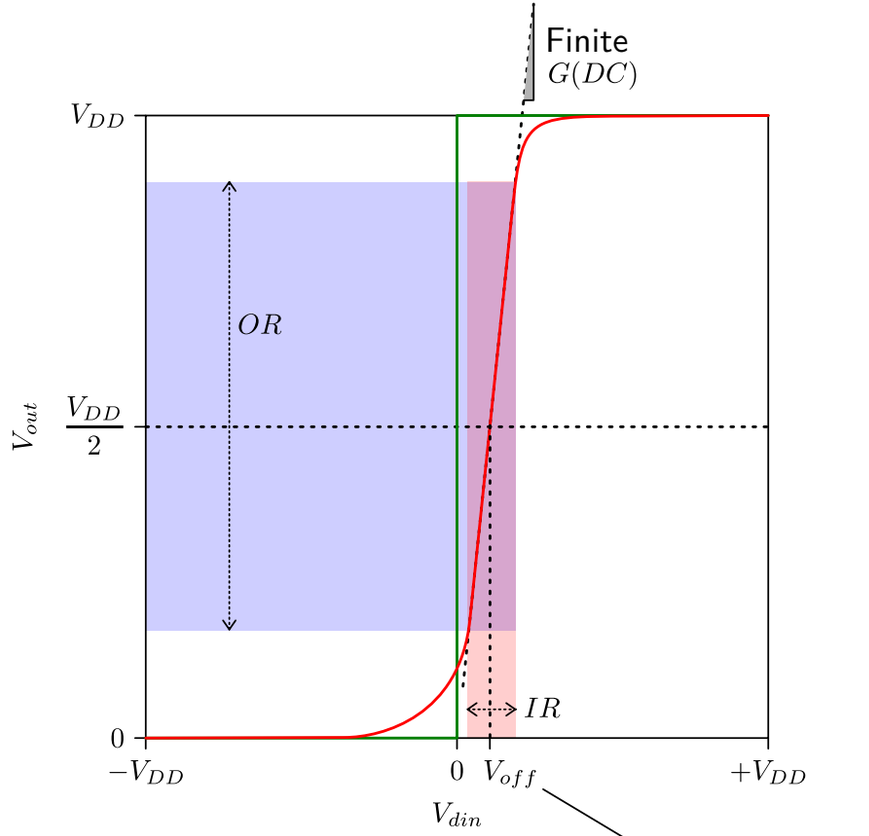


OpAmp Performance Parameters

- **Large signal static** figures (ideal):
  - Input range IR $(\rightarrow 0)$
  - Output range OR $(\rightarrow V_{DD})$
  - Equivalent input offset V_{off} $(\rightarrow 0)$
  - Open loop differential DC gain $G(DC)$ $(\rightarrow \infty)$



- Open-loop differential DC voltage transfer curve (**VTC**) at constant common mode:



$V_{DD} \equiv$ supply voltage

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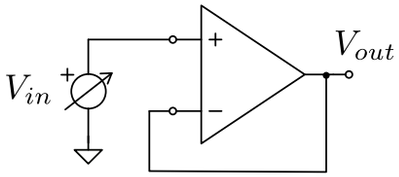
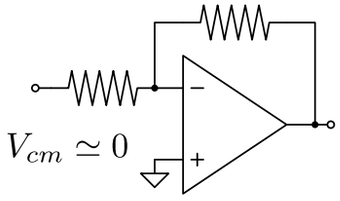
  - Common mode range $CMR_{l,h}$ $(\rightarrow 0, V_{DD})$



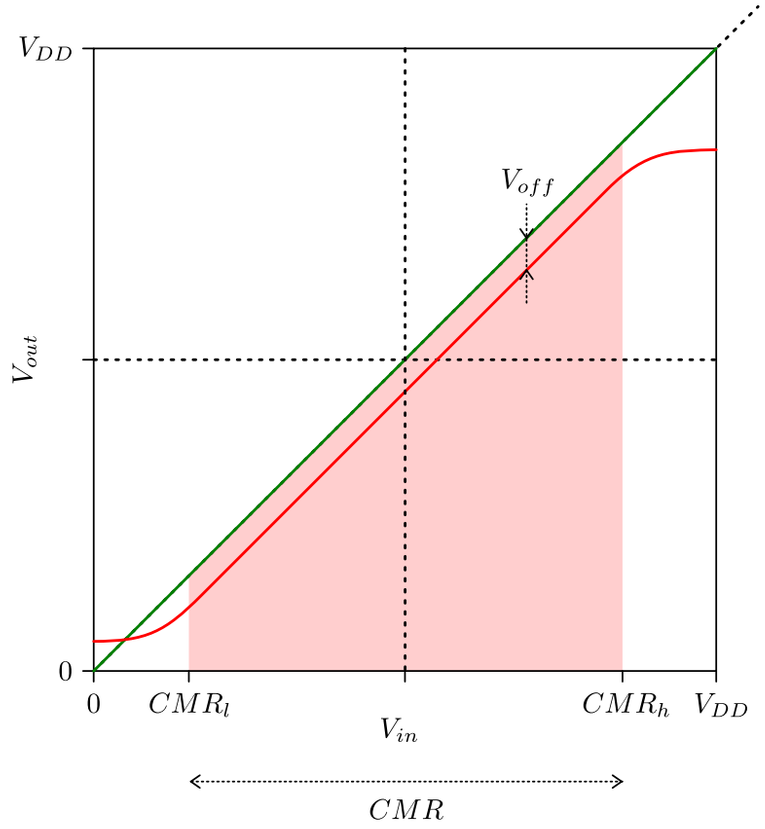
$$V_{out} = \frac{G}{1+G} V_{in}$$

$$\begin{cases} V_{din} = V_{inp} - V_{inn} \\ V_{cm} = \dfrac{V_{inp} + V_{inn}}{2} \end{cases} \qquad V_{cm} = \frac{1}{2}\frac{1+2G}{1+G} V_{in} \simeq V_{in}$$

Depending on feedback topology!

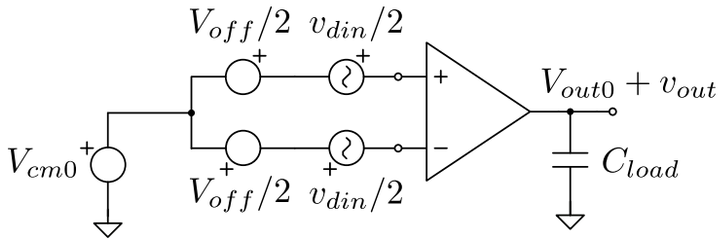


- **Input common-mode** DC sweep:

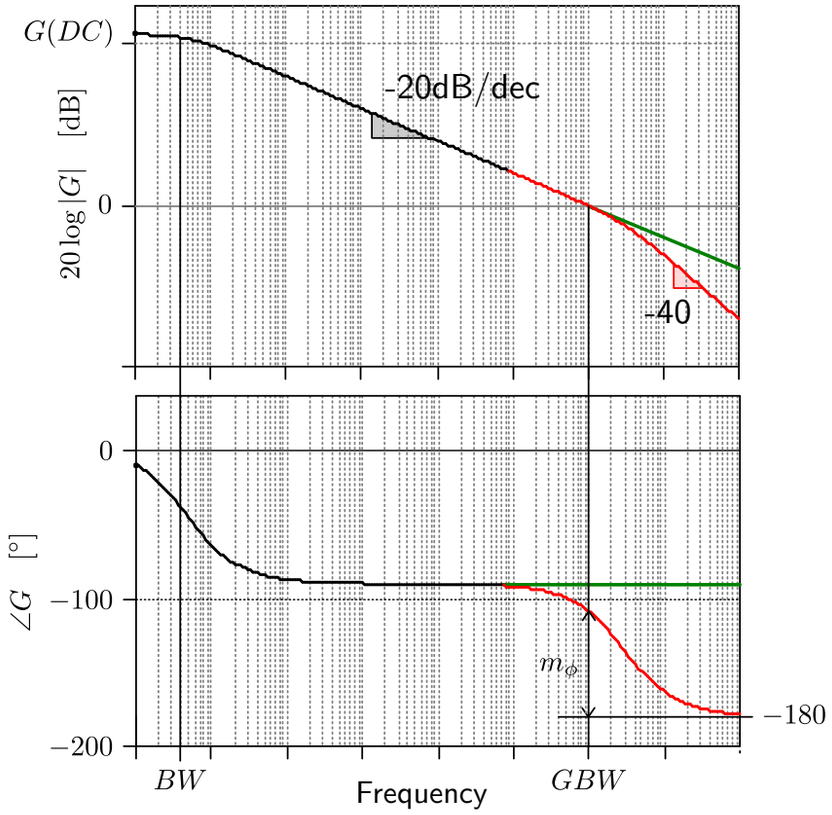


OpAmp Performance Parameters

- **Small signal dynamic** figures (ideal):
  - Open loop differential DC gain $G(DC)$ $(\rightarrow \infty)$
  - Bandwidth BW $(\rightarrow \infty)$
  - Gain-bandwidth product GBW $(\rightarrow \infty)$
  - Phase margin m_ϕ $(\rightarrow 90^\circ)$
  - Equivalent input noise v_{neq} $(\rightarrow 0)$



- **AC Bode** diagram:



OpAmp Performance Parameters

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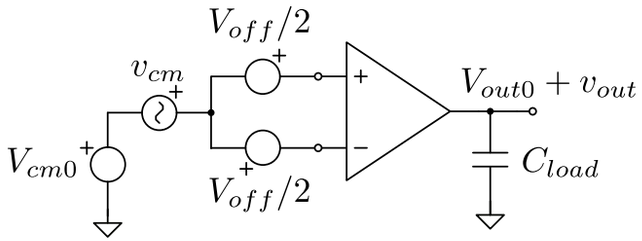
  - Equivalent input noise v_{neq} $(\to 0)$
  - Common mode rejection ratio $CMRR$ $(\to \infty)$



$$CMRR \doteq \frac{G}{G_{cm}}$$

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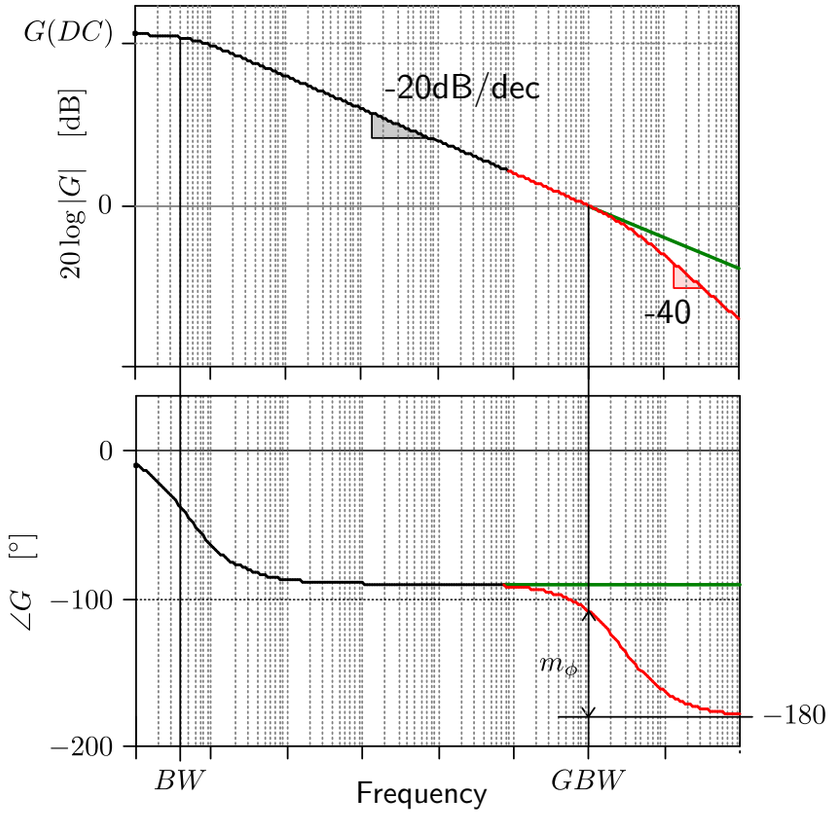

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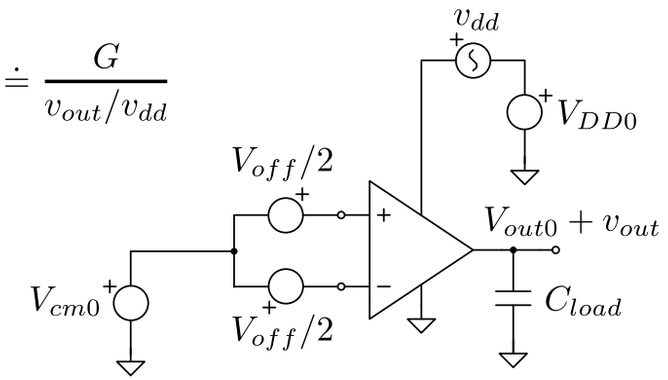
  - Gain-bandwidth product GBW $(\rightarrow \infty)$
  - Phase margin m_ϕ $(\rightarrow 90^\circ)$
  - Equivalent input noise v_{neq} $(\rightarrow 0)$
  - Common mode rejection ratio $CMRR$ $(\rightarrow \infty)$
  - Power supply rejection ratio $PSRR_{+/-}(\rightarrow \infty)$

$$PSRR_+ \doteq \frac{G}{v_{out}/v_{dd}}$$



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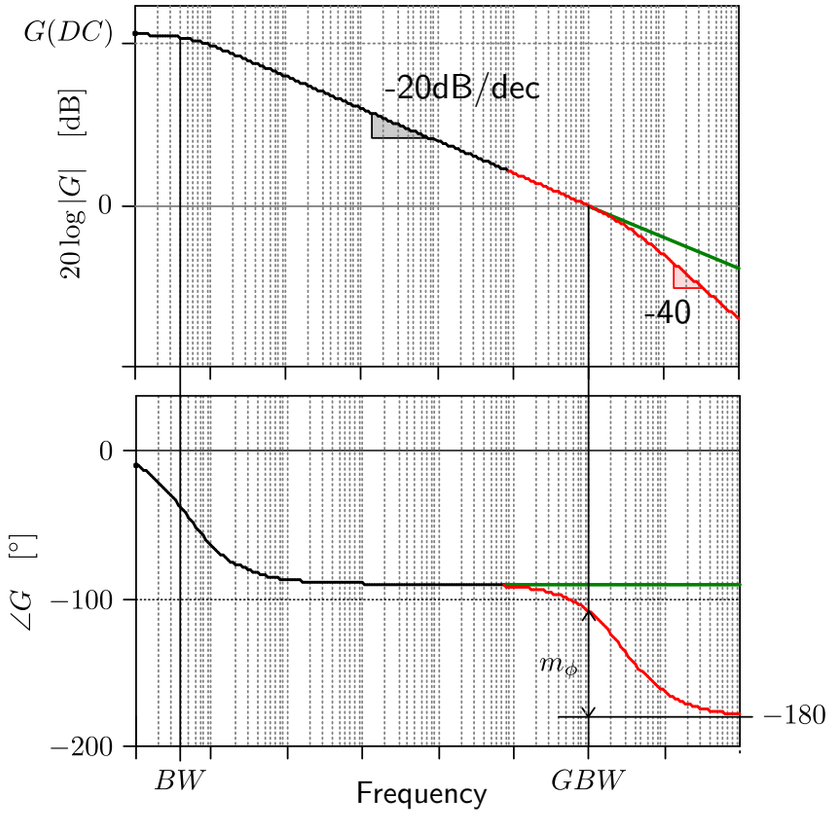

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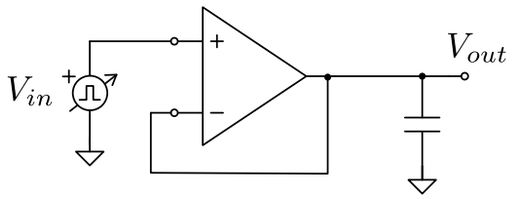
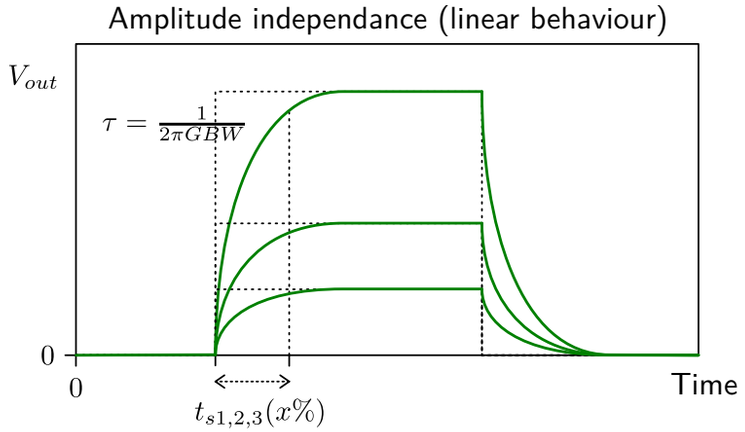
- **Large signal dynamic** figures (ideal)
  - Settling time $t_s(x\%) \quad (\rightarrow 0)$

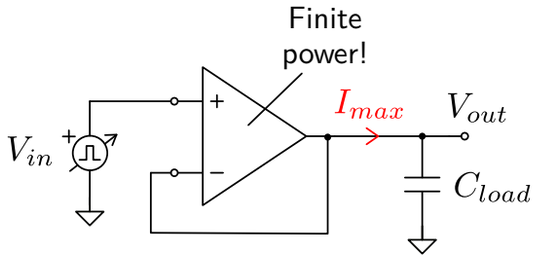


- Transient **step response**:



OpAmp Performance Parameters

- **Large signal dynamic** figures (ideal)
  - Settling time $t_s(x\%)$ $(\rightarrow 0)$
  - Slew rate $SR_{+/-}$ $(\rightarrow \infty)$



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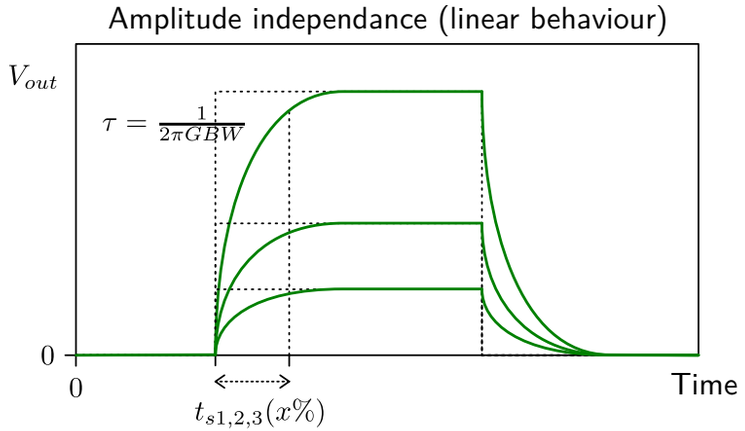
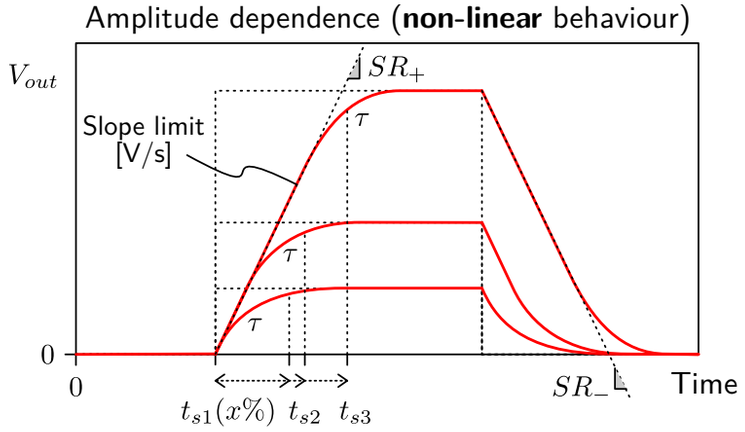
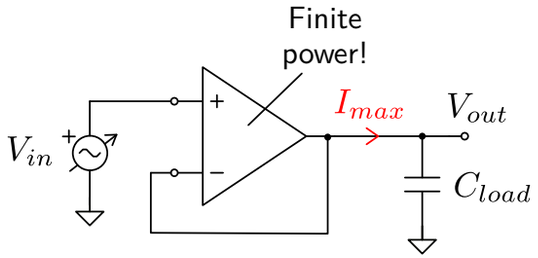




OpAmp Performance Parameters

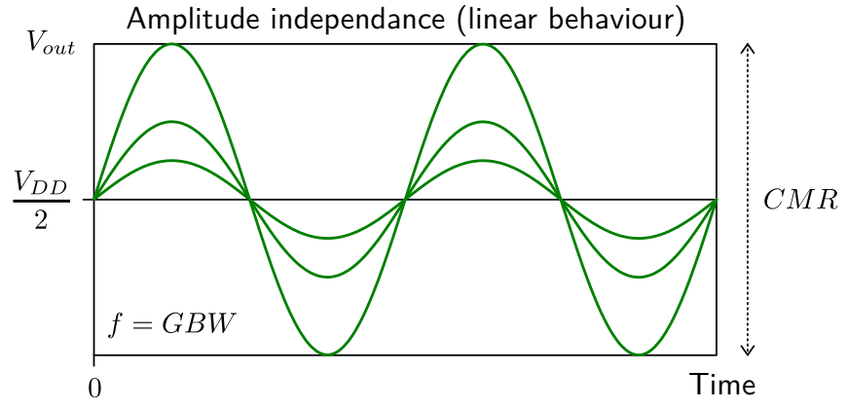
- **Large signal dynamic** figures (ideal)
  - Settling time $t_s(x\%)$ $(\rightarrow 0)$
  - Slew rate $SR_{+/-}$ $(\rightarrow \infty)$
  - Maximum frequency f_{max} $(\rightarrow \infty)$

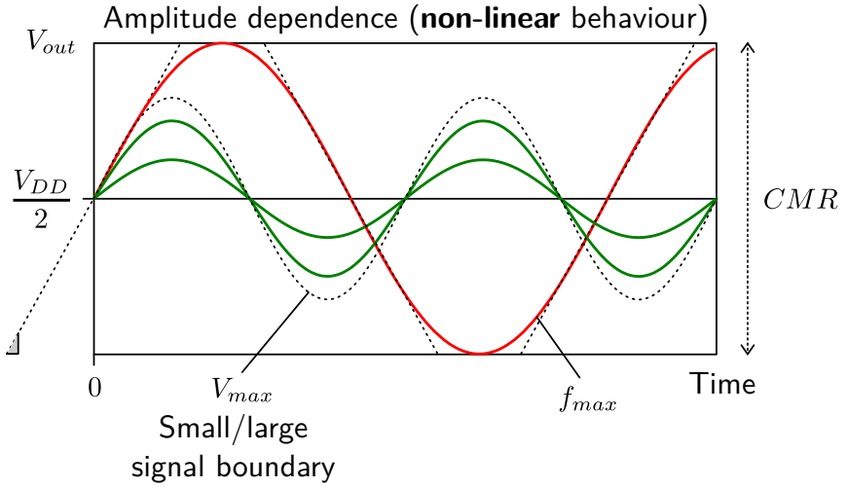


$$f_{max} = \frac{SR}{\pi CMR} \ll GBW$$

$$V_{max} = \frac{SR}{2\pi GBW} \ll CMR \qquad SR \doteq \min(SR_+, SR_-)$$

- Transient **harmonic response**:





OpAmp Performance Parameters

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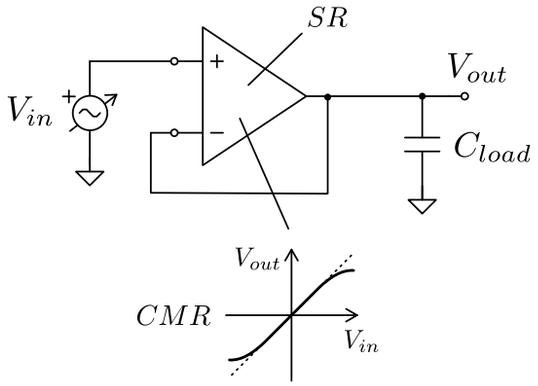
  - Settling time $t_s(x\%)$ $(\rightarrow 0)$
  - Slew rate $SR_{+/-}$ $(\rightarrow \infty)$
  - Maximum frequency f_{max} $(\rightarrow \infty)$
  - Total harmonic distortion THD $(\rightarrow 0)$



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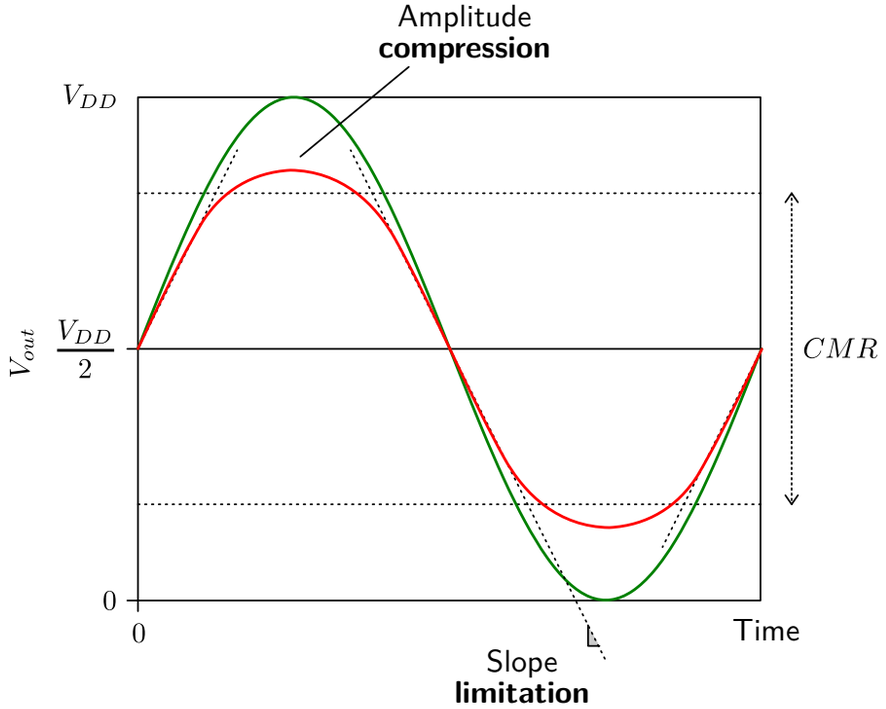
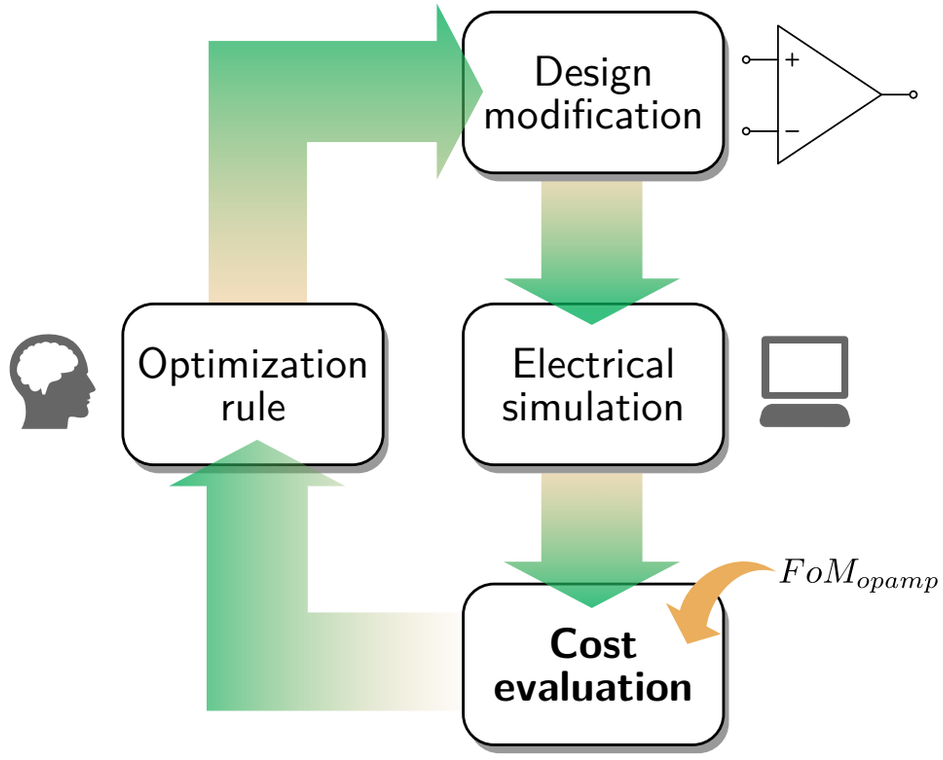


- Both static and dynamic non-linearity = **signal distortion**

OpAmp FoMs

- **Quantitative** design comparison
- Useful in circuit **optimization**:



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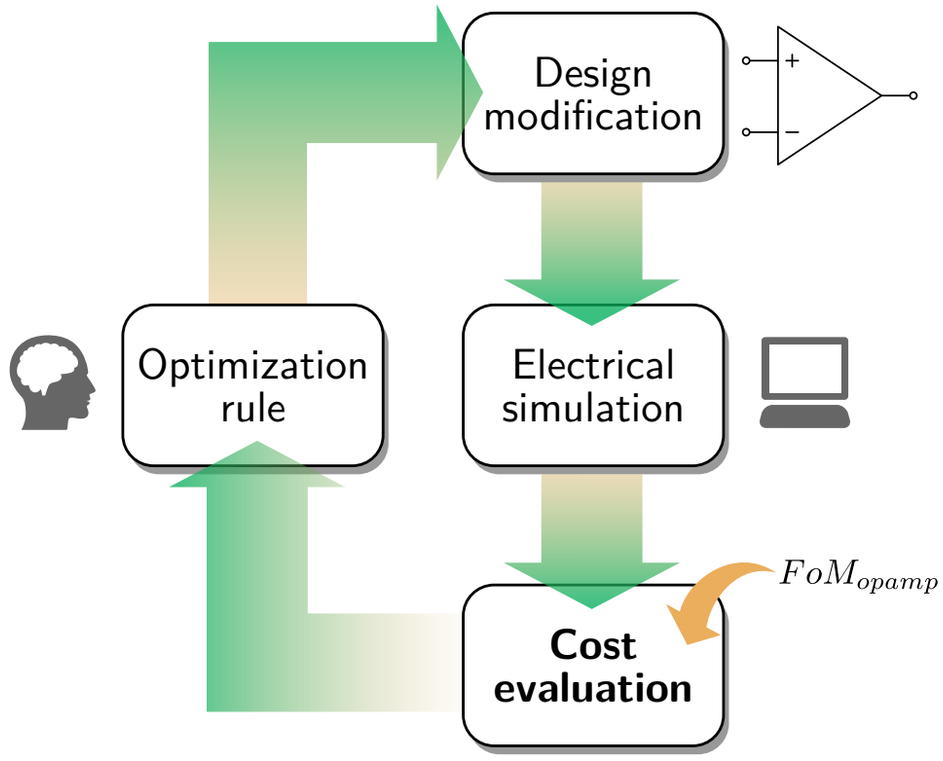
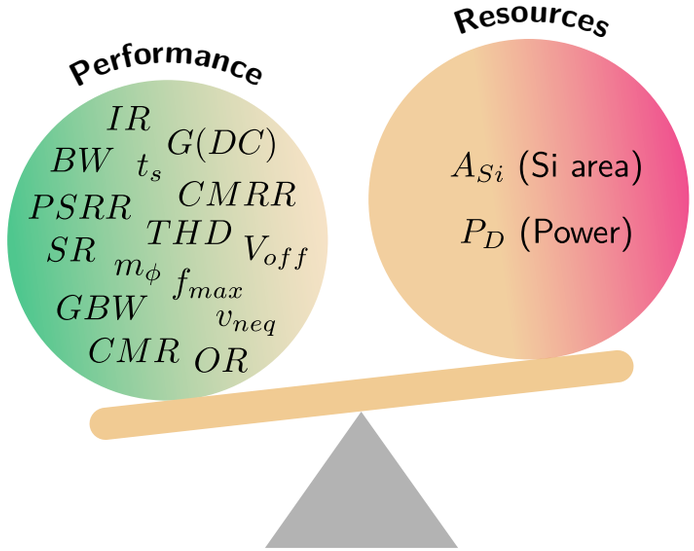


- ▼ **Too many** performance parameters!



- ▼ Application **specific** FoMs...

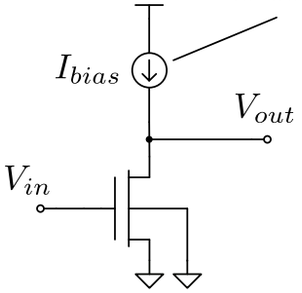
$$FoM_{opamp} \equiv \begin{cases} \dfrac{C_{load} SR}{P_D} & \text{e.g. line buffer} \\ \dfrac{1}{P_D v_{neq}^2 A_{Si}} & \text{e.g. pre-amplifier} \\ \dfrac{C_{load} GBW}{P_D} & \text{e.g. RF amplifier} \end{cases}$$

Single-Transistor Topologies

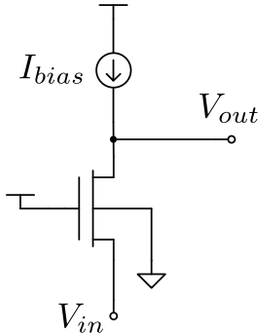
- Operational voltage amplifier (**OpAmp**)?

Supposing **forward saturation**, **drain** is selected as output port due to its **high impedance** (**CLM**):

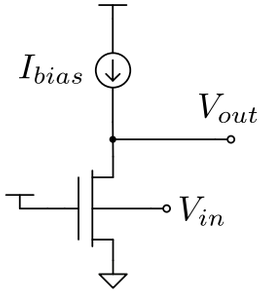
Current-driven bias point to control circuit **power**



Common source



Common gate



Back gate

Single-Transistor Topologies

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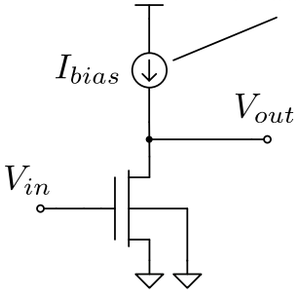


Common source

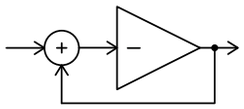
Power efficiency

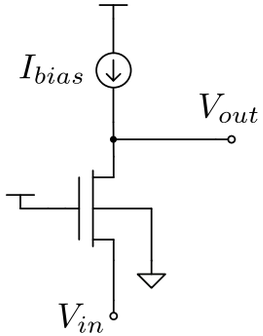
$\Delta V_{SB} \equiv n\Delta V_{GB}$

$1 < n < 2$

- Moderate $\mathbf{G_m/I_D}$
- ▲ High input **impedance**
- ▲ **Inverting** amplifier

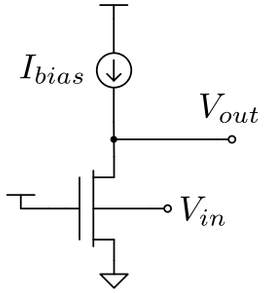
Easier feedback





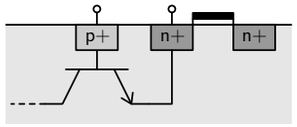
Common gate

- ▲ Highest $\mathbf{G_m/I_D}$
- ▼ Low input **impedance**
- ▼ **Non-inverting** amplifier



Back gate

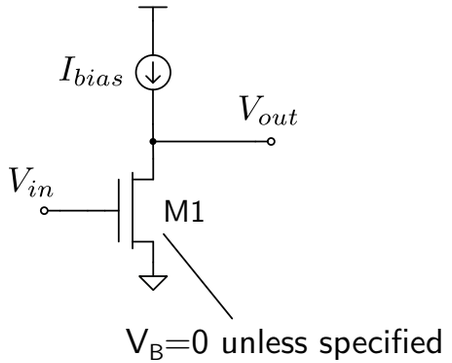
- ▼ Lowest G_m/I_D
- ▼ Low input **impedance**
- ▲ **Inverting** amplifier
- ▼ **Latchup**
- ▼ **Triple**-well required



Voltage Transfer Curve

- **Large signal** analysis of common source amplifier:

M1 operating in **strong inversion** and **forward saturation**:



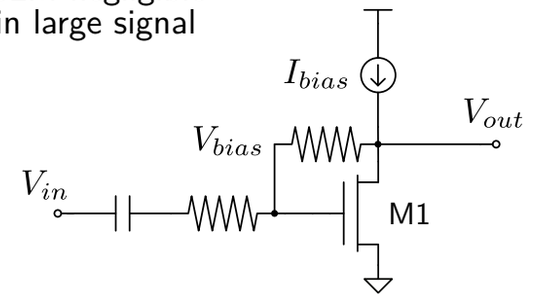
$$I_D = \frac{\beta}{2n}\left(V_{GB} - V_{TH}\right)^2 \left[1 + \lambda\left(V_{DB} - V_{sat}\right)\right]$$

$\left(\frac{W}{L}\right)$

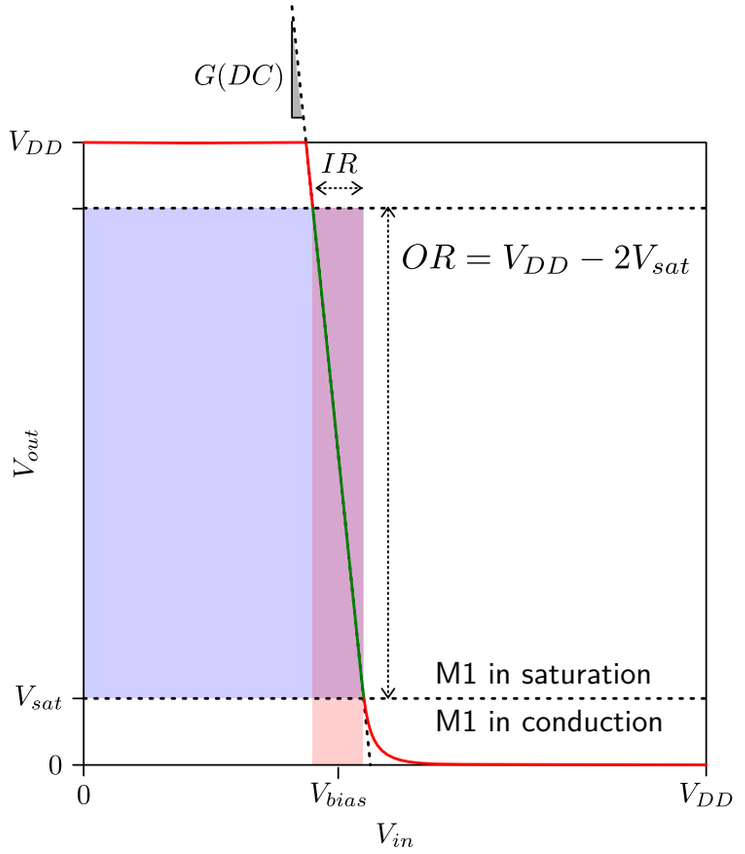
CLM negligible in large signal

$$I_{bias} \equiv \frac{\beta}{2n}\left(V_{bias} - V_{TH}\right)^2$$

$$V_{bias} = \sqrt{\frac{2nI_{bias}}{\beta}} + V_{TH}$$



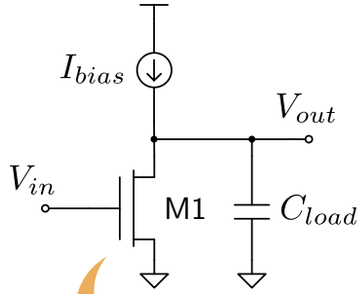
e.g. autobiasing



$$V_{sat} = \frac{V_{GB} - V_{TH}}{n} = \frac{V_{bias} - V_{TH}}{n} = \sqrt{\frac{2I_{bias}}{n\beta}}$$

Gain and Frequency Response

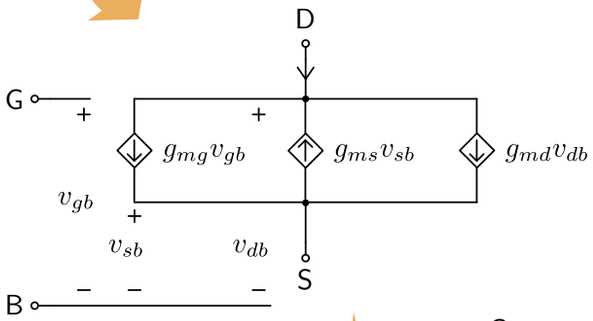
- Common source **small signal** analysis:

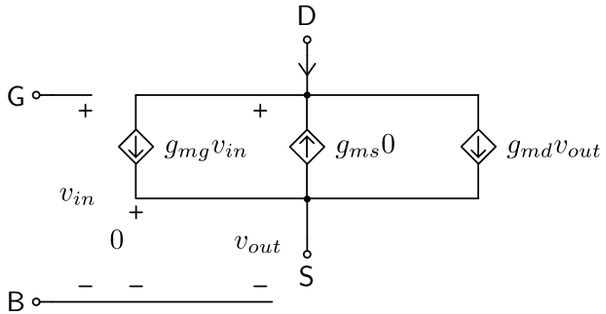


$$V_{GB} = V_{bias} + v_{in}$$

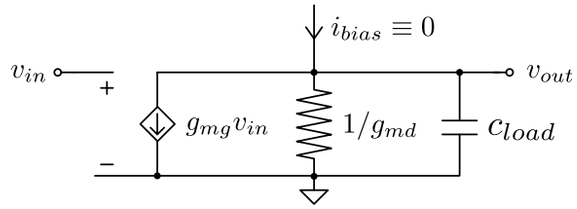
$$V_{DB} = \frac{V_{DD}}{2} + v_{out}$$

$$V_{SB} \equiv 0$$





- **Incremental** equivalent circuit:



M1 **strong inversion** and forward **saturation** bias point

$$I_{bias} \gg I_S = 2n\beta U_t^2$$

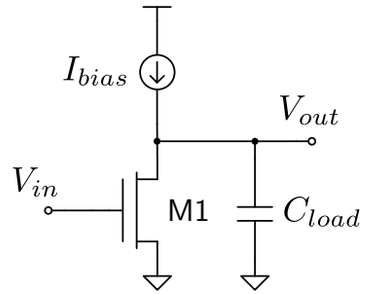
$$V_{bias} \gg V_{TH}$$

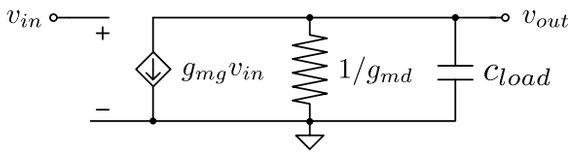
$$V_{out} \gg V_{sat}$$

$$\begin{cases} g_{mg} = \sqrt{\dfrac{2\beta I_D}{n}} \equiv \sqrt{\dfrac{2\beta I_{bias}}{n}} \\ g_{md} = \lambda I_D \equiv \lambda I_{bias} \end{cases}$$

Gain and Frequency Response

- **Incremental** equivalent circuit:





M1 **strong inversion** and forward **saturation** bias point

$$\begin{cases} g_{mg} = \sqrt{\dfrac{2\beta I_D}{n}} \equiv \sqrt{\dfrac{2\beta I_{bias}}{n}} \\ g_{md} = \lambda I_D \equiv \lambda I_{bias} \end{cases}$$

$\left(\frac{W}{L}\right)$; $I_D \propto \frac{1}{L}$

- DC voltage **gain**

$$G \doteq \frac{v_{out}}{v_{in}}$$

$$G(DC) = -\frac{g_{mg}}{g_{md}}$$

$$G(DC) = -\frac{1}{\lambda}\sqrt{\frac{2\beta}{nI_{bias}}}\uparrow$$

$\left(\frac{W}{L}\right)\uparrow$ 3dB/oct

6dB/oct $L\uparrow$

$I_{bias}\downarrow$ 3dB/oct

In general, for **CMOS** amplifiers:

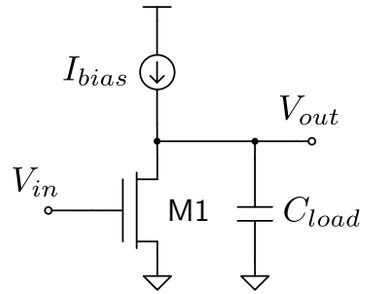
$$|G(DC)| = g_{in}r_{out}$$

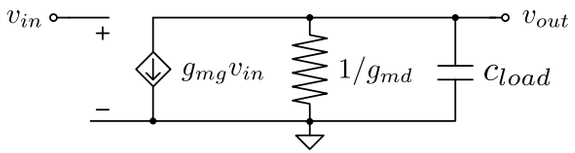
input **transconductance** $v \rightarrow i$

output **resistance** $i \rightarrow v$

Gain and Frequency Response

- **Incremental** equivalent circuit:





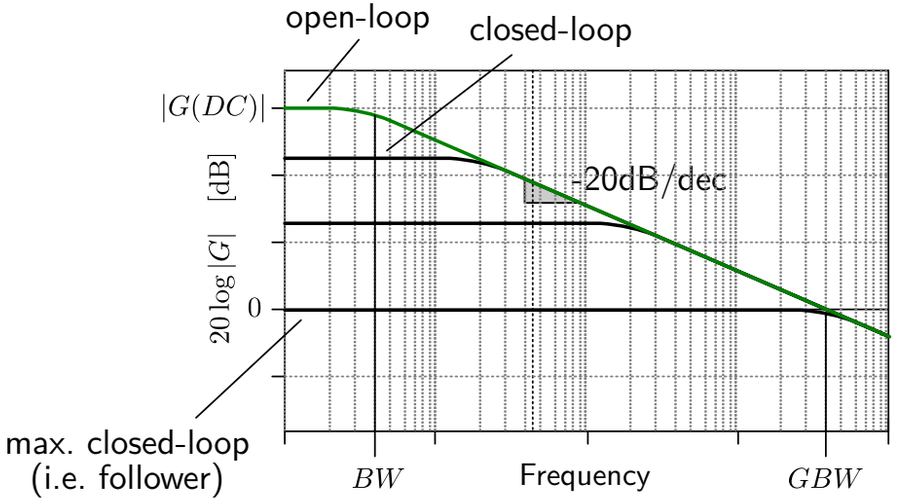
M1 **strong inversion** and forward **saturation** bias point

$$\begin{cases} g_{mg} = \sqrt{\frac{2\beta I_D}{n}} \equiv \sqrt{\frac{2\beta I_{bias}}{n}} \\ g_{md} = \lambda I_D \equiv \lambda I_{bias} \end{cases}$$

($\frac{W}{L}$) ; $\propto \frac{1}{L}$

- Spectral **bandwidth**

$$G(DC) = -\frac{g_{mg}}{g_{md}}$$



$$BW = \frac{g_{md}}{2\pi c_{load}}$$

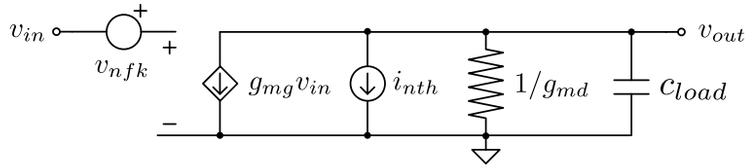
$$GBW = \frac{g_{mg}}{2\pi c_{load}} = \frac{1}{2\pi c_{load}}\sqrt{\frac{2\beta I_{bias}}{n}} \uparrow$$

$I_{bias} \uparrow$ 0.5oct/oct

$(\frac{W}{L}) \uparrow$ 0.5oct/oct

Dynamic Range

- **Noise** equivalent circuit:



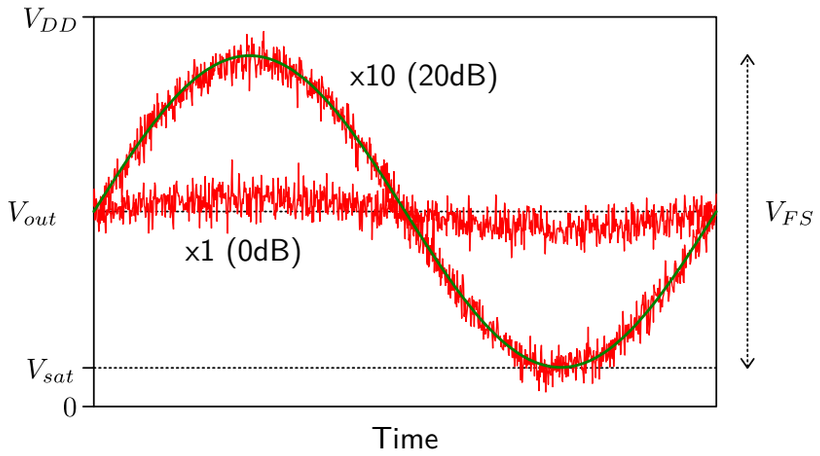
$$\frac{dv_{nfk}^2}{df} = \frac{K_{fk}}{WL}\frac{1}{f} \qquad \frac{di_{nth}^2}{df} = \frac{8}{3}KTng_{mg}$$

Uncorrelated phenomena and low-frequency:

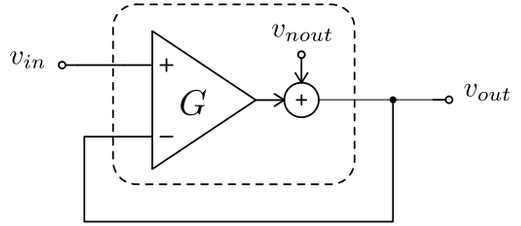
$$\frac{dv_{nout}^2}{df} = \frac{8}{3}KTn\frac{g_{mg}}{g_{md}^2} + \frac{K_{fk}}{WL}\left(\frac{g_{mg}}{g_{md}}\right)^2\frac{1}{f} \quad |G(DC)|^2$$

$$v_{nout}^2 = \frac{8}{3}KTn\frac{g_{mg}}{g_{md}^2}\underbrace{(f_2 - f_1)}_{BW} + \frac{K_{fk}}{WL}\left(\frac{g_{mg}}{g_{md}}\right)^2\ln\frac{f_2}{f_1}$$

- **Thermal** noise contribution only (f > flicker corner):



Equivalent input noise:

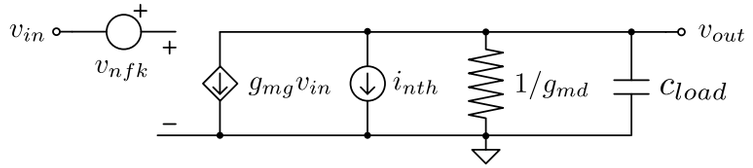


$$v_{out} = v_{nout} + G(v_{in} - v_{out})$$

$$v_{out} = \frac{Gv_{in} + v_{nout}}{1+G} \simeq v_{in} + \underbrace{\frac{v_{nout}}{G}}_{v_{nin}}$$

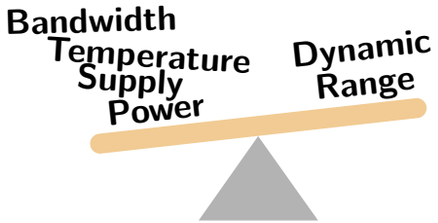
Dynamic Range

- **Noise** equivalent circuit:

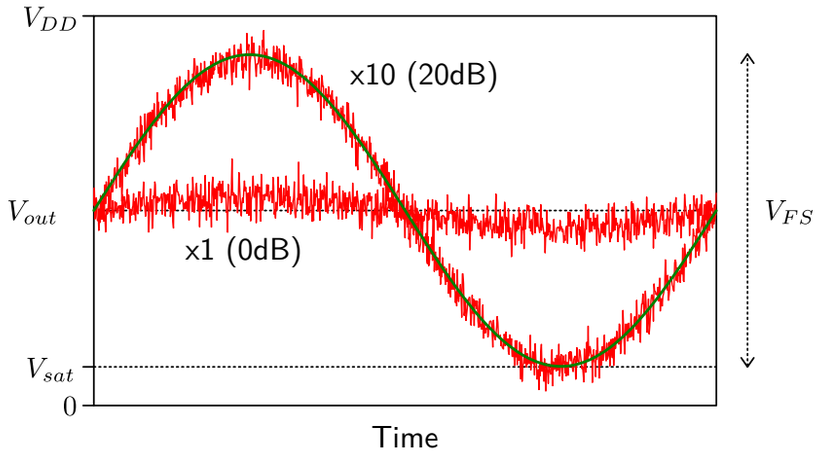


$$\frac{dv_{nfk}^2}{df} = \frac{K_{fk}}{WL}\frac{1}{f} \qquad \frac{di_{nth}^2}{df} = \frac{8}{3}KTng_{mg}$$

$$v_{nout}^2 = \frac{8}{3}KTn\frac{g_{mg}}{g_{md}^2}\underbrace{(f_2 - f_1)}_{BW} + \frac{K_{fk}}{WL}\left(\frac{g_{mg}}{g_{md}}\right)^2 \ln\frac{f_2}{f_1}$$



- **Thermal** noise contribution only (f > flicker corner):



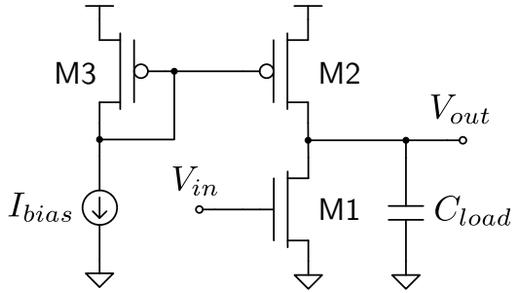
$$v_{nin}^2 \doteq \frac{v_{nout}^2}{|G(DC)|^2} = \frac{8}{3}\frac{KTn}{g_{mg}}BW = \frac{8}{3}\frac{KTn^{3/2}}{\sqrt{2\beta}}\frac{BW}{\sqrt{I_{bias}}}$$

$$DR = \left(\frac{V_{FS}/2\sqrt{2}}{v_{nin}}\right)^2 = \frac{3\sqrt{2}}{64}\frac{(V_{DD}-2V_{sat})^2}{KTBW}\sqrt{\frac{\beta I_{bias}}{n^3}}$$

$V_{DD}\uparrow$ $\left(\frac{W}{L}\right)\uparrow$ 1.5dB/oct $\uparrow$ $T\downarrow$ 3dB/oct

Full CMOS Circuit

- Similar performance analysis:

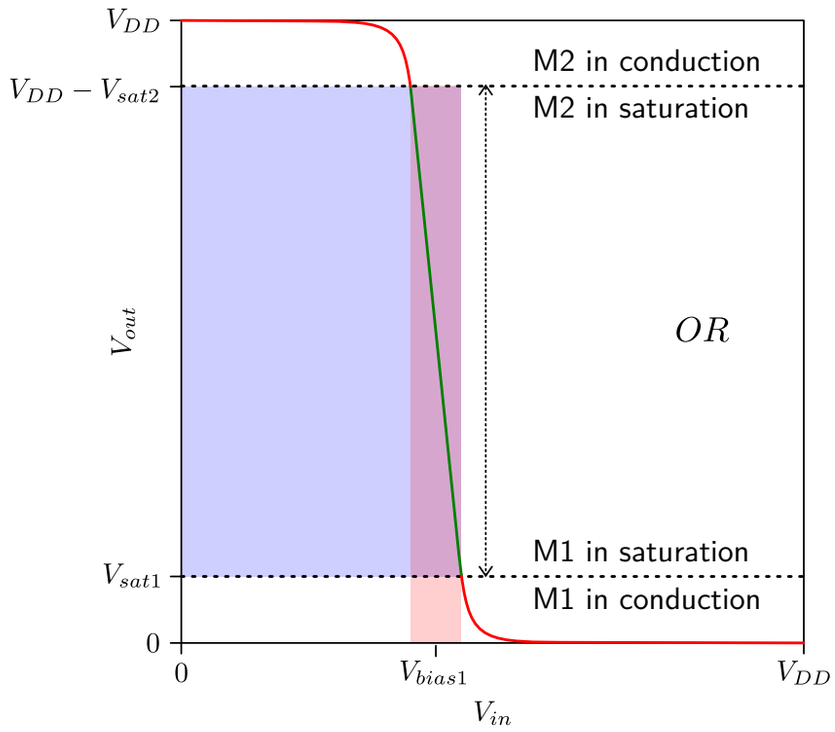


All operating in **strong inversion** and forward **saturation** bias points:

$$V_{sat1} = \sqrt{\frac{2I_{bias}}{n\beta_1}} \qquad V_{sat2} = \sqrt{\frac{2I_{bias}}{n\beta_2}}$$

$\left(\frac{W}{L}\right)_2$

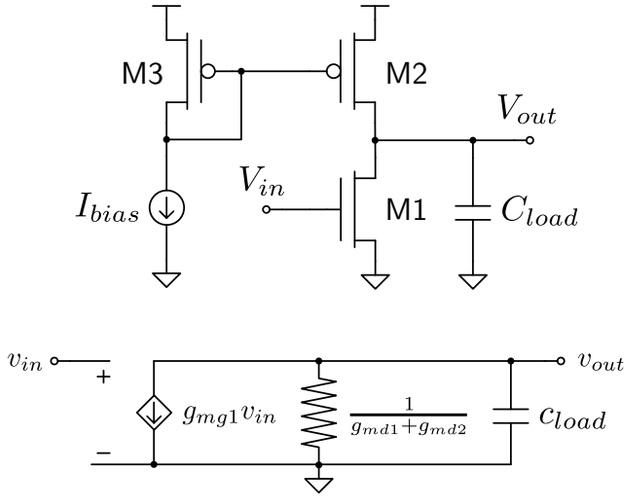
- Large signal **VTC**:



$$OR = V_{DD} - V_{sat1} - V_{sat2}$$

Full CMOS Circuit

- Similar performance analysis:



All operating in **strong inversion** and forward **saturation** bias points:

$$\left(\frac{W}{L}\right)_x \quad \begin{cases} g_{mgx} = \sqrt{\dfrac{2\beta_x I_{bias}}{n}} \\ g_{mdx} = \lambda_x I_{bias} \end{cases} \quad L_x$$

- Small signal **gain** and **bandwidth**:

$$G(DC) = -\frac{g_{mg1}}{g_{md1}+g_{md2}}$$

$$G(DC) = -\frac{1}{\lambda_1+\lambda_2}\sqrt{\frac{2\beta_1}{nI_{bias}}}\uparrow$$

$\left(\frac{W}{L}\right)_1 \uparrow$ 3dB/oct

6dB/oct $L_{1,2}\uparrow$

$I_{bias}\uparrow$ 3dB/oct

$$BW = \frac{g_{md1}+g_{md2}}{2\pi c_{load}}$$

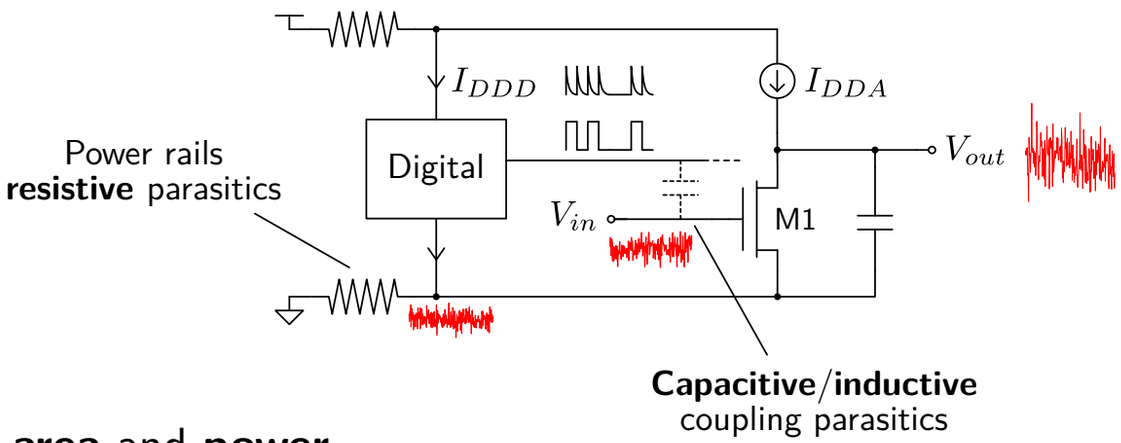
$$GBW = \frac{g_{mg1}}{2\pi c_{load}} = \frac{1}{2\pi c_{load}}\sqrt{\frac{2\beta_1 I_{bias}}{n}}\uparrow$$

$I_{bias}\uparrow$ 0.5oct/oct

$\left(\frac{W}{L}\right)_1 \uparrow$ 0.5oct/oct

Fully-Differential vs Single-Ended

- **Single-ended** OpAmps:



- ▲ Compact **area** and **power**
- ▼ Poor **signal integrity**
- Dynamic sources of **interference**:
  - Large signals (e.g. digital states)
  - Power supply currents
  - EM fields
  - Temperature gradients
  - Mechanical stress

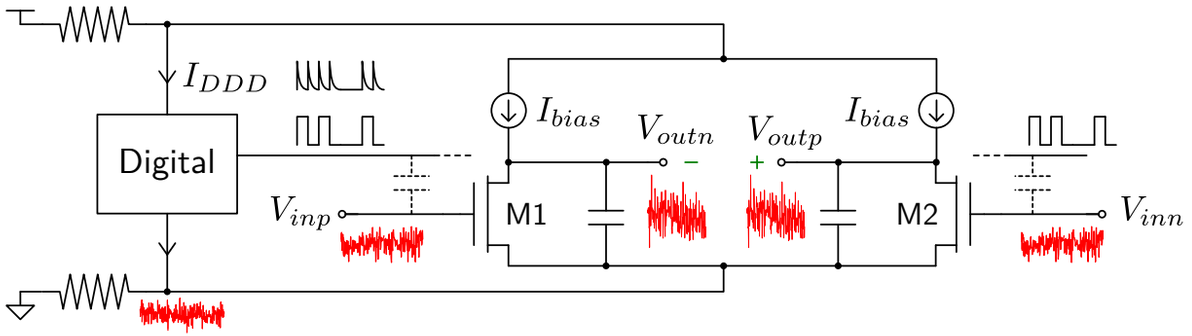
Fully-Differential vs Single-Ended

- **Pseudo-differential** OpAmps:

Signal true **info**

$$\begin{cases} V_{ind} \doteq V_{inp} - V_{inn} \\ V_{inc} \doteq \dfrac{V_{inp} + V_{inn}}{2} \end{cases}$$

Signal **baseline** only



$$\begin{cases} V_{outd} \doteq V_{outp} - V_{outn} \\ V_{outc} \doteq \dfrac{V_{outp} + V_{outn}}{2} \end{cases}$$

- ▲ Interference **rejection**
- ▼ **Area** and **power** overheads (x2)

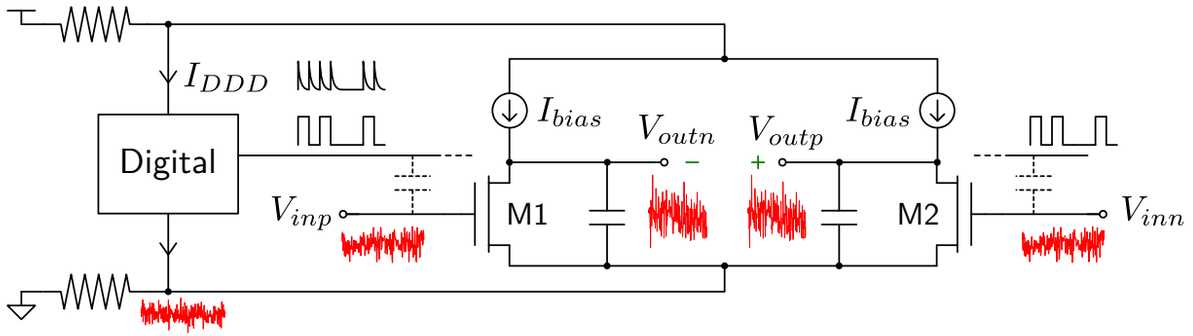
Fully-Differential vs Single-Ended

- **Pseudo-differential** OpAmps:

Signal true **info**

$$\begin{cases} V_{ind} \doteq V_{inp} - V_{inn} \\ V_{inc} \doteq \dfrac{V_{inp} + V_{inn}}{2} \end{cases}$$

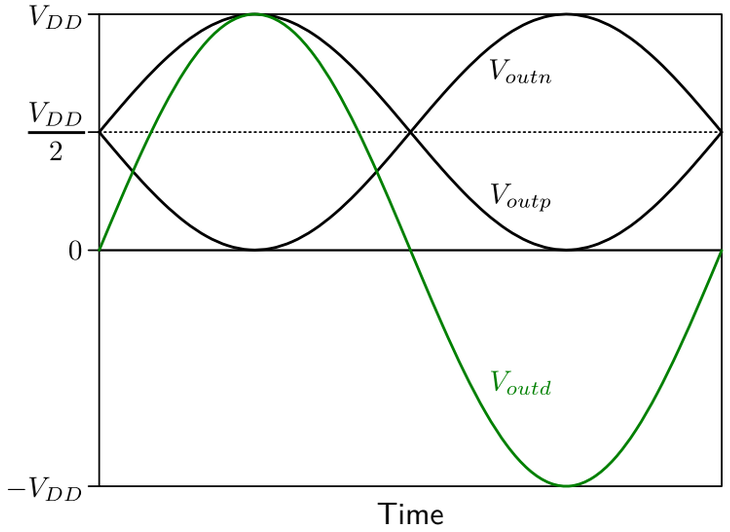
Signal **baseline** only



$$\begin{cases} V_{outd} \doteq V_{outp} - V_{outn} \\ V_{outc} \doteq \dfrac{V_{outp} + V_{outn}}{2} \end{cases}$$

- ▲ Interference **rejection**
- ▼ **Area** and **power** overheads (x2)
- ▲ **Full-scale** extension (+6dB)
- ▼ **Noise** increase (+3dB)

} SNR (+3dB)



Fully-Differential vs Single-Ended

- **Pseudo-differential** OpAmps:

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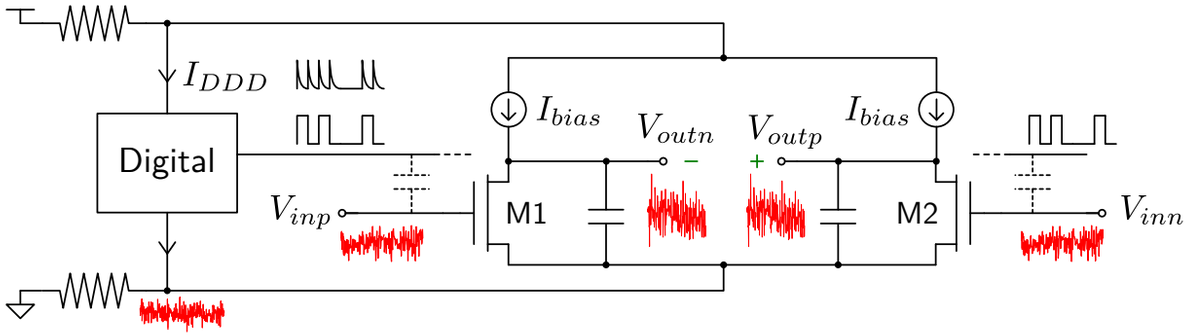
Signal **baseline** only

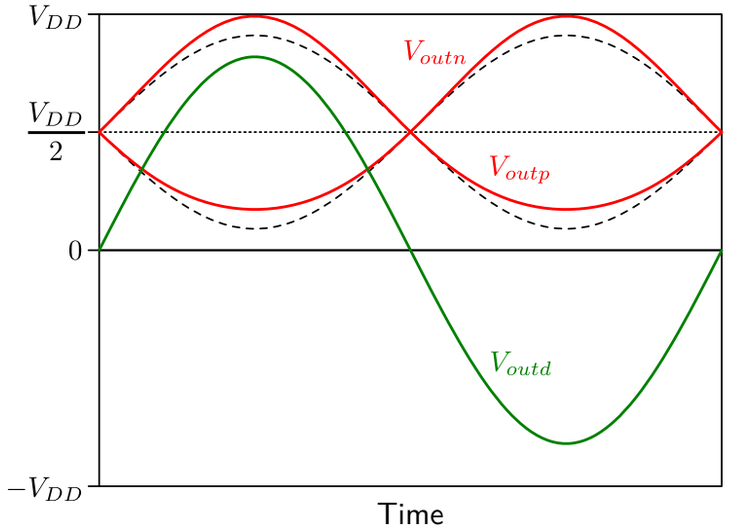


$$\begin{cases} V_{outd} \doteq V_{outp} - V_{outn} \\ V_{outc} \doteq \dfrac{V_{outp} + V_{outn}}{2} \end{cases}$$

- ▲ Interference **rejection**
- ▼ **Area** and **power** overheads (x2)
- ▲ **Full-scale** extension (+6dB)
- ▼ **Noise** increase (+3dB)

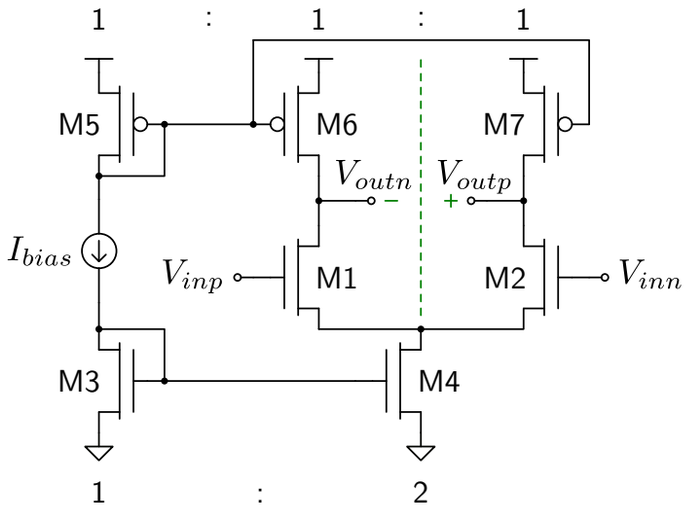
} SNR (+3dB)

- ▲ **Distortion** cancellation (even harm.)
- ▼ Limited by device **matching**



Fully-Differential OpAmps

- **Basic** CMOS topology:



device **multiplicity**

$$M \times \frac{W}{L}$$

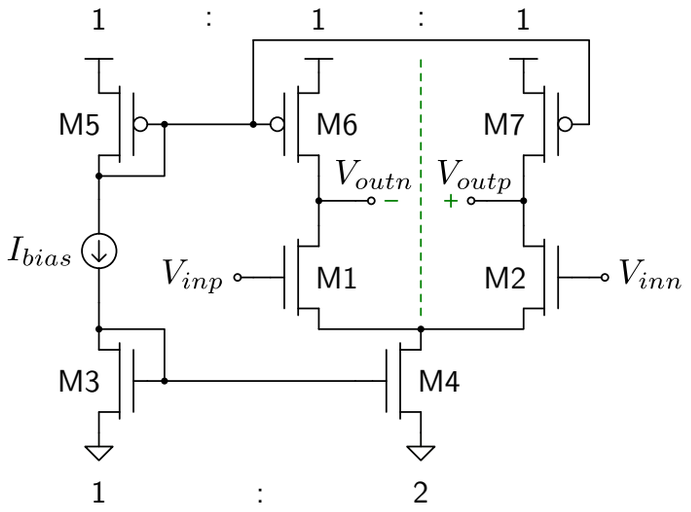
same aspect ratio

$$\begin{cases} V_{ind} \doteq V_{inp} - V_{inn} \\ V_{inc} \doteq \dfrac{V_{inp} + V_{inn}}{2} \end{cases}$$

$$\begin{cases} V_{outd} \doteq V_{outp} - V_{outn} \\ V_{outc} \doteq \dfrac{V_{outp} + V_{outn}}{2} \end{cases}$$

Fully-Differential OpAmps

- **Basic** CMOS topology:



device **multiplicity**

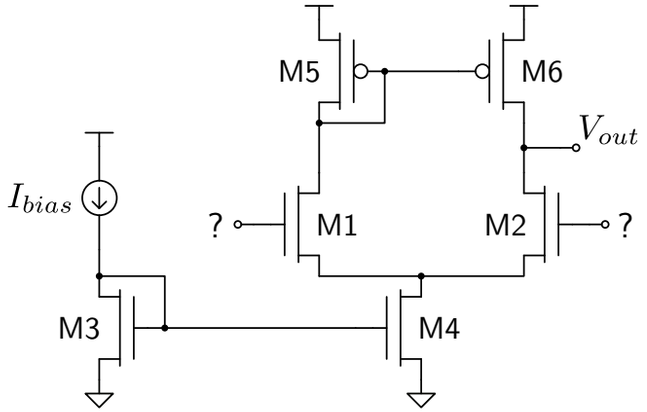
$$M \times \frac{W}{L}$$

same aspect ratio

$$\begin{cases} V_{ind} \doteq V_{inp} - V_{inn} \\ V_{inc} \doteq \dfrac{V_{inp} + V_{inn}}{2} \end{cases}$$

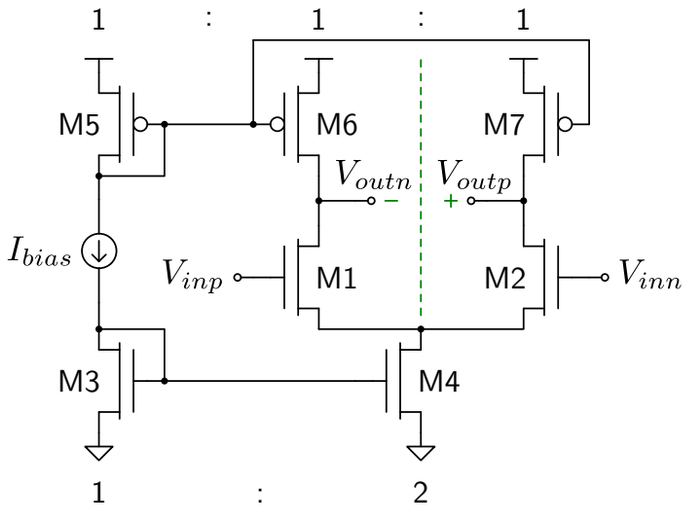
$$\begin{cases} V_{outd} \doteq V_{outp} - V_{outn} \\ V_{outc} \doteq \dfrac{V_{outp} + V_{outn}}{2} \end{cases}$$

- Differential **input** only:



Fully-Differential OpAmps

- **Basic** CMOS topology:



device **multiplicity**

$M \times \frac{W}{L}$

same aspect ratio

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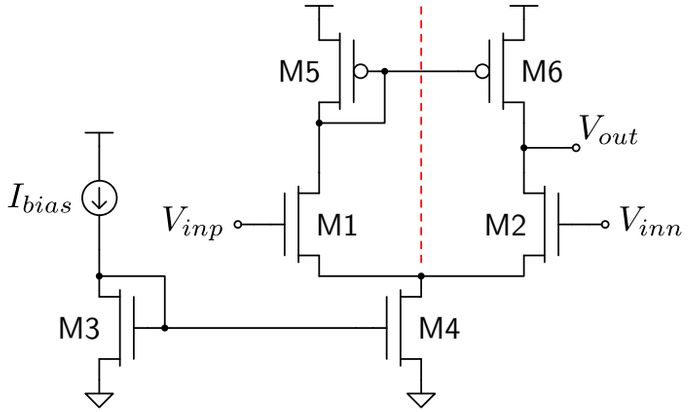
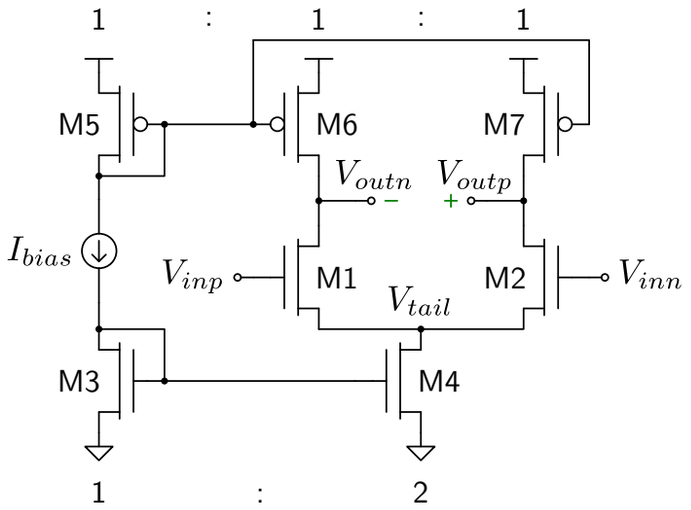
- Differential **input** only:



- ▼ M5-6 current mirror **asymmetry**
- ▼ Not full **cancellation** of unwanted terms
- ▲ Mostly used for **single-ended** signaling

Fully-Differential OpAmps

- **Basic** CMOS topology:

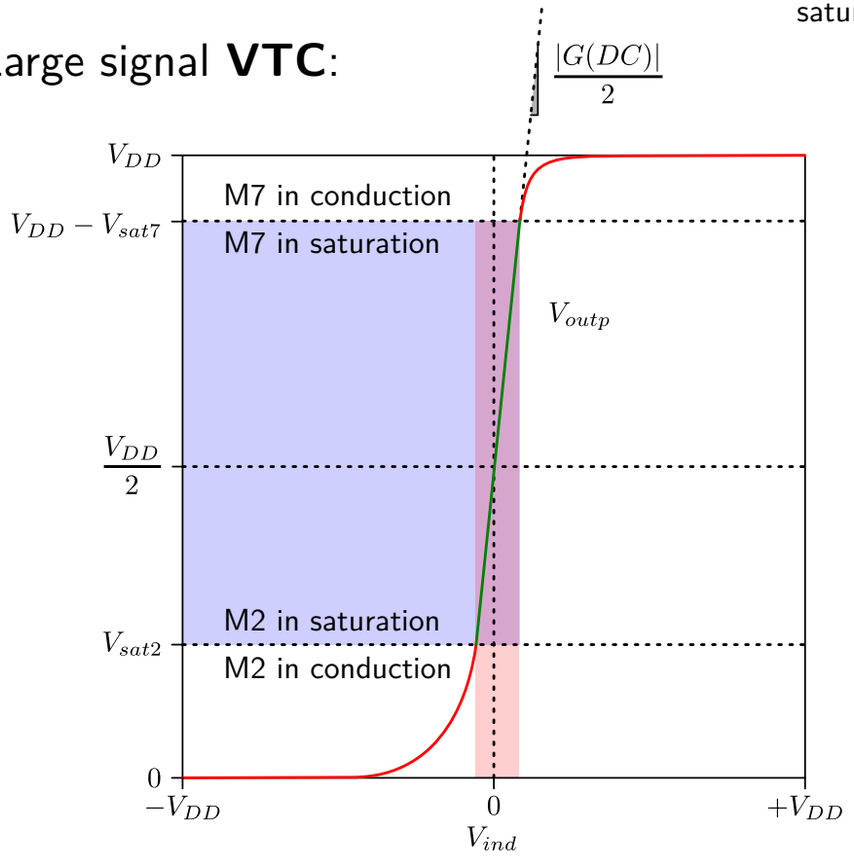


$$\begin{cases} V_{ind} \doteq V_{inp} - V_{inn} \\ V_{inc} \doteq \dfrac{V_{inp} + V_{inn}}{2} \end{cases}$$

$$\begin{cases} V_{outd} \doteq V_{outp} - V_{outn} \\ V_{outc} \doteq \dfrac{V_{outp} + V_{outn}}{2} \end{cases}$$

All operating in strong inversion saturation + neglecting CLM

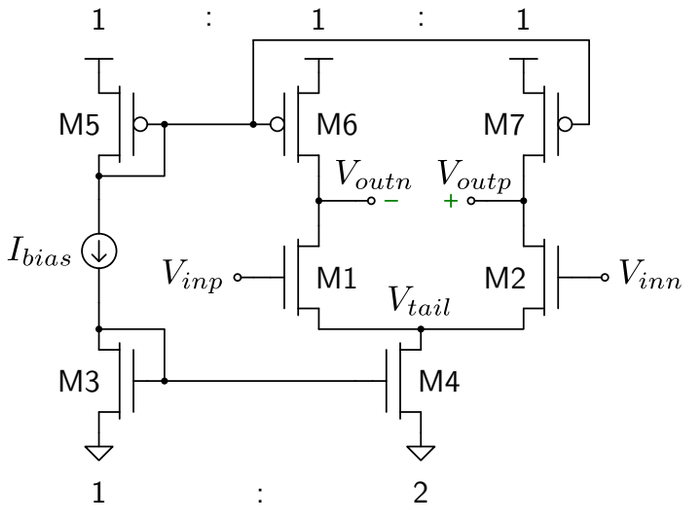
- Large signal **VTC**:



$$V_{sat7} = \sqrt{\frac{2I_{bias}}{n\beta_7}} \qquad V_{sat2} \simeq \frac{V_{inc} - V_{TH}}{n}$$

Fully-Differential OpAmps

- **Basic** CMOS topology:

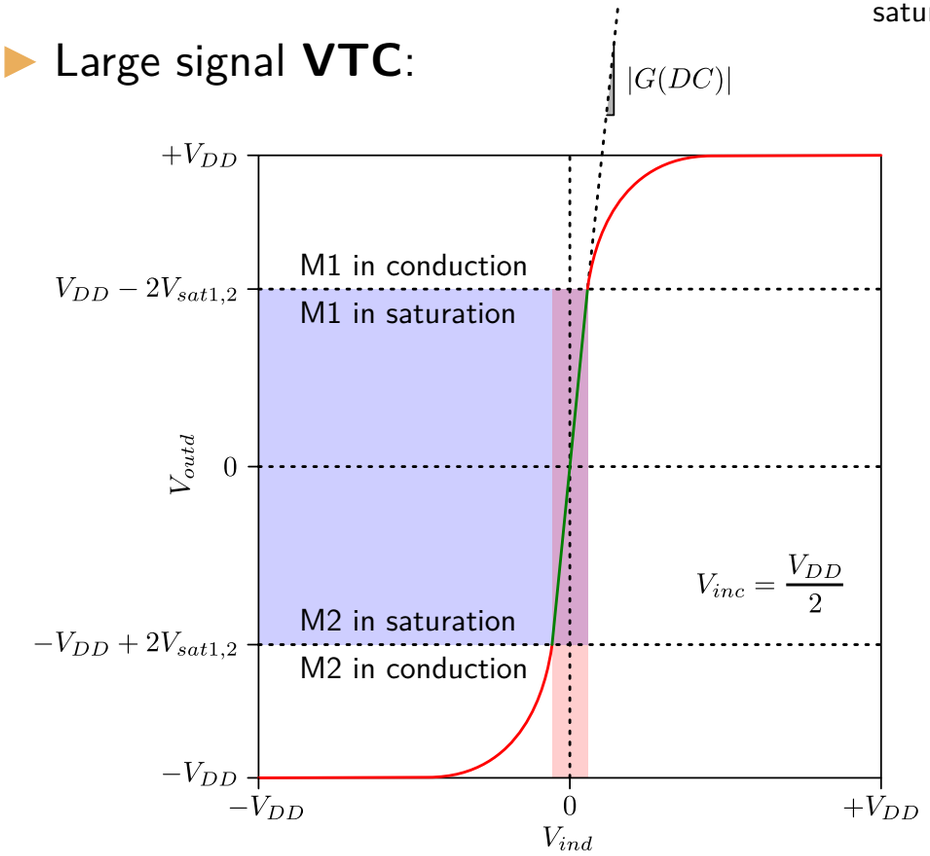


  - Reduced **output range**

$$OR = 2V_{DD} - 4V_{sat1,2} \qquad V_{sat1,2} \simeq \frac{V_{inc} - V_{TH}}{n}$$

All operating in strong inversion saturation + neglecting CLM

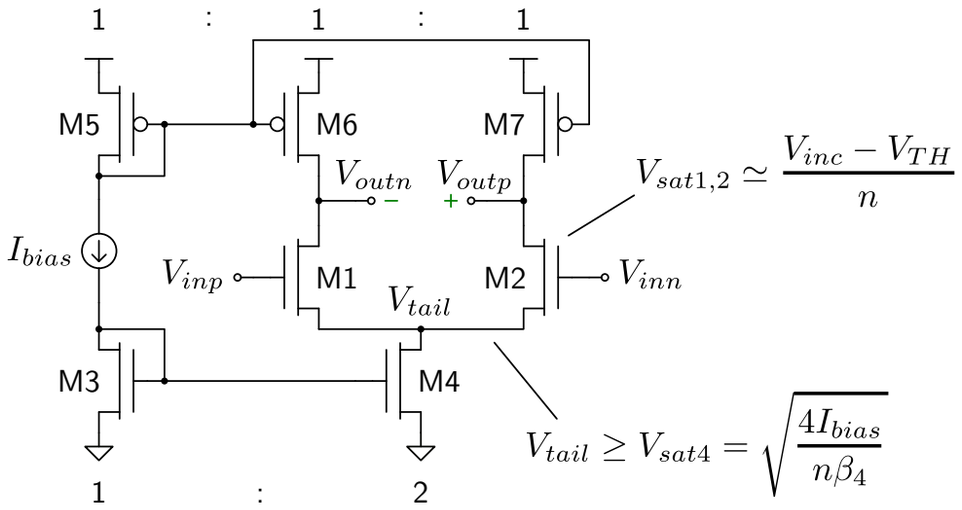
- Large signal **VTC**:



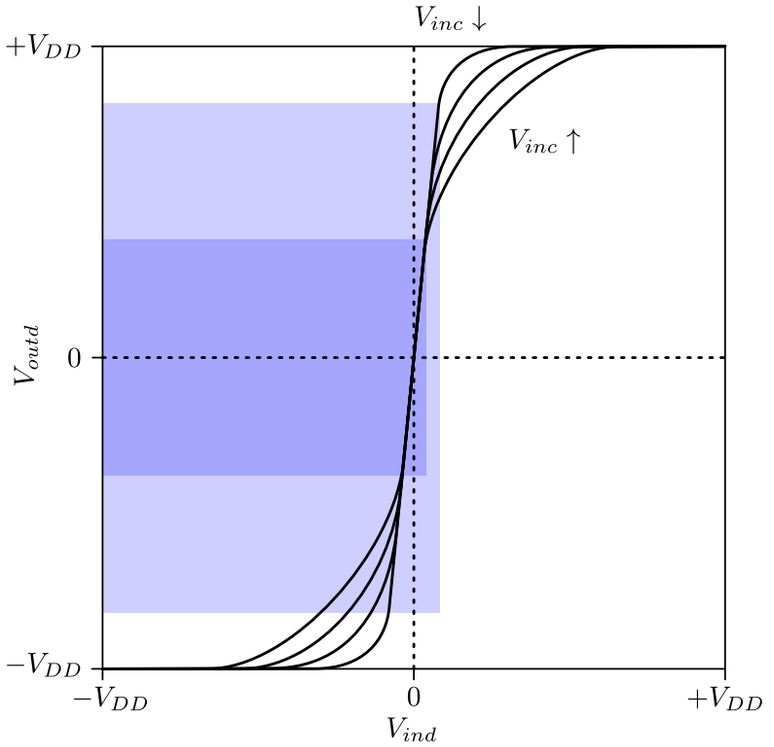
Fully-Differential OpAmps

All operating in strong inversion
saturation + neglecting CLM

- **Basic** CMOS topology:



- Large signal **VTC**:



- Reduced **output range**

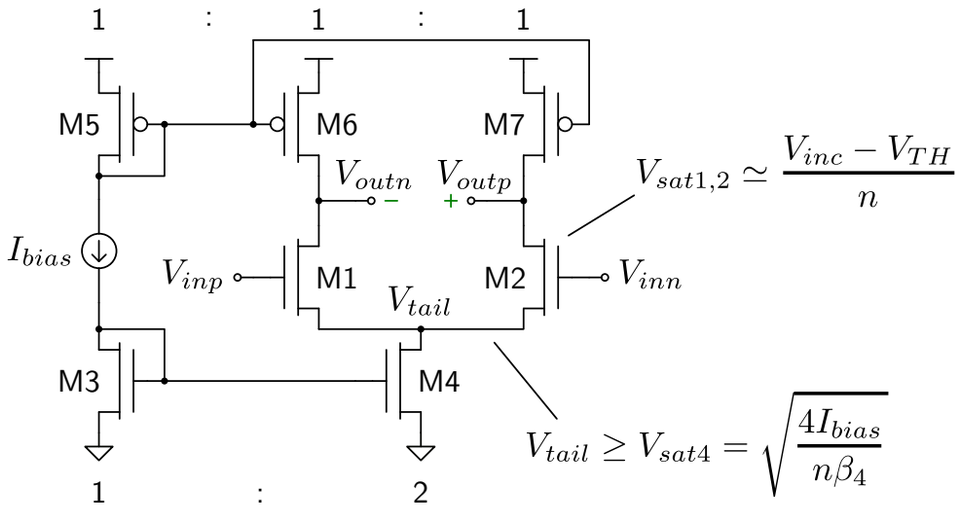
$$OR = 2V_{DD} - 4V_{sat1,2}$$

$$I_{bias} = \frac{\beta_{1,2}}{2n}\left(V_{inc} - V_{TH} - nV_{tail}\right)^2$$

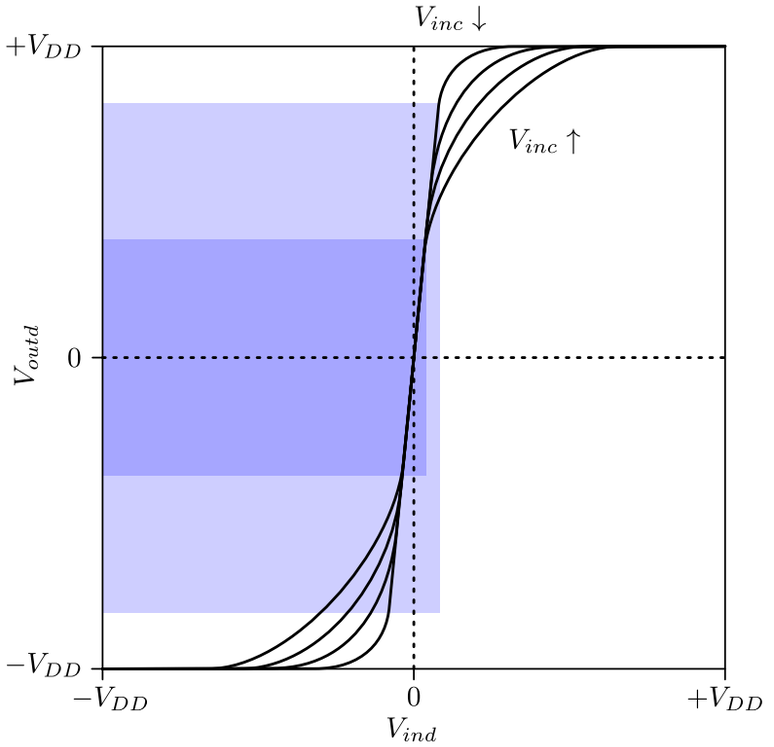
Fully-Differential OpAmps

All operating in strong inversion saturation + neglecting CLM

- **Basic** CMOS topology:



- Large signal **VTC**:



- Reduced **output range**

$$OR = 2V_{DD} - 4V_{sat1,2}$$

$$I_{bias} = \frac{\beta_{1,2}}{2n}\left(V_{inc} - V_{TH} - nV_{tail}\right)^2$$

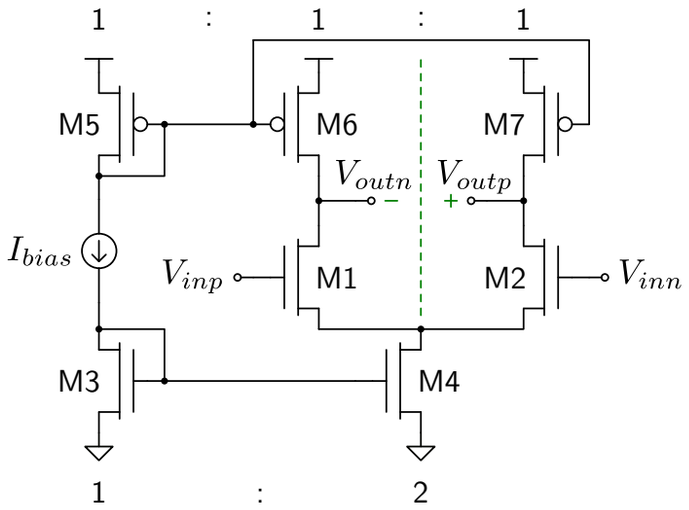
$$V_{sat1,2} = \sqrt{\frac{2I_{bias}}{n\beta_{1,2}}} + V_{sat4}$$

$$OR = 2V_{DD} - 4\sqrt{\frac{2I_{bias}}{n\beta_{un}}}\left[\sqrt{\left(\frac{L}{W}\right)_{1,2}} + \sqrt{2\left(\frac{L}{W}\right)_4}\right] \uparrow \quad \left(\frac{W}{L}\right)_{1,2} \uparrow \quad \left(\frac{W}{L}\right)_4 \uparrow$$

Fully-Differential OpAmps

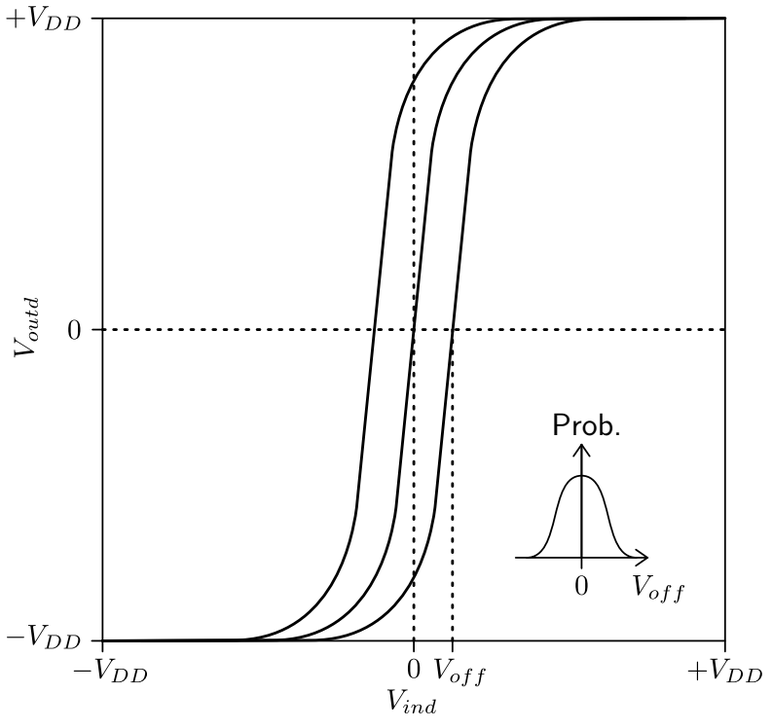
All operating in strong inversion saturation + neglecting CLM

- **Basic** CMOS topology:



  - Reduced **output range**
  - More **offset** contributions

- Large signal **VTC**:



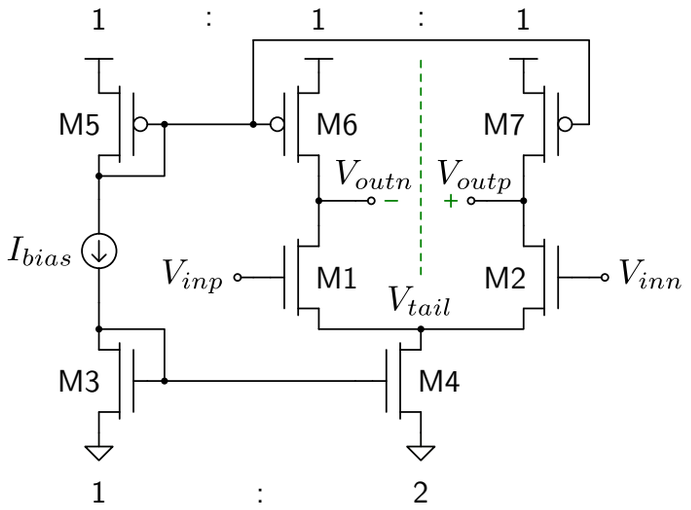
Threshold voltage **mismatching** only

Pelgrom's Law

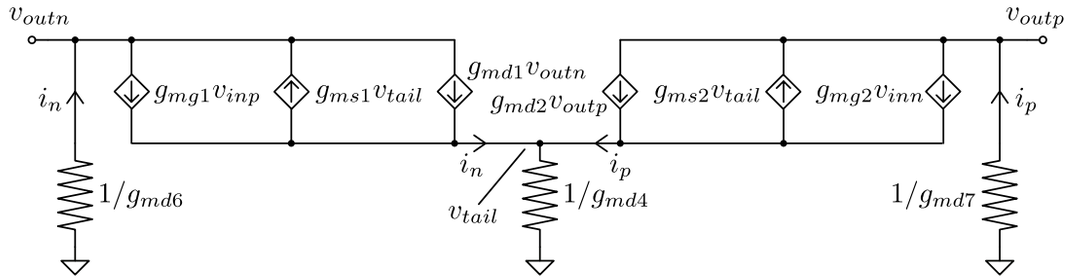
$$\sigma^2(V_{off}) = \sigma^2(\Delta V_{TH1,2}) + \left(\frac{g_{mg3,4}}{g_{mg1,2}}\right)^2 \sigma^2(\Delta V_{TH6,7}) = \frac{A^2_{VTHN}}{(WL)_{1,2}} + \underbrace{\frac{\beta_{up}}{\beta_{un}} \frac{(W/L)_{6,7}}{(W/L)_{1,2}} \frac{A^2_{VTHP}}{(WL)_{6,7}}}_{\text{neglegible}} \quad \downarrow \quad (WL)_{1,2} \uparrow$$

Fully-Differential OpAmps

- **Basic** CMOS topology:



- Small signal **differential** and **common** DC gains:



$$\begin{cases} i_p = g_{mg2}v_{inn} - g_{ms2}v_{tial} + g_{md2}v_{outp} \\ i_n = g_{mg1}v_{inp} - g_{ms1}v_{tial} + g_{md1}v_{outn} \end{cases} \qquad \begin{cases} g_{md7}v_{outp} = -i_p \\ g_{md6}v_{outn} = -i_n \end{cases}$$

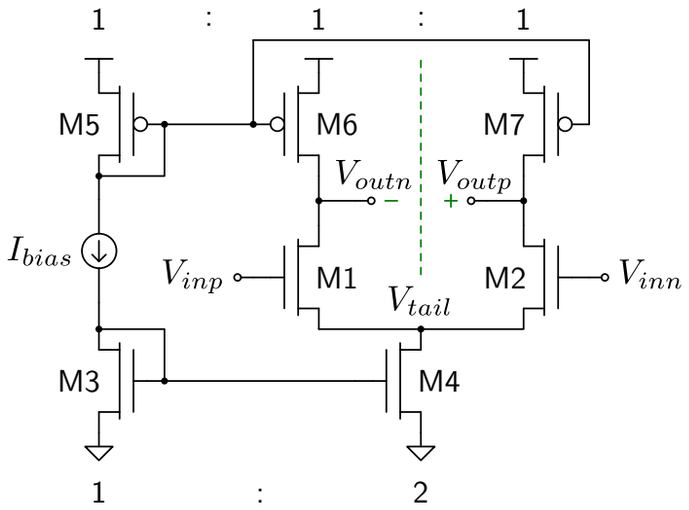
$$i_n + i_p = g_{md4}v_{tail}$$

$$(g_{md7}+g_{md2})v_{outp} - (g_{md6}+g_{md1})v_{outn} + \frac{g_{ms1}-g_{ms2}}{g_{ms1}+g_{ms2}+g_{md4}}(g_{md2}v_{outp}+g_{md1}v_{outn}) =$$

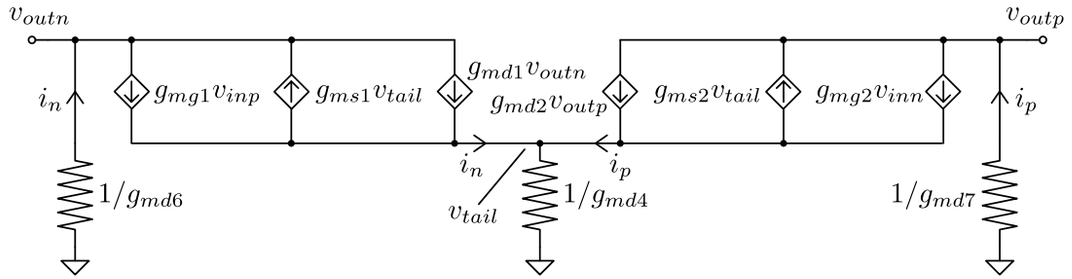
$$= g_{mg1}v_{inp} - g_{mg2}v_{inn} + \frac{g_{ms2}-g_{ms1}}{g_{ms1}+g_{ms2}+g_{md4}}(g_{mg1}v_{inp}+g_{mg2}v_{inn})$$

Fully-Differential OpAmps

- **Basic** CMOS topology:



- Small signal **differential** and **common** DC gains:



$$\begin{cases} i_p = g_{mg2}v_{inn} - g_{ms2}v_{tial} + g_{md2}v_{outp} \\ i_n = g_{mg1}v_{inp} - g_{ms1}v_{tial} + g_{md1}v_{outn} \end{cases} \qquad \begin{cases} g_{md7}v_{outp} = -i_p \\ g_{md6}v_{outn} = -i_n \end{cases}$$

$$i_n + i_p = g_{md4}v_{tail}$$

differential output (v_{outd}) — **common output** (v_{outc})

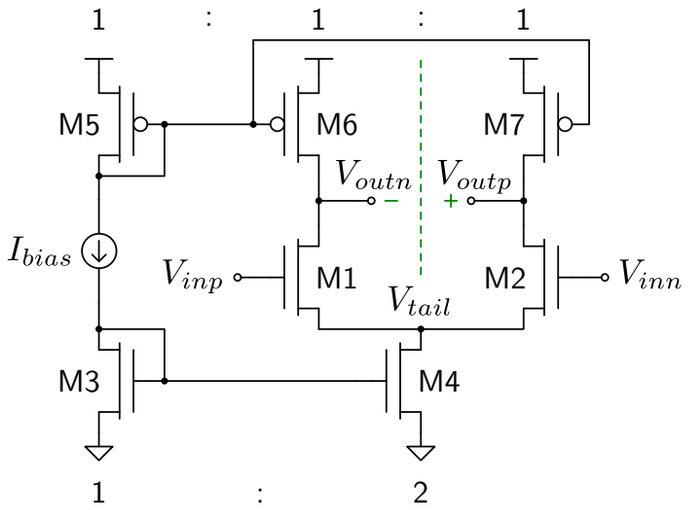
$$(g_{md7}+g_{md2})v_{outp} - (g_{md6}+g_{md1})v_{outn} + \frac{g_{ms1}-g_{ms2}}{g_{ms1}+g_{ms2}+g_{md4}}(g_{md2}v_{outp} + g_{md1}v_{outn}) =$$

$$= g_{mg1}v_{inp} - g_{mg2}v_{inn} + \frac{g_{ms2}-g_{ms1}}{g_{ms1}+g_{ms2}+g_{md4}}(g_{mg1}v_{inp} + g_{mg2}v_{inn})$$

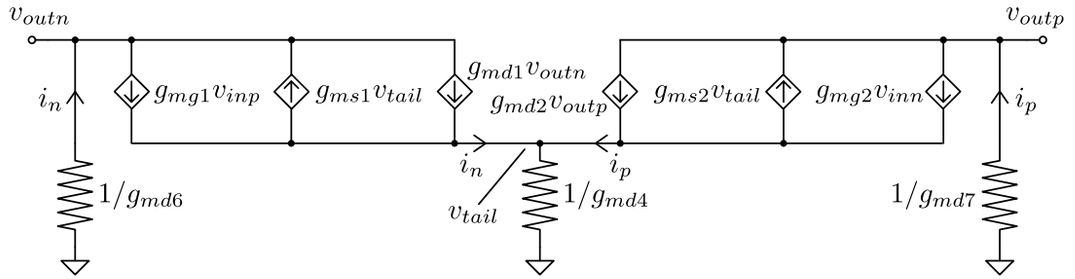
v_{ind} — **differential input** | v_{inc} — **common input**

Fully-Differential OpAmps

- **Basic** CMOS topology:



- Small signal **differential** and **common** DC gains:



- **Perfect matching** (M1=M2 and M6=M7):

$$\left.\begin{aligned} G_d &\doteq \frac{v_{outd}}{v_{ind}} = \frac{g_{mg1,2}}{g_{md1,2}+g_{md6,7}} \\ G_c &\doteq \frac{v_{outd}}{v_{inc}} \equiv 0 \end{aligned}\right\} CMRR \doteq \frac{G_d}{G_c} = \infty$$

differential output v_{outd}

$$(g_{md7}+g_{md2})v_{outp} - (g_{md6}+g_{md1})v_{outn} + \frac{g_{ms1}-g_{ms2}}{g_{ms1}+g_{ms2}+g_{md4}}(g_{md2}v_{outp}+g_{md1}v_{outn}) =$$

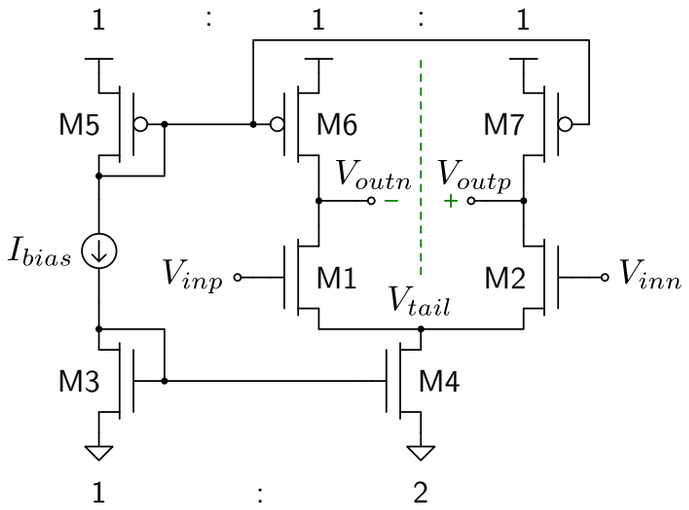
$$= g_{mg1}v_{inp} - g_{mg2}v_{inn} + \frac{g_{ms2}-g_{ms1}}{g_{ms1}+g_{ms2}+g_{md4}}(g_{mg1}v_{inp}+g_{mg2}v_{inn})$$

v_{ind}

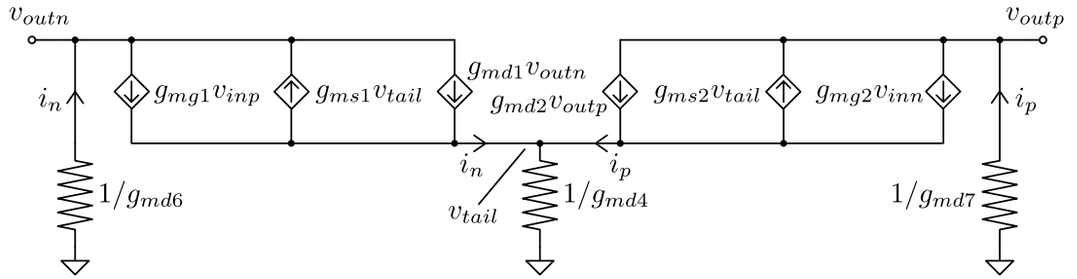
differential input

Fully-Differential OpAmps

- **Basic** CMOS topology:



- Small signal **differential** and **common** DC gains:



- **Real matching** (e.g. $V_{TH1} \neq V_{TH2}$):

$$\begin{cases} g_{mg1,2} = \dfrac{g_{mg1} + g_{mg2}}{2} \\ \Delta g_{mg1,2} = \dfrac{g_{mg1} - g_{mg2}}{2} \end{cases}$$

$$(g_{md1,2}+g_{md6,7})v_{outd} = g_{mg1,2}v_{ind} + 2\Delta g_{mg1,2}v_{inc} - \frac{2\Delta g_{mg1,2}}{2g_{mg1,2} + g_{md4}/n}(2g_{mg1,2}v_{inc} + \Delta g_{mg1,2}v_{ind})$$

Neglecting common output

- **Perfect matching** (M1=M2 and M6=M7):

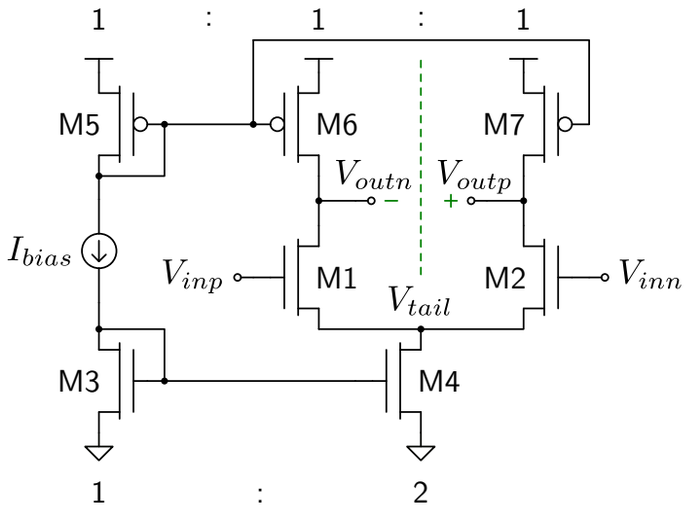
$$\left.\begin{aligned} G_d &\doteq \frac{v_{outd}}{v_{ind}} = \frac{g_{mg1,2}}{g_{md1,2} + g_{md6,7}} \\ G_c &\doteq \frac{v_{outd}}{v_{inc}} \equiv 0 \end{aligned}\right\} CMRR \doteq \frac{G_d}{G_c} = \infty$$

$$CMRR = \frac{g_{mg1,2}}{2\Delta g_{mg1,2}}\left(\frac{2ng_{mg1,2}}{g_{md4}} + 1\right) \quad \uparrow$$

Matching ↑ — Tail current sink **impedance** ↑

Fully-Differential OpAmps

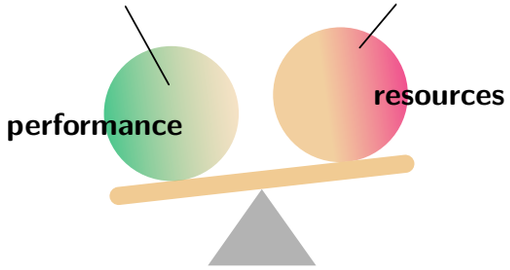
- **Basic** CMOS topology:



- Reduced **output range**
- **Matching** is critical

- Summary of **design guidelines**:

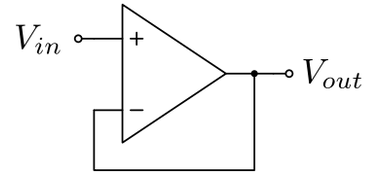
$OR \uparrow$	$\left(\frac{W}{L}\right)_{1,2} \uparrow$	$\left(\frac{W}{L}\right)_{3,4} \uparrow$	$I_{bias} \downarrow$
$\sigma(V_{off}) \downarrow$	$(WL)_{1,2} \uparrow$	$\left(\frac{W}{L}\right)_{1,2} \uparrow$	$I_{bias} \uparrow$
$G_d \uparrow$	$\left(\frac{W}{L}\right)_{1,2} \uparrow$	$L_{1,2,5,6,7} \uparrow$	$I_{bias} \downarrow$
$CMRR \uparrow$	$(WL)_{1,2} \uparrow$	$L_{3,4} \uparrow$	$I_{bias} \downarrow$
$GBW \uparrow$	$\left(\frac{W}{L}\right)_{1,2} \uparrow$		$I_{bias} \uparrow$
$v_{nin}^2 \downarrow$	$\left(\frac{W}{L}\right)_{1,2} \uparrow$		$I_{bias} \uparrow$

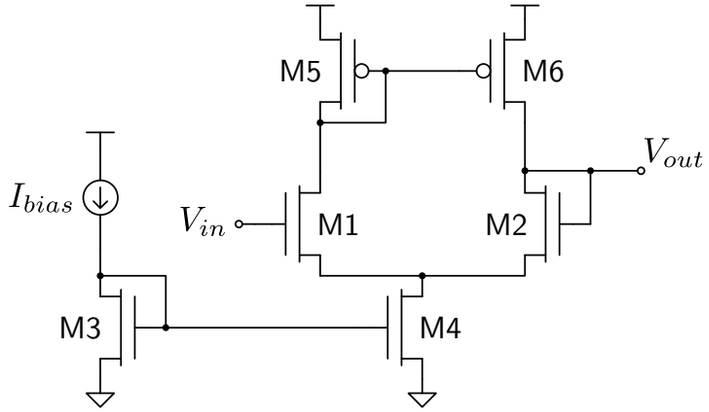


Common-Mode Output Issue

- **Single-ended** differential OpAmps:

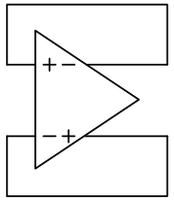
e.g. max. feedback

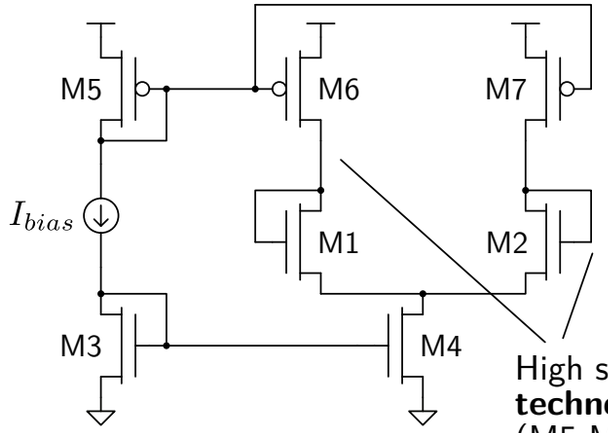




$$V_{inc} \simeq V_{out} \simeq V_{in}$$

- **Fully-differential** OpAmps:





High sensitivity to **technology mismatching** (M5-M6|7 and M3-M4)!

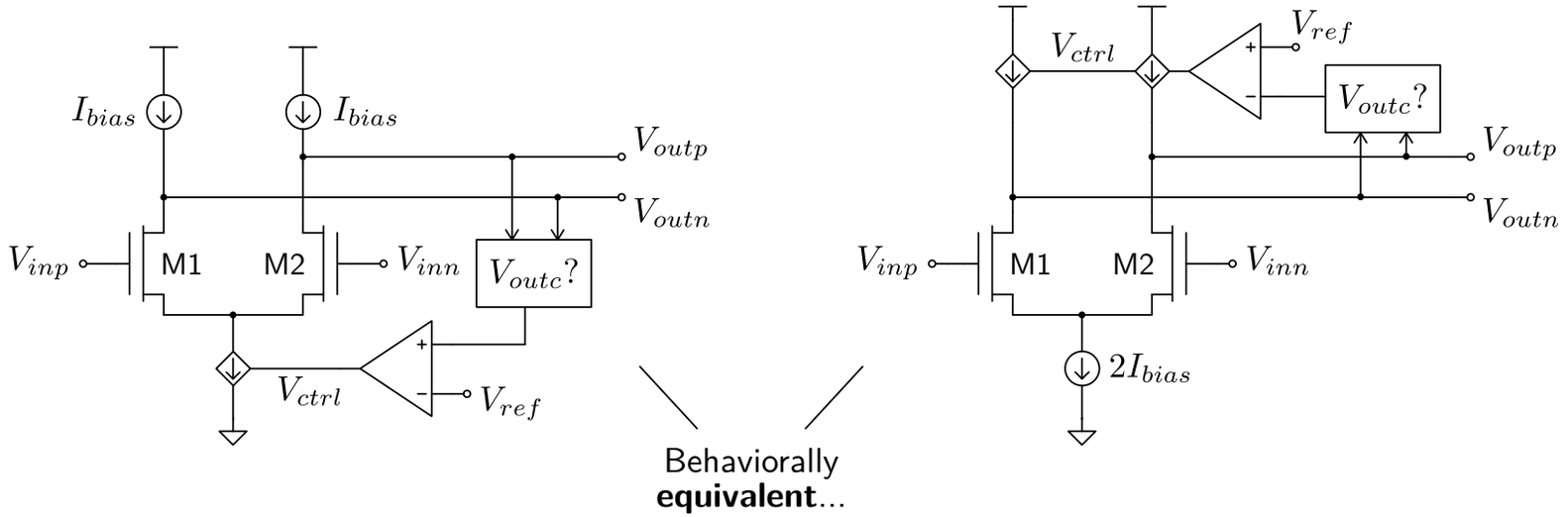
$$V_{inc} \equiv V_{outc} = ?$$

▲ **Well-defined** and **stable** common-mode level

▼ Specific auxiliary **control circuitry** is needed in practice...

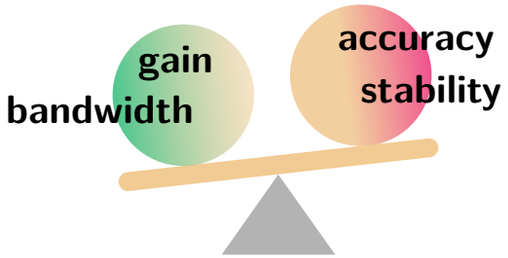
Common-Mode Output Issue

- Common-mode feedback (**CMFB**) loop:



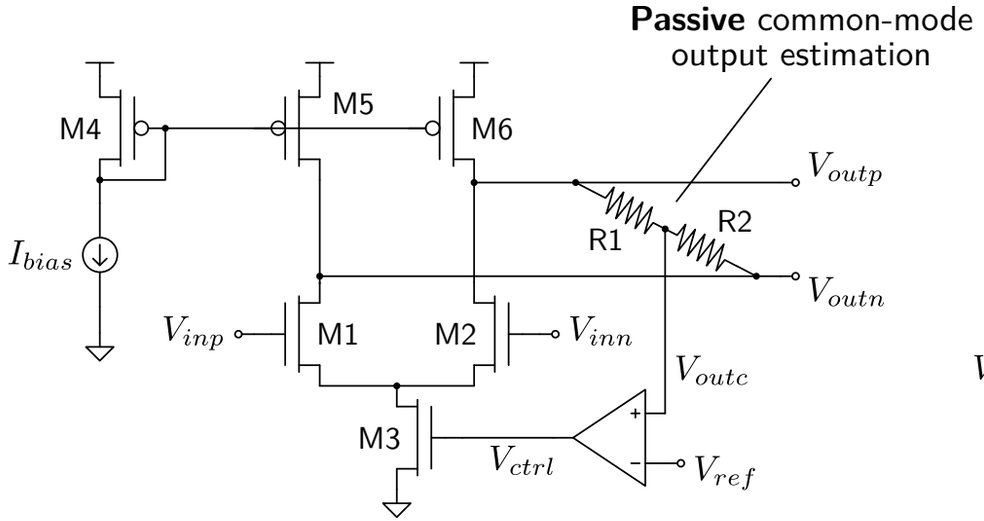
- CMFB control **functionality**:
  - **Sensing** common-mode output
  - Computing **error** according to **reference** level
  - Applying needed common-mode **correction**
- **Not** to be confused with **CMRR**!

- Multi-stage OpAmps require one **CMFB** loops for **each stage**
- **CMFB** control design?



Continuous-Time CMFB

- **Resistive**-based sensing:

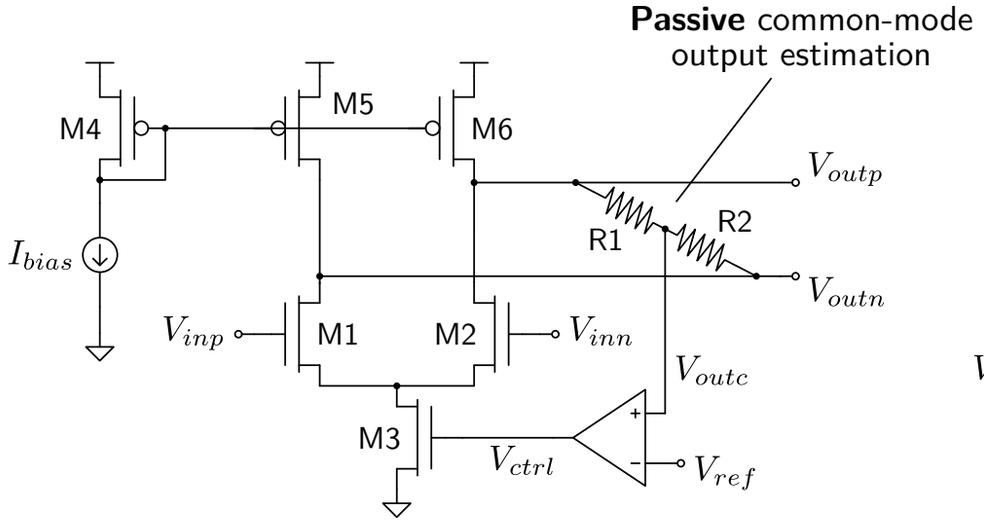


$$V_{outc} = \frac{R_2}{R_1 + R_2} V_{outp} + \frac{R_1}{R_1 + R_2} V_{outn}$$

$$V_{outc}|_{R_1 \equiv R_2} = \frac{V_{outp} + V_{outn}}{2}$$

Continuous-Time CMFB

- **Resistive**-based sensing:



$$V_{outc} = \frac{R_2}{R_1 + R_2} V_{outp} + \frac{R_1}{R_1 + R_2} V_{outn}$$

$$V_{outc}|_{R_1 \equiv R_2} = \frac{V_{outp} + V_{outn}}{2}$$

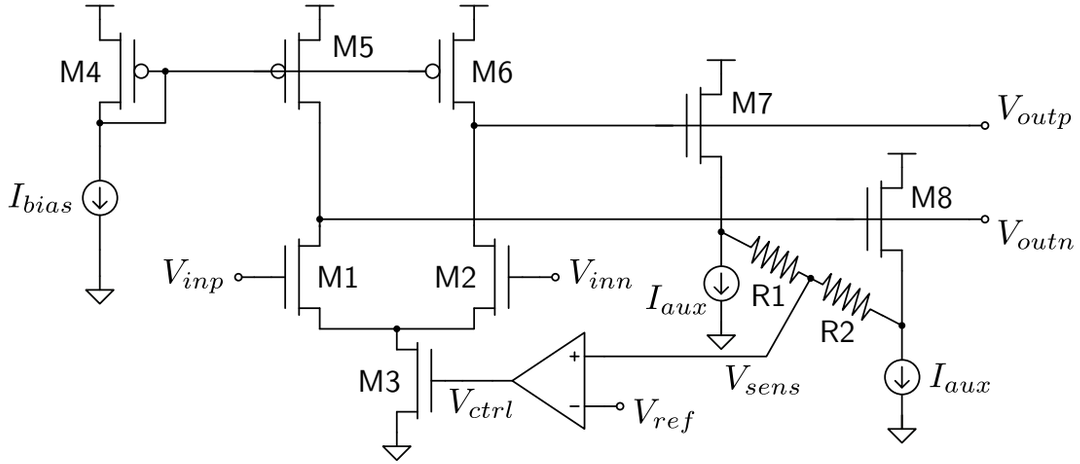
- ▲ OpAmp original **OR** is preserved
- ▼ Resistive **extra loading**...

$R_{1,2} \uparrow$

...or limited CMFB **bandwidth**

Continuous-Time CMFB

- **Resistive**-based sensing:

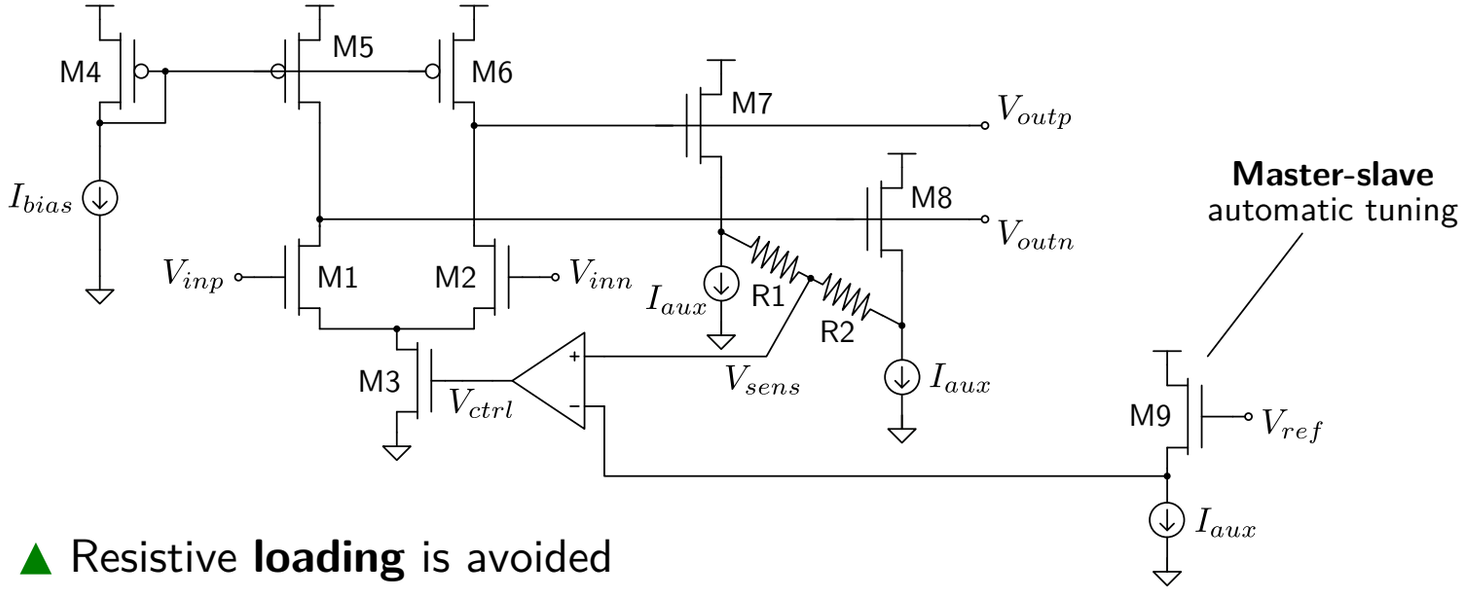


- ▲ Resistive **loading** is avoided
- ▼ **OR** severe reduction
- ▼ **Power** consumption overhead
- ▼ Common-mode output level is **technology** dependent!

$$V_{outc} = nV_{ref} + V_{TH} + \sqrt{\frac{2nI_{aux}}{\beta_{7,8}}}$$

Continuous-Time CMFB

- **Resistive**-based sensing:

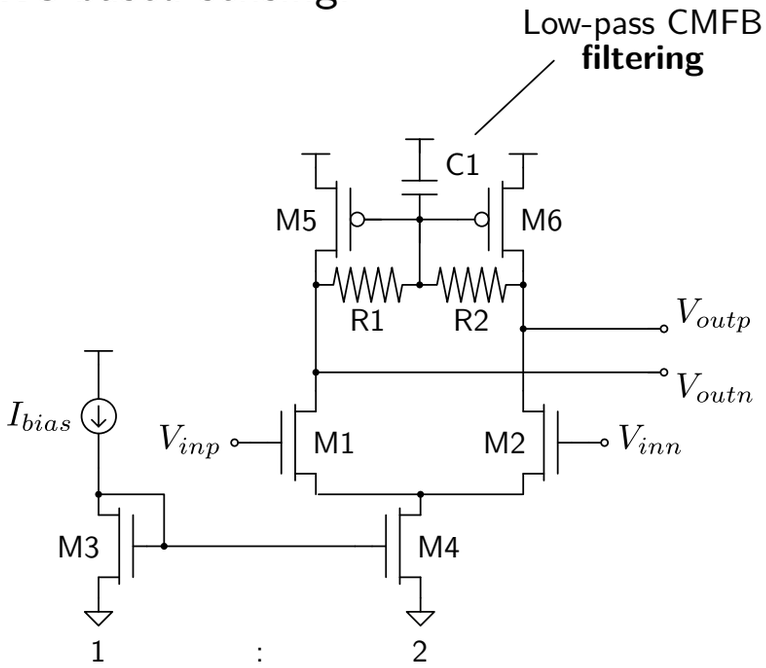


- ▲ Resistive **loading** is avoided
- ▼ **OR** severe reduction
- ▼ **Power** consumption overhead
- ~~▼ Common-mode output level is **technology** dependent!~~

$$V_{outc} \equiv V_{ref}$$

Continuous-Time CMFB

- **Resistive**-based sensing:

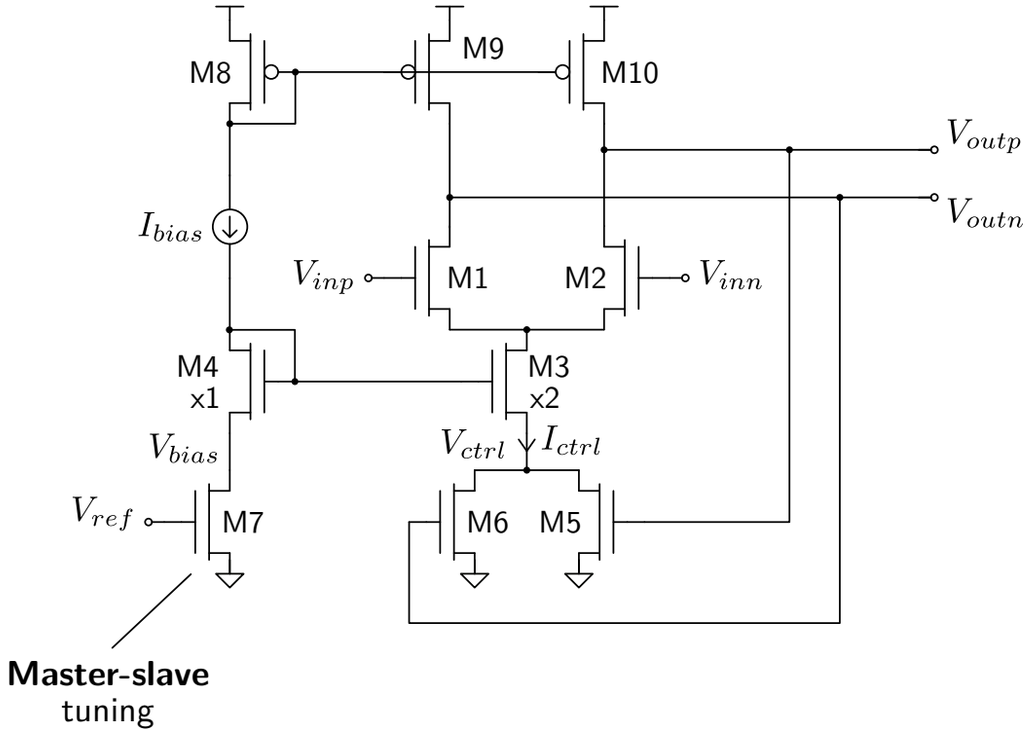


$$V_{outc} = V_{DD} - V_{TH} - \sqrt{\frac{2nI_{bias}}{\beta_{5,6}}}$$

- ▲ **Compact** circuit solution
- ▲ No **power** consumption overhead
- ▼ Common-mode output defined by **technology**
- ▼ Strong **OR** reduction

Continuous-Time CMFB

- **MOS**-based sensing:



Supposing M5, M6 and M7 working in **deep conduction:**

$$I_{ctrl} = \beta_5 \left(V_{outp} - V_{TH} + n\frac{V_{ctrl}}{2} \right) V_{ctrl} + \beta_6 \left(V_{outn} - V_{TH} + n\frac{V_{ctrl}}{2} \right) V_{ctrl}$$

By **CMFB symmetry** (M5=M6)**:**

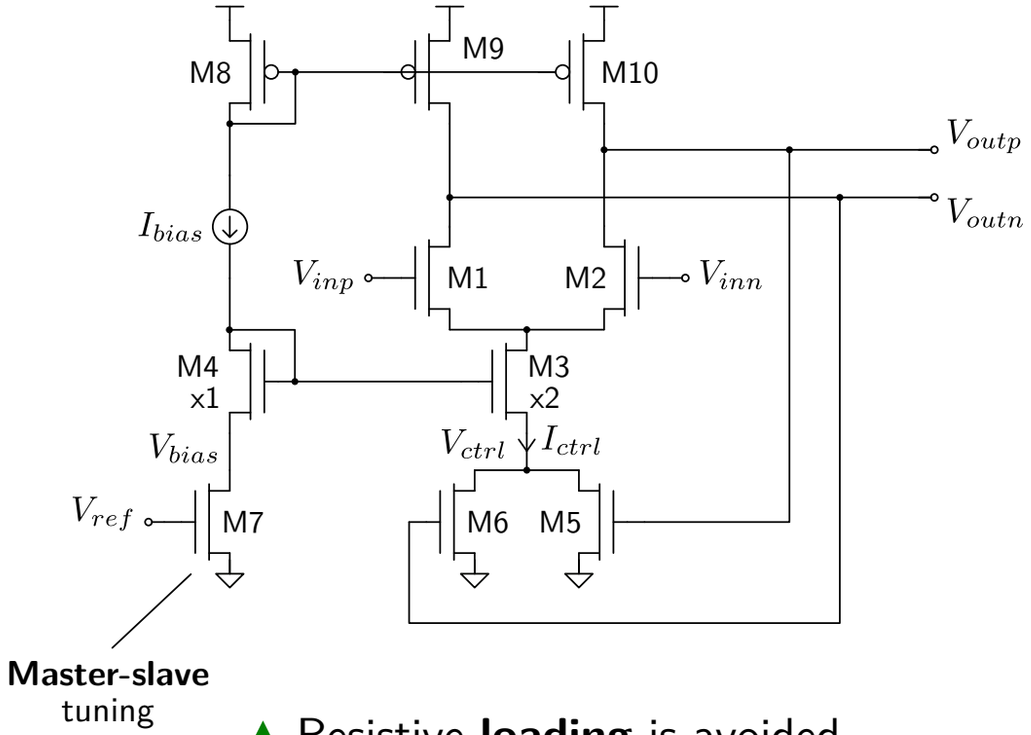
$$I_{ctrl} = f(\underbrace{V_{outp} + V_{outn}}_{\propto V_{outc}}) \qquad \frac{dI_{ctrl}}{dV_{outd}} \equiv 0$$

By **bias symmetry** (M5|6=M7 and M3=M4)**:**

$$V_{ctrl} \equiv V_{bias} \qquad I_{ctrl} \equiv 2I_{bias} \qquad V_{outc} \equiv V_{ref}$$

Continuous-Time CMFB

- **MOS**-based sensing:



▲ Resistive **loading** is avoided

▲ No **power** consumption overhead

Supposing M5, M6 and M7 working in **deep conduction:**

$$I_{ctrl} = \beta_5 \left(V_{outp} - V_{TH} + n\frac{V_{ctrl}}{2} \right) V_{ctrl} + \beta_6 \left(V_{outn} - V_{TH} + n\frac{V_{ctrl}}{2} \right) V_{ctrl}$$

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$$V_{ctrl} \equiv V_{bias} \qquad I_{ctrl} \equiv 2I_{bias} \qquad V_{outc} \equiv V_{ref}$$

▲ Negligible **OR** reduction

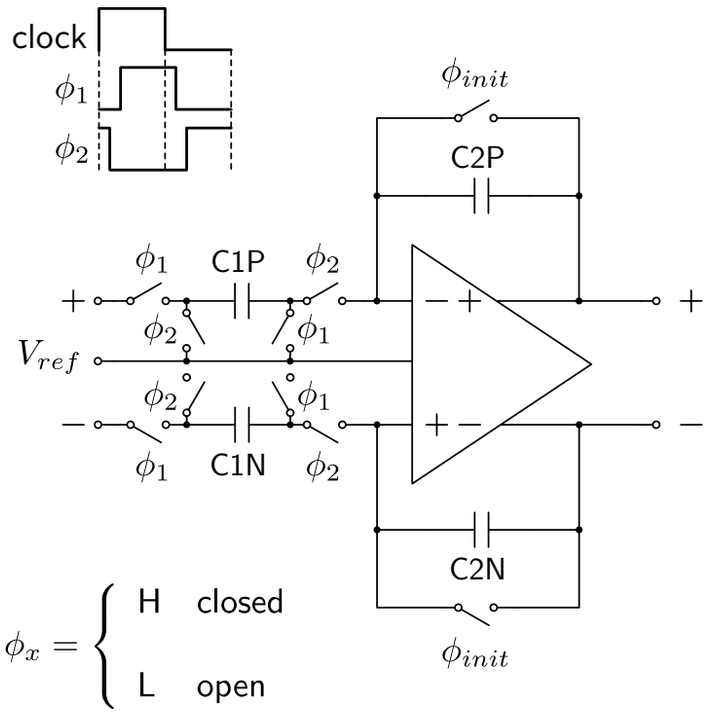
▲ **Technology** compensation

▼ Gain **non-linearity**

Discrete-Time CMFB

- Switched-capacitor (**SC**) implementation:

e.g. fully-differential **integrator** stage



Discrete-Time CMFB

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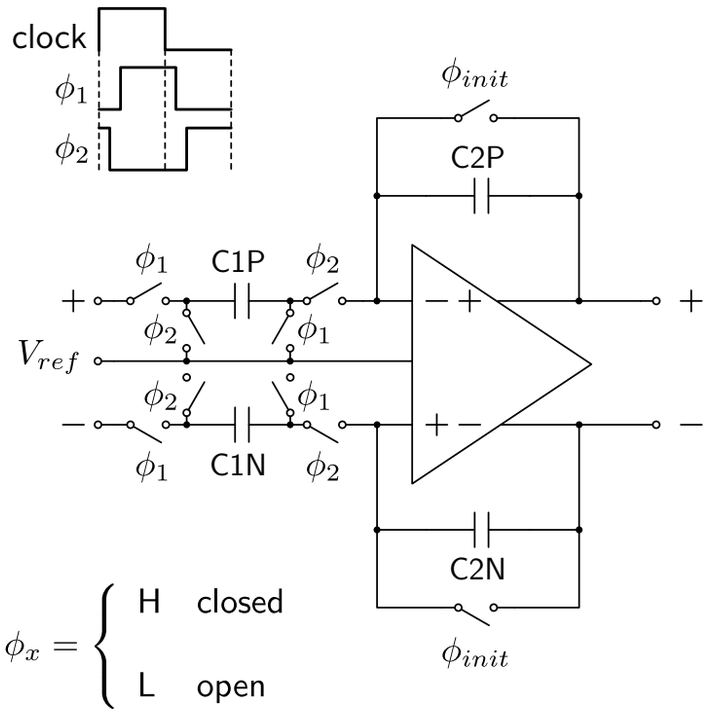
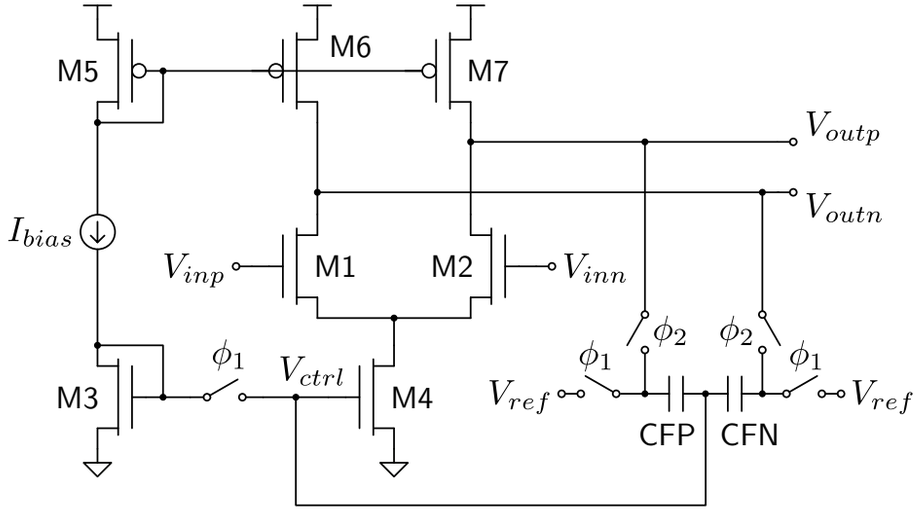


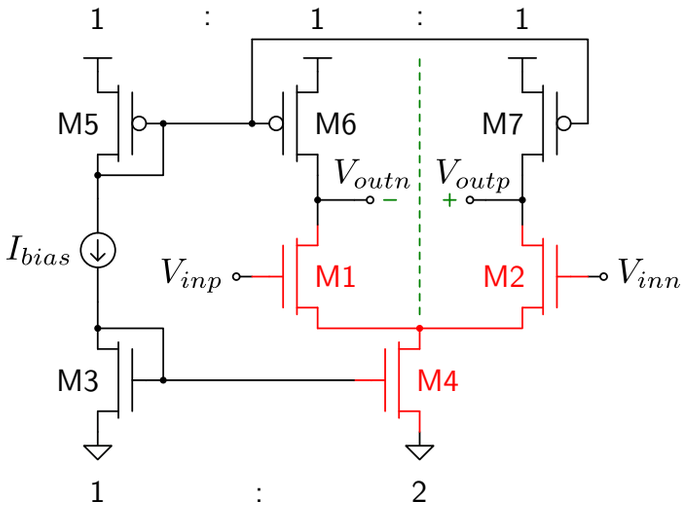


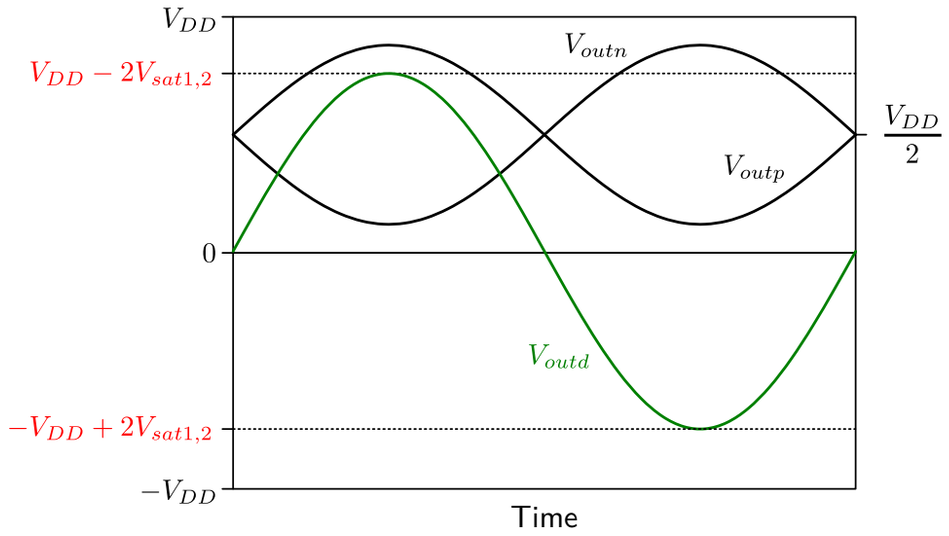
- **Capacitive** CMFB sensing
- ▲ Reduced **power** overheads
- ▼ Low loop-**gain**

Output Range Issue

- **Basic** fully-differential topology (not showing CMFB):

$$V_{outd} \doteq V_{outp} - V_{outn}$$



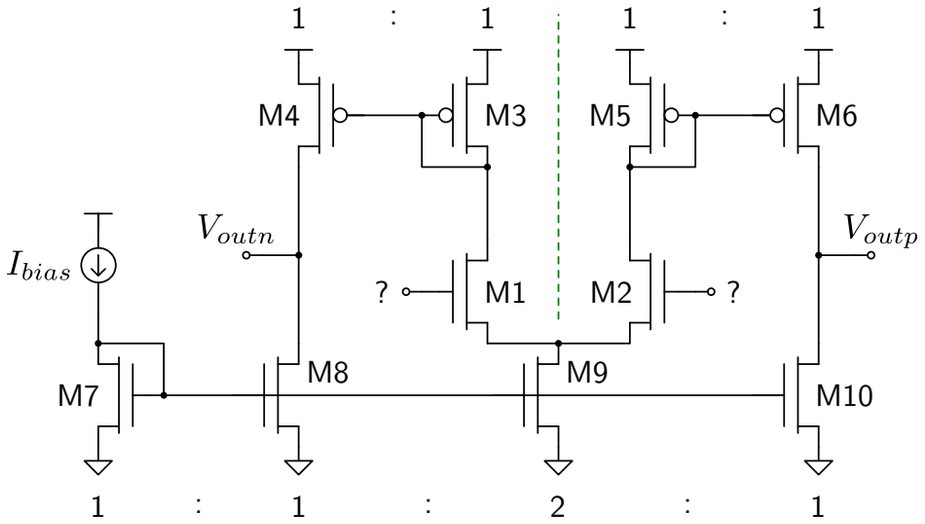


- **OR** improvement requires very large aspect ratios!
- Not compatible with other optimization rules (e.g. **CMRR**)

$$OR = 2V_{DD} - 4\sqrt{\frac{2I_{bias}}{n\beta_{un}}}\left[\sqrt{\left(\frac{L}{W}\right)_{1,2}} + \sqrt{2\left(\frac{L}{W}\right)_{4}}\right] \uparrow \qquad \left(\frac{W}{L}\right)_{1,2} \uparrow \quad \left(\frac{W}{L}\right)_{4} \uparrow$$

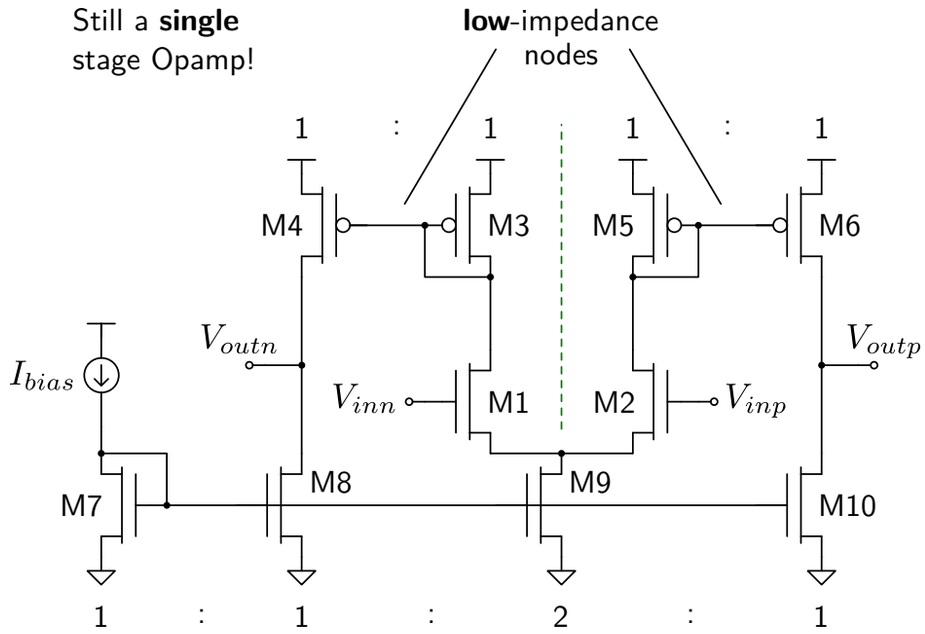
Folded Topologies

- Fully-differential **folded** OpAmp (not showing CMFB):



Folded Topologies

- Fully-differential **folded** OpAmp (not showing CMFB):



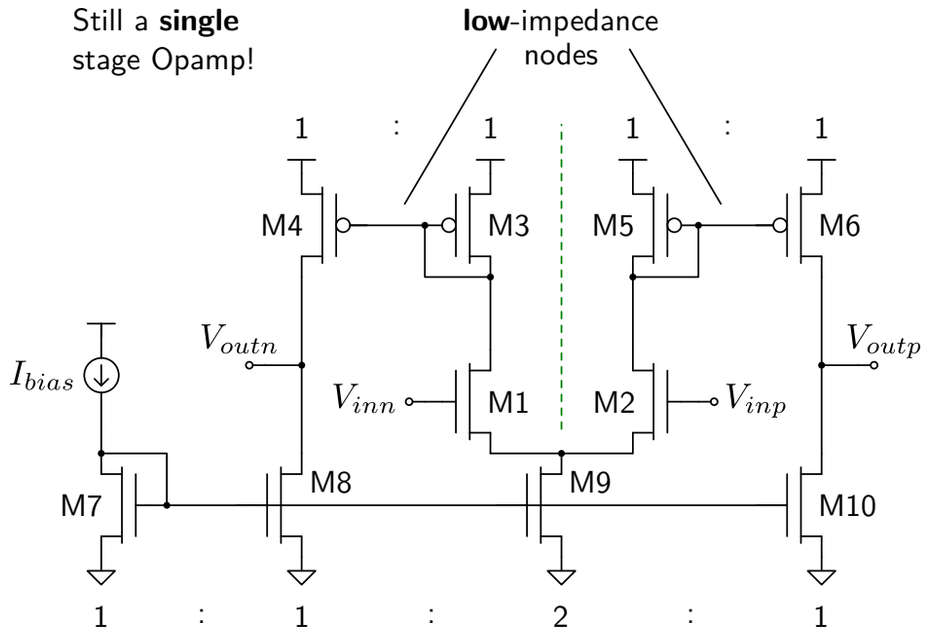
All operating in strong inversion saturation + neglecting CLM

- Static **power** consumption (x2)
- Device silicon **area** (x2)

Folded Topologies

- Fully-differential **folded** OpAmp (not showing CMFB):

All operating in strong inversion
saturation + neglecting CLM



$$V_{sat10} < V_{outp} < V_{DD} - V_{sat6}$$

$$V_{sat10} = \sqrt{\frac{2I_{bias}}{n\beta_{10}}} \qquad V_{sat6} = \sqrt{\frac{2I_{bias}}{n\beta_{6}}}$$

$$V_{outd} \doteq V_{outp} - V_{outn}$$

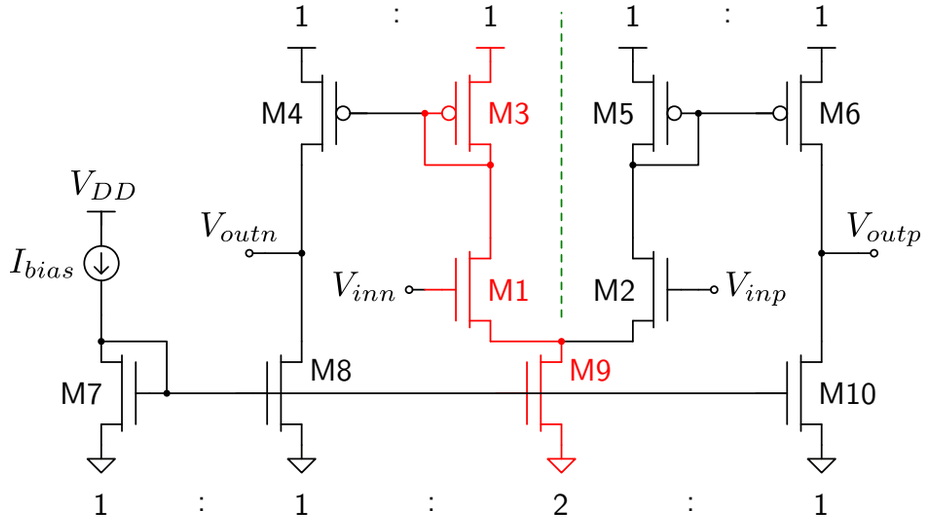
$$OR = 2V_{DD} - 4\sqrt{\frac{2I_{bias}}{n\,min\left(\beta_{un}\left(\frac{W}{L}\right)_{8,10}, \beta_{up}\left(\frac{W}{L}\right)_{4,6}\right)}}$$

- ▼ Static **power** consumption (x2)
- ▼ Device silicon **area** (x2)
- ▲ Full-scale **OR** optimization

Folded Topologies

All operating in strong inversion
saturation + neglecting CLM

- Fully-differential **folded** OpAmp (not showing CMFB):



$$V_{DD} > |V_{GB3,5}| + V_{sat1,2}$$

$$\sqrt{\frac{2I_{bias}}{n\beta_{un}}}\left[\sqrt{\left(\frac{L}{W}\right)_{1,2}}+\sqrt{2\left(\frac{L}{W}\right)_{9}}\right]$$

$$I_{bias} = \frac{\beta_{3,5}}{2n}\left(|V_{GB3,5}| - |V_{THP}|\right)^2$$

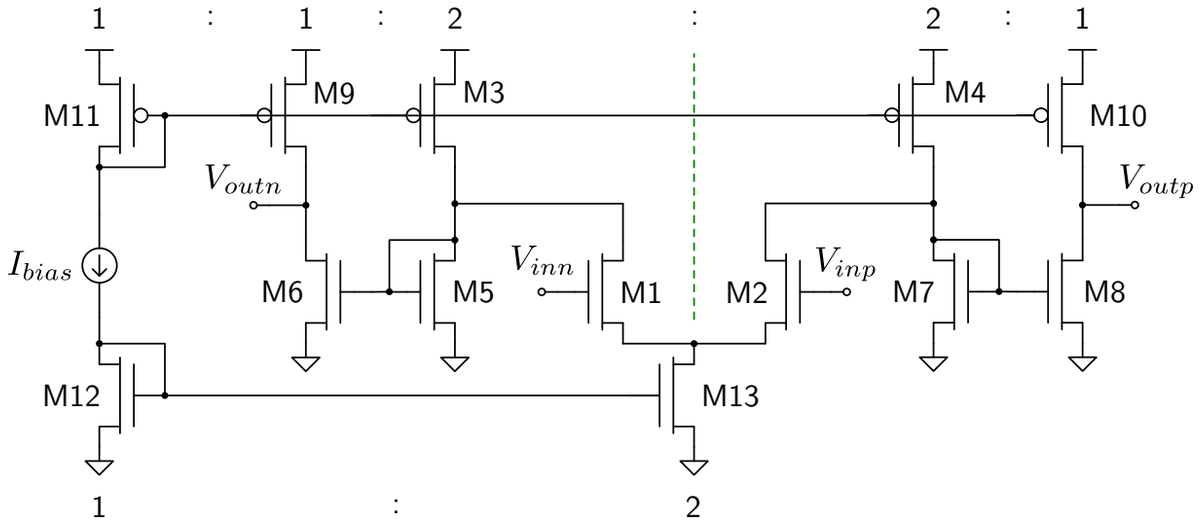
$$V_{DD} \geq |V_{THP}| + \sqrt{\frac{2nI_{bias}}{\beta_{up}}\left(\frac{L}{W}\right)_{3,5}} + \sqrt{\frac{2I_{bias}}{n\beta_{un}}}\left[\sqrt{\left(\frac{L}{W}\right)_{1,2}}+\sqrt{2\left(\frac{L}{W}\right)_{9}}\right]$$

$V_{DDmin} \simeq$ 1 threshold + 3 saturation voltages

- ▼ Static **power** consumption (x2)
- ▼ Device silicon **area** (x2)
- ▲ Full-scale **OR** optimization
- ▼ High **supply voltage** needed...

Folded Topologies

- Fully-differential **dual folded** OpAmp (not showing CMFB):

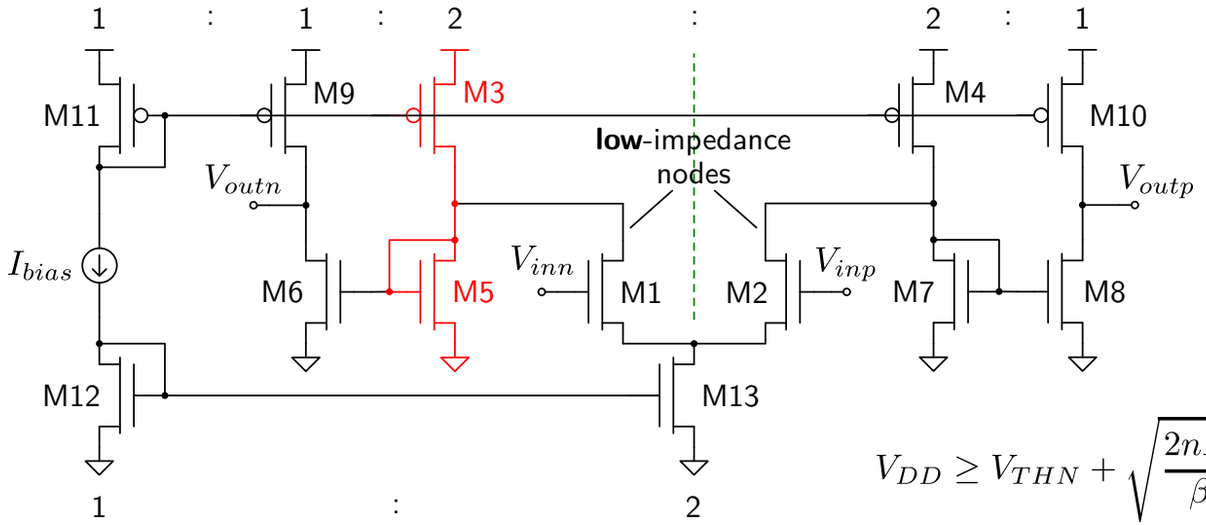


- Static **power** consumption (x3)
- Device silicon **area** (x3)

Folded Topologies

All operating in strong inversion
saturation + neglecting CLM

- Fully-differential **dual folded** OpAmp (not showing CMFB):



Still a **single** stage Opamp!

Suposing: $V_{GB5,7} \geq V_{sat1,2}$

$$V_{DD} \geq V_{GB5,7} + V_{sat3,4}$$

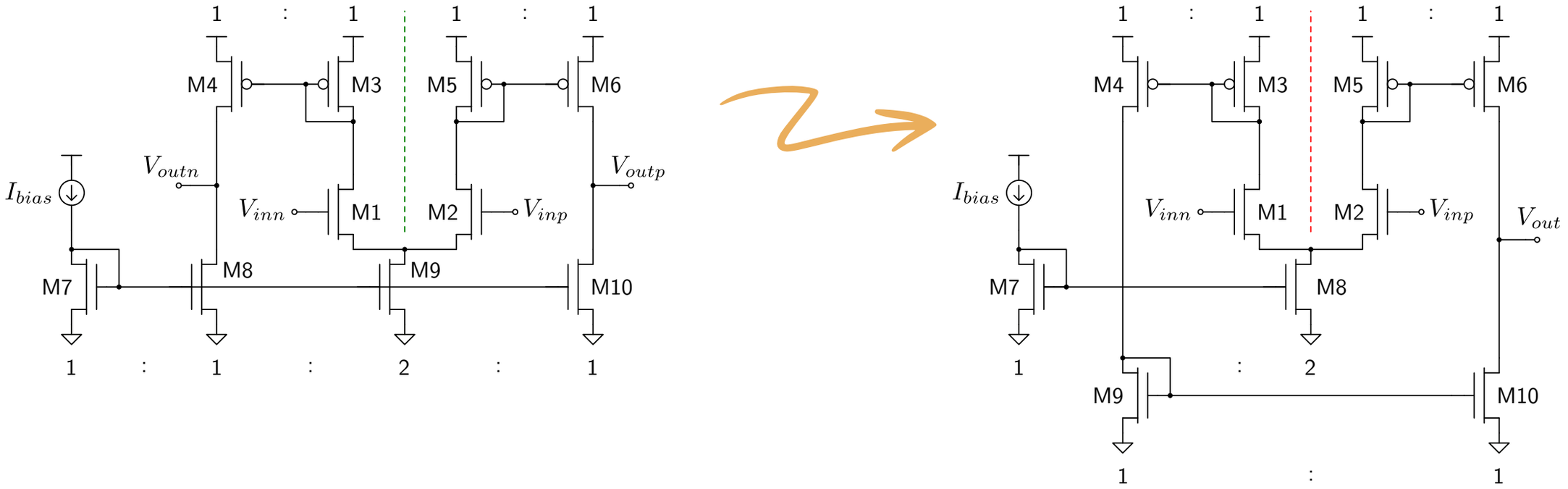
$$V_{DD} \geq V_{THN} + \sqrt{\frac{2nI_{bias}}{\beta_{un}}\left(\frac{L}{W}\right)_{5,7}} + \sqrt{\frac{2I_{bias}}{n\beta_{up}}\left(\frac{L}{W}\right)_{3,4}}$$

$V_{DDmin} \simeq$ 1 threshold + 2 saturation voltages

- ▼ Static **power** consumption (x3)
- ▼ Device silicon **area** (x3)
- ▲ Same **OR** optimization
- ▲ Compatible with low **supply voltage**

Folded Topologies

- **Single-ended folded** OpAmp counterparts:



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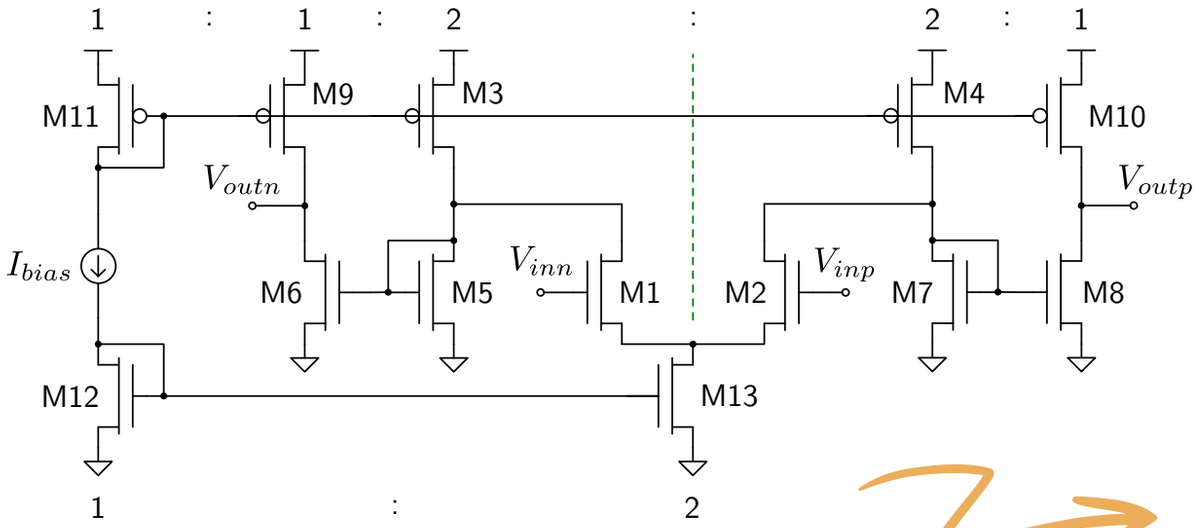
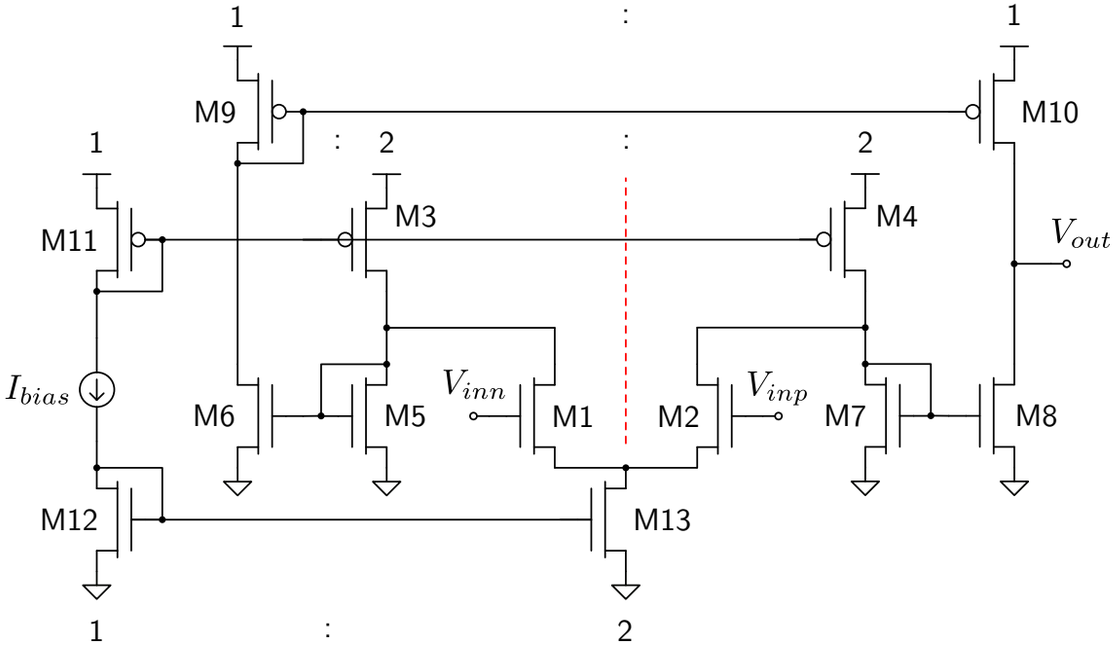
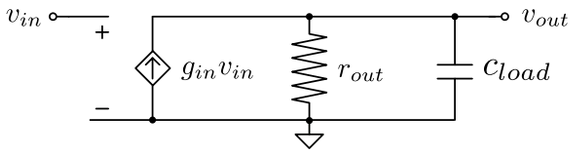




Principle Basis

- CMOS OpAmp general **linear model**:



$$|G(DC)| = g_{in} r_{out}$$

input **transconductance** $v \rightarrow i$

output **resistance** $i \rightarrow v$

$$g_{in} \propto \begin{cases} g_{mg} \\ g_{ms} \end{cases} \qquad r_{out} \propto \frac{1}{g_{md}}$$

- Enhancement by increasing MOSFET **output impedance**?

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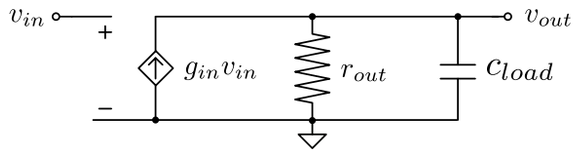

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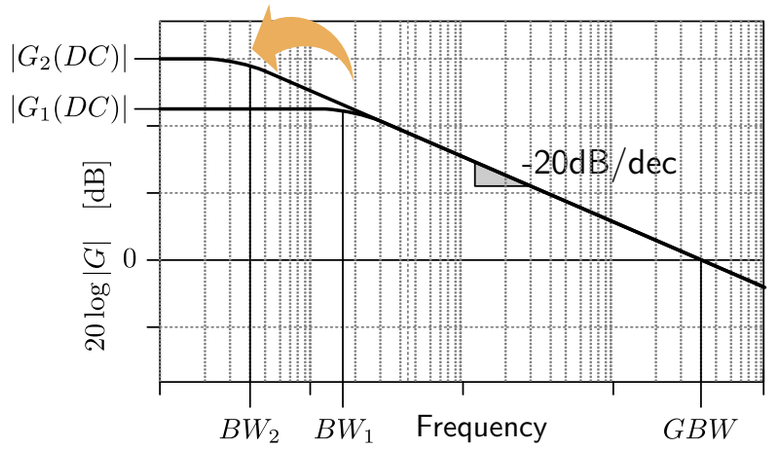


$$BW = \frac{1}{2\pi r_{out} c_{load}} \qquad GBW = \frac{g_{in}}{2\pi c_{load}}$$

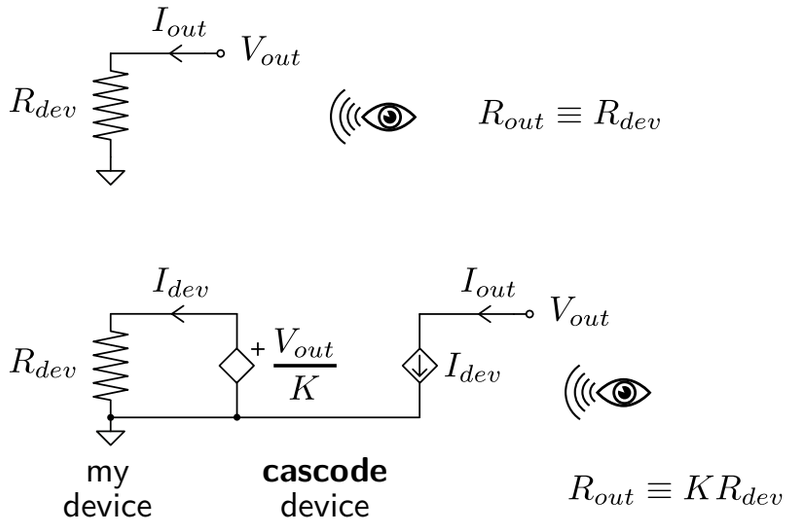
▲ **Gain** improvement:

- Accurate **feedback** functions
- Lower equivalent input **noise**

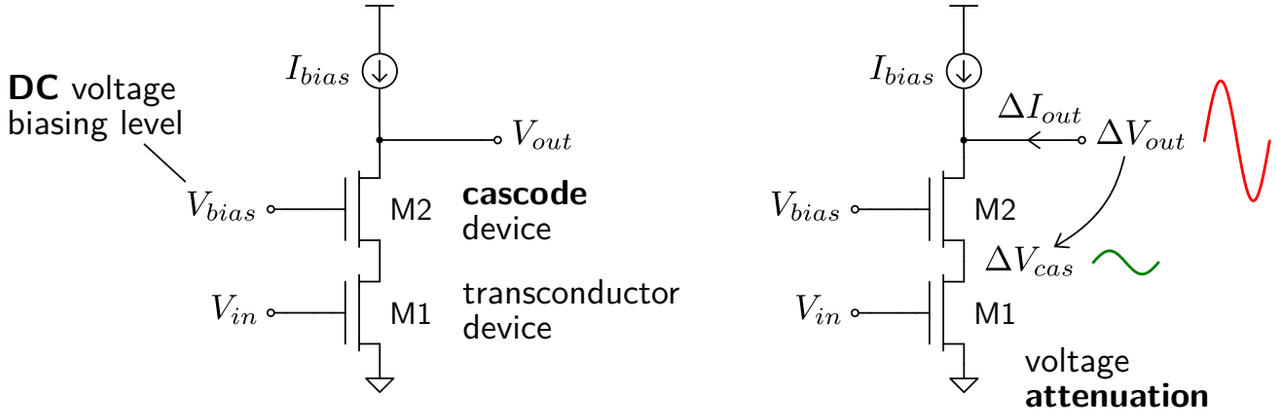
▼ No **speed** enhancement (GBW)

Principle of Operation

- Output impedance **multiplier**:



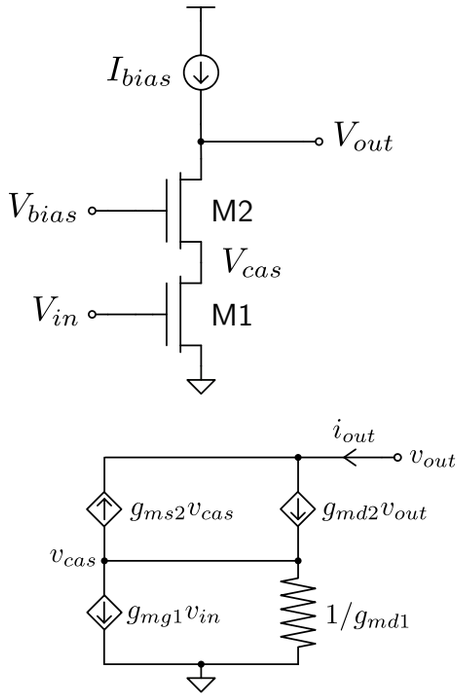
- Introducing cascoding in **OpAmps**:



- Aplicable to most analog basic building **blocks** (e.g. current mirror, voltage differential pair...)

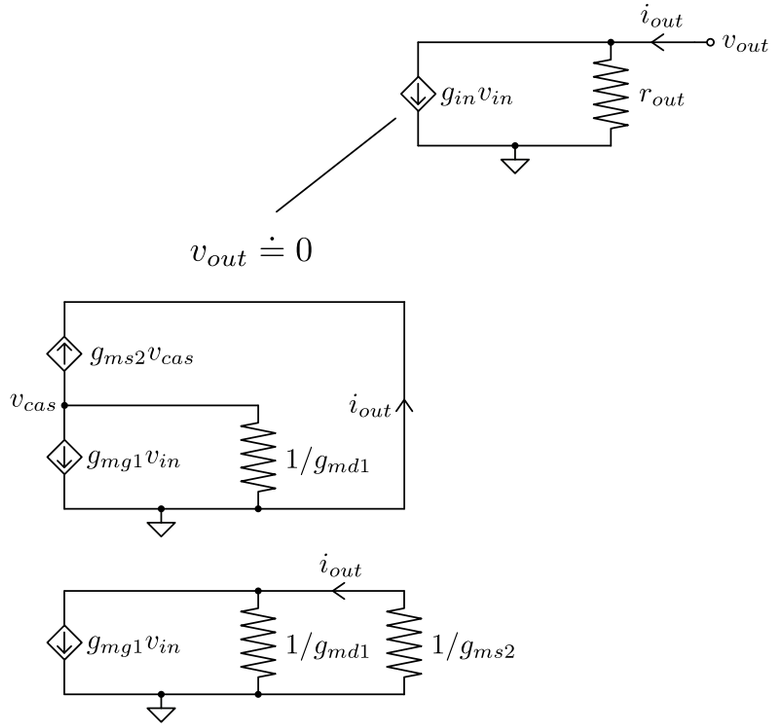
Basic Cascode OpAmp

- Low-frequency **small-signal** analysis:



$$\begin{cases} i_{out} = g_{md2}v_{out} - g_{ms2}v_{cas} \\ g_{md1}v_{cas} = i_{out} - g_{mg1}v_{in} \end{cases}$$

- CMOS OpAmp **model**:



$$g_{in} \doteq \frac{i_{out}}{v_{in}} = g_{mg1}\frac{g_{ms2}}{g_{ms2} + g_{md1}}$$

Basic Cascode OpAmp

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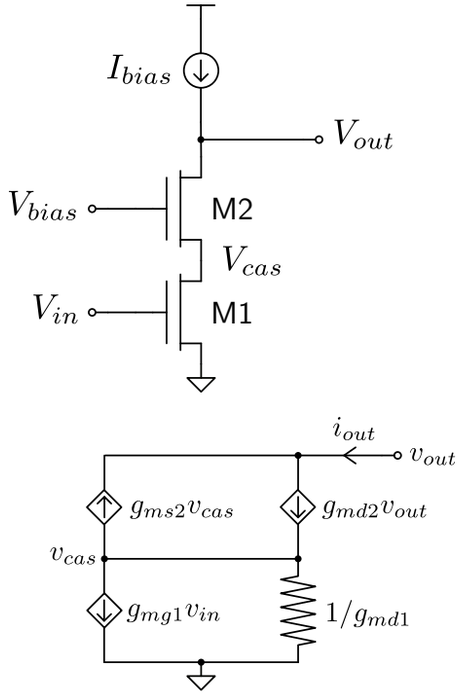

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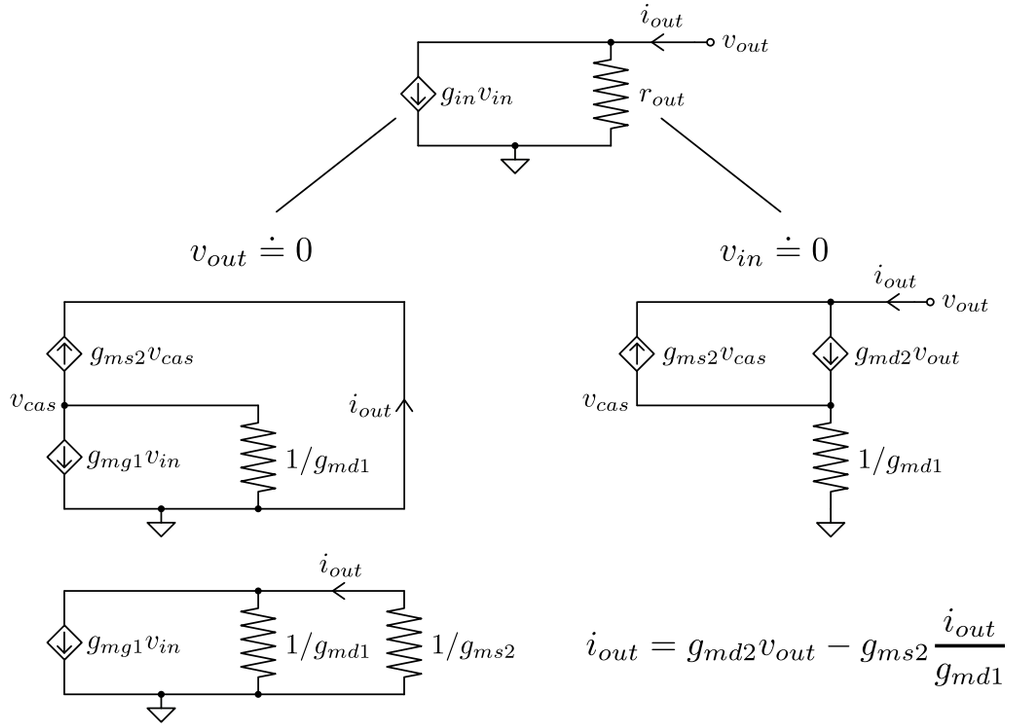
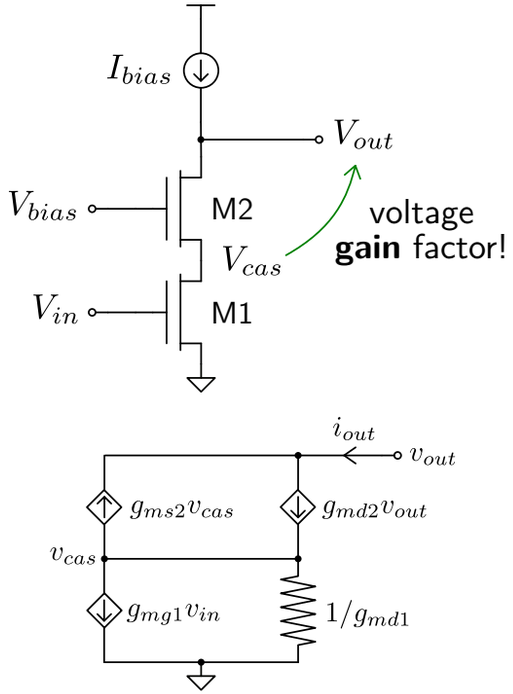


$$i_{out} = g_{md2}v_{out} - g_{ms2}\frac{i_{out}}{g_{md1}}$$

$$g_{in} \doteq \frac{i_{out}}{v_{in}} = g_{mg1}\frac{g_{ms2}}{g_{ms2}+g_{md1}} \qquad r_{out} \doteq \frac{v_{out}}{i_{out}} = \frac{1}{g_{md2}} + \frac{1}{g_{md1}}\frac{g_{ms2}}{g_{md2}}$$

Basic Cascode OpAmp

- Low-frequency **small-signal** analysis:



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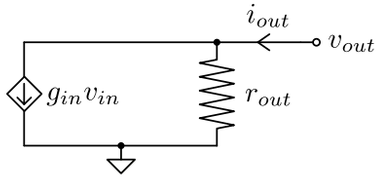


$$g_{in} = g_{mg1}\frac{g_{ms2}}{g_{ms2}+g_{md1}} \simeq g_{mg1}$$

similar
transconductance

$$r_{out} = \frac{1}{g_{md2}} + \frac{1}{g_{md1}}\frac{g_{ms2}}{g_{md2}}$$

series combination

voltage **gain** factor!

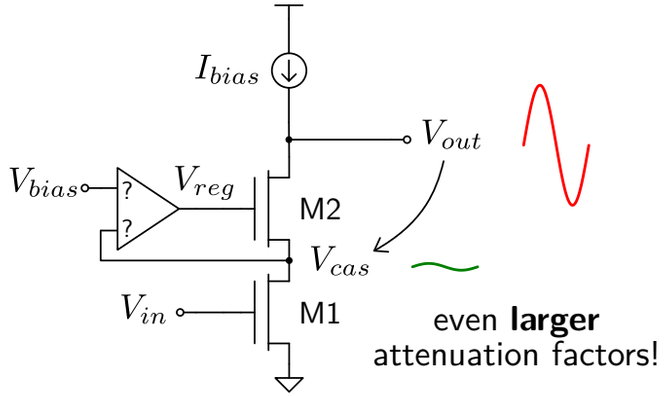
higher
output impedance

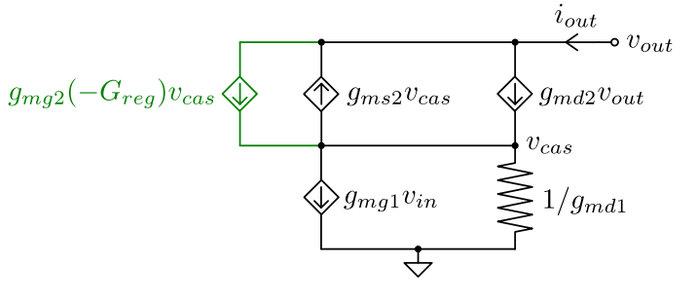
output impedance of **cascode** device

output impedance of **transconductor** device

Regulated Cascode OpAmp

- Low-frequency **small-signal** analysis:





Regulated Cascode OpAmp

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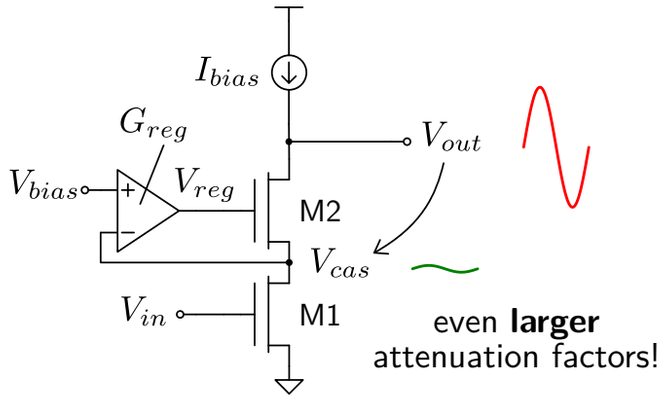
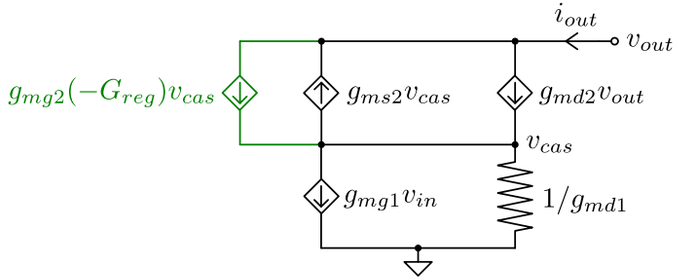
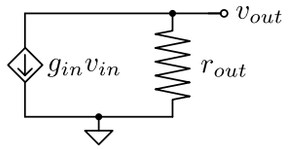




- CMOS OpAmp **model**:



$$g_{in} = g_{mg1}\frac{g_{ms2}+g_{mg2}G_{reg}}{g_{ms2}+g_{mg2}G_{reg}+g_{md1}} \simeq g_{mg1}$$

$$r_{out} = \frac{1}{g_{md2}} + \frac{1}{g_{md1}}\frac{g_{ms2}+g_{mg2}G_{reg}}{g_{md2}} \simeq \frac{1}{g_{md1}}\frac{g_{mg2}}{g_{md2}}G_{reg}$$

Regulated Cascode OpAmp

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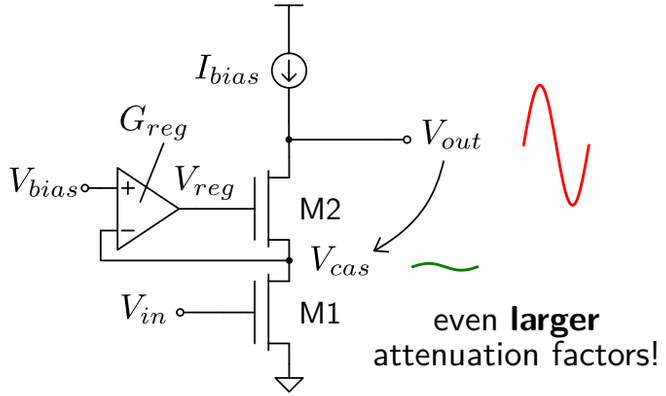

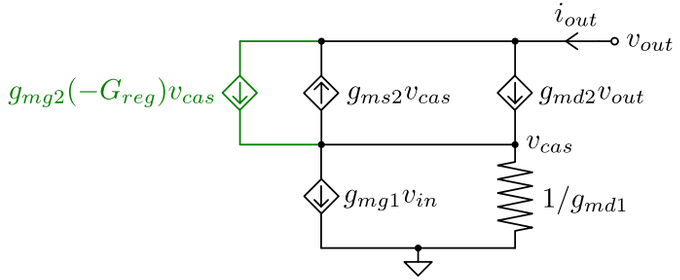

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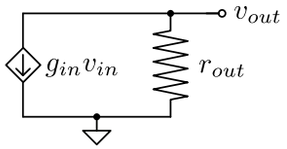
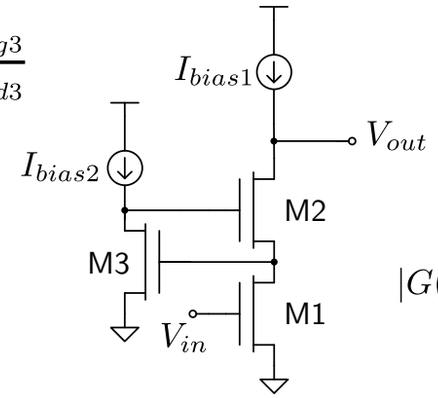


$$g_{in} = g_{mg1}\frac{g_{ms2}+g_{mg2}G_{reg}}{g_{ms2}+g_{mg2}G_{reg}+g_{md1}} \simeq g_{mg1}$$

$$r_{out} = \frac{1}{g_{md2}} + \frac{1}{g_{md1}}\frac{g_{ms2}+g_{mg2}G_{reg}}{g_{md2}} \simeq \frac{1}{g_{md1}}\frac{g_{mg2}}{g_{md2}}G_{reg}$$

- **Minimalist** implementation:

$$G_{reg} \equiv \frac{g_{mg3}}{g_{md3}}$$

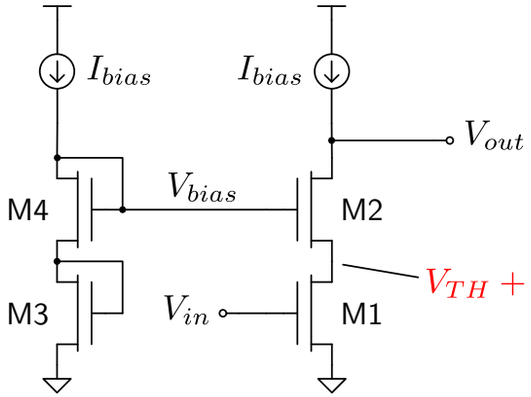


$$|G(DC)| \simeq \frac{g_{mg1}}{g_{md1}}\frac{g_{mg2}}{g_{md2}}\frac{g_{mg3}}{g_{md3}}$$

Output Range Optimization

All operating in strong inversion
saturation + neglecting CLM

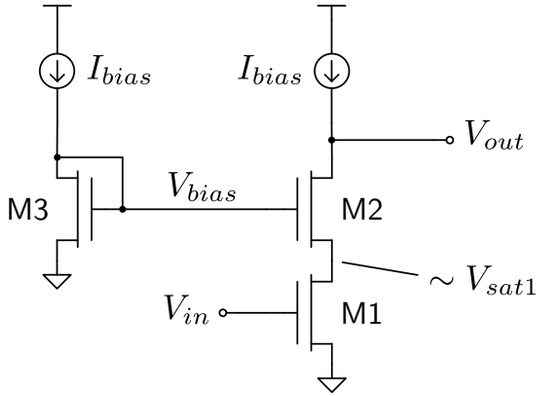
- **Basic** cascode DC biasing:



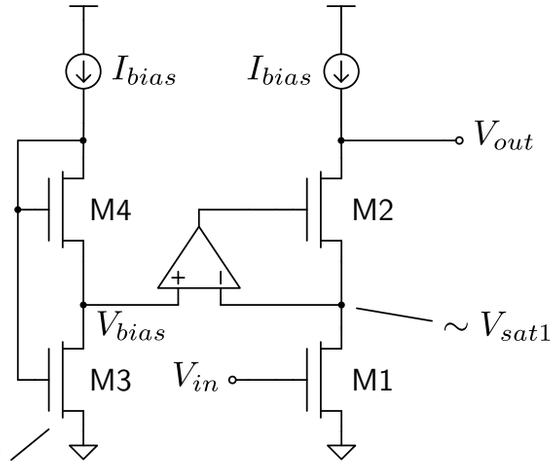
supposing M2=M4:

$$V_{TH} + \sqrt{\frac{2nI_{bias}}{\beta_{un}\left(\frac{W}{L}\right)_3}} \gg V_{sat1}$$

alternative **low-voltage** approach:



- **Regulated** cascode DC biasing:



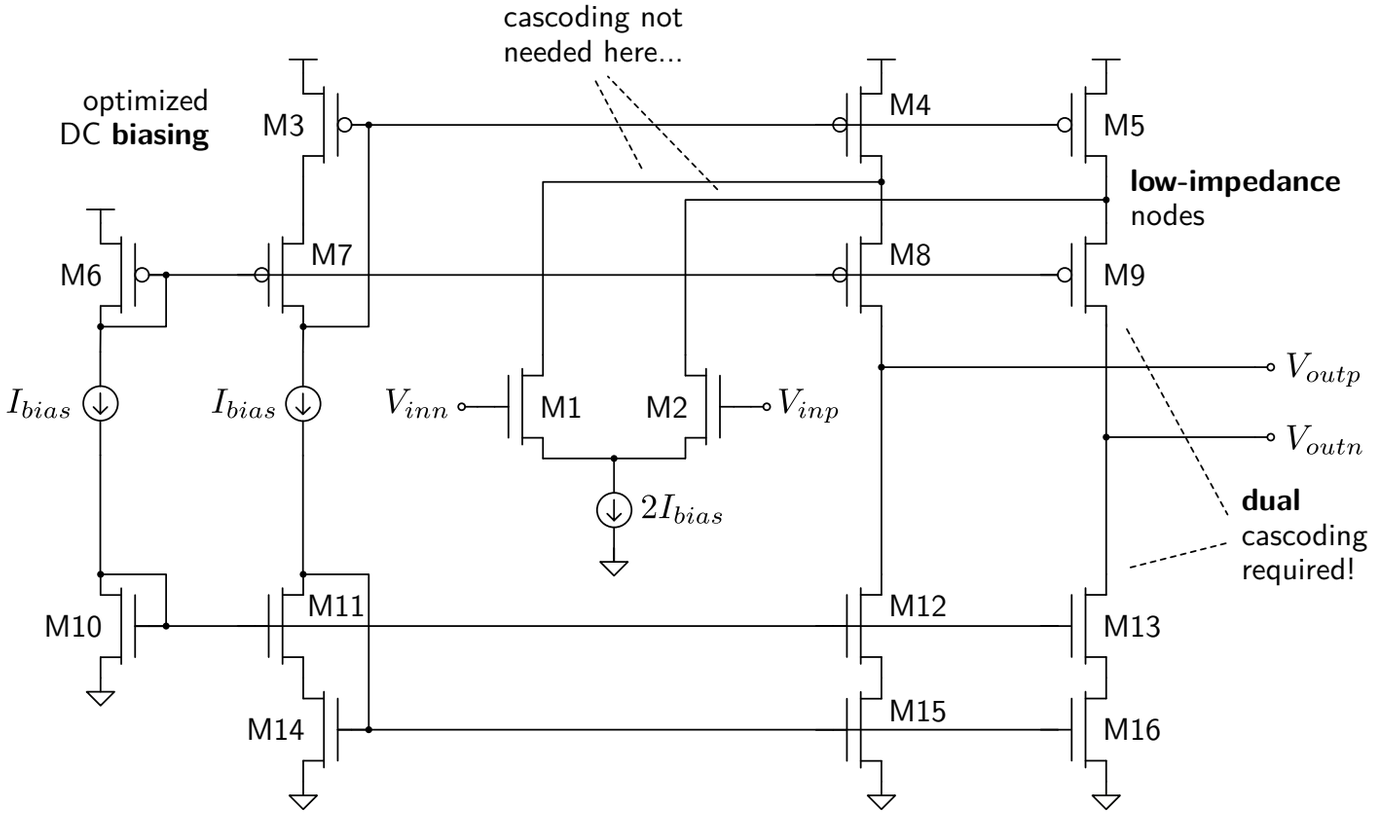
$$\begin{cases} I_{bias} = \beta_3 \left(V_{GB3,4} - V_{TH} + \frac{n}{2}V_{bias}\right) V_{bias} \\ I_{bias} = \frac{\beta_4}{2n}\left(V_{GB3,4} - V_{TH} - nV_{bias}\right)^2 \end{cases}$$

$V_{bias} \equiv V_{sat1}$:

$$\sqrt{\frac{2}{(W/L)_4}} = \sqrt{\frac{1}{2(W/L)_3}\frac{(W/L)_1}{(W/L)_3}} - 3\sqrt{\frac{1}{2(W/L)_1}}$$

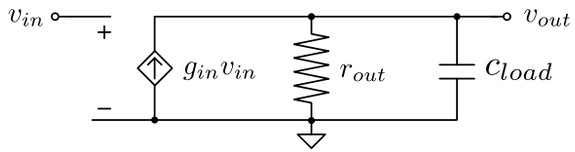
Practical Cascode OpAmps

- **Fully differential** + **folded** + **cascode** topology example:



Principle Basis

- CMOS OpAmp general **linear model**:



$$|G(DC)| = g_{in} r_{out}$$

input **transconductance** $v \rightarrow i$

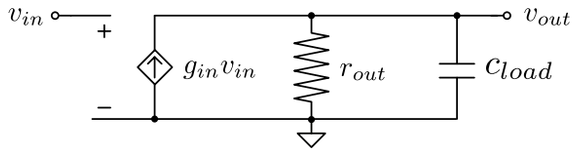
output **resistance** $i \rightarrow v$

$$g_{in} \propto \begin{cases} g_{mg} \\ g_{ms} \end{cases} \qquad r_{out} \propto \frac{1}{g_{md}}$$

- Enhancement by increasing MOSFET **input transconductance**?

Principle Basis

- CMOS OpAmp general **linear model**:



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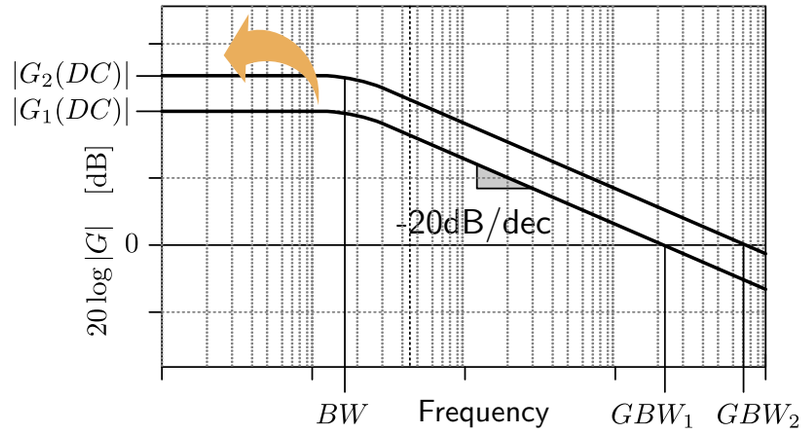
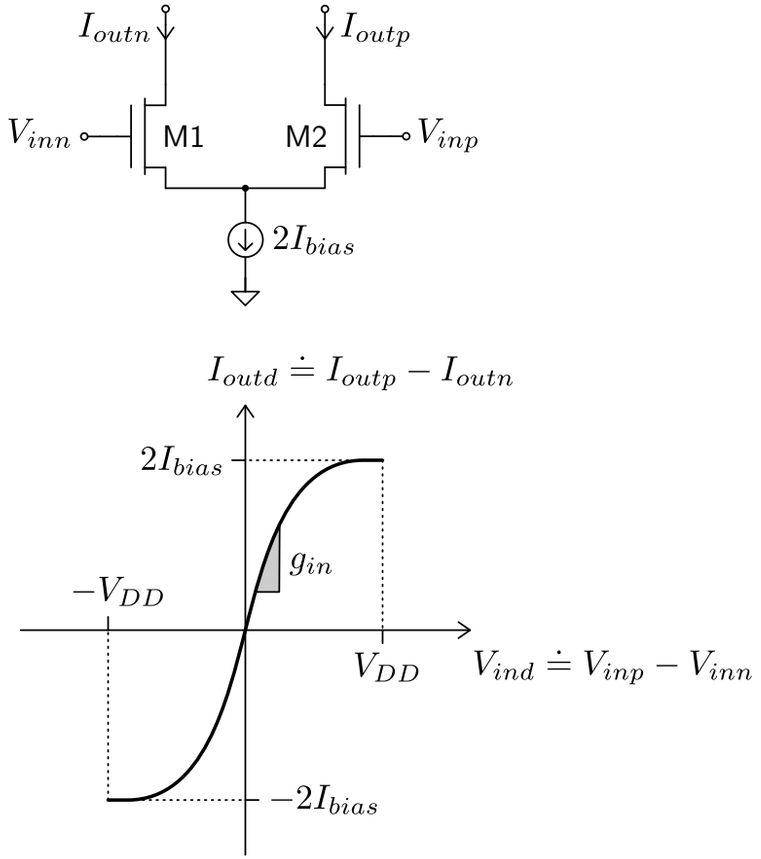


$$BW = \frac{1}{2\pi r_{out} c_{load}} \qquad GBW = \frac{g_{in}}{2\pi c_{load}}$$

- **Gain** improvement:
  - Accurate **feedback** functions
  - Lower equivalent input **noise**
- **Speed** enhancement (GBW)

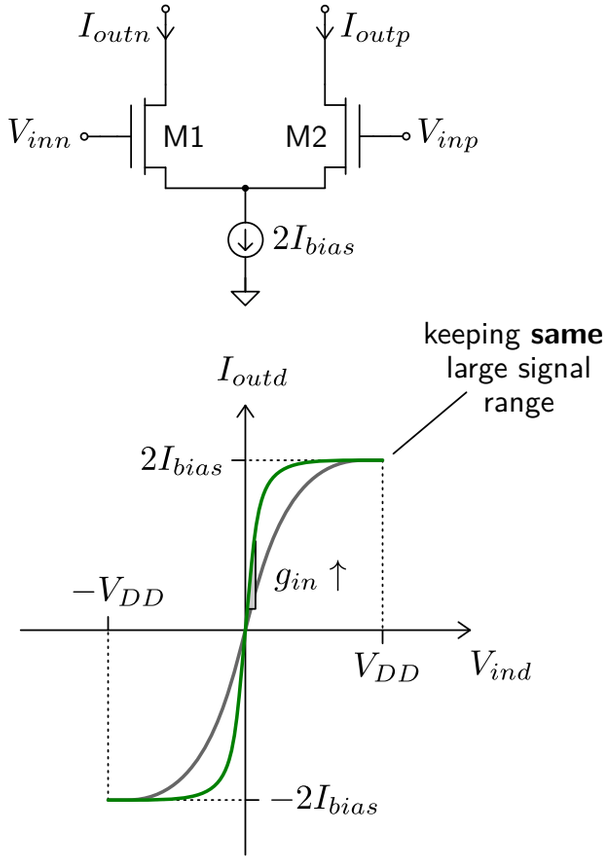
Partial Positive Feedback

- **Basic** differential transconductor:

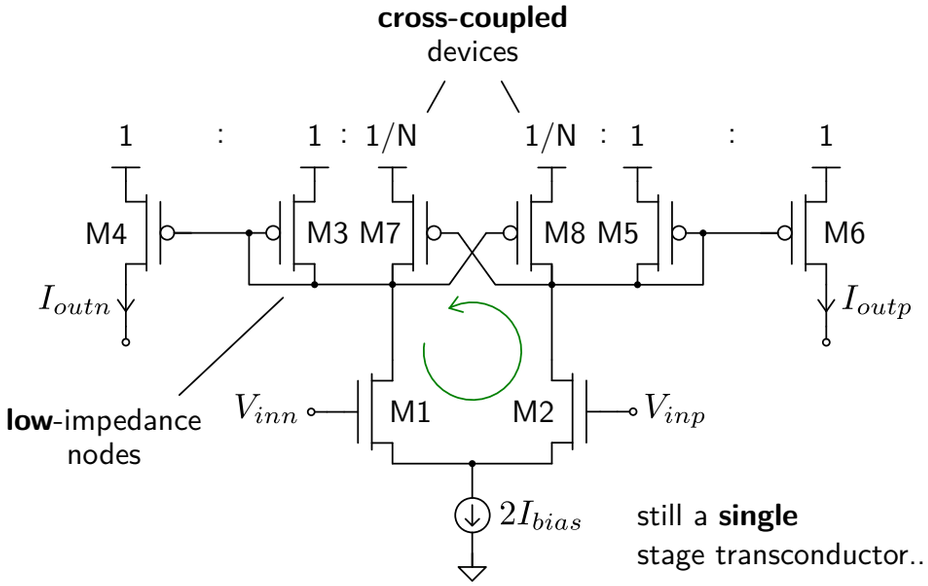


Partial Positive Feedback

- **Basic** differential transconductor:

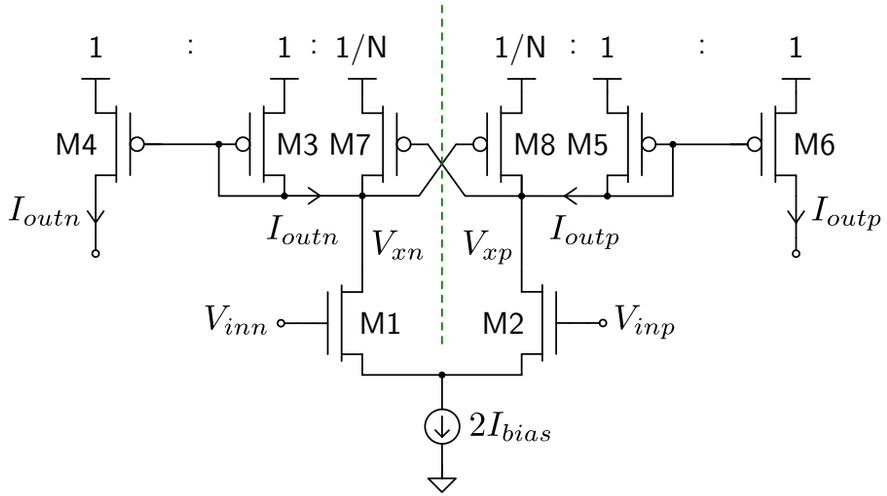


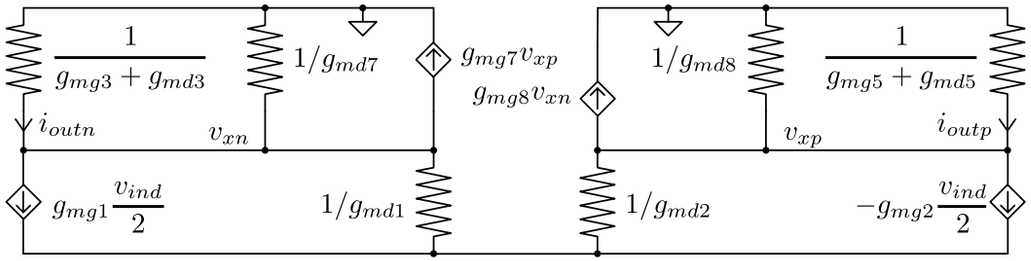
- Introducing **local positive** feedback:
  - **Folded** structure
  - **Cross**-coupled pair
  - **Partial** feedback design by sizing ratio



Partial Positive Feedback

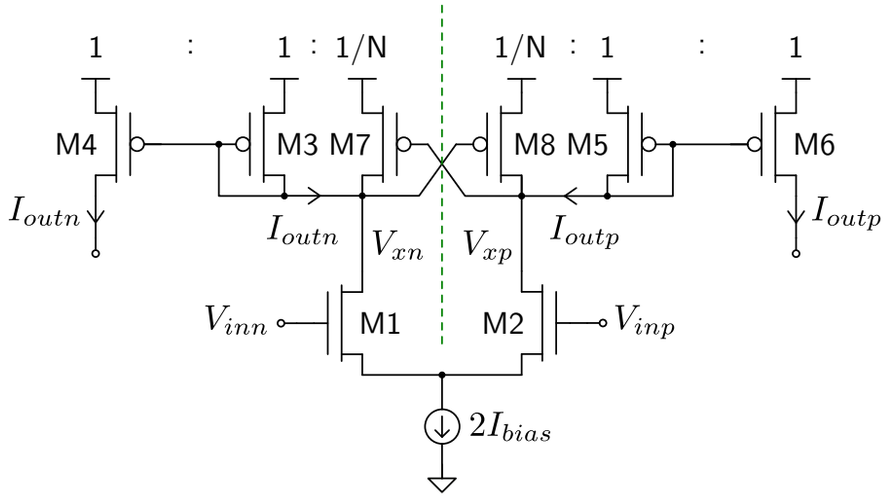
- Small signal **transconductance**:

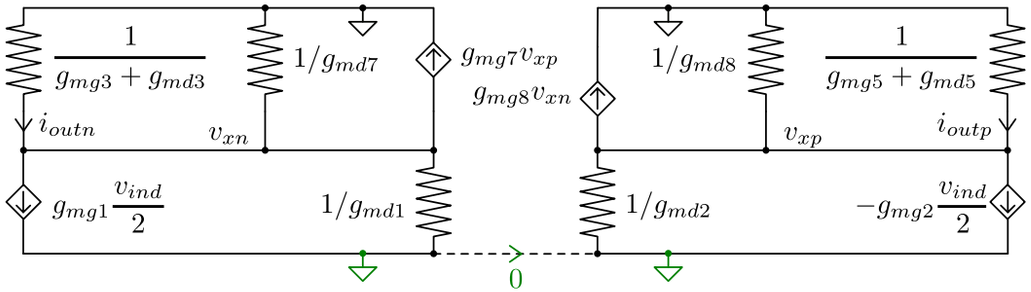




Partial Positive Feedback

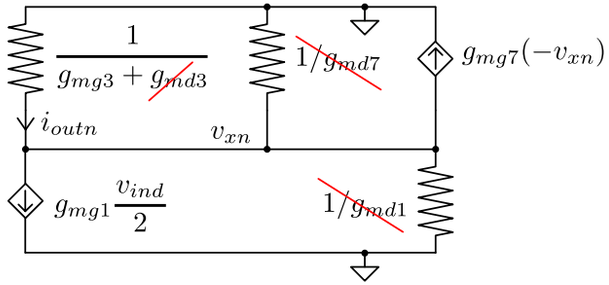
- Small signal **transconductance**:

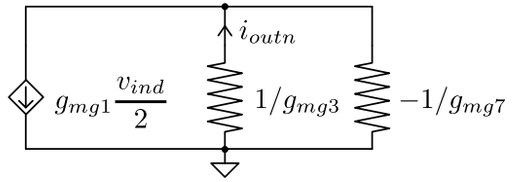




$i_{outn} \equiv -i_{outp}$ common-mode = **virtual ground** $v_{xn} \equiv -v_{xp}$

- **Half-circuit** analysis:
  - Perfect symmetry (no mismatching)
  - Infinite tail sink resistance
  - Purely differential input



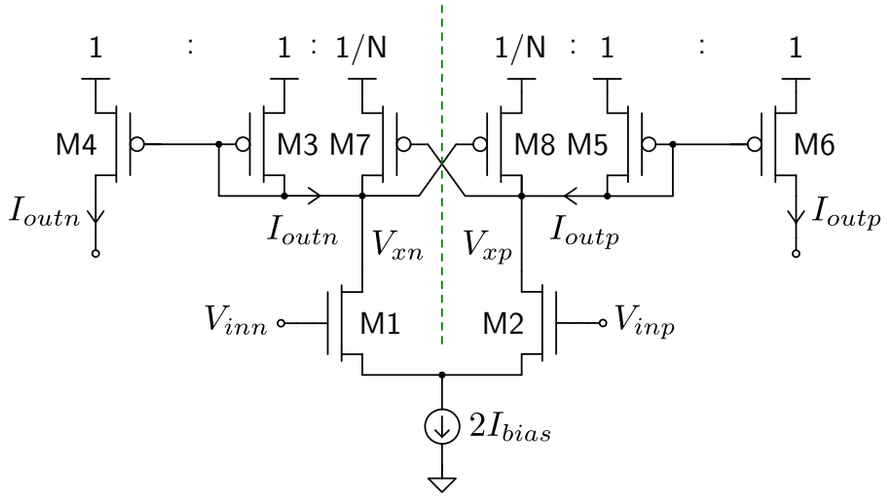


$$g_{inp} \doteq \frac{i_{outd}}{v_{ind}}$$

$$i_{outd} \doteq i_{outp} - i_{outn} \equiv |2i_{outn}|$$

Partial Positive Feedback

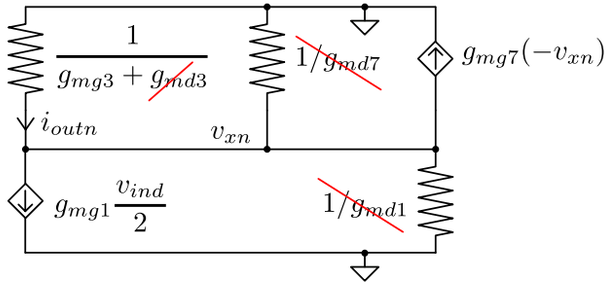
- Small signal **transconductance**:

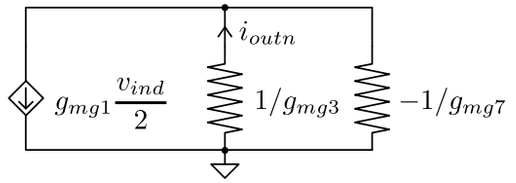


$$i_{outn} = g_{mg1}\frac{v_{ind}}{2}\frac{g_{mg3}}{g_{mg3} - g_{mg7}}$$

$$g_{inp} = g_{mg1,2}\frac{g_{mg3,5}}{g_{mg3,5} - g_{mg7,8}} \uparrow \begin{cases} g_{mg1,2} & N \gg 1 \\ \infty & N \equiv 1 \\ 0 & N \ll 1 \end{cases}$$

- **Half-circuit** analysis:
  - Perfect symmetry (no mismatching)
  - Infinite tail sink resistance
  - Purely differential input



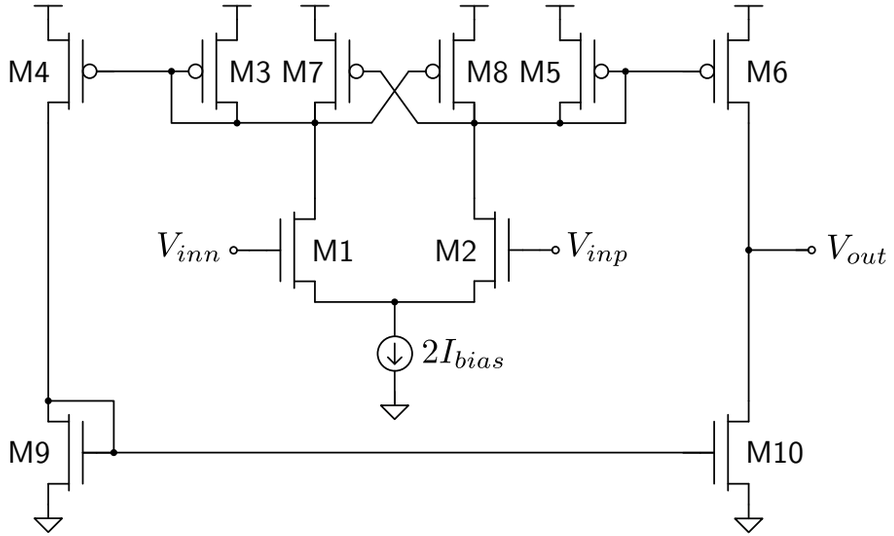


$$g_{inp} \doteq \frac{i_{outd}}{v_{ind}}$$

$$i_{outd} \doteq i_{outp} - i_{outn} \equiv |2i_{outn}|$$

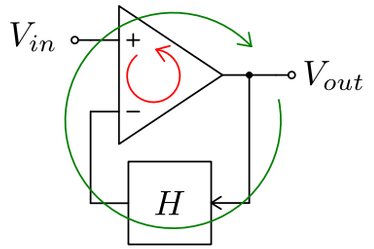
Practical Gain Enhanced OpAmp

- **Single-ended** + **folded** + **cross-coupled** example:

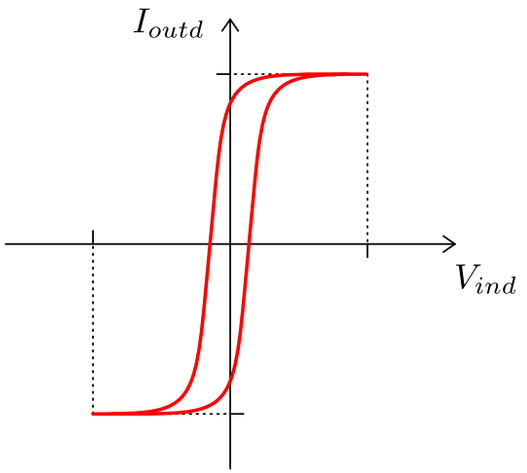


- ▲ Larger **gain** and **GBW**
- ▲ Compatible with **folding** and **cascoding**

Local **positive** feedback **vs** global **negative** feedback:

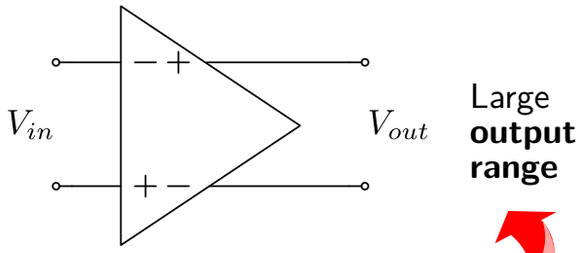


- ▼ Prone to **instability**
- ▼ It can generate **hysteresis**



Splitting Functions

- **Single** stage CMOS OpAmp limitations:



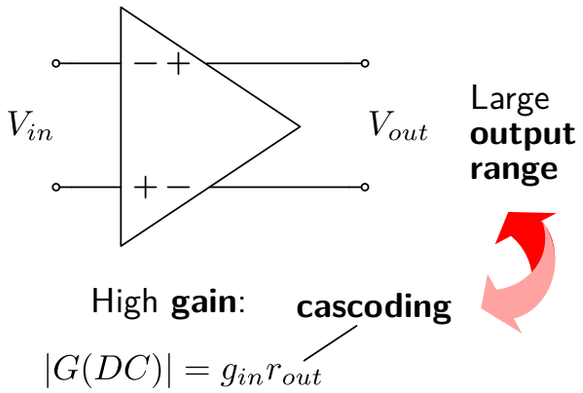
Large **output range**

High **gain**: **cascoding**

$$|G(DC)| = g_{in} r_{out}$$

Splitting Functions

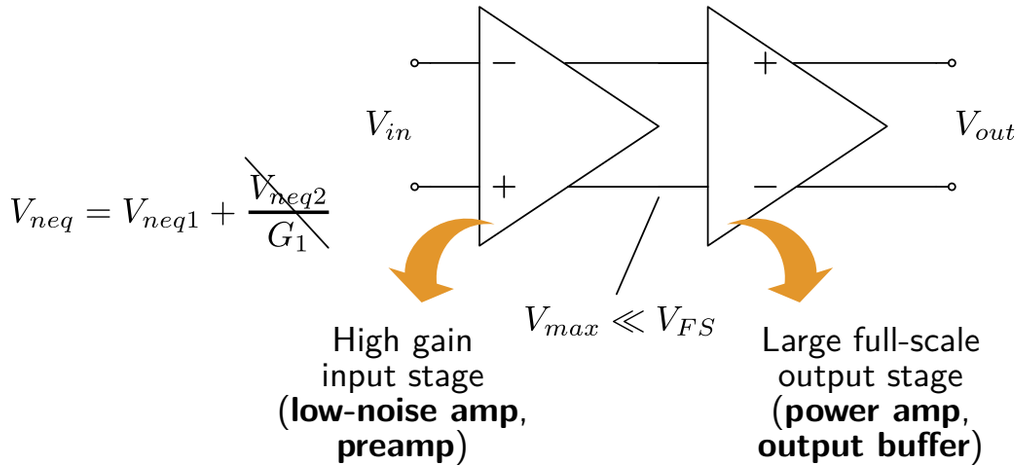
▼ **Single** stage CMOS OpAmp limitations:



▶ Introducing **two-stage** architectures:

$$G = G_1 G_2$$

$$|G_1(DC)| = g_{in1} r_{out1} \qquad |G_2(DC)| = g_{in2} r_{out2}$$



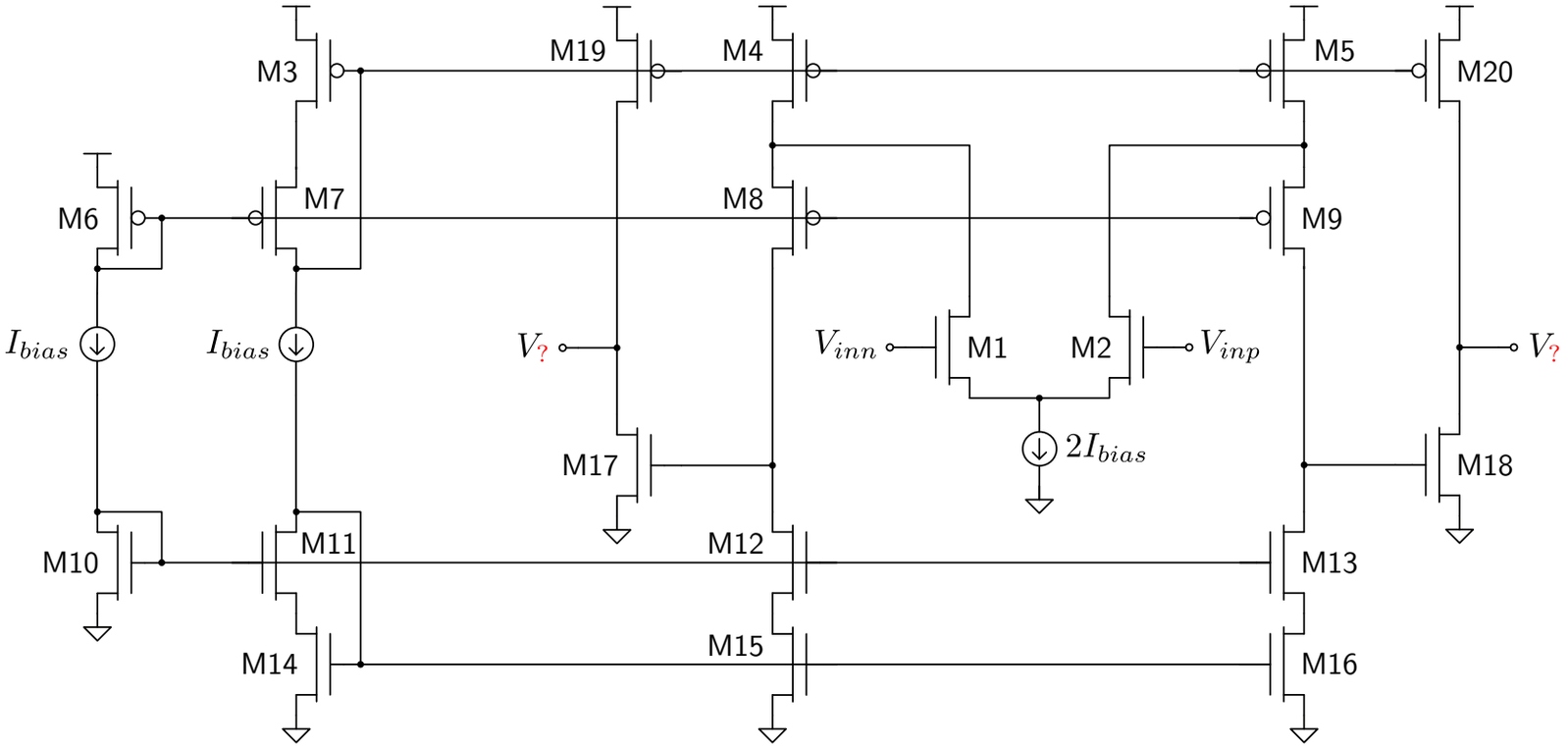
▲ Improved **dynamic range** performance

▼ **Area** and **power** overheads...

▼ **Frequency compensation** required!

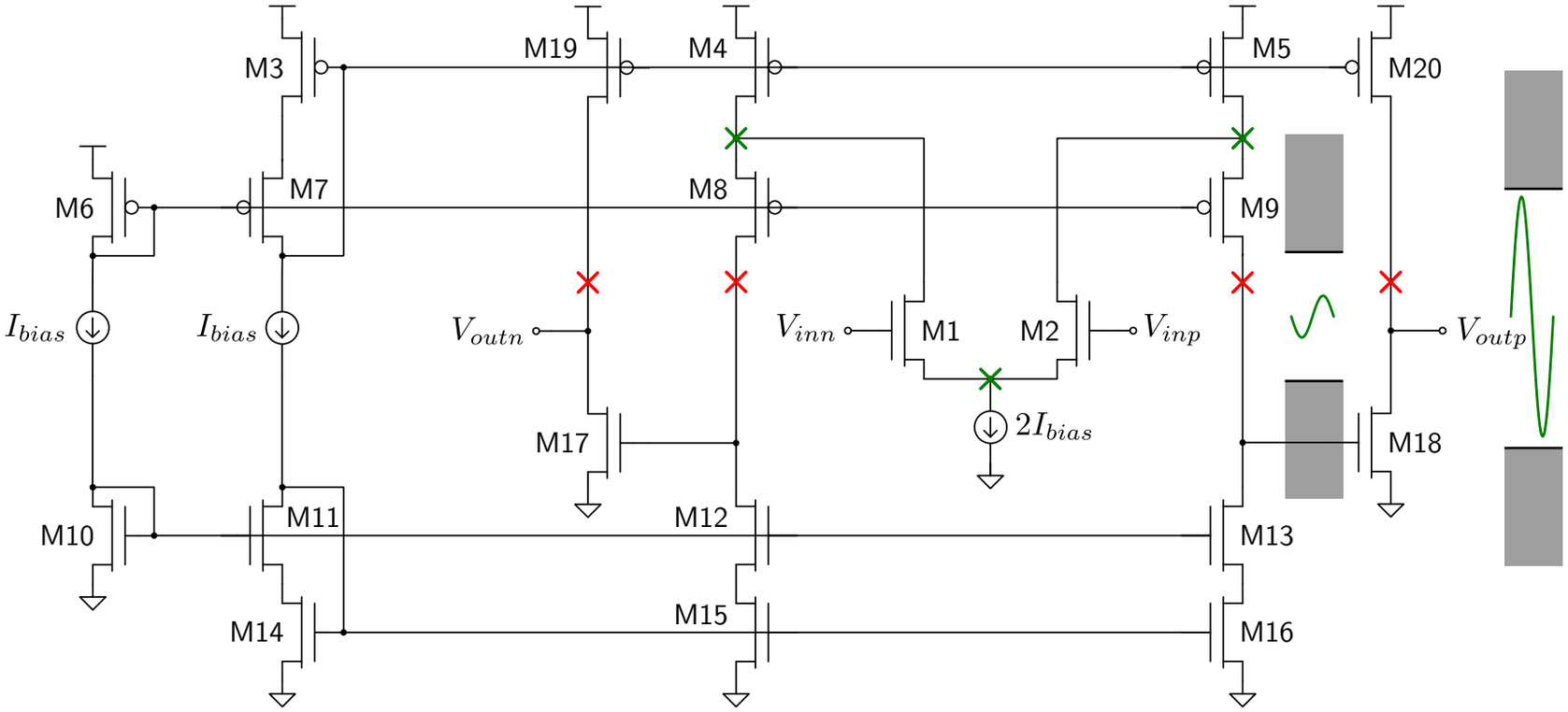
Practical Example

- **Two-stage** fully differential folded cascode OpAmp topology:



Practical Example

- **Two-stage** fully differential folded cascode OpAmp topology:

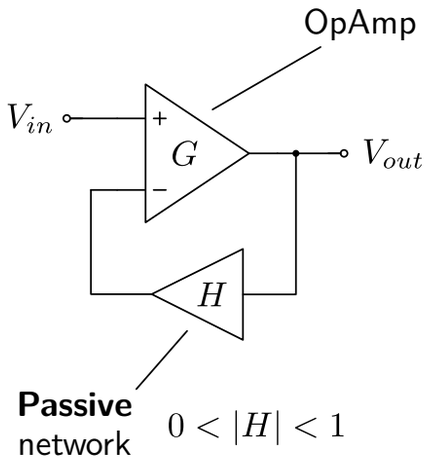


high-impedance nodes with dynamic signals

- Frequency compensation strategy is needed under **feedback** (closed loop) operation...

Single Stage OpAmp Case

- Basic **control** theory:



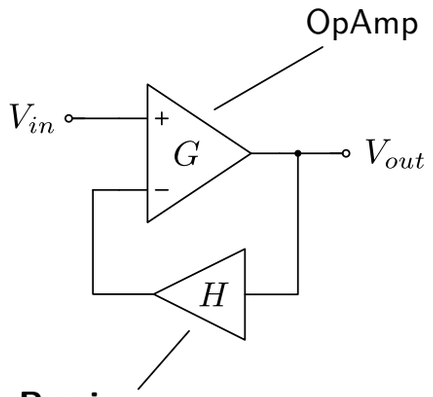
$$|H| = \begin{cases} 0 & \text{open loop} \\ 1 & \text{follower} \end{cases}$$

$$\frac{V_{out}}{V_{in}} = \frac{G}{1+GH} \simeq \frac{1}{H}$$

$G \to \infty$

Single Stage OpAmp Case

- Basic **control** theory:



$$|H| = \begin{cases} 0 & \text{open loop} \\ 1 & \text{follower} \end{cases}$$

$$\frac{V_{out}}{V_{in}} = \frac{G}{1+GH} \simeq \frac{1}{H} \quad (G \to \infty)$$

- **Single pole** amplifier:

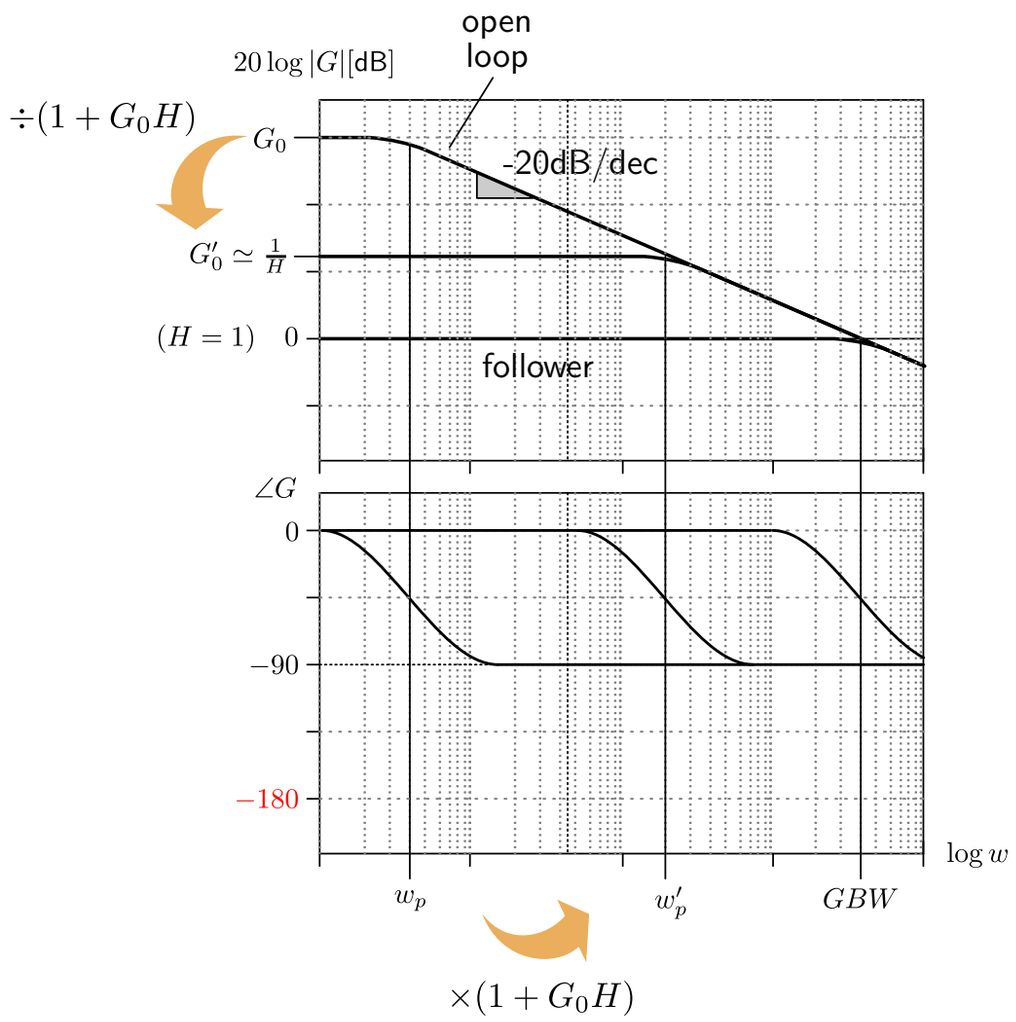
$$G(s) = \frac{G_0}{1+\frac{s}{w_p}}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{\frac{G_0}{1+\frac{s}{w_p}}}{1+\frac{G_0}{1+\frac{s}{w_p}}H} = \frac{G_0}{1+\frac{s}{w_p}+G_0H}$$

$$\frac{V_{out}}{V_{in}}(s) = \underbrace{\frac{G_0}{1+G_0H}}_{G_0'} \frac{1}{1+\underbrace{\frac{s}{w_p(1+G_0H)}}_{w_p'}}$$

$$\frac{G_0'}{G_0} = \frac{1}{1+G_0H} \qquad \frac{w_p'}{w_p} = 1+G_0H$$

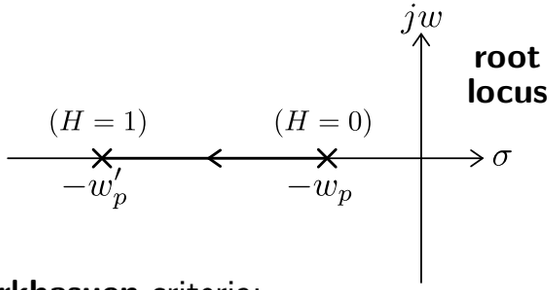
Single Stage OpAmp Case



- **Single pole** amplifier:

$$\frac{V_{out}}{V_{in}}(s) = \underbrace{\frac{G_0}{1+G_0H}}_{G_0'} \frac{1}{1+\underbrace{\frac{s}{w_p(1+G_0H)}}_{w_p'}}$$

$$G_0' \simeq \frac{1}{H} \qquad \frac{w_p'}{w_p} = 1+G_0H$$



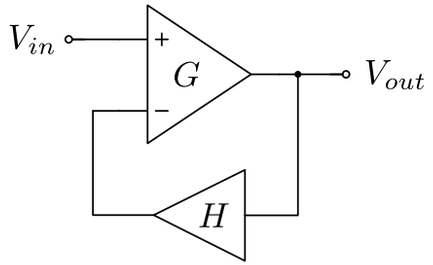
Barkhasuen criteria:

$$|GH(jw)| = 1 \quad \angle GH(jw) = -180°$$

▲ Intrinsically **stable**!

Two-Stage OpAmp Case

- **Double pole** analysis:



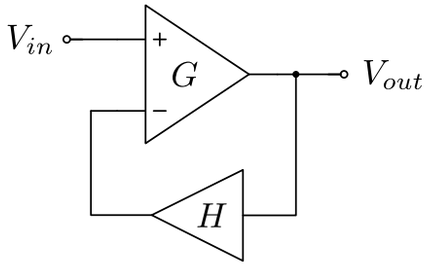
$$G(s) = \frac{G_0}{\left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right)}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{G_0}{\left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right) + G_0 H}$$

$$w'_{p1,2} = -\frac{w_{p1} + w_{p2}}{2} \pm \frac{1}{2}\sqrt{(w_{p1} + w_{p2})^2 - 4(1 + G_0 H) w_{p1} w_{p2}}$$

Two-Stage OpAmp Case

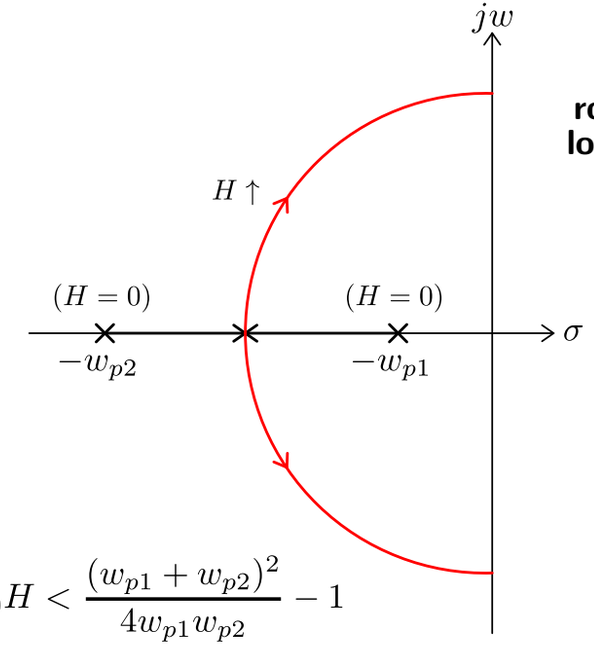
- **Double pole** analysis:



$$G(s) = \frac{G_0}{\left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right)}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{G_0}{\left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right)+G_0H}$$

$$w'_{p1,2} = -\frac{w_{p1}+w_{p2}}{2} \pm \frac{1}{2}\sqrt{(w_{p1}+w_{p2})^2 - 4(1+G_0H)w_{p1}w_{p2}}$$



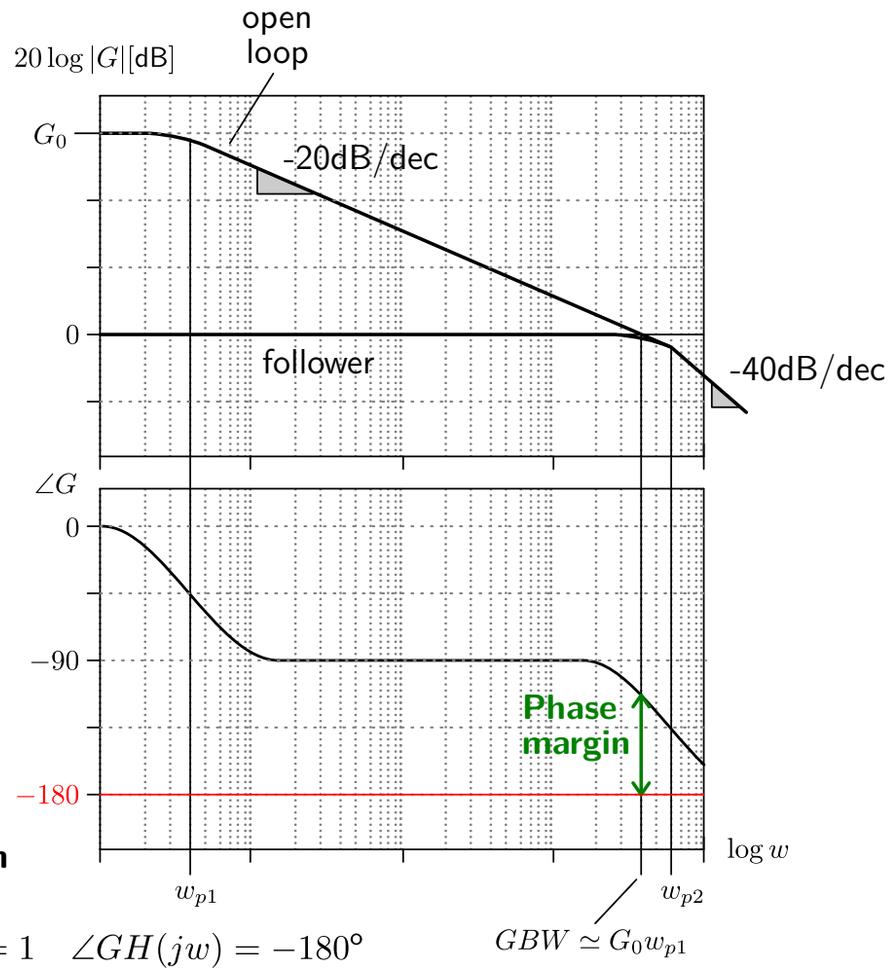
$$G_0H < \frac{(w_{p1}+w_{p2})^2}{4w_{p1}w_{p2}} - 1$$

$$H < \frac{1}{4G_0}\left(\frac{w_{p1}}{w_{p2}} + \frac{w_{p2}}{w_{p1}} - 2\right)\uparrow$$ in order to cover up to **H=1**

dominant pole splitting is required! $\frac{w_{p2}}{G_0 w_{p1}}\uparrow$ or $\frac{w_{p1}}{G_0 w_{p2}}\uparrow$

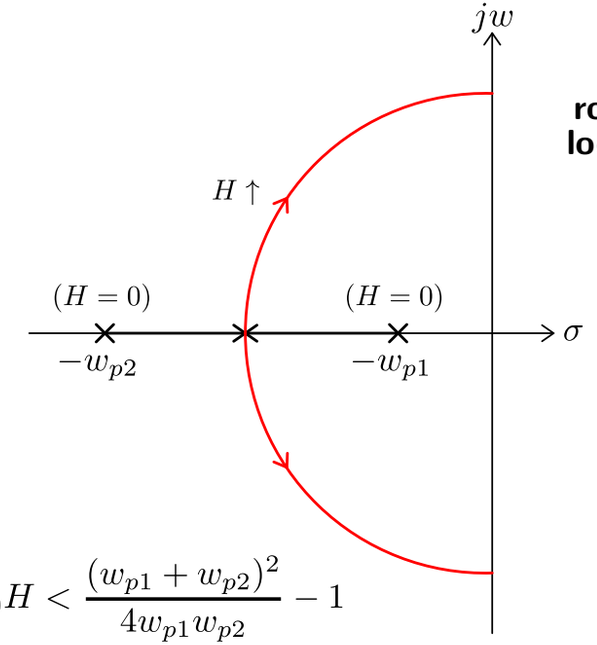
Two-Stage OpAmp Case

- **Double pole** analysis:



Barkhasuen criteria:

$|GH(jw)| = 1 \quad \angle GH(jw) = -180°$



$$G_0 H < \frac{(w_{p1}+w_{p2})^2}{4w_{p1}w_{p2}} - 1$$

$$H < \frac{1}{4G_0}\left(\frac{w_{p1}}{w_{p2}} + \frac{w_{p2}}{w_{p1}} - 2\right)\uparrow$$

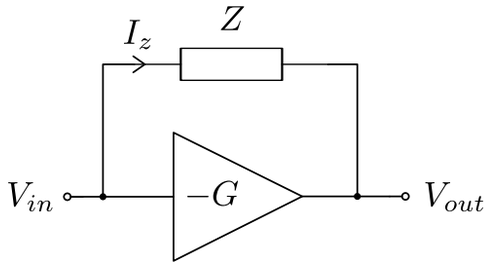
in order to cover up to **H=1**

dominant pole splitting is required!

$$\frac{w_{p2}}{G_0 w_{p1}}\uparrow \quad \text{or} \quad \frac{w_{p1}}{G_0 w_{p2}}\uparrow$$

Principle of Operation

- **Transimpedance** amplifier:



$$\begin{cases} V_{out} = -GV_{in} \\ I_z = \dfrac{V_{in} - V_{out}}{Z} \end{cases}$$

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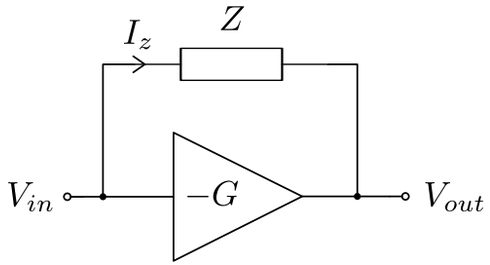
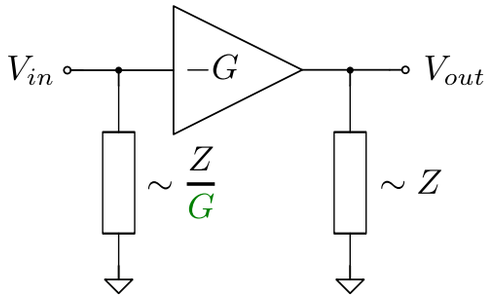
- **Transimpedance** amplifier:

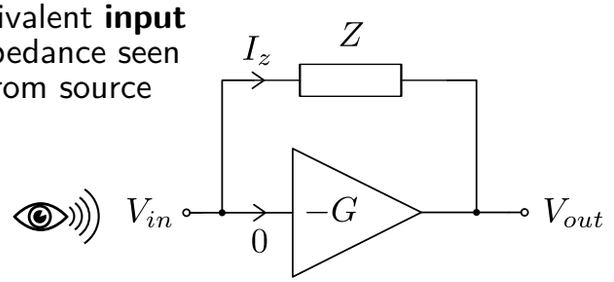


$$\begin{cases} V_{out} = -GV_{in} \\ I_z = \dfrac{V_{in} - V_{out}}{Z} \end{cases}$$

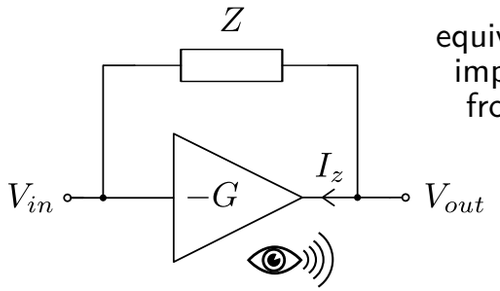
- **Miller** effect:



equivalent **input** impedance seen from source



$$Z_{in} \doteq \frac{V_{in}}{I_z} = \frac{V_{in}}{V_{in} - V_{out}} Z = \frac{Z}{1+G}$$

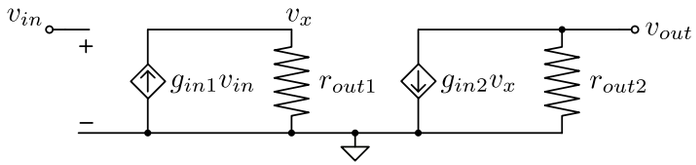


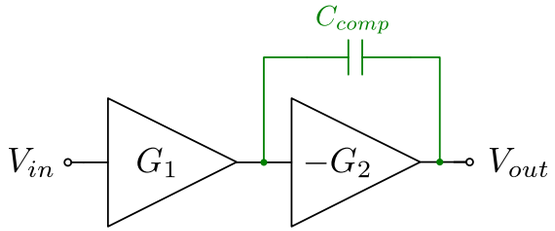
equivalent **output** impedance seen from amplifier

$$Z_{out} \doteq \frac{V_{out}}{-I_z} = \frac{V_{out}}{V_{out} - V_{in}} Z = \frac{G}{1+G} Z$$

Pole Adjustment

- **Transcapacitive** impedance case: $Z(s) \doteq \frac{1}{C_{comp}s}$



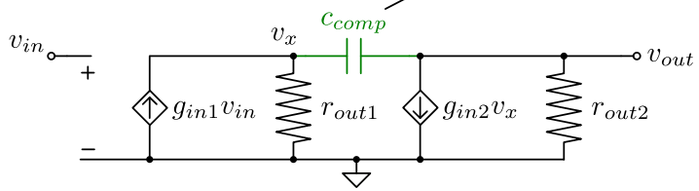


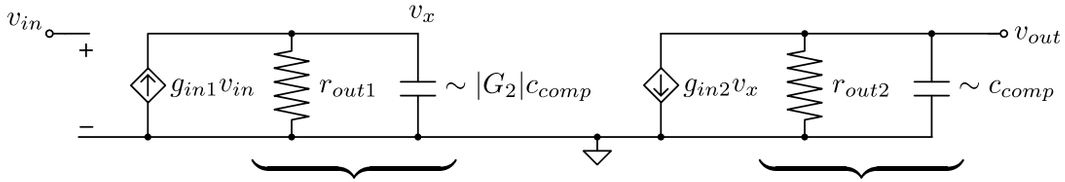
$G_1(DC) = g_{in1}r_{out1}$

$G_2(DC) = -g_{in2}r_{out2}$

two-stage OpAmp **small signal** model

Miller compensation



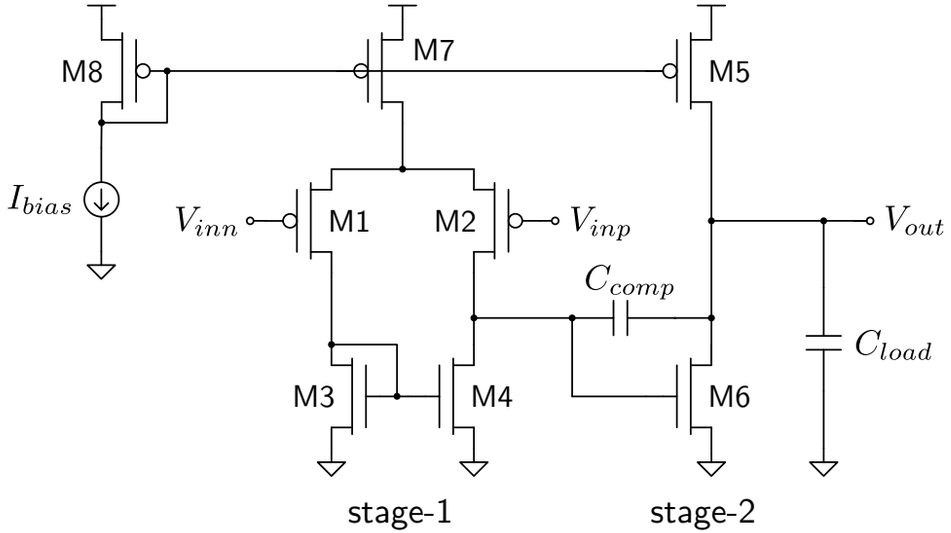


dominant pole

second pole

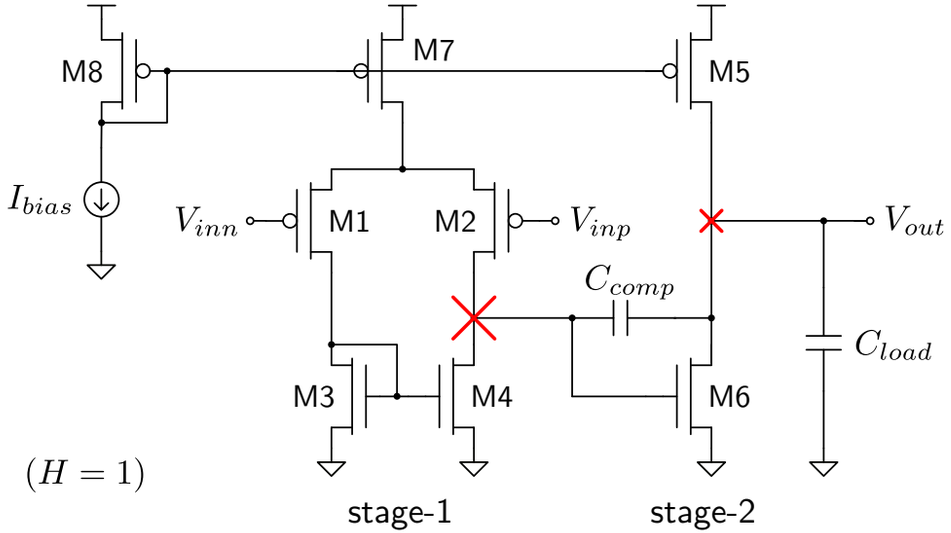
Practical Example

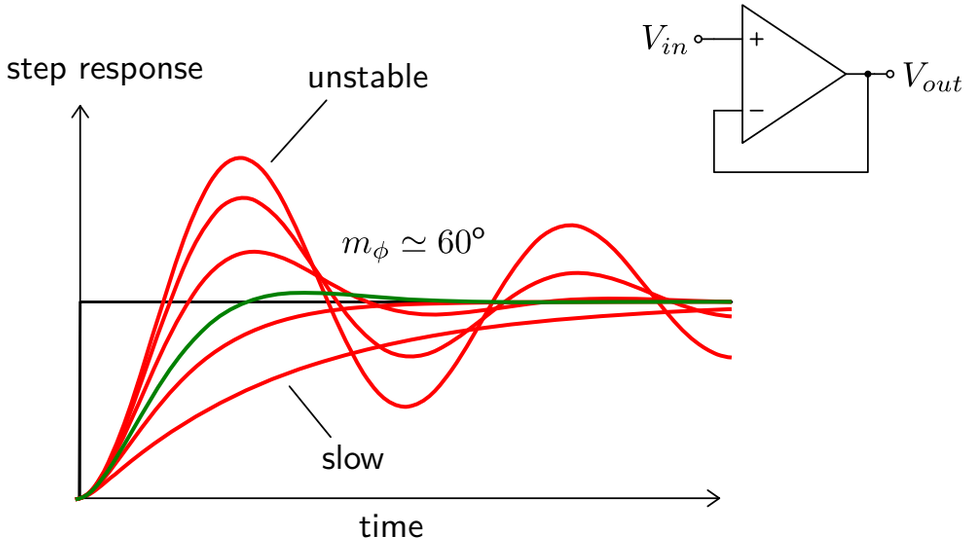
- **Two-stage** single-ended **Miller-compensated** OpAmp topology:



Practical Example

- **Two-stage** single-ended **Miller-compensated** OpAmp topology:





$(H = 1)$

$f'_{p1} \simeq GBW$

$$GBW = (g_{in1}r_{out1})(g_{in2}r_{out2})\frac{1}{2\pi}\frac{1}{r_{out1}c_{comp}(g_{in2}r_{out2})}$$

Miller

$$GBW = \frac{g_{mg1,2}}{2\pi c_{comp}}$$

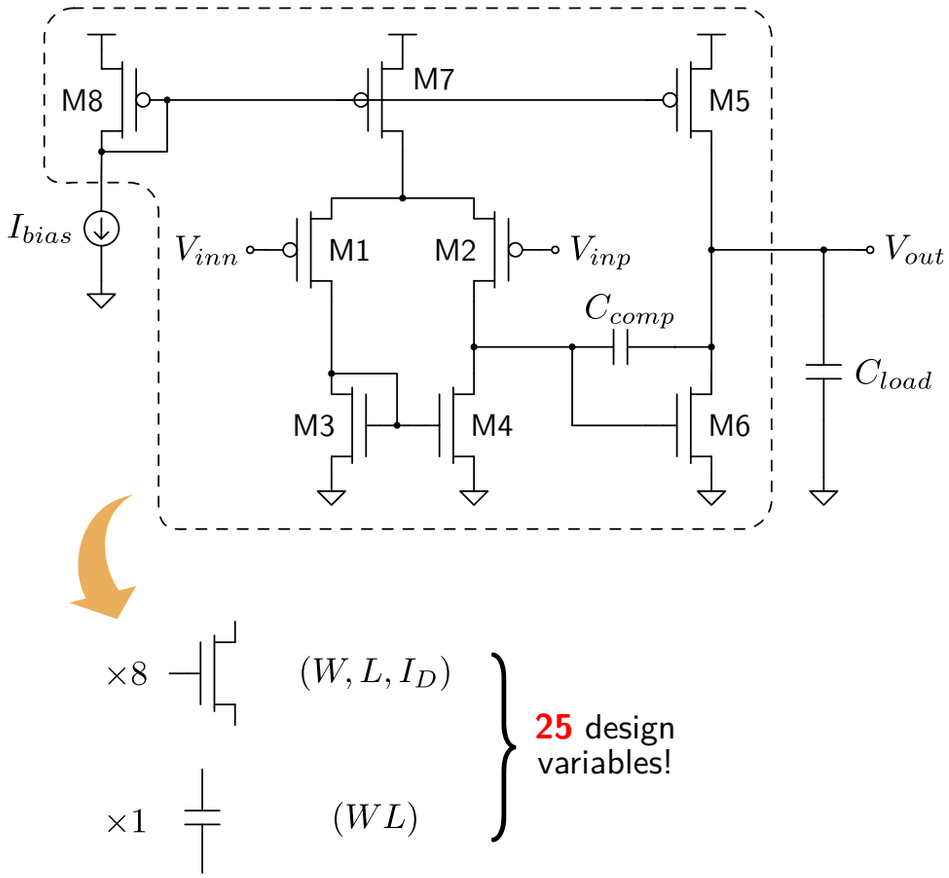
$m_\phi \geq 60° \quad \rightarrow \quad f'_{p2} \geq 2.2 f'_{p1}$

$$f'_{p2} = \frac{g_{mg6}}{2\pi(c_{load} + c_{comp})}$$

$$\frac{g_{mg6}}{g_{mg1,2}} \geq 2.2\left(1 + \frac{c_{load}}{c_{comp}}\right)$$

Design Variables

- Single-ended **Miller** OpAmp example:



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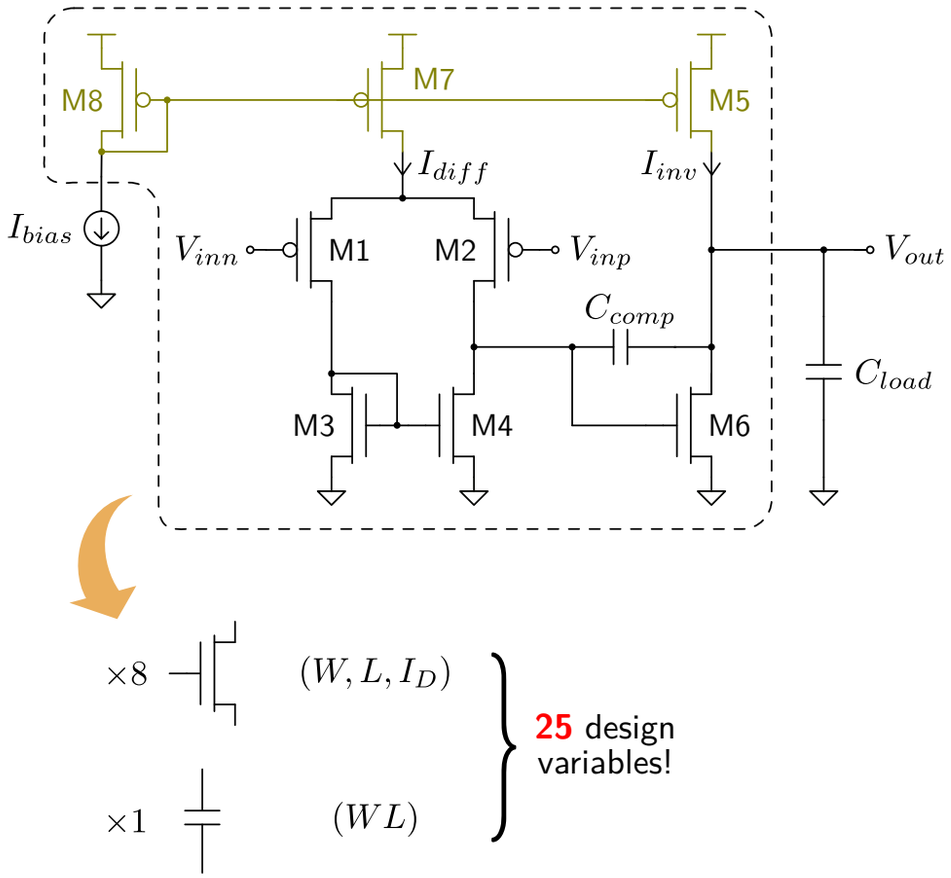
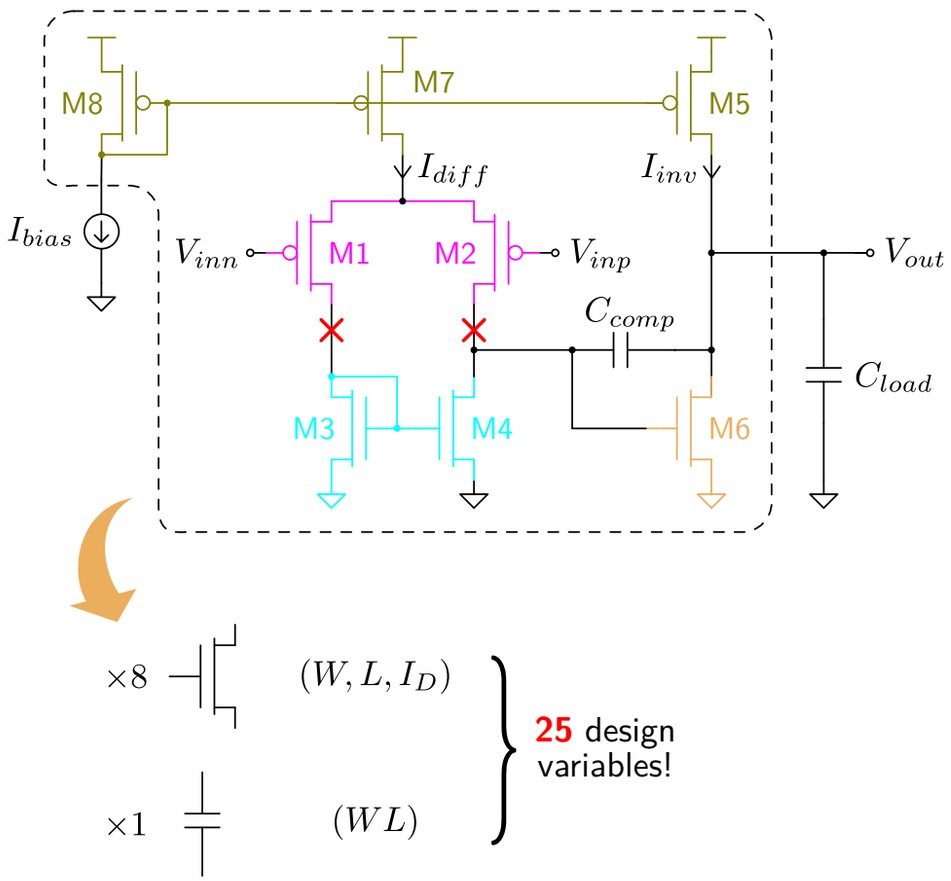


- Device **matching** groups:
  - Current **biasing**

$$I_{diff} \doteq \underbrace{\frac{(W/L)_7}{(W/L)_8}}_{m_{diff}} I_{bias} \qquad I_{inv} \doteq \underbrace{\frac{(W/L)_5}{(W/L)_8}}_{m_{inv}} I_{bias}$$

Design Variables

- Single-ended **Miller** OpAmp example:



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  - Null systematic **offset**

$$\left(\frac{W}{L}\right)_1 \equiv \left(\frac{W}{L}\right)_2 \doteq \left(\frac{W}{L}\right)_{diff}$$

$$\left(\frac{W}{L}\right)_3 \equiv \left(\frac{W}{L}\right)_4 \doteq \left(\frac{W}{L}\right)_{sing}$$

$$\frac{I_{diff}/2}{I_{inv}} \equiv \frac{(W/L)_3}{(W/L)_6}$$

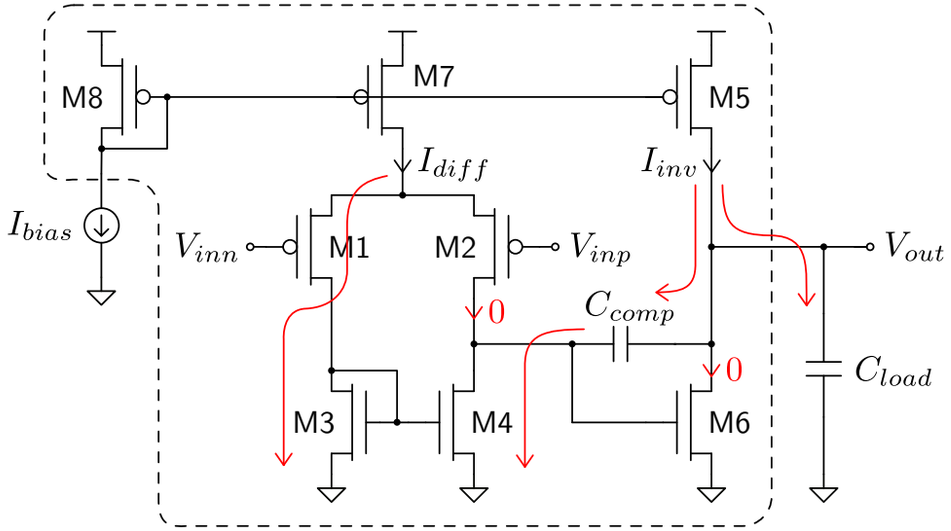
8 design variables!

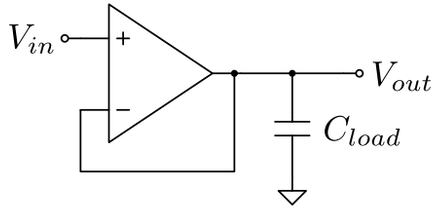
$$\left\{ \left(\frac{W}{L}\right)_{diff} \quad \left(\frac{W}{L}\right)_{sing} \quad \left(\frac{W}{L}\right)_{inv} \right.$$

$$\left. I_{bias} \quad I_{diff} \quad I_{inv} \quad C_{comp} \quad L \right\}$$

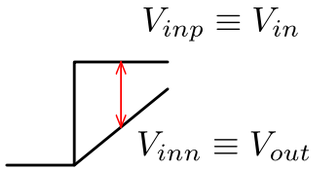
Design Equations

- Single-ended **Miller** OpAmp example:





$$SR_+ = \frac{I_{inv} - I_{diff}}{C_{comp} + C_{load}}$$



Design Equations

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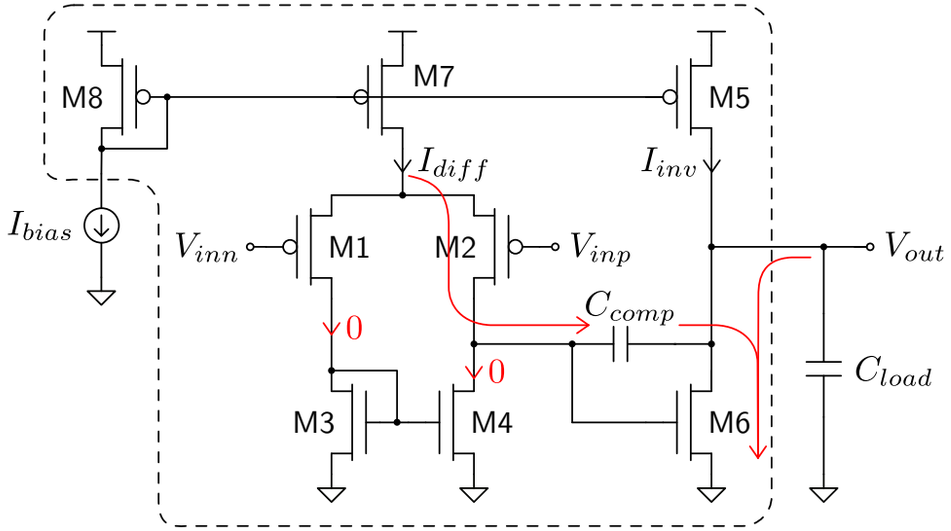
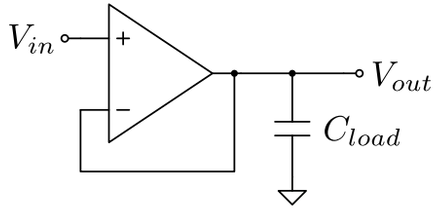
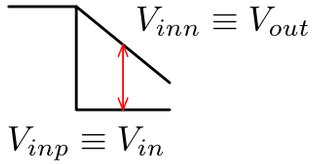




$$SR_+ = \frac{I_{inv} - I_{diff}}{C_{comp} + C_{load}}$$

$$SR_- = \frac{I_{diff}}{C_{comp}}$$



Design Equations

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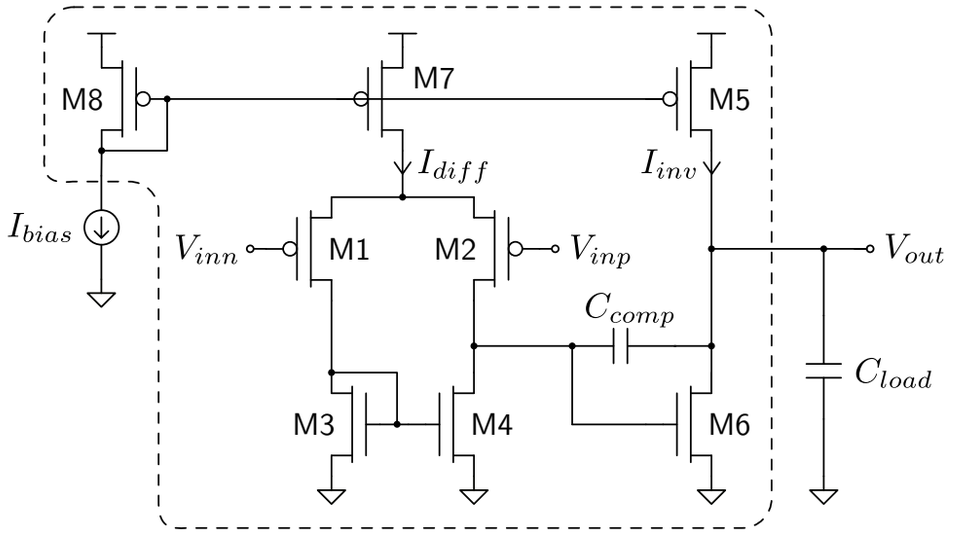

strong inversion
forward **saturation**
for all transistors

$$SR_+ = \frac{I_{inv} - I_{diff}}{C_{comp} + C_{load}}$$

$$SR_- = \frac{I_{diff}}{C_{comp}}$$

$$m_\phi \geq 60° : \quad \frac{g_{mg6}}{g_{mg1,2}} \geq 2.2\left(1 + \frac{C_{load}}{C_{comp}}\right)$$

$$\sqrt{2\frac{\beta_N}{\beta_P}\frac{(W/L)_{inv}}{(W/L)_{diff}}\frac{I_{inv}}{I_{diff}}} \geq 2.2\left(1 + \frac{C_{load}}{C_{comp}}\right)$$

$$GBW = \frac{g_{mg1,2}}{2\pi C_{comp}} = \frac{1}{2\pi C_{comp}}\sqrt{\frac{\beta_P}{n}\left(\frac{W}{L}\right)_{diff} I_{diff}}$$

$$\frac{I_{diff}/2}{I_{inv}} \equiv \frac{(W/L)_{sing}}{(W/L)_{inv}}$$

$$G(DC) = \frac{g_{mg1,2}}{g_{md1,2} + g_{md3,4}}\frac{g_{mg6}}{g_{md5} + g_{md6}} = \frac{2}{n(\lambda_N + \lambda_P)^2}\sqrt{\frac{2\beta_P\beta_N\left(\frac{W}{L}\right)_{diff}\left(\frac{W}{L}\right)_{inv}}{I_{diff}I_{inv}}}$$

$(\lambda_N + \lambda_P) \propto \frac{1}{L}$