3. DAC Architectures and CMOS Circuits

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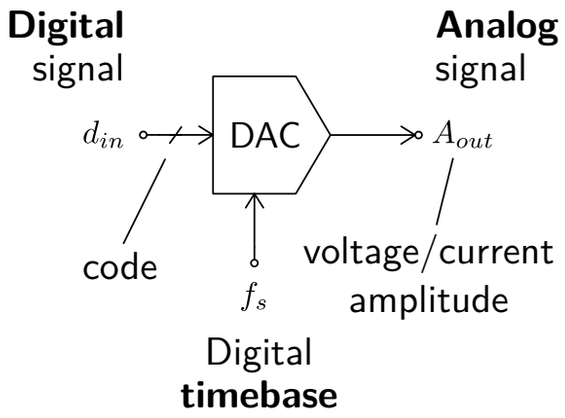
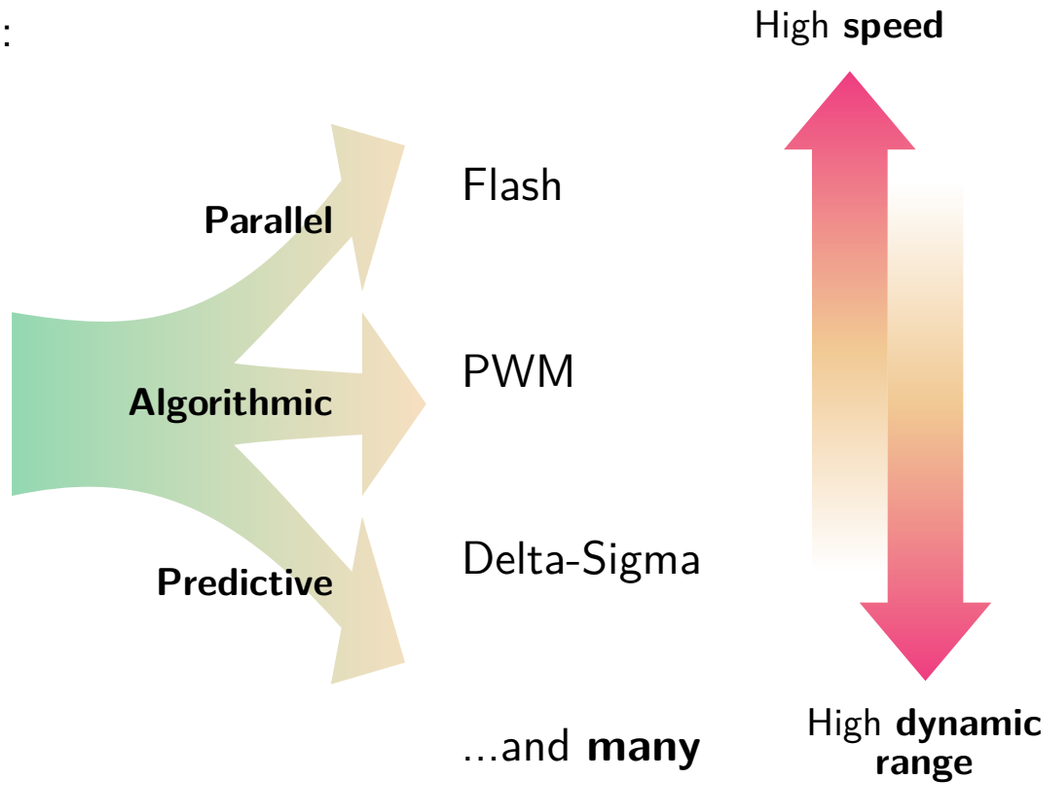
DAC Families

- Classification based on **architecture** approach:

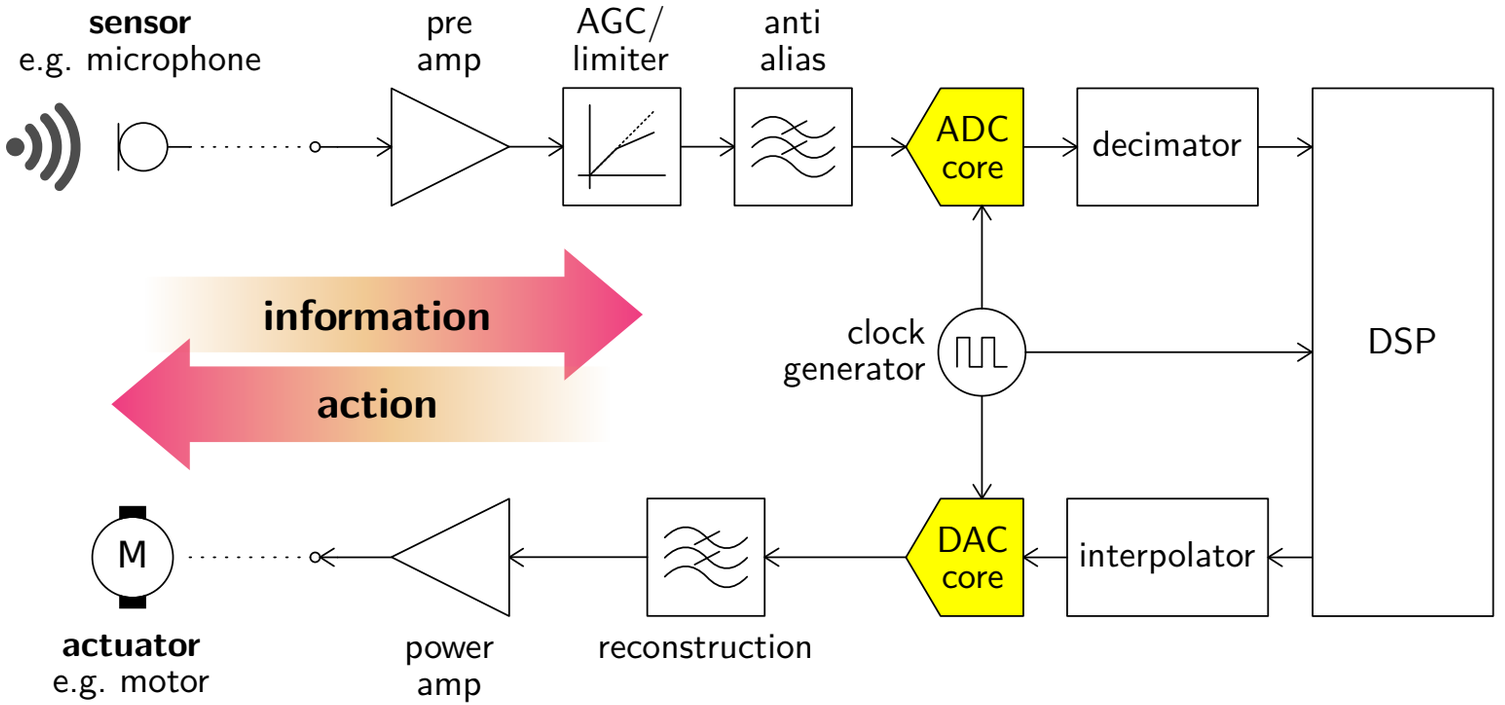




- Distinctive **characteristics**:
  - Feedforward vs feedback control
  - Single vs multiple stages
  - Amplitude vs time domains
- Typically **mixed** solutions...

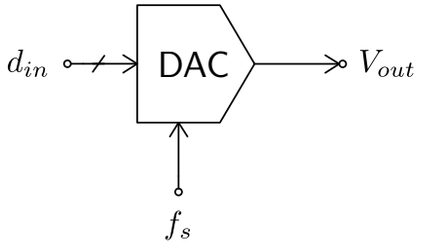
DAC vs ADC Design

- **Asymmetrical** system architecture and signal purpose:



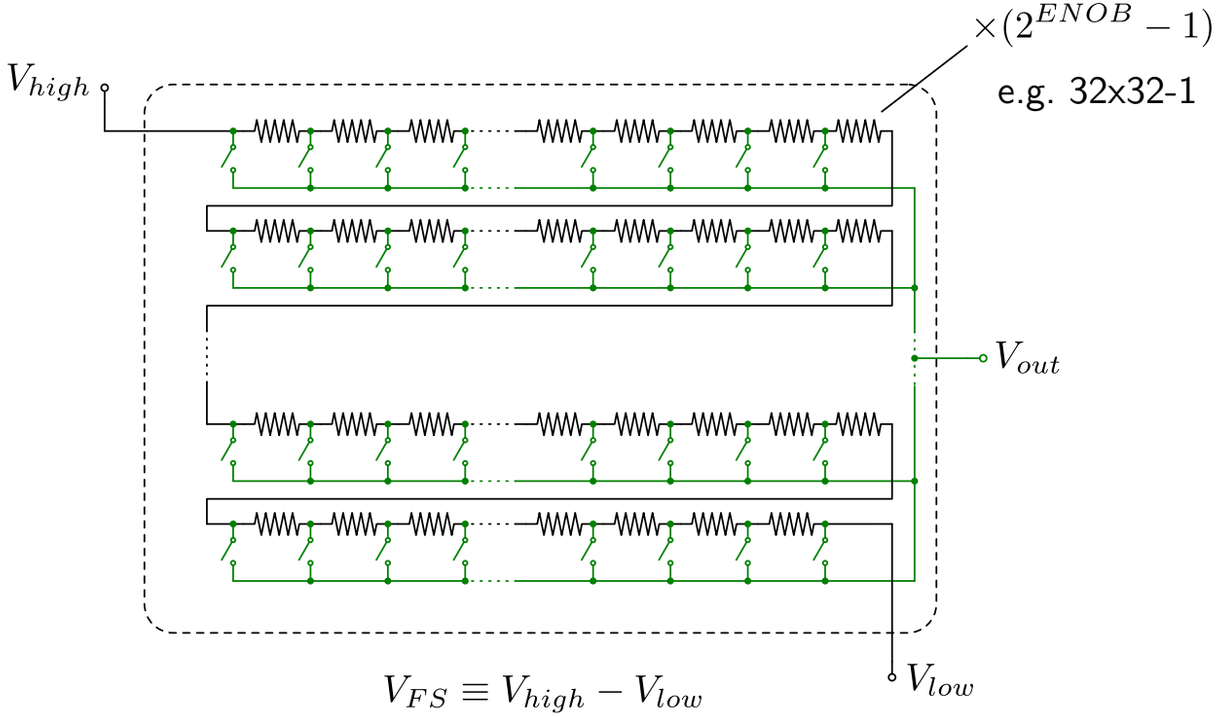
...typically **ADC** is more performance demanding!

Basic Flash Architecture

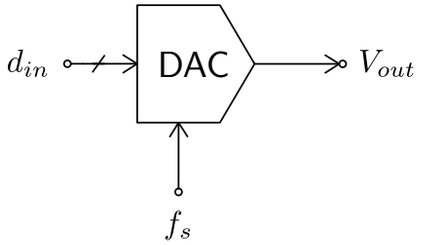


- All **parallel** and **segmented** (unitary) resistive ladder:

e.g. **single-ended**
10-bit flash DAC



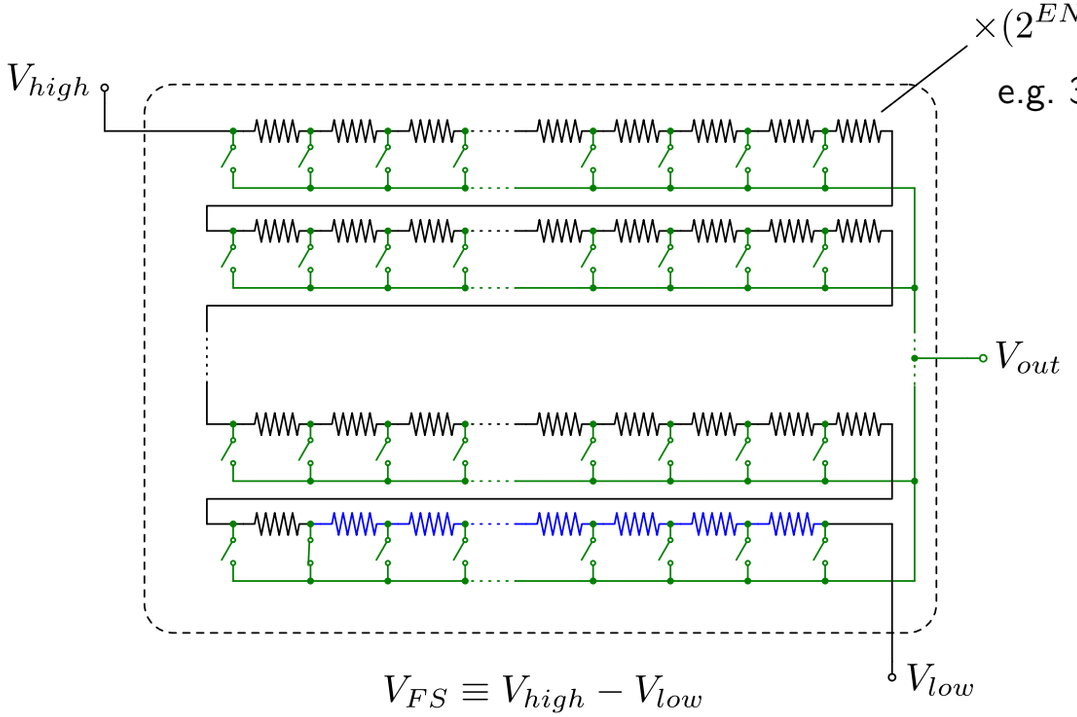
Basic Flash Architecture



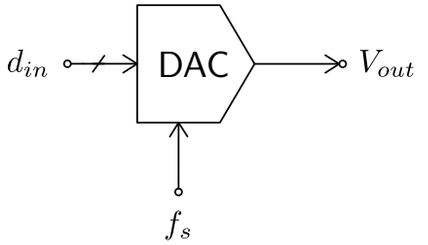
- All **parallel** and **segmented** (unitary) resistive ladder:

$$V_{out} = V_{low} + \frac{R_{sel}}{R_{total}} V_{FS}$$

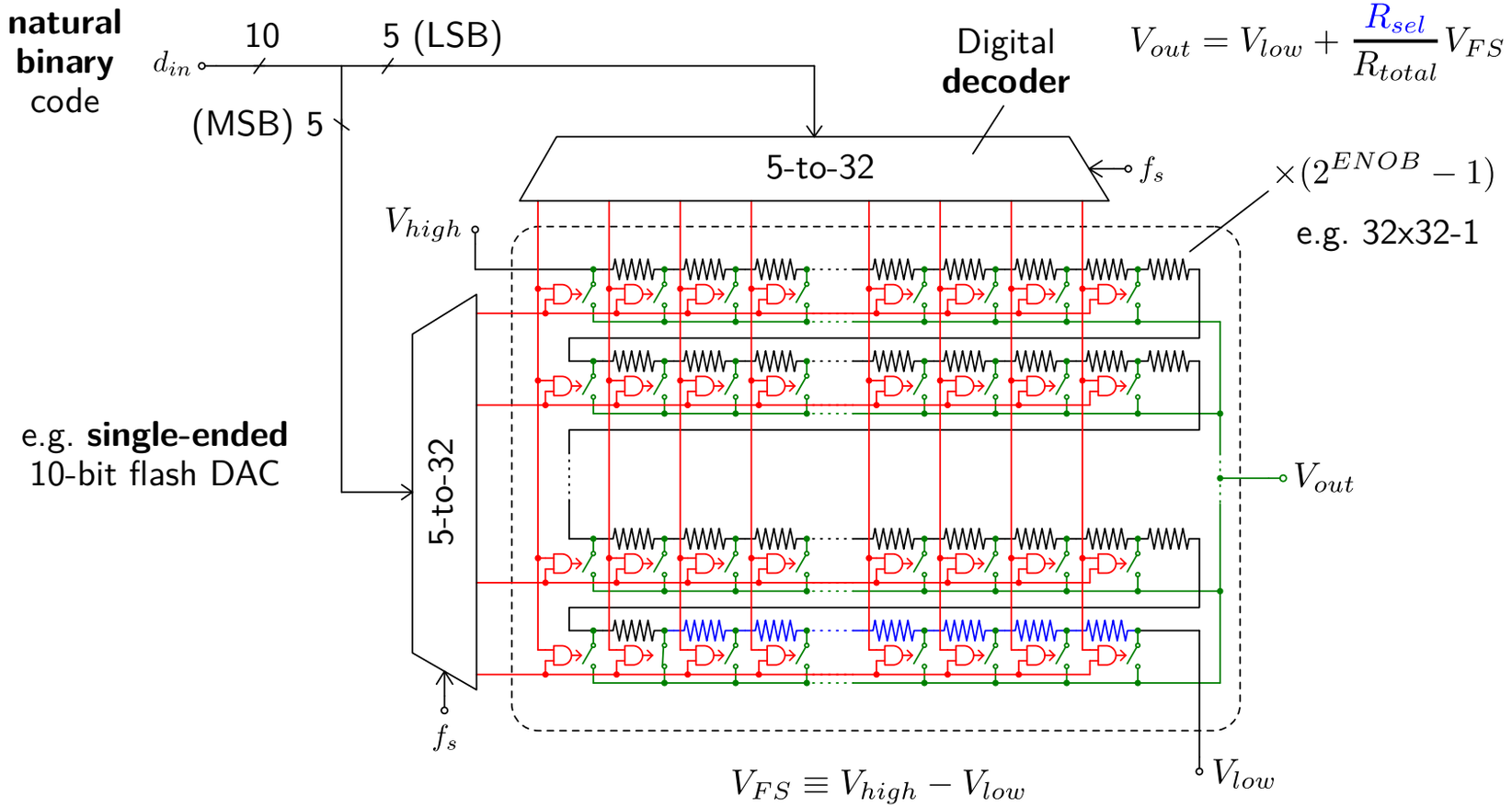
e.g. **single-ended**
10-bit flash DAC



Basic Flash Architecture



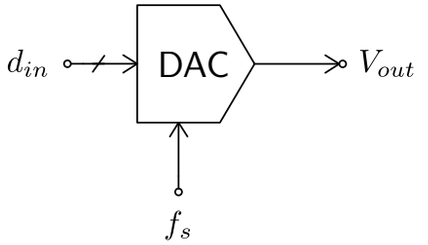
- All **parallel** and **segmented** (unitary) resistive ladder:



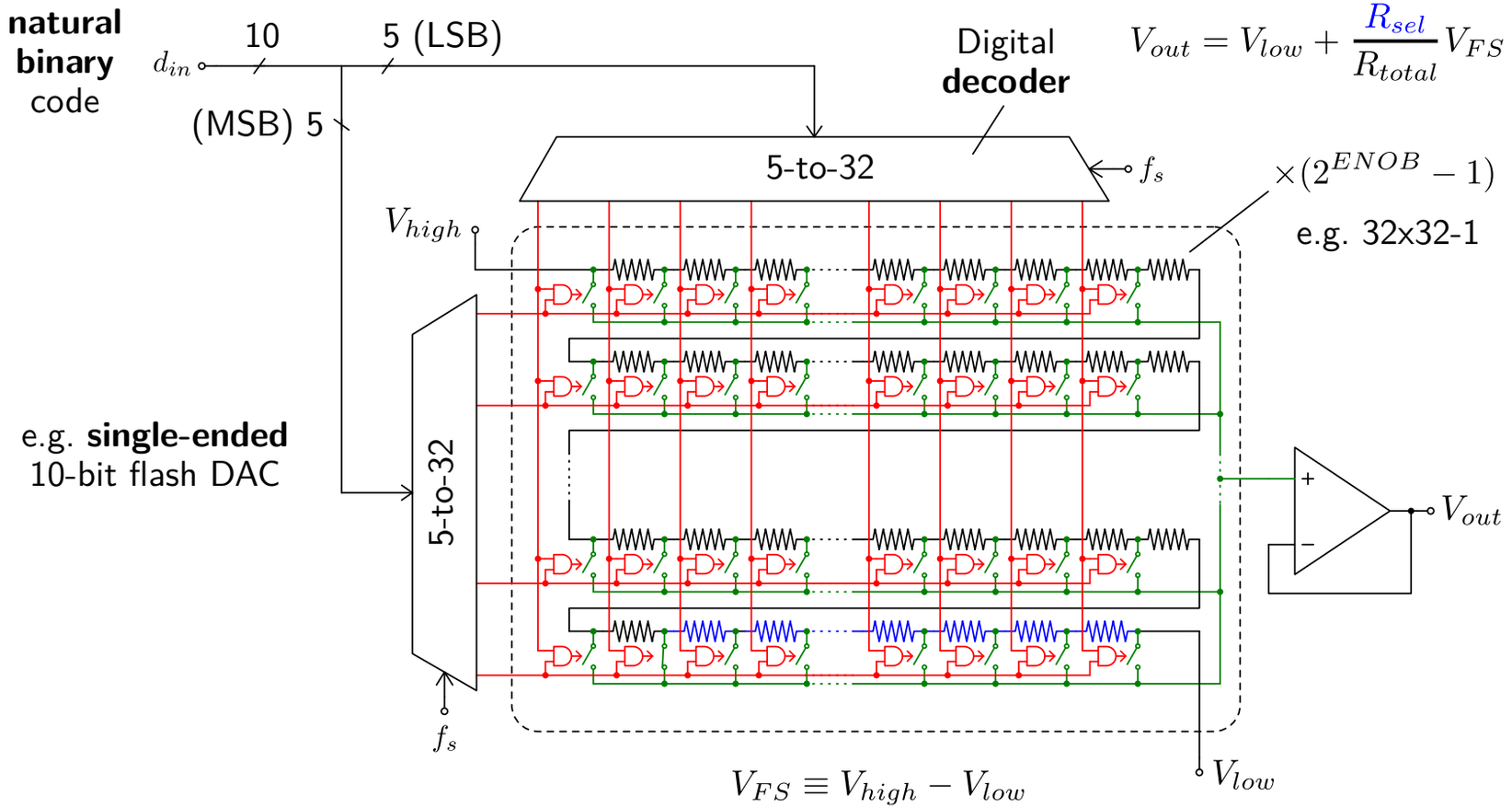
$$V_{out} = V_{low} + \frac{R_{sel}}{R_{total}} V_{FS}$$

- Non-constant **output impedance**

Basic Flash Architecture

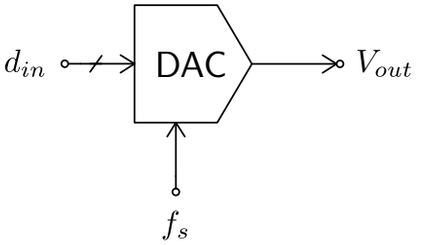


- All **parallel** and **segmented** (unitary) resistive ladder:

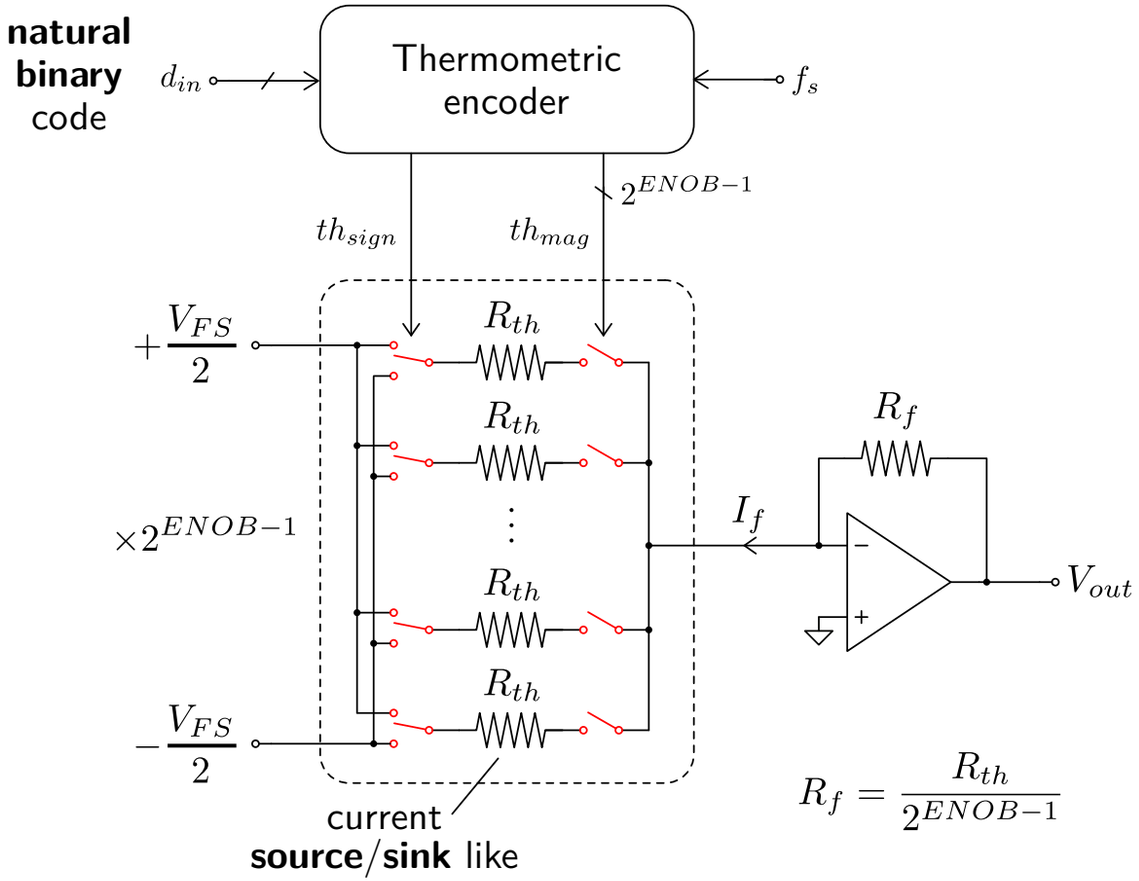


- Distortion due to **switch** on-resistance variability

Switch Optimization



- **Thermometric** switched-resistor flash DAC:

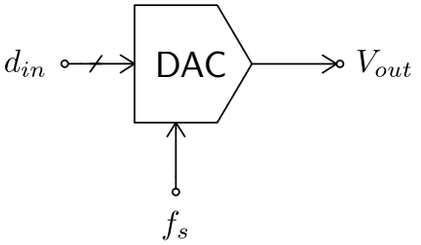


$$R_f = \frac{R_{th}}{2^{ENOB-1}}$$

$$\begin{cases} I_f = (-1)^{th_{sign}} \dfrac{V_{FS}/2}{R_{th}} \sum th_{mag} \\ V_{out} = I_f R_f \end{cases}$$

$$V_{out} = \frac{R_f}{R_{th}} \frac{V_{FS}}{2} (-1)^{th_{sign}} \sum th_{mag}$$

Switch Optimization



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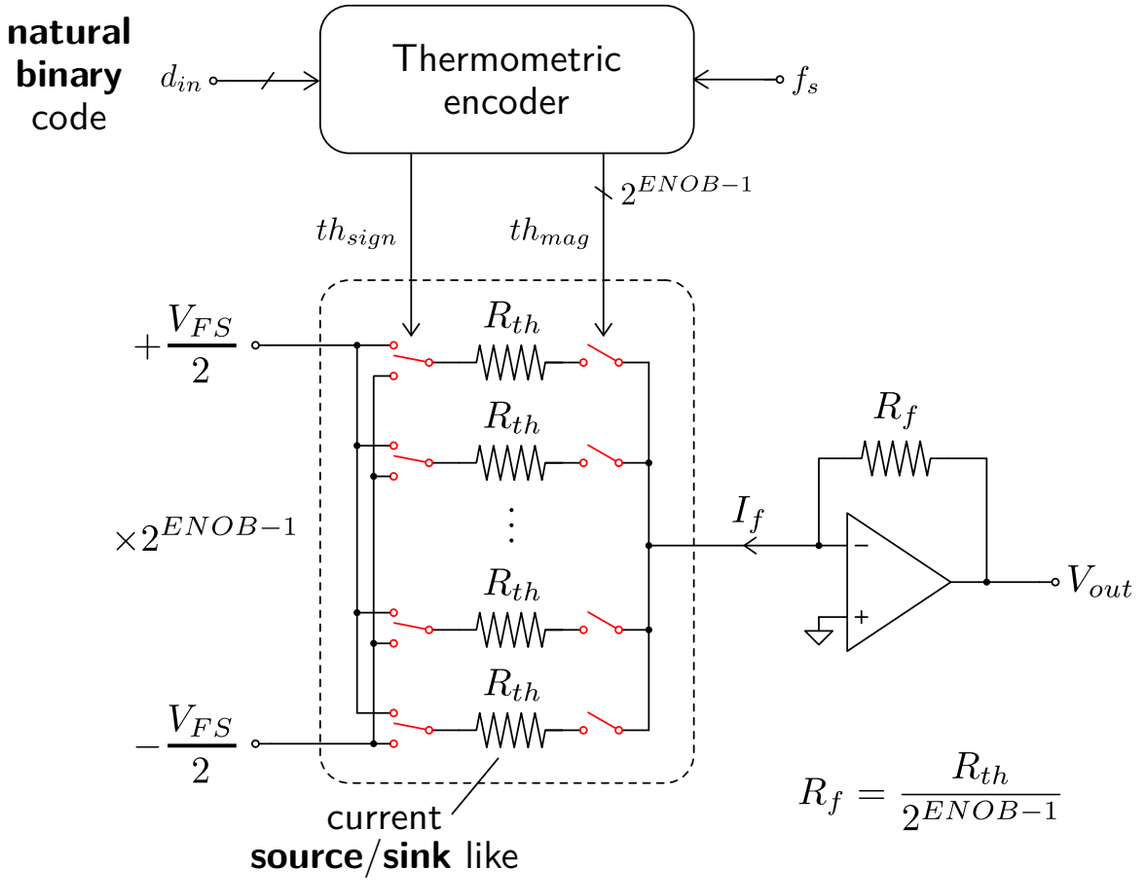


$$R_f = \frac{R_{th}}{2^{ENOB-1}}$$

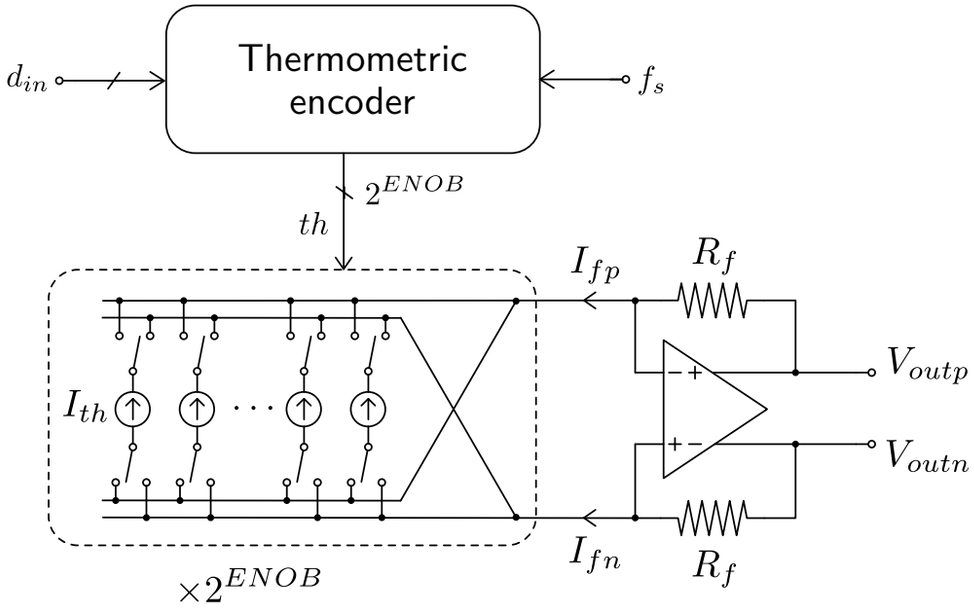
$$\frac{dv_{nout}^2}{df} = 4KT\left[R_f + th_{mag}R_{th}\left(\frac{R_f}{R_{th}}\right)^2\right]$$

$$\frac{dv_{nout}^2}{df} = 4KTR_f\left(1 + th_{mag}\frac{R_f}{R_{th}}\right) \leq 8KTR_f$$

- Switch non-linearity minimized thanks to its **signal independent** bias point

CMOS Circuits

- Thermometric switched-current (**SI**) **fully-differential** flash DAC:



continuous-time waveform!

$$V_{out} = V_{outp} - V_{outn}$$

$$\frac{V_{FS}}{2} = 2^{ENOB+1} I_{th} R_f$$

- ▼ MOSFET **noise** contributions!
- ▲ Always-on SI cell to reduce **glitches**

CMOS Circuits

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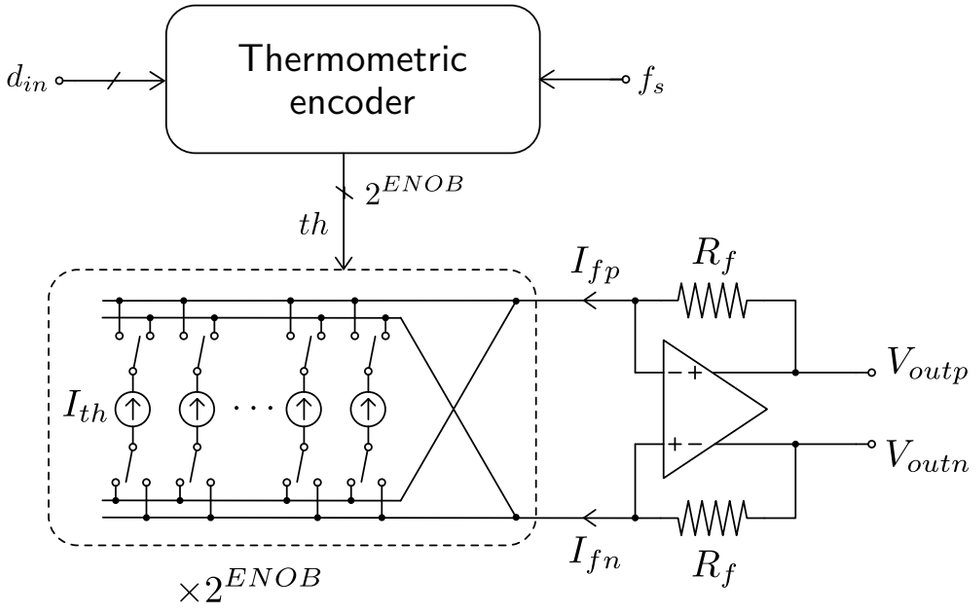
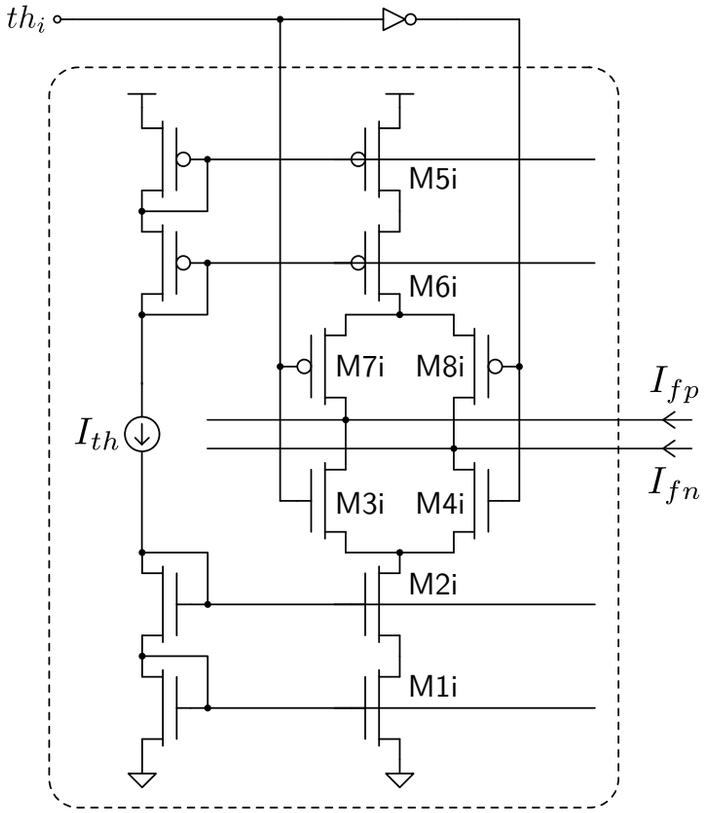


- SI **CMOS** modular cell:

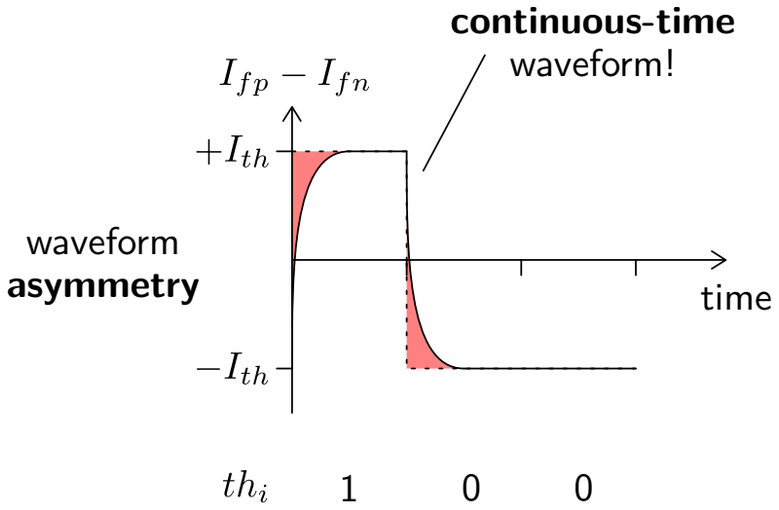


- Good current control thanks to...

OpAmp virtual ground + **cascode** topologies

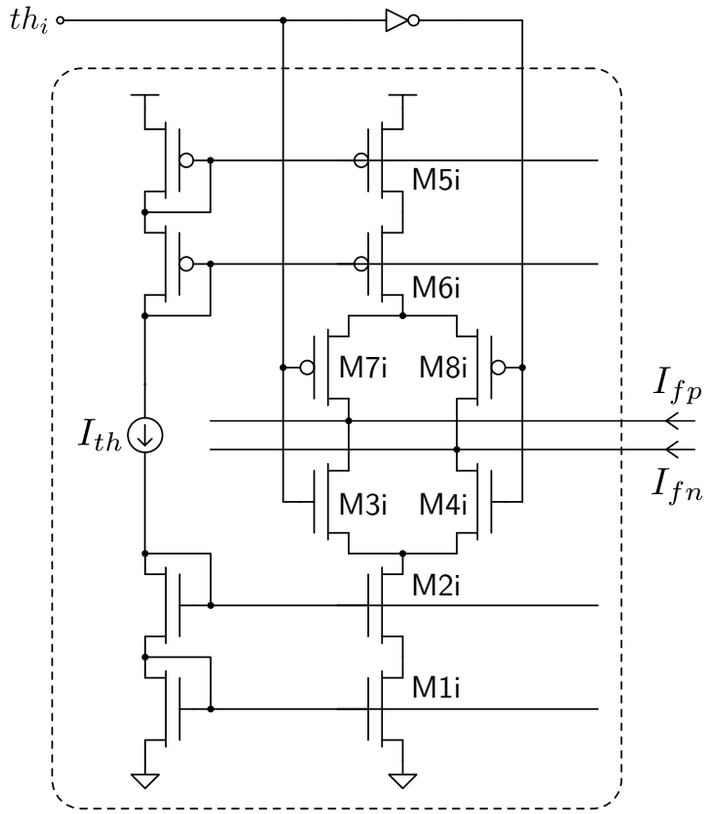
CMOS Circuits

- Regular versus return-to-zero (**RTZ**) digital signalling:



- Inter-symbol interference depends on input code, so it generates **signal distortion**!

- SI **CMOS** modular cell:



CMOS Circuits

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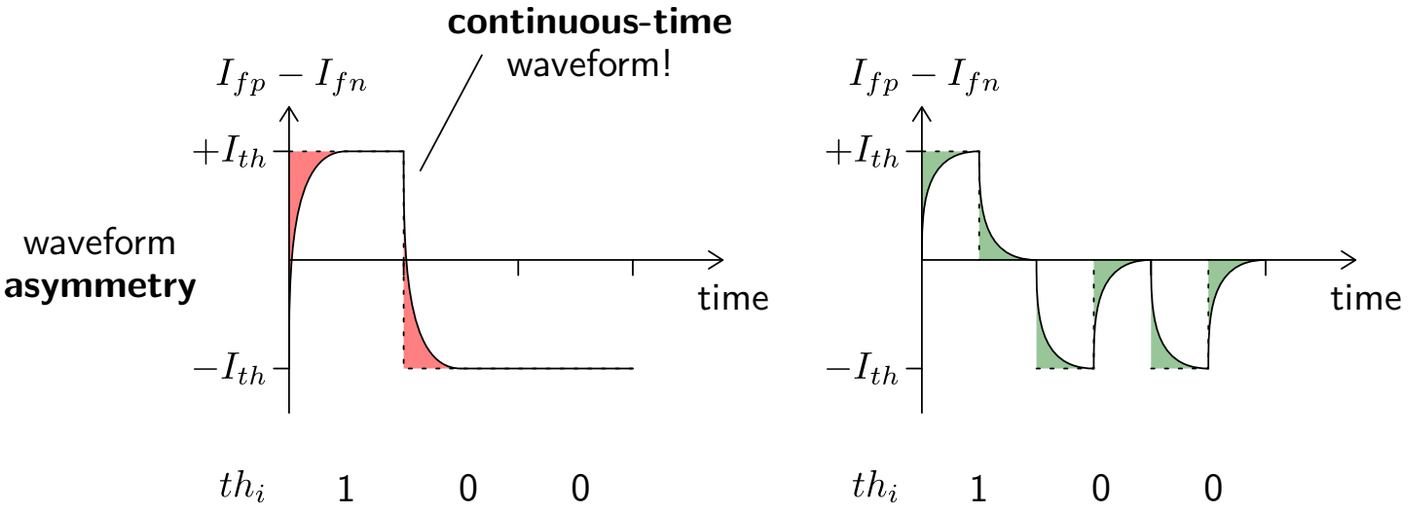
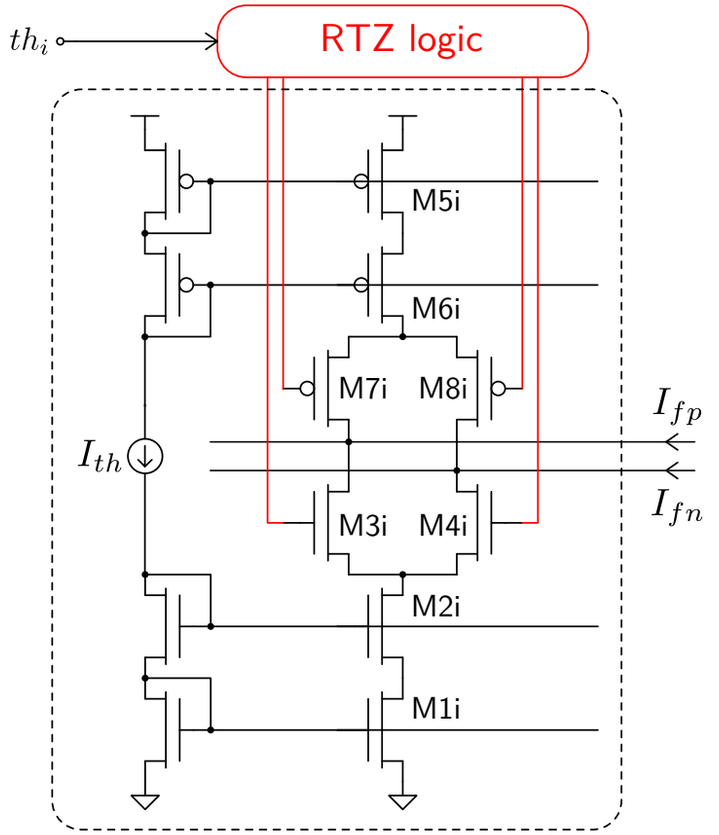


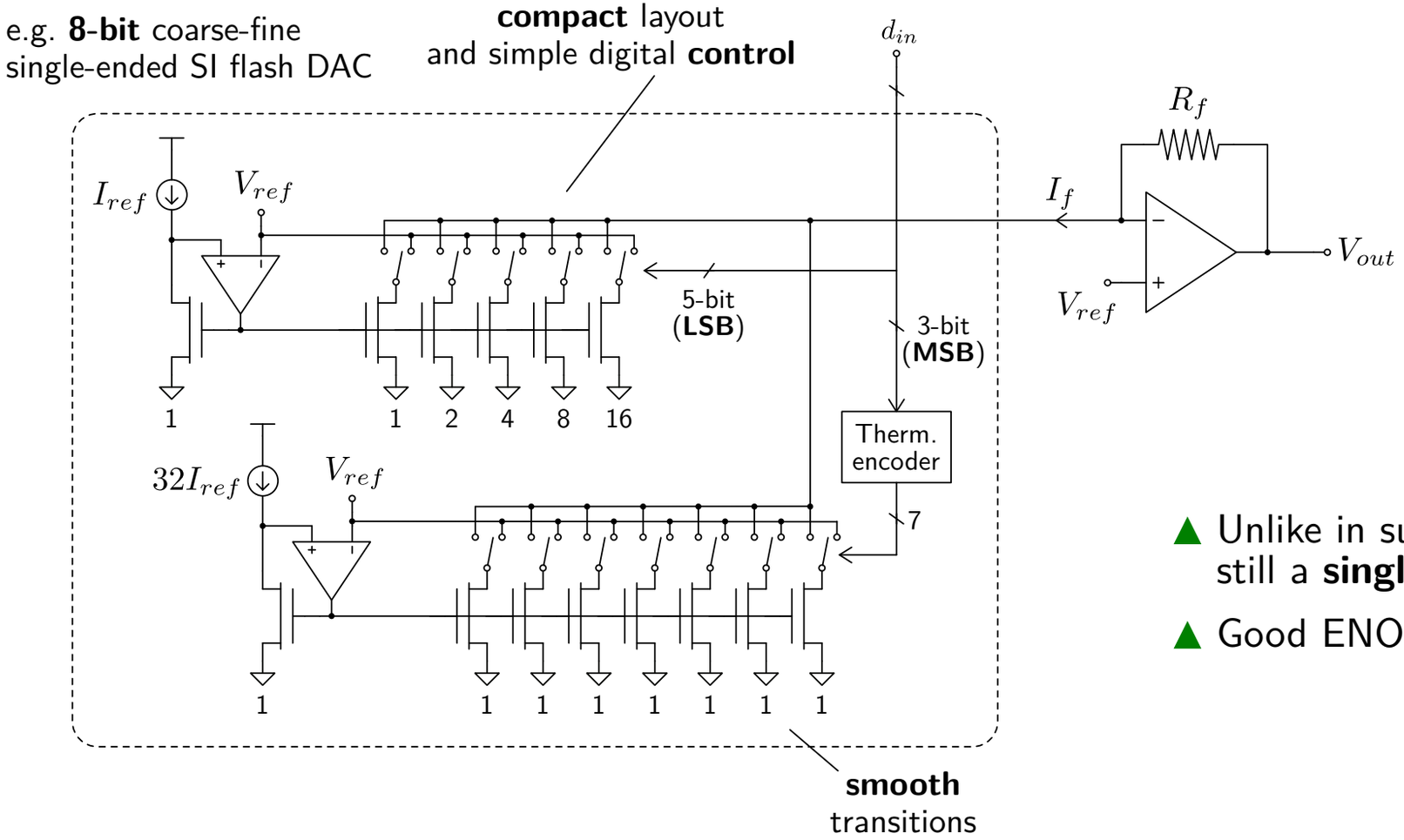
- SI **CMOS** modular cell:



- ▲ RTZ minimizes inter-symbol interference
- ▼ Full-scale reduction due to RTZ **duty cycle**
- ▼ Poor **scalability** with ENOB

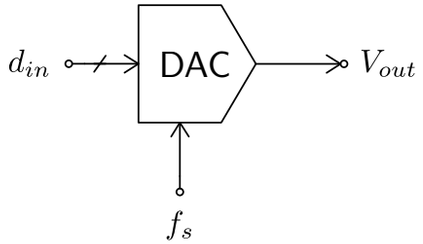
Sub-Ranging Architectures

- Mixed **segmented** (coarse) and **binary weighted** (fine) solutions:

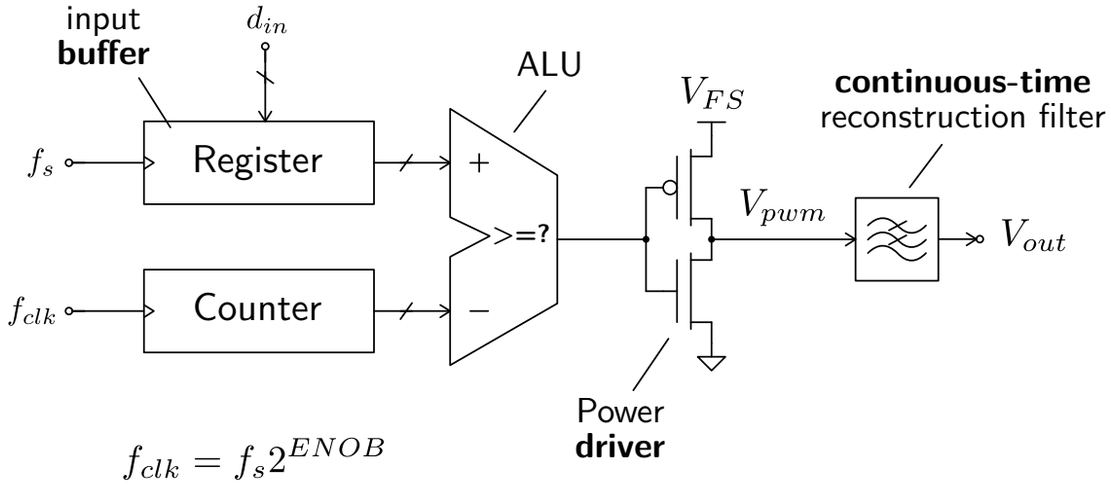


- Unlike in sub-ranging ADCs, still a **single step** conversion!
- Good ENOB **scalability**

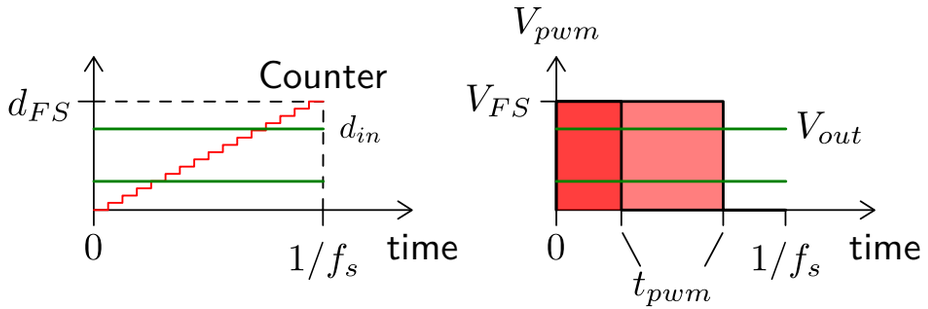
Digital Pulse Width Modulation



- **Discrete amplitude** and **continuous-time** domains:



$$f_{clk} = f_s 2^{ENOB}$$

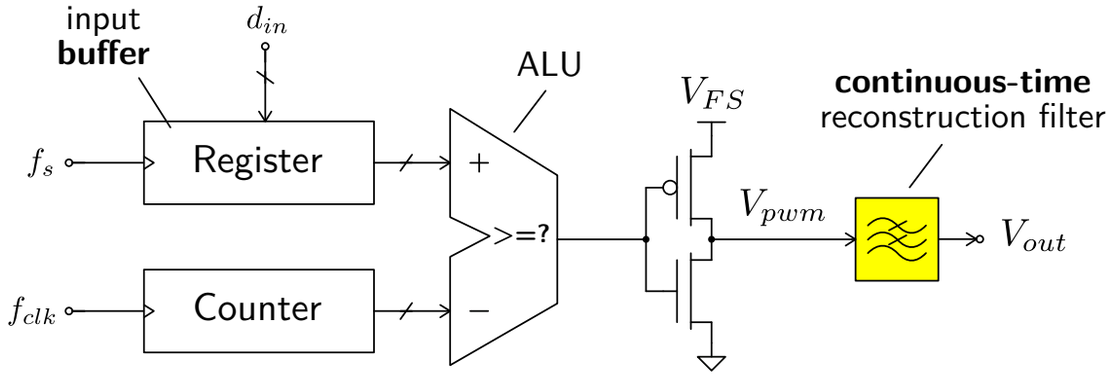


$$V_{out} = t_{pwm} f_s V_{FS} = \frac{d_{in}}{f_{clk}} f_s V_{FS}$$

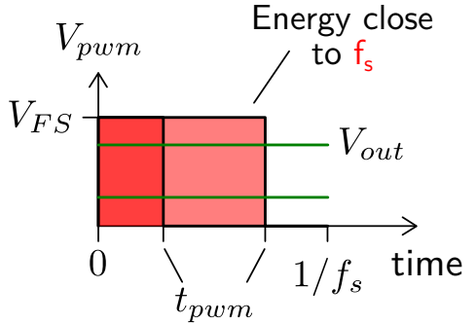
$$V_{out} = \frac{d_{in}}{2^{ENOB}} V_{FS}$$

Digital Pulse Width Modulation

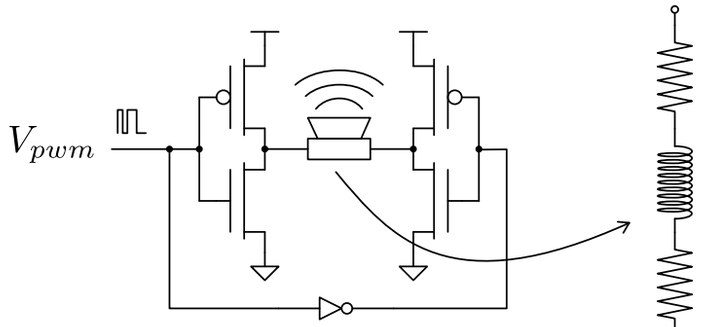
- **Discrete amplitude** and **continuous-time** domains:



$$f_{clk} = f_s 2^{ENOB}$$



- Ouptut **actuator** can be reused as reconstruction filter:

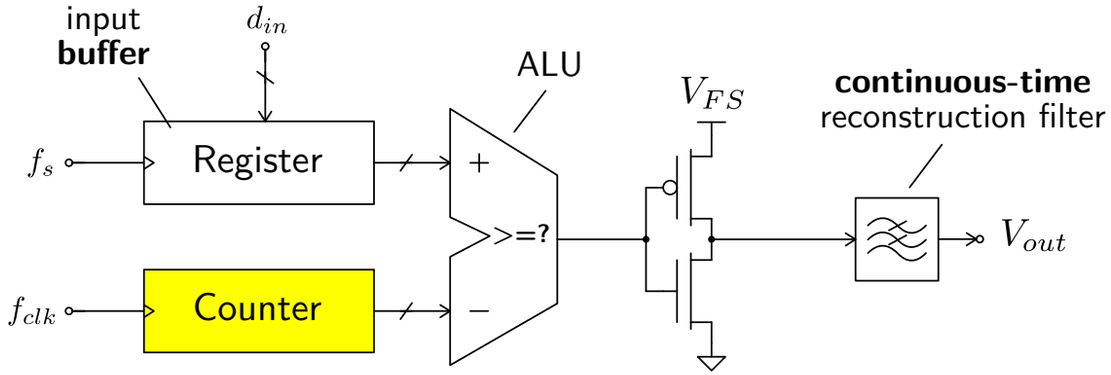


e.g. **Class-D** audio driver

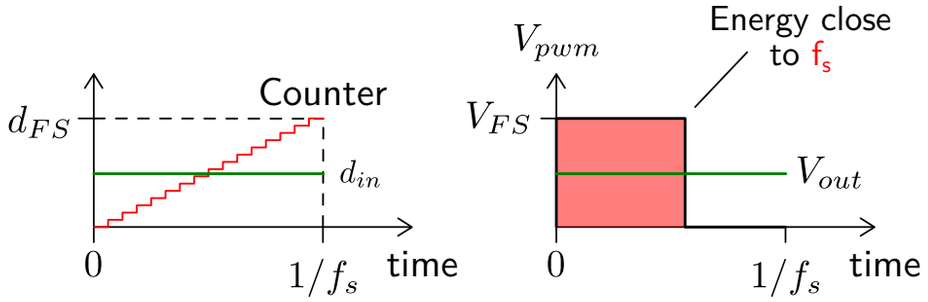
- **Overclocking**
- Output filter **selectivity**

Digital Pulse Width Modulation

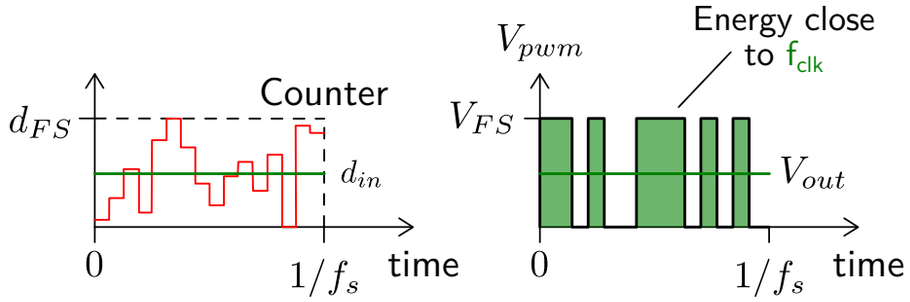
- **Discrete amplitude** and **continuous-time** domains:



$$f_{clk} = f_s 2^{ENOB}$$

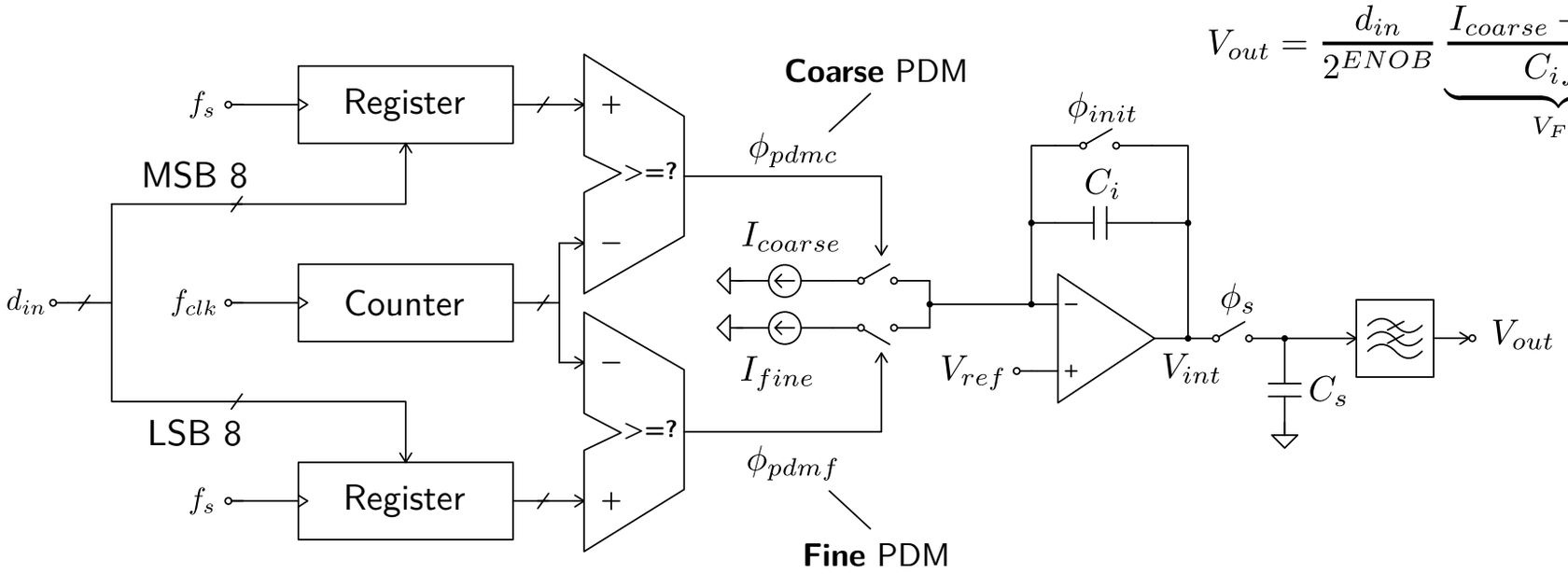


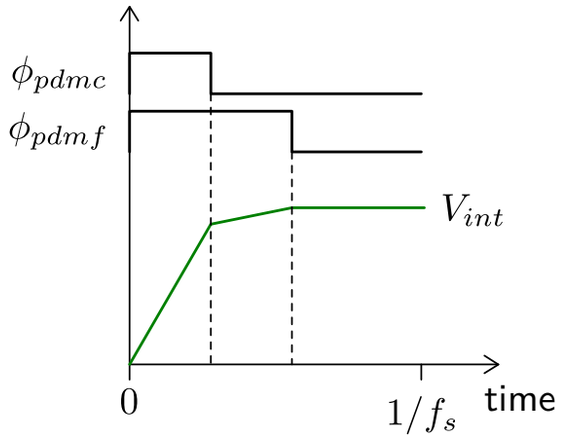
- **Relaxing** output filter selectivity through non-monotonic counters, e.g. linear-feedback shift registers (LFSRs)



Dual-Ramp Analog Integration

- **Sub-ranging** PDM DAC architecture:





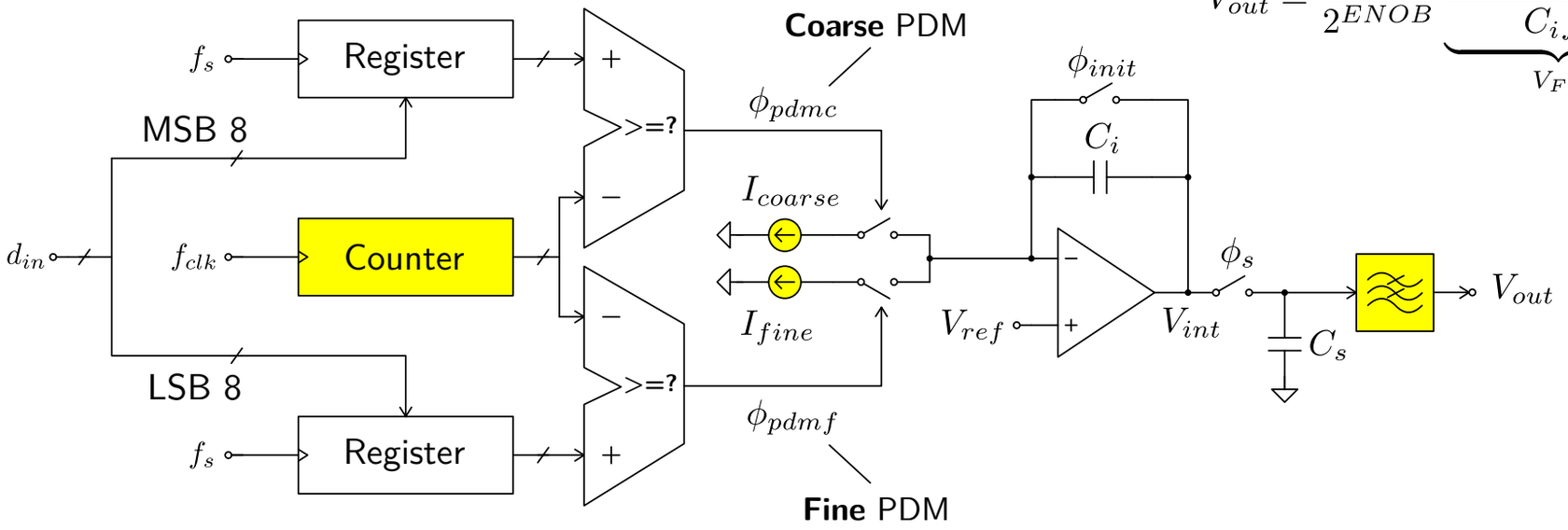
Dual-Ramp Analog Integration

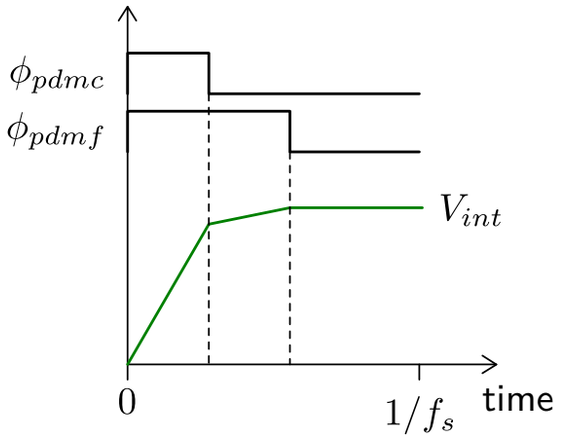
$$f_{clk} = 2^{\frac{ENOB}{2}} f_s$$

$$I_{coarse} = 2^{\frac{ENOB}{2}} I_{fine}$$

$$V_{out} = \frac{d_{in}}{2^{ENOB}} \underbrace{\frac{I_{coarse} + I_{fine}}{C_i f_s}}_{V_{FS}}$$

- **Sub-ranging** PDM DAC architecture:



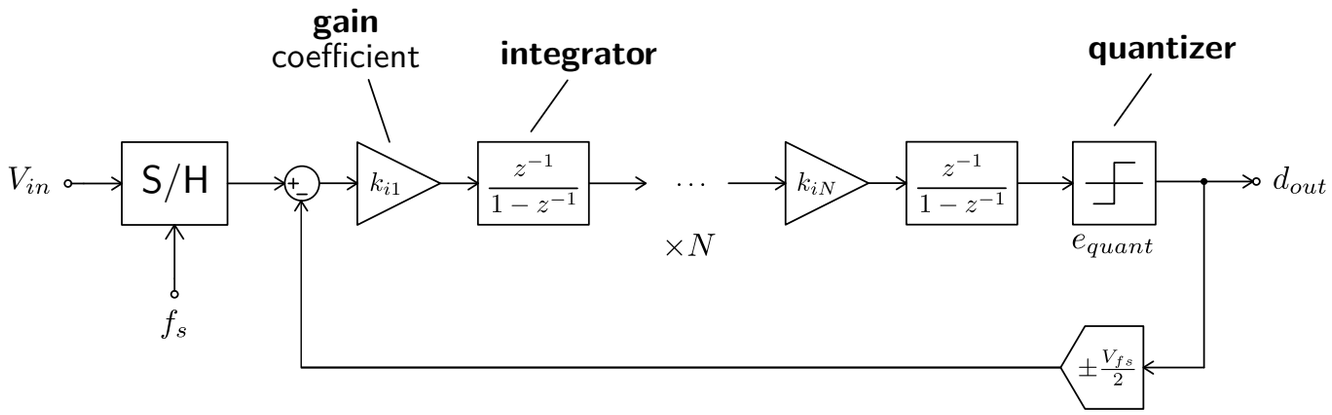


- ▲ **Relaxing** output filter selectivity
- ▲ Strong reduction of **clock speed** requirements
- ▼ Coarse-fine **matching**

e.g. **16-bit** dual ramp DAC

$$\begin{cases} f_{clk} = 256 f_s \\ I_{coarse} = 256 I_{fine} \end{cases}$$

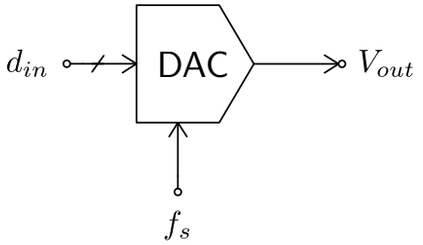
Analog vs Digital DSM

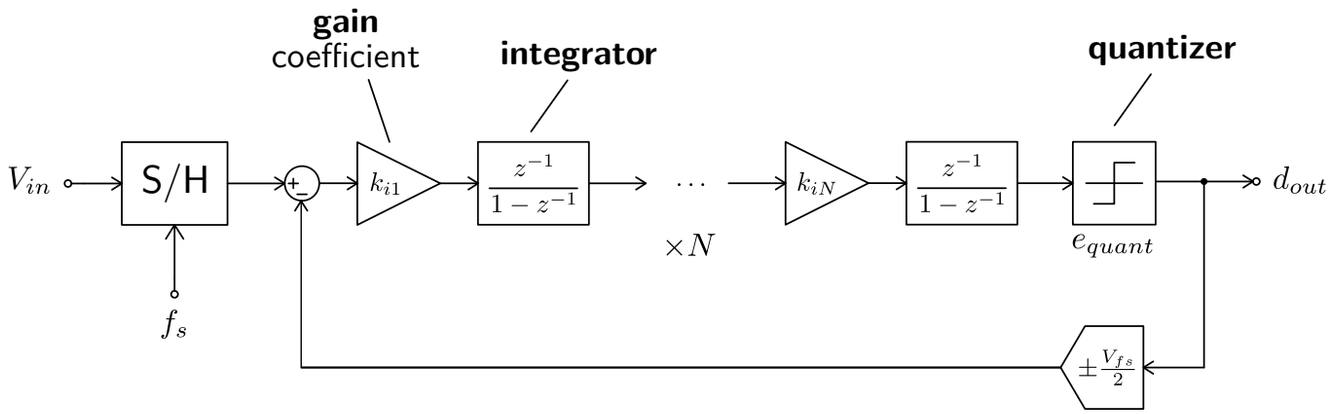


high-pass filter
(quantization noise shaping)

$$D_{out}(z) = z^{-N} V_{in}(z) + \left(1 - z^{-1}\right)^N E_{quant}(z)$$

Analog vs Digital DSM





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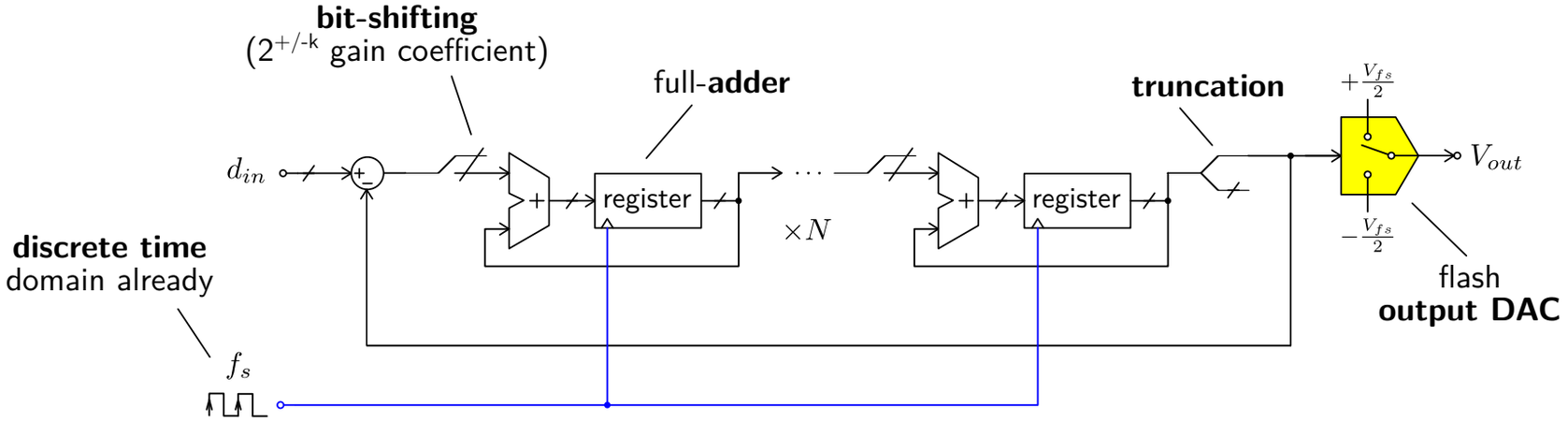
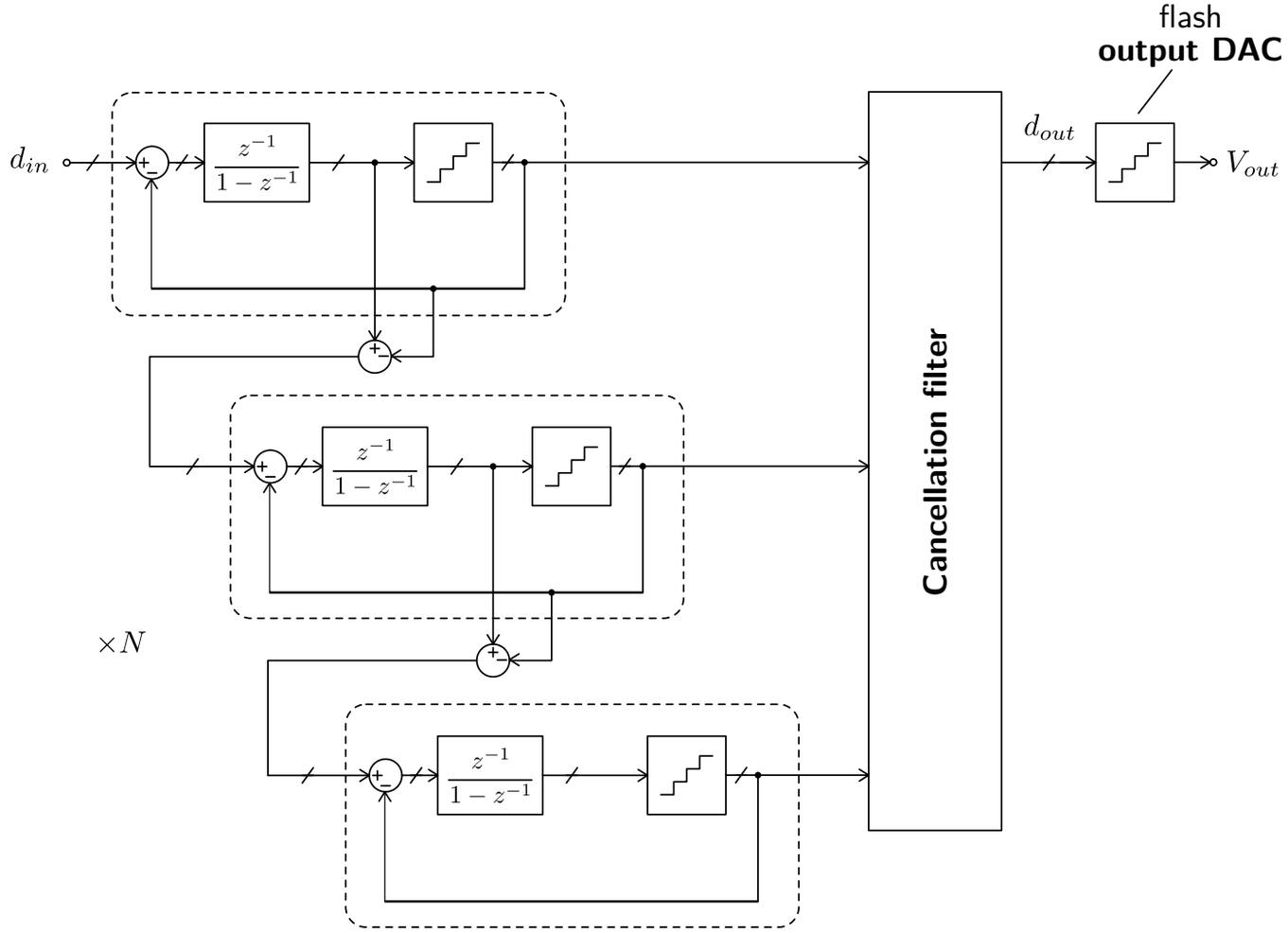


- ▲ Flash output DAC with **reduced** number of levels
- ▼ Possibility of loop **instability** for N>2

Multi-Stage Noise Shaping (MASH)

- **Cascade** of 1st-order DSM
- **Forward** digital cancellation
- Intrinsically **stable**



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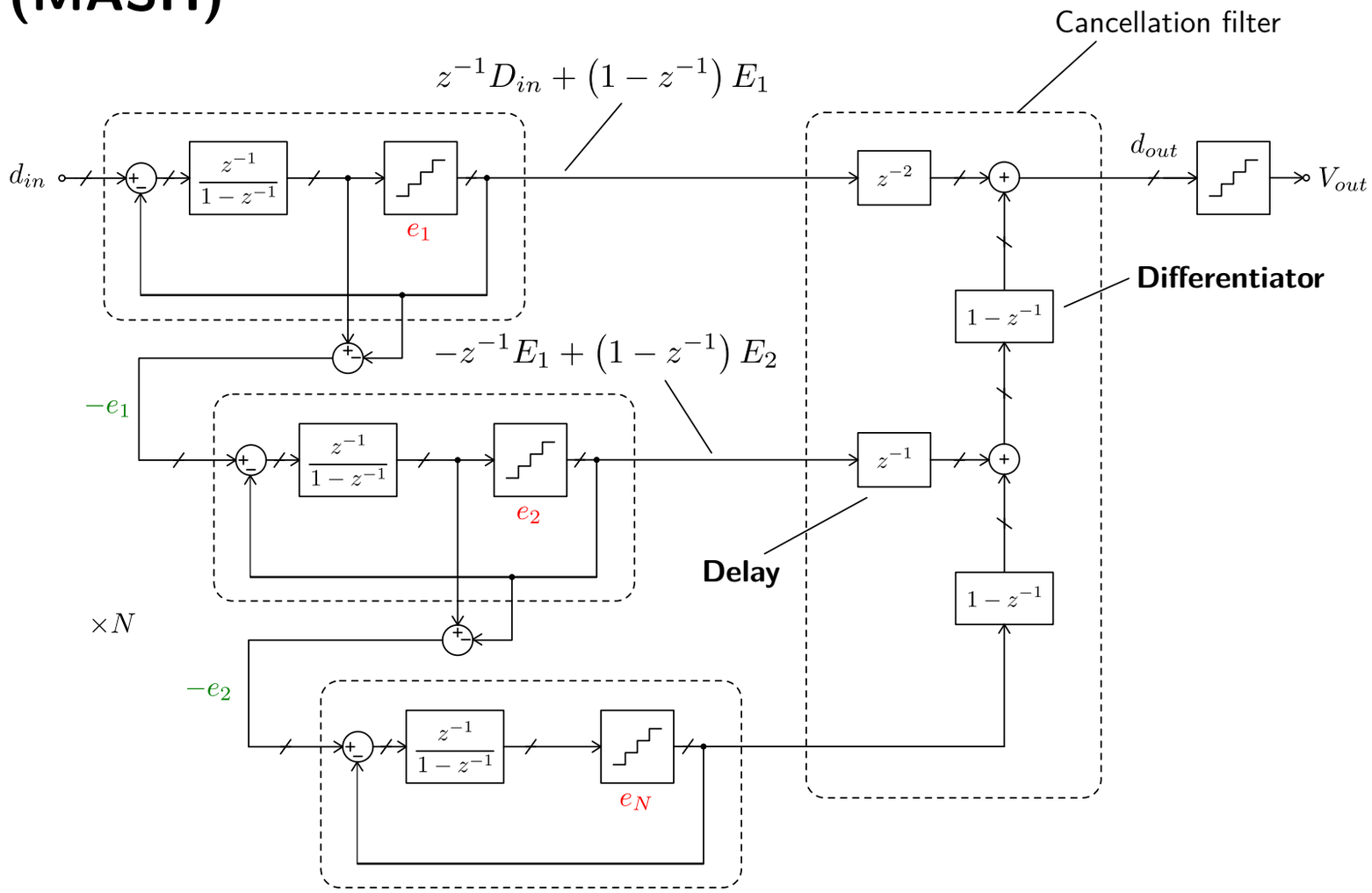
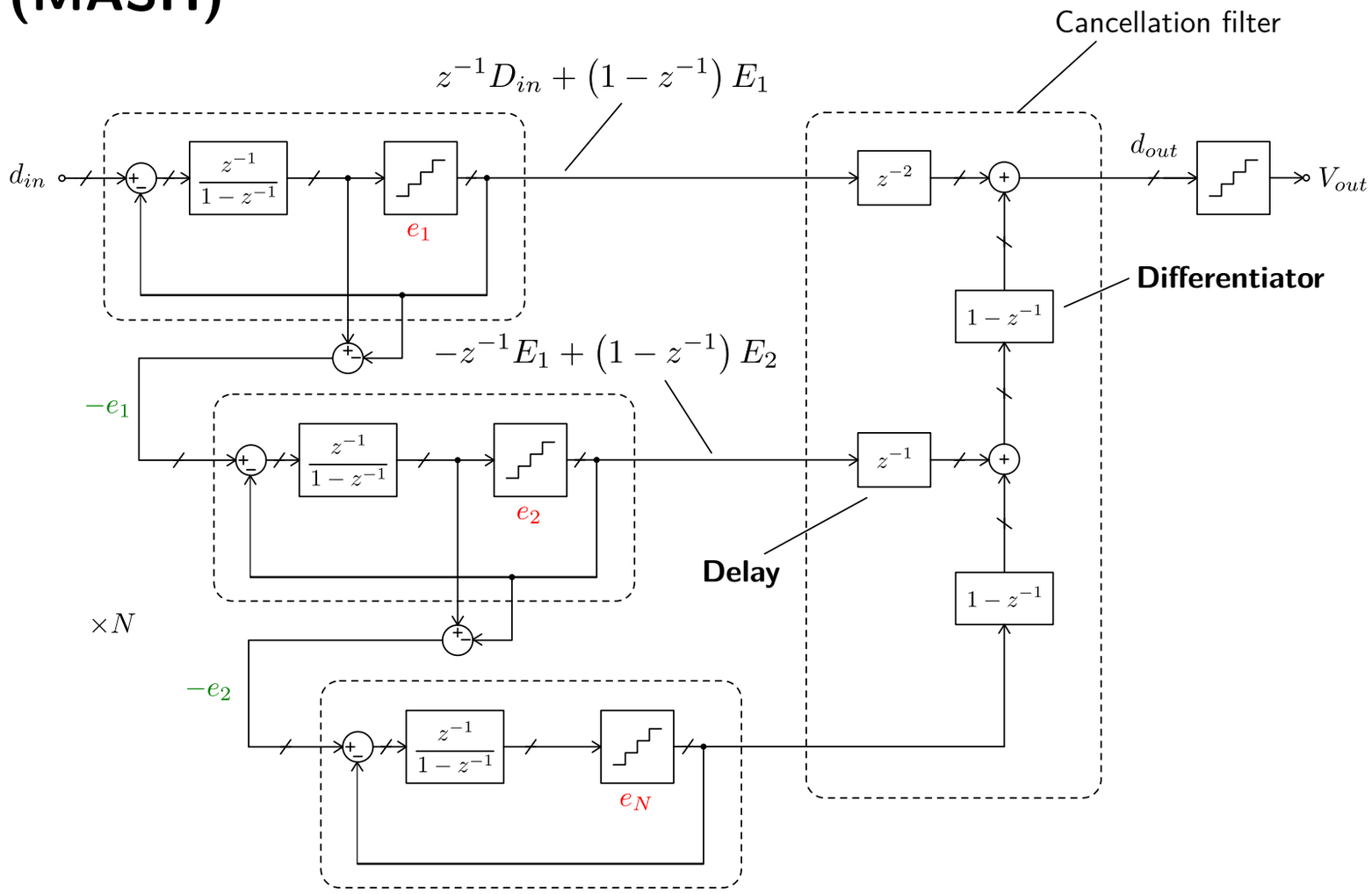


$$D_{out} = z^{-2}\left[z^{-1}D_{in} + \left(1 - z^{-1}\right)E_1\right] + \left(1 - z^{-1}\right)z^{-1}\left[-z^{-1}E_1 + \left(1 - z^{-1}\right)E_2\right] + \left(1 - z^{-1}\right)^2\left[-z^{-1}E_2 + \left(1 - z^{-1}\right)E_N\right]$$

Multi-Stage Noise Shaping (MASH)

- **Cascade** of 1st-order DSM
- **Forward** digital cancellation
- ▲ Intrinsically **stable**
- Each DSM **cancels** quantization errors of previous one
- ▼ Not suitable for ADC DSM due to **mismatching** at cancellation stage
- ▲ **N-order** noise **shaping:**

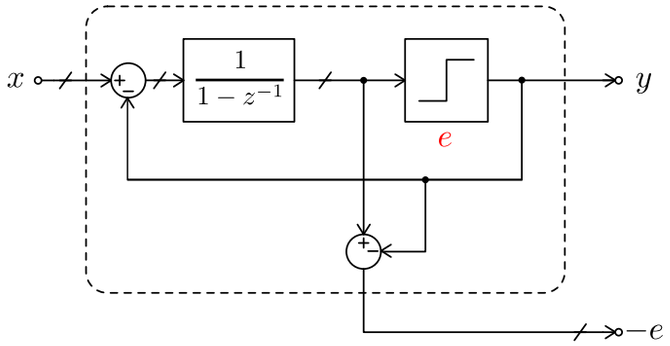
$$D_{out} = z^{-N} D_{in} + \left(1 - z^{-1}\right)^N E_N$$



$$D_{out} = z^{-2}\left[z^{-1}D_{in} + \cancel{\left(1 - z^{-1}\right)E_1}\right] + \left(1 - z^{-1}\right)z^{-1}\left[\cancel{-z^{-1}E_1} + \cancel{\left(1 - z^{-1}\right)E_2}\right] + \left(1 - z^{-1}\right)^2\left[\cancel{-z^{-1}E_2} + \left(1 - z^{-1}\right)E_N\right]$$

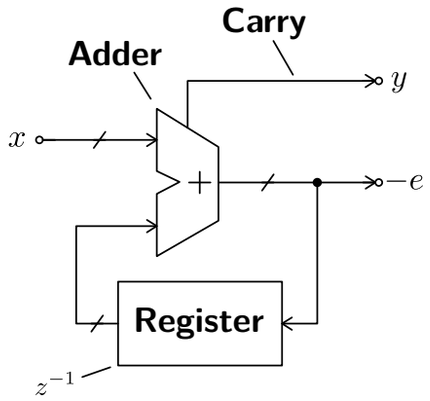
Multi-Stage Noise Shaping (MASH)

- Example for **1-bit quantization** 1st-order DSM stage:



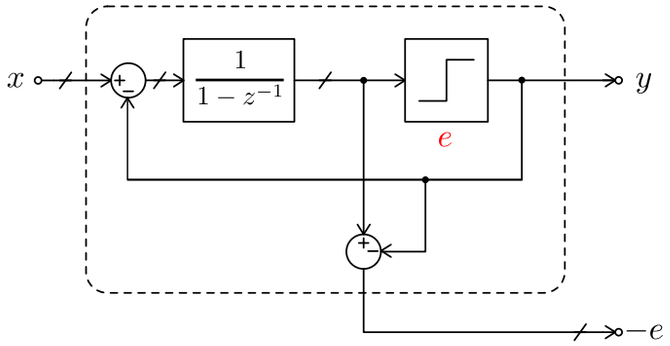
$$Y = X + \left(1 - z^{-1}\right) E$$

- **Compact** solution:



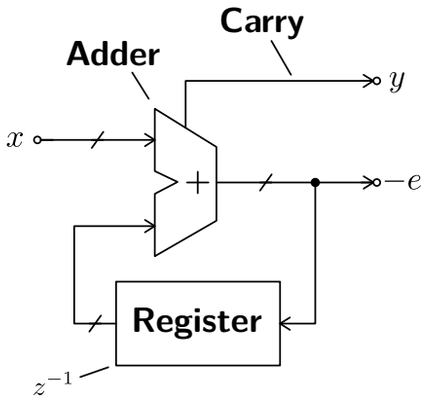
Multi-Stage Noise Shaping (MASH)

- Example for **1-bit quantization** 1st-order DSM stage:



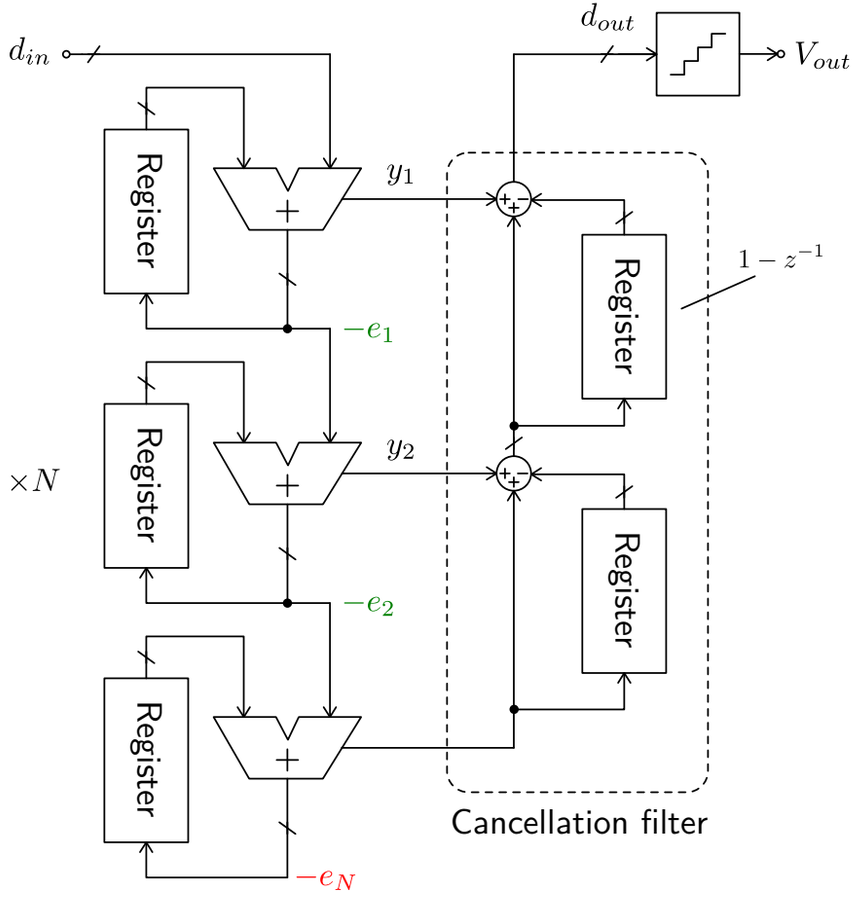
$$Y = X + \left(1 - z^{-1}\right) E$$

- **Compact** solution:

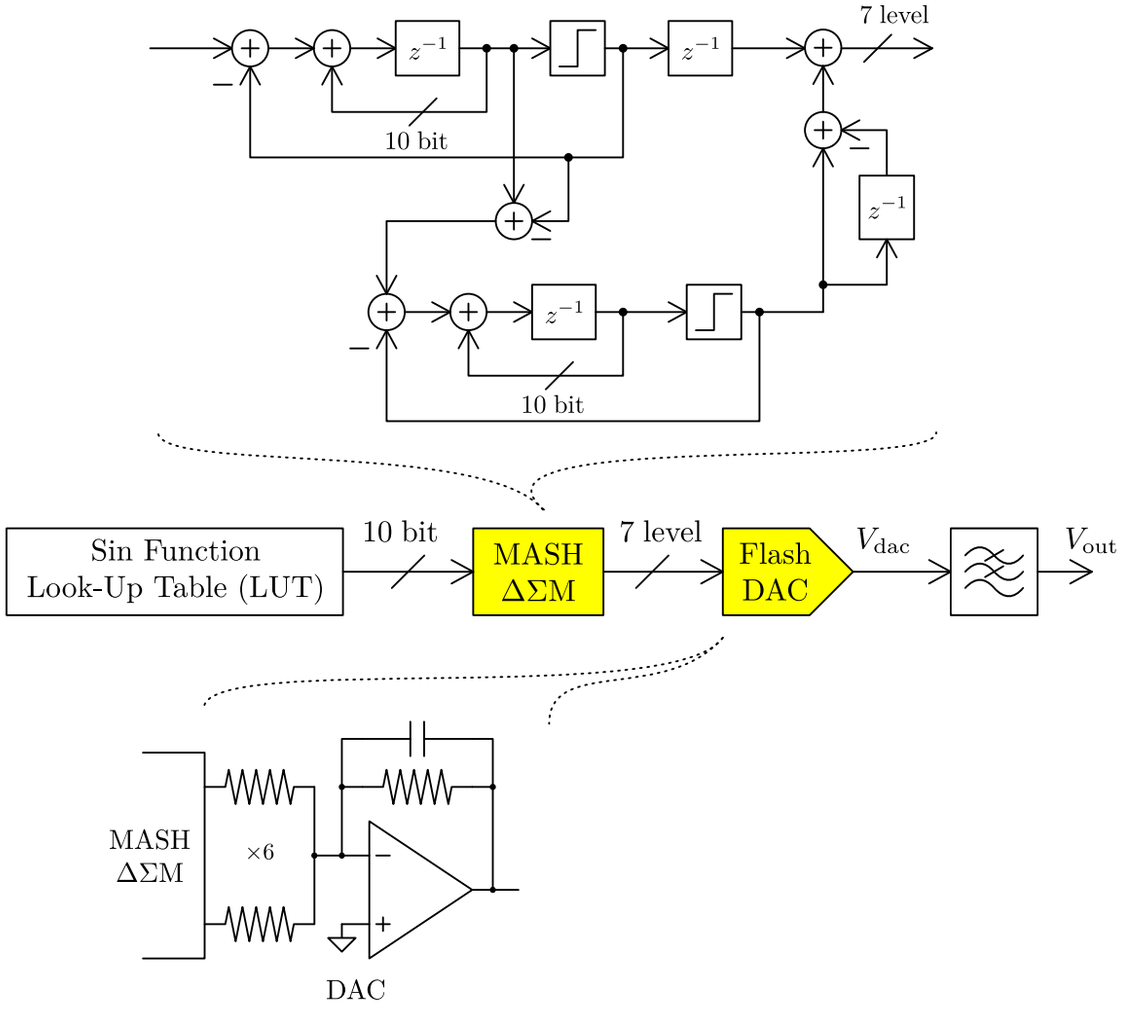


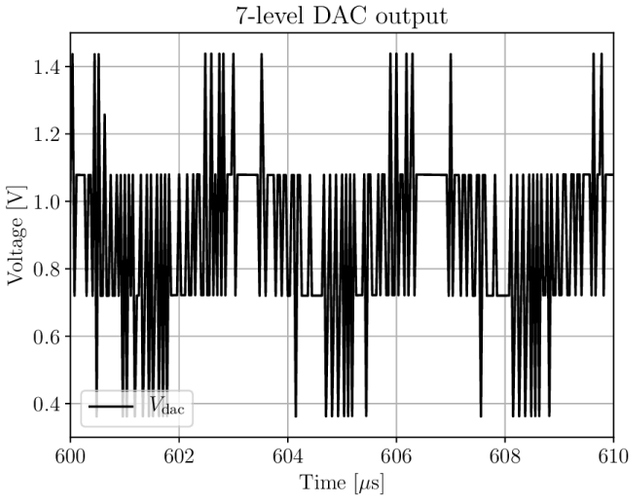
$$Y_1 = D_{in} + \left(1 - z^{-1}\right) E_1$$

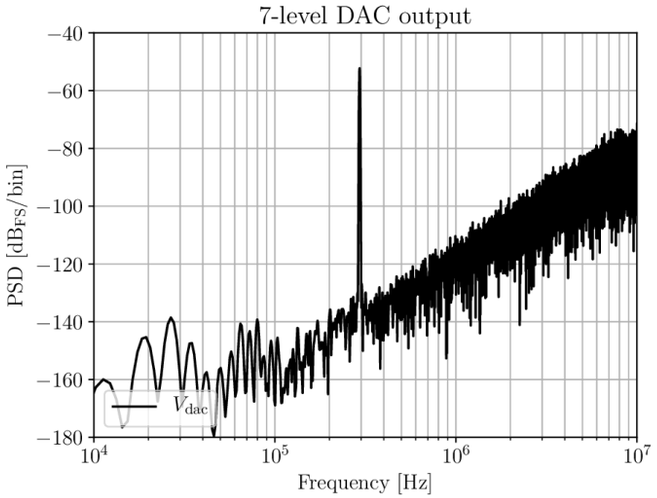
$$Y_2 = -E_1 + \left(1 - z^{-1}\right) E_2$$



Example of Application: Periodic Function Generator







Example of Application: Periodic Function Generator