2. ADC Architectures and CMOS Circuits

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1 ADC Classification

2 Flash Converters

3 Sub-Ranging, Time-Interleaving and Pipelining

4 Successive-Approximation Converters

5 Integrating Techniques

6 Delta-Sigma Modulation

7 Time-Domain Converters

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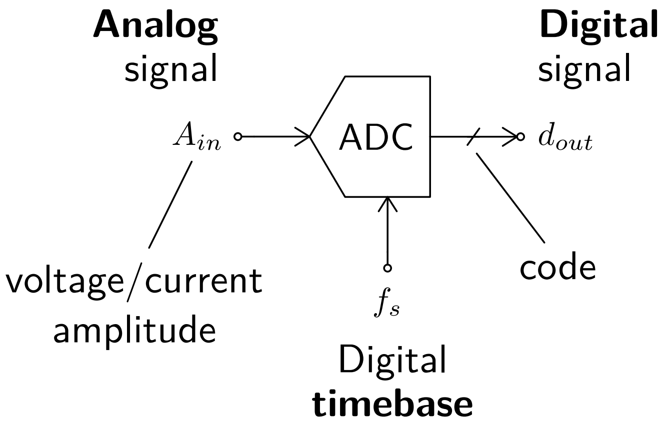
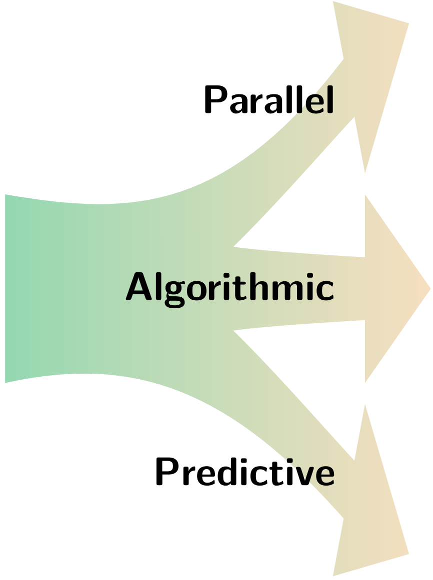
ADC Families

- Classification based on **architecture** approach:





Flash
Sub-ranging
Interleaved
Pipeline
SAR
Integrating
Delta-Sigma
...and **many more**!

- Distinctive **characteristics**:
  - Feedforward vs feedback control
  - Single vs multiple stages
  - Amplitude vs time domains

- Typically **mixed** solutions...

ADC Evolution

$$FOM_W \doteq \frac{P_D}{f_{nyq} \cdot 2^{ENOB}}$$

$$FOM_W \simeq 5\mu\text{J/conv-step}$$

$$FOM_S \doteq SNDR_{max} + 10\log\frac{f_{nyq}}{2P_D}$$

$$FOM_S \simeq 85\text{dB}$$

EPSCO DATRAC, B.M. Gordon, 1953

11bit 50kSps 500W SAR ADC

0.5m x 0.4m x 0.65m, 70kg

Vacuum tube technology

↗ W. Kester
Analog-Digital Conversion
analog.com

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$FOM_S \simeq 85\text{dB}$

+70 years

+100dB!

e.g. 500μW ($\div 10^6$) and 500MSps ($\times 10^4$)

Solid-state technology

EPSCO DATRAC, B.M. Gordon, 1953

11bit 50kSps 500W SAR ADC

0.5m x 0.4m x 0.65m, 70kg

Vacuum tube technology

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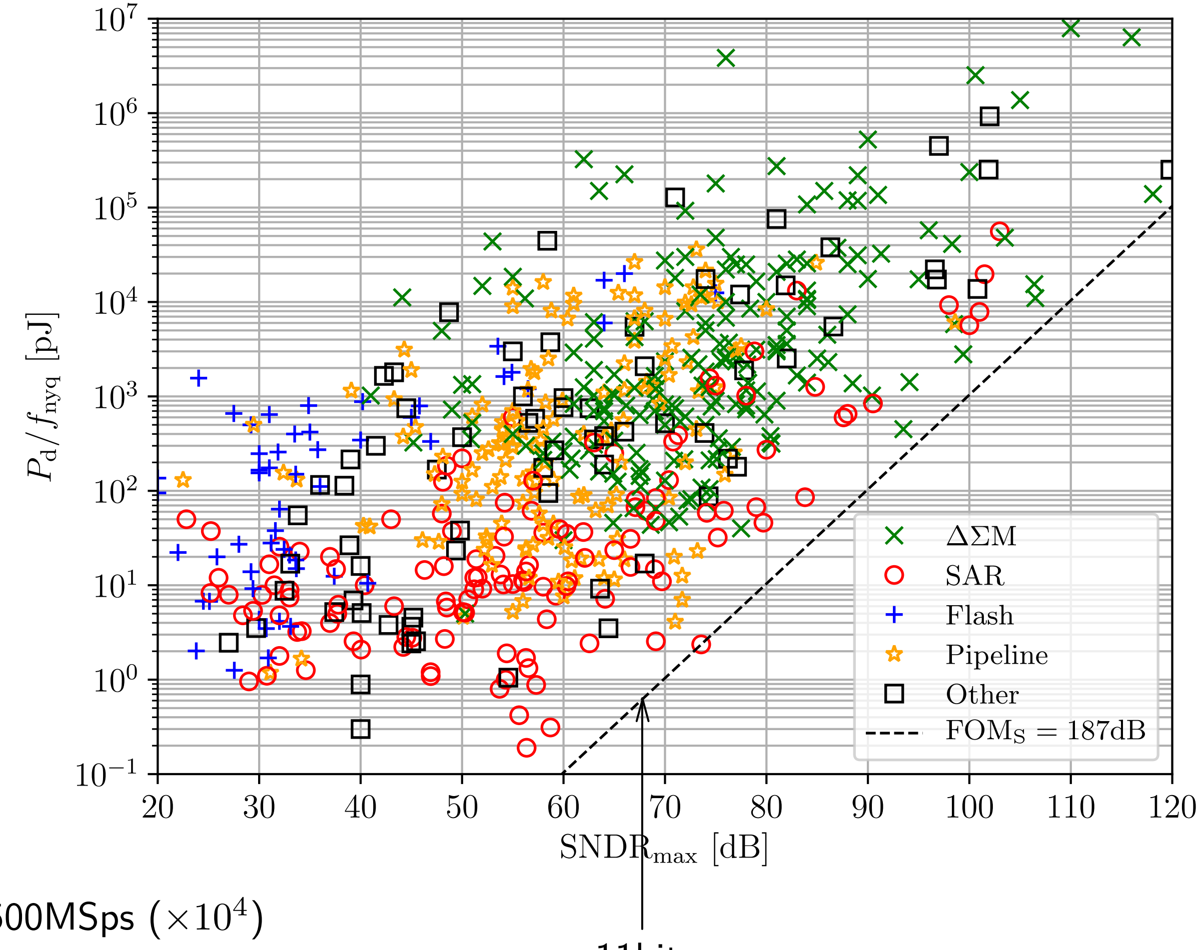
github.com/bmurmann/ADC-survey



ADC Evolution

- **Performance** enhancement:
  - Architecture strategy
  - Circuit design
  - Integration technology

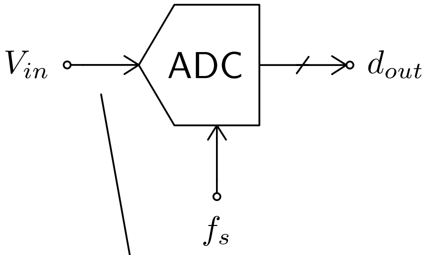
- Still room for further **improvement?**

$$SNR_{max} = \frac{(V_{FS}/2\sqrt{2})^2}{KT/C_s}\,\frac{f_s}{f_{nyq}}$$

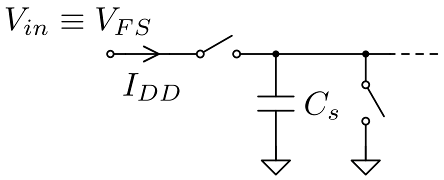
$$P_{min} = \underbrace{C_s V_{FS} f_s}_{I_{DD}} V_{DD}$$

$$P_{min}|_{V_{FS}\equiv V_{DD}} \simeq C_s f_s V_{FS}^2$$

$$E_{min} \doteq \frac{P_{min}}{f_{nyq}} \equiv 8KT\,SNR_{max}$$



Considering power delivered by the signal source only:



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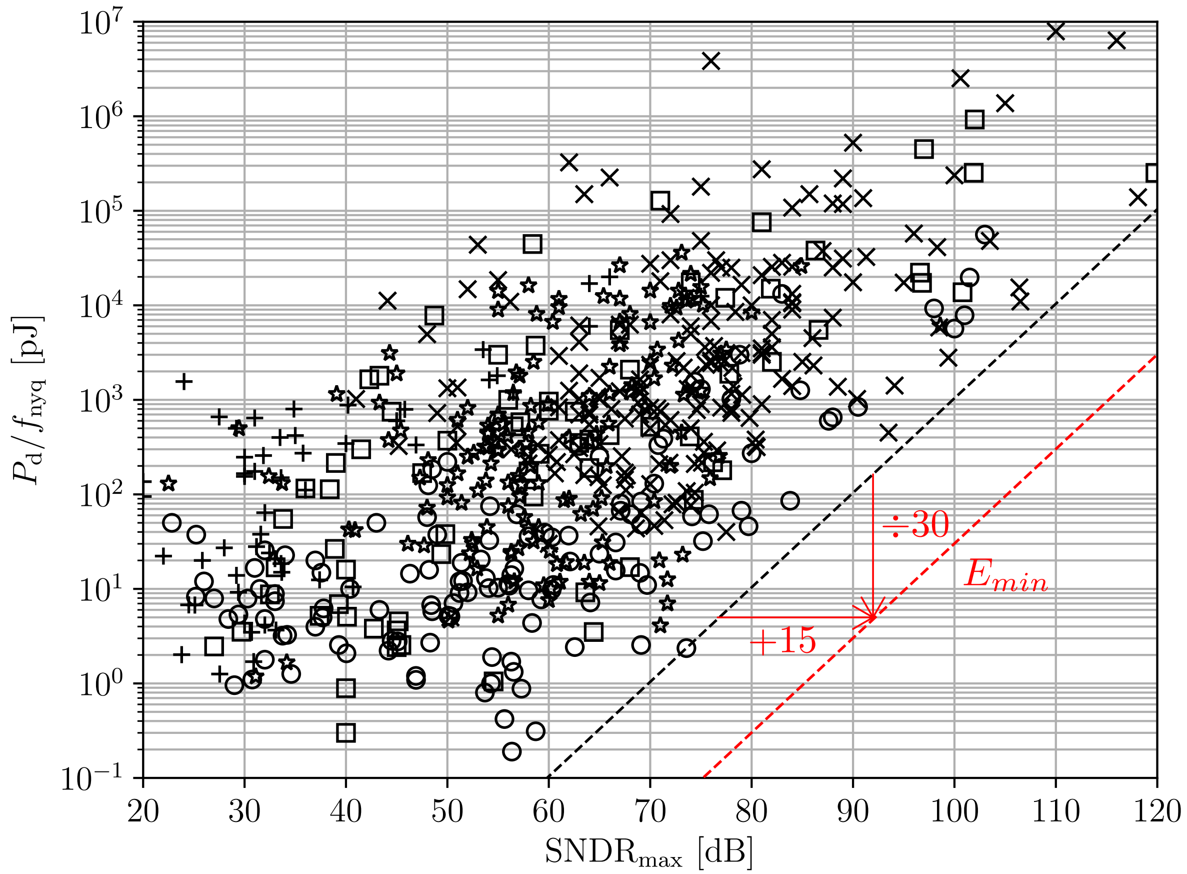

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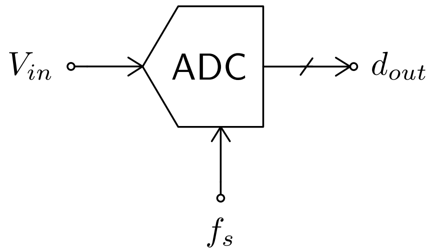
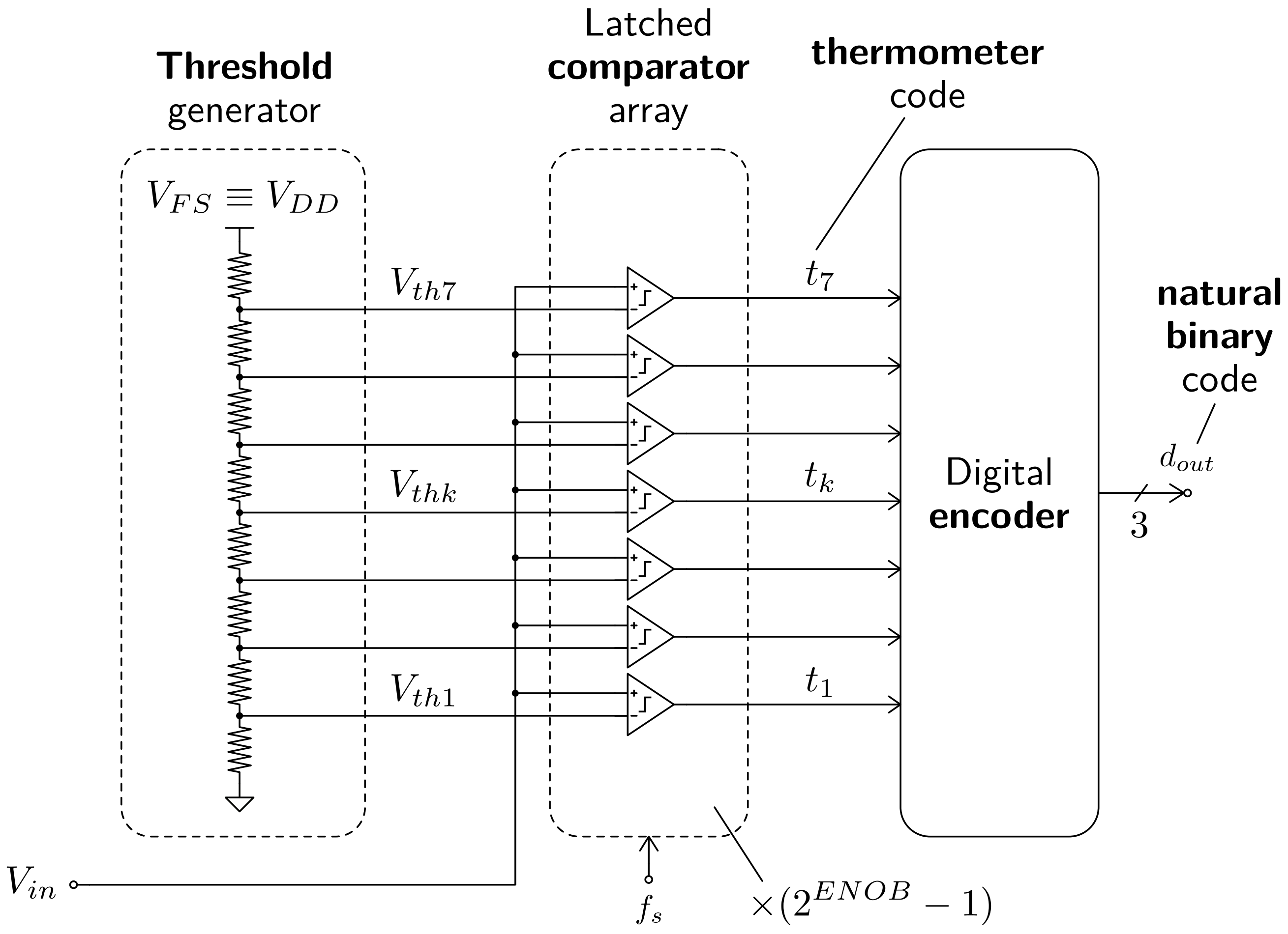
Basic Flash Architecture

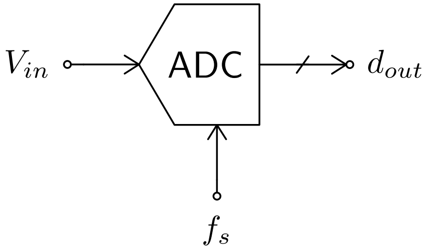


- Building **blocks**:



e.g. **single-ended** 3-bit flash ADC

Basic Flash Architecture



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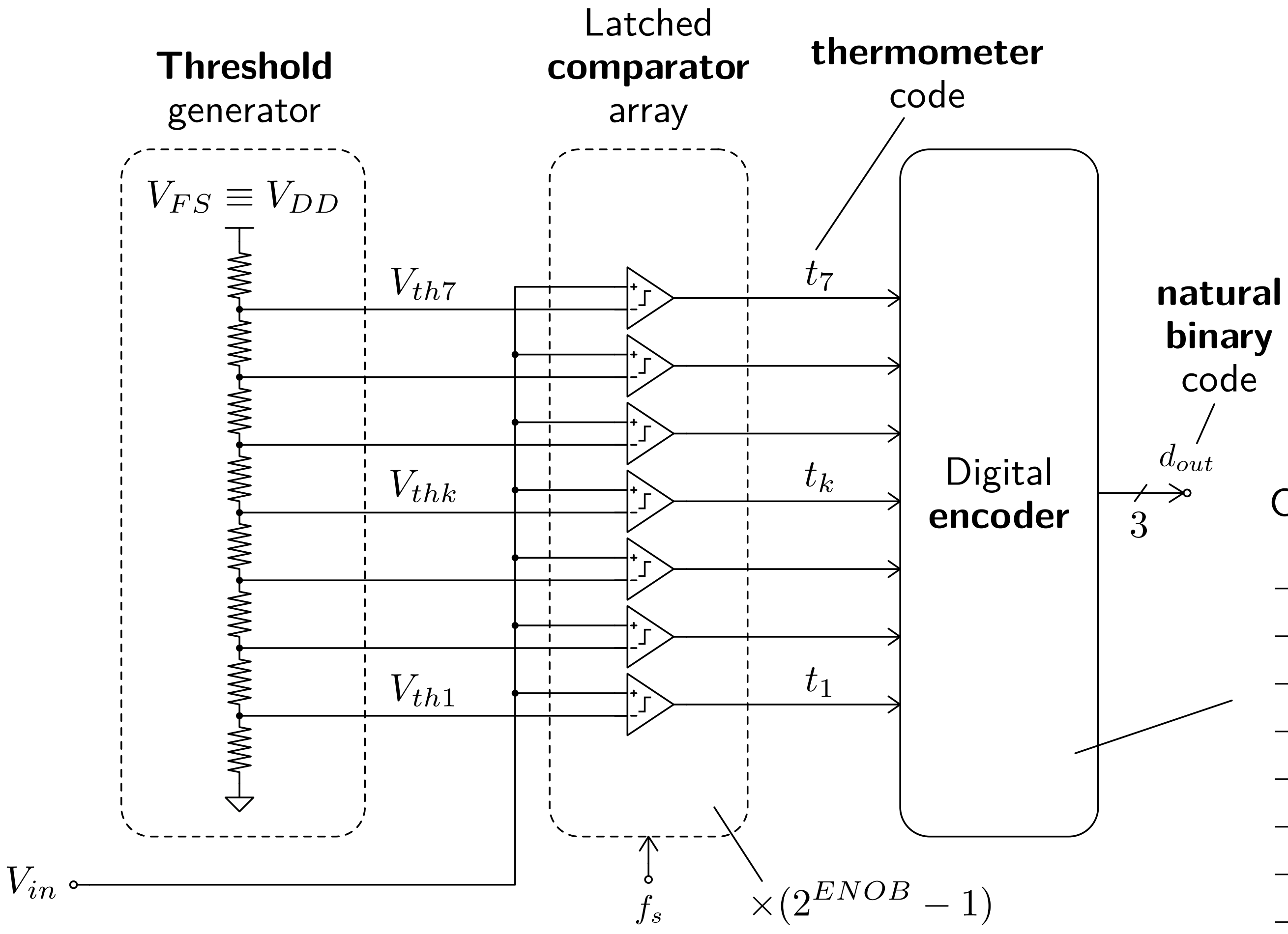


- ▲ 1 clock cycle conversion **time**
- ▼ Area and power **scaling** by 2^{ENOB}
- ▼ Distortion due to technology **mismatching**

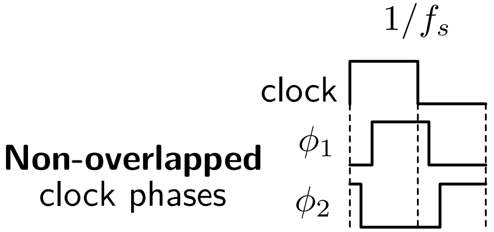
e.g. **single-ended** 3-bit flash ADC

Combinational-only logic:

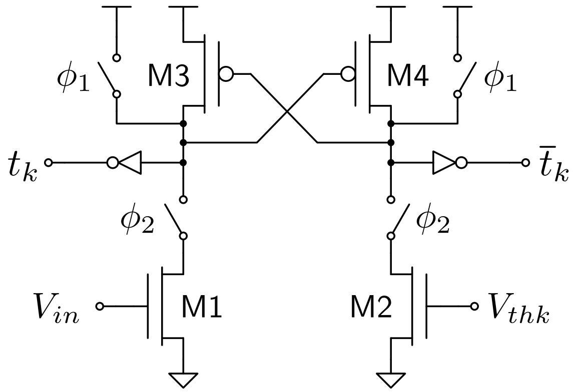
t_7	t_6	t_5	t_4	t_3	t_2	t_1	d_{out}<2:0>
0	0	0	0	0	0	0	000
0	0	0	0	0	0	1	001
0	0	0	0	0	1	1	010
0	0	0	0	1	1	1	011
0	0	0	1	1	1	1	100
0	0	1	1	1	1	1	101
0	1	1	1	1	1	1	110
1	1	1	1	1	1	1	111

Latched Comparator Design

- Compact **CMOS** circuit:



$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$



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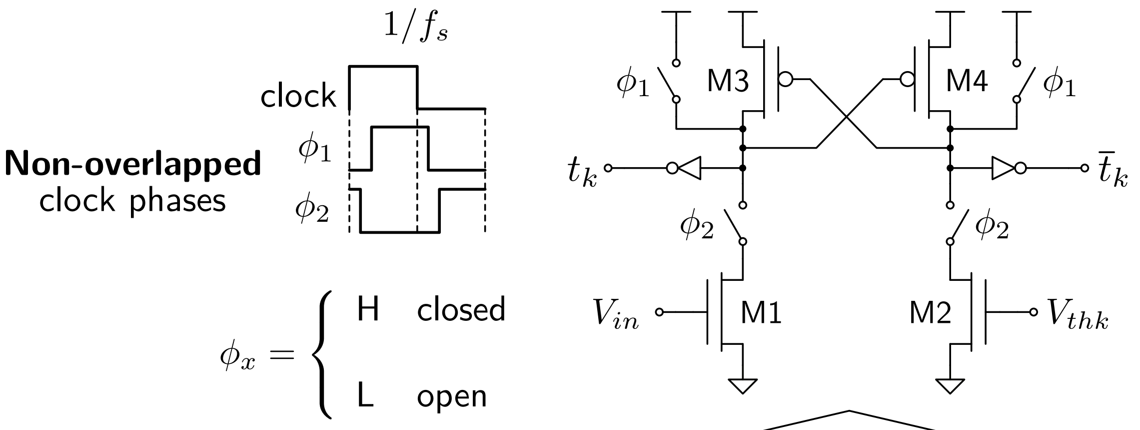
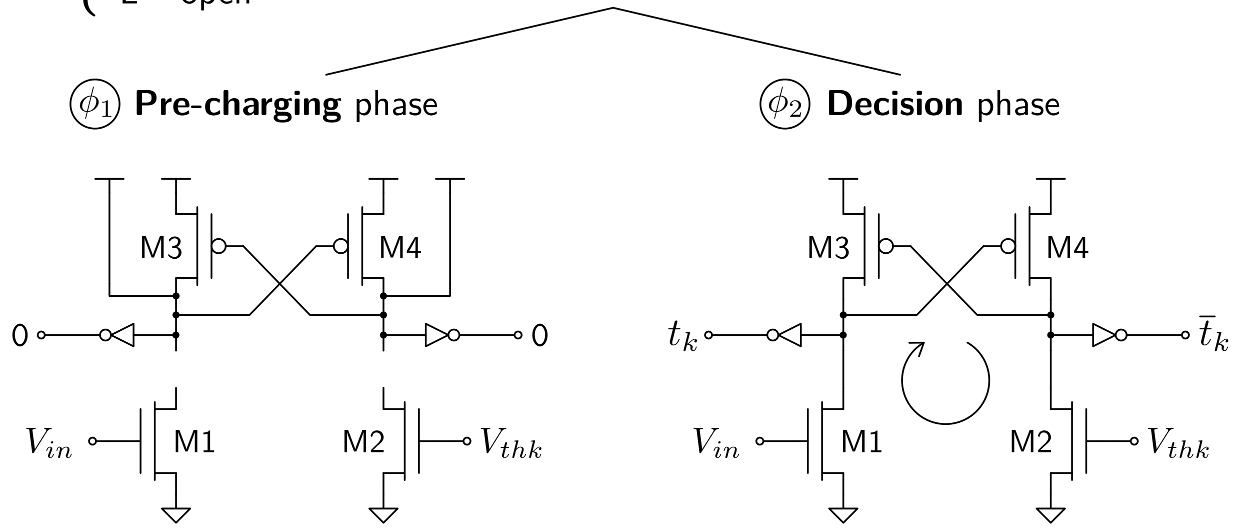


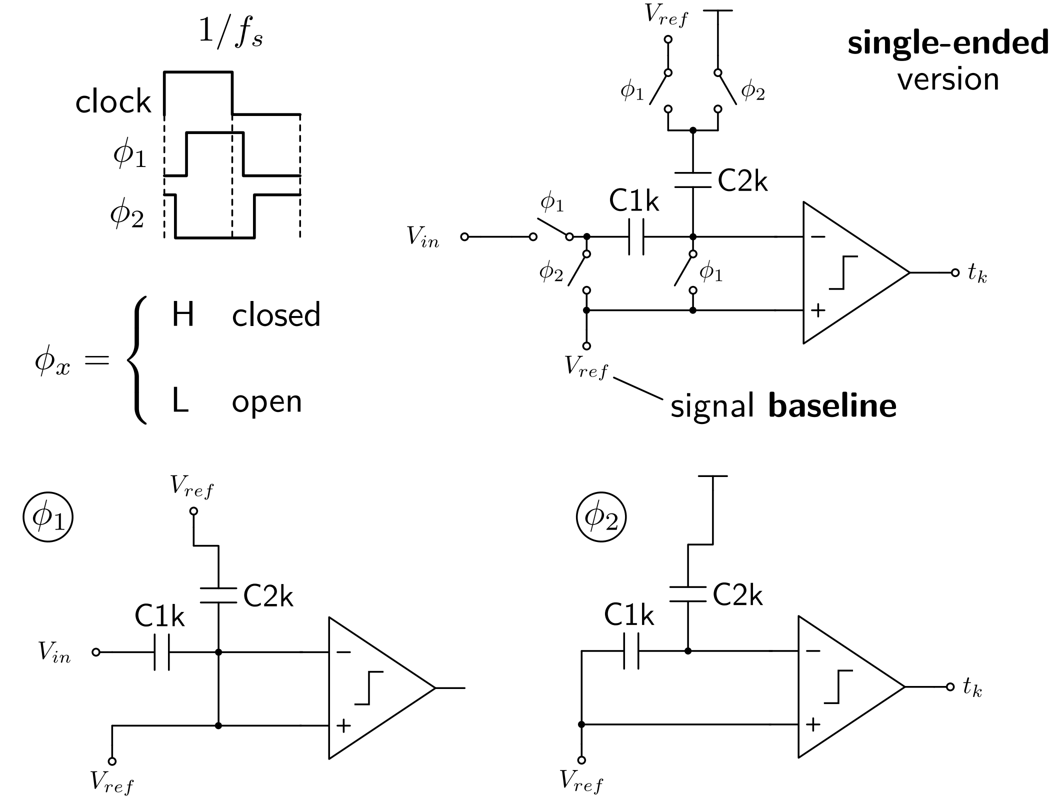
- ▲ **High-speed** operation
- ▼ Each comparator crosses at **different** threshold V_{thk}
- ▼ Threshold voltage **offset**?



- **Positive feedback** to speed-up comparison
- **Symmetrical** loading

Comparator Optimization

- By attaching an array of switched-capacitor (SC) **level shifters**:



$$t_k = sign\left[V_{ref} - \left(V_{ref} + \frac{C_{1k}}{C_{1k}+C_{2k}}(V_{ref} - V_{in}) + \frac{C_{2k}}{C_{1k}+C_{2k}}(V_{DD} - V_{ref})\right)\right]$$

Comparator Optimization

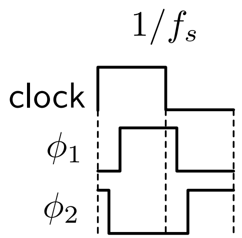
- By attaching an array of switched-capacitor (SC) **level shifters**:

$$t_k = \frac{C_{1k}}{C_{1k} + C_{2k}} sign \left[(V_{in} - V_{ref}) - \frac{C_{2k}}{C_{1k}} (V_{DD} - V_{ref}) \right]$$

effective signal

effective k-threshold

- ▲ All comparators latch at the **same** level (V_{ref})
- ▲ **Single** comparator design
- ▲ Low quiescent **power** (resistor-less thresholds)
- ▼ Capacitor **area** overhead
- ▼ Input **capacitance** increased



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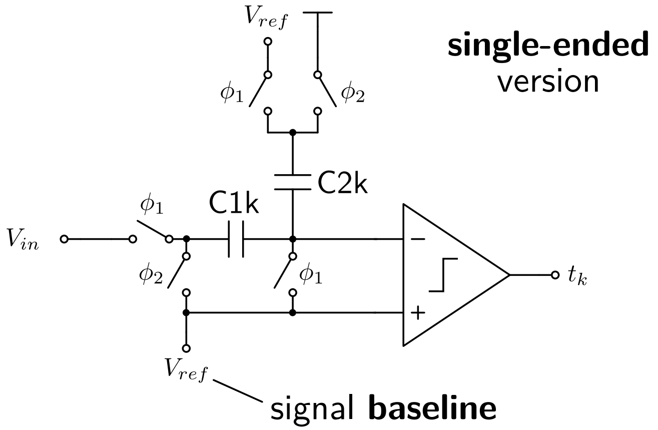

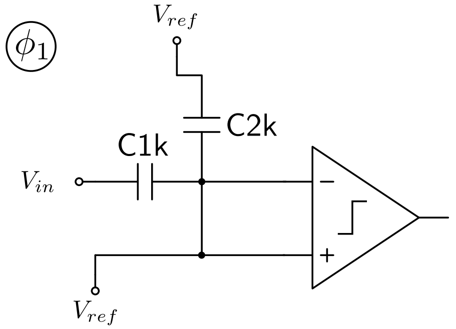

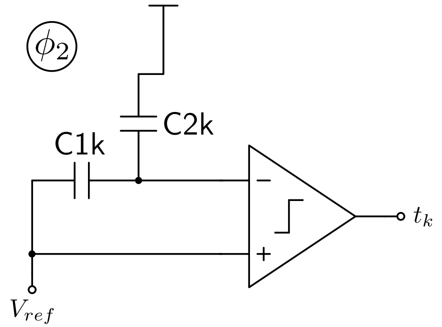

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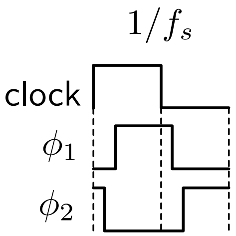

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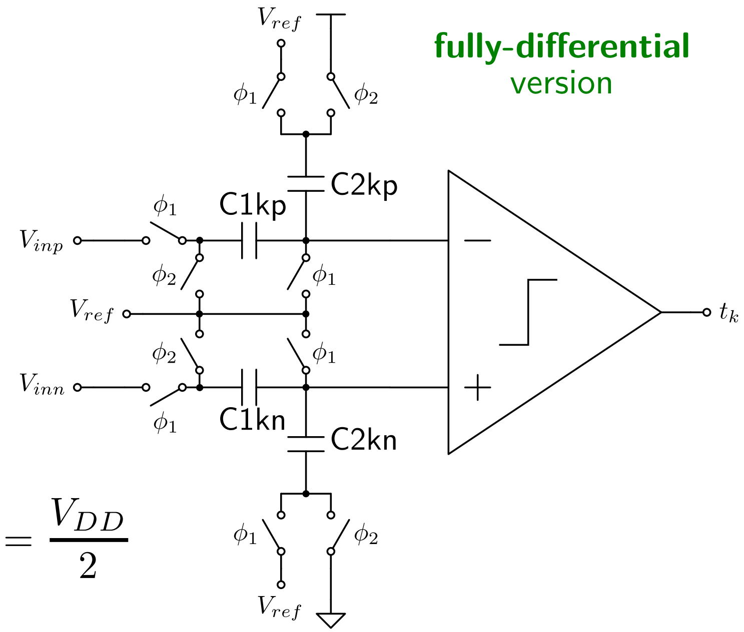
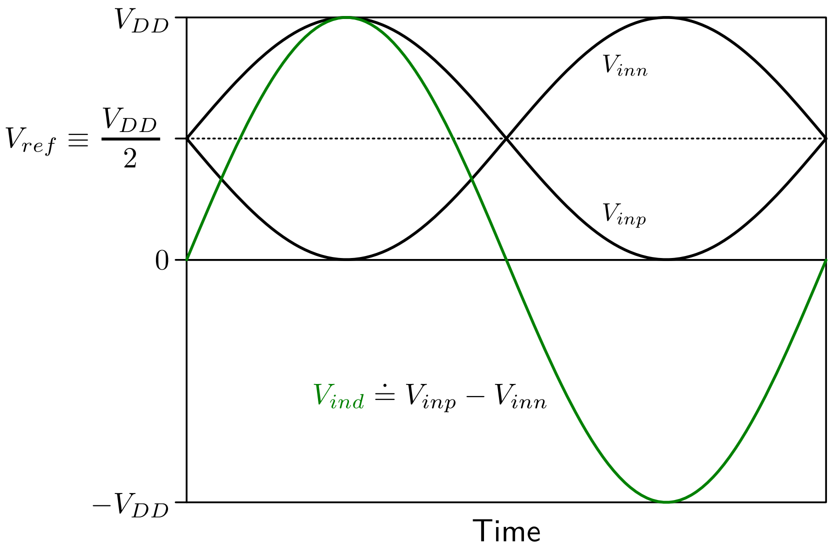


$$V_{ref} = \frac{V_{DD}}{2}$$

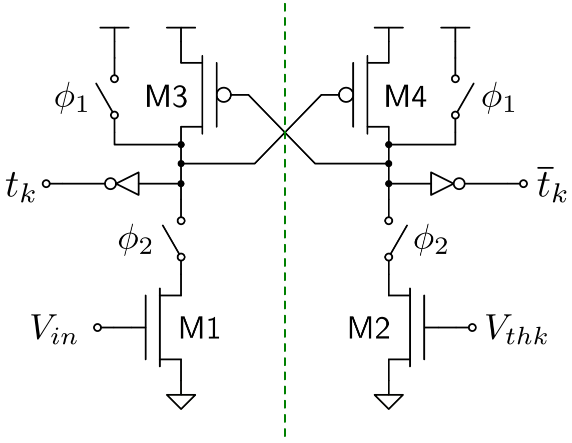
- ▲ Interference **rejection**
- ▲ **Full-scale** extension (+6dB)
- ▲ **SNR** enhancement (+3dB)
- ▲ **Distortion** cancellation (even harmonics)



- ▼ **Area** and **power** overheads (x2)
- ▼ Higher **symmetry** requirements

Comparators Offset

- MOSFET V_{TH} **mismatching** effects:



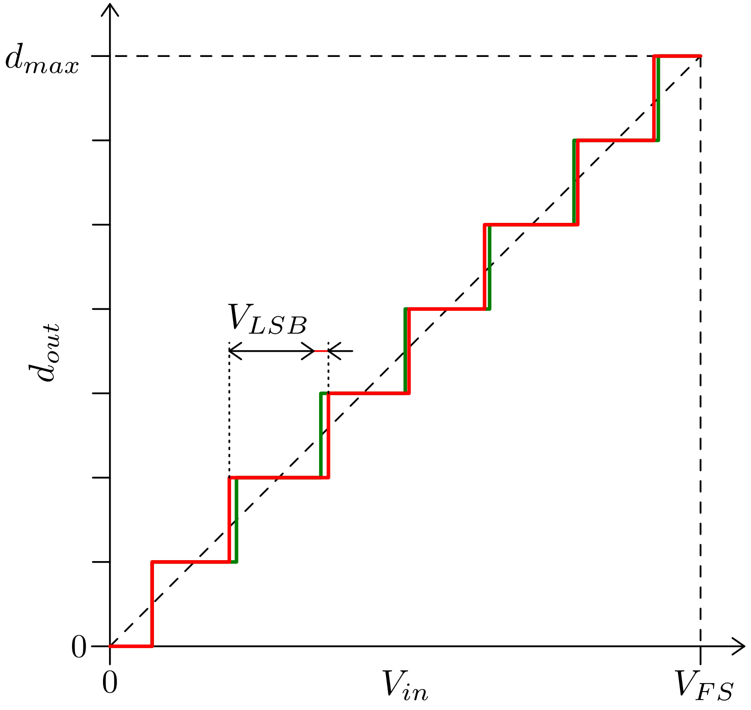
$$\sigma^2(V_{off}) = \sigma^2(\Delta V_{TH1,2}) + \left(\frac{g_{mg3,4}}{g_{mg1,2}}\right)^2 \sigma^2(\Delta V_{TH3,4})$$

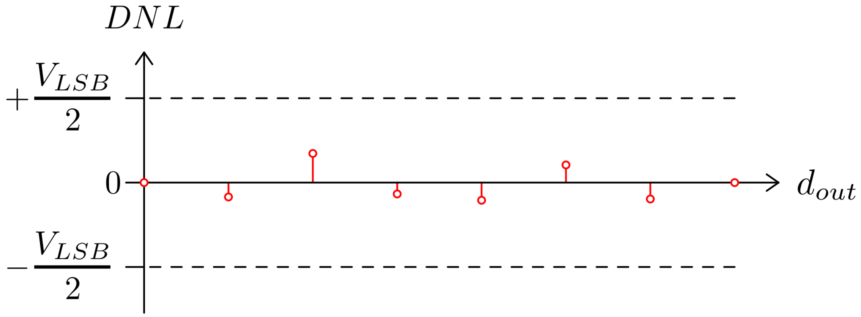
$$\sigma(V_{off}) \simeq \sigma(\Delta V_{TH1,2}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$$

CMOS **technology**

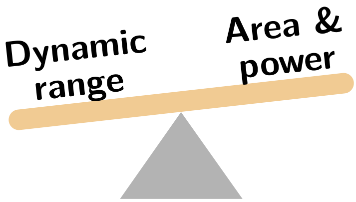
$\left(\frac{W}{L}\right)_{1,2} \gg \left(\frac{W}{L}\right)_{3,4}$

Pelgrom's Law





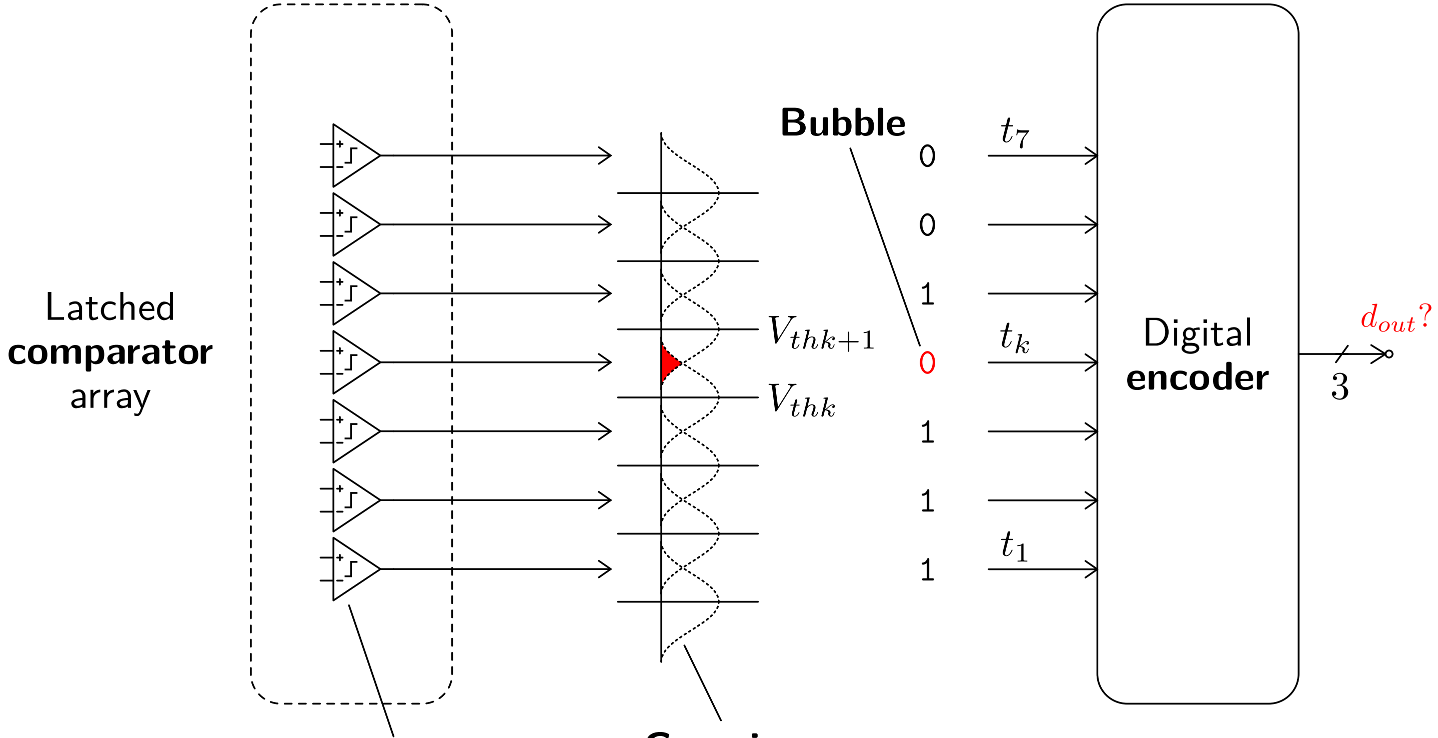
- Distortion due to **DNL**
- Transistor scaling impacts **input capacitance**



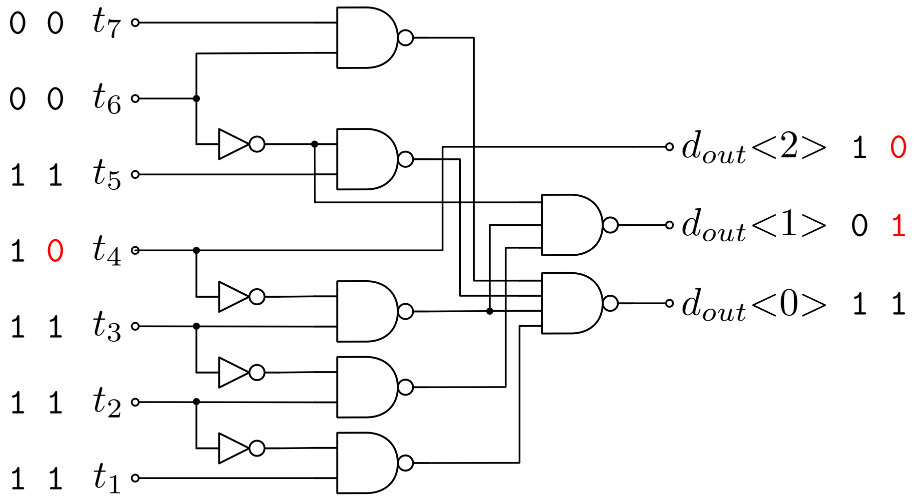
Comparators Offset

- Thermometer code **bubbles**!

- **Error propagation** depends on enconding logic implementation:



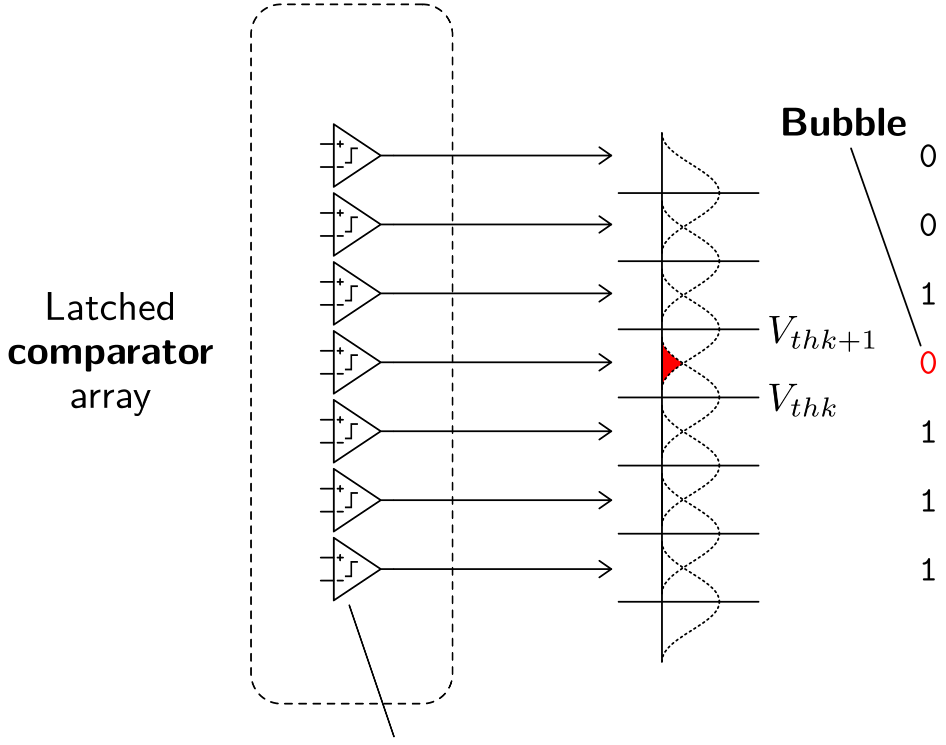
$$\sigma(V_{off}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$$



e.g. 7-to-3 NAND encoder

Comparators Offset

- Thermometer code **bubbles**!
- **Digitally-assisted** co-design:



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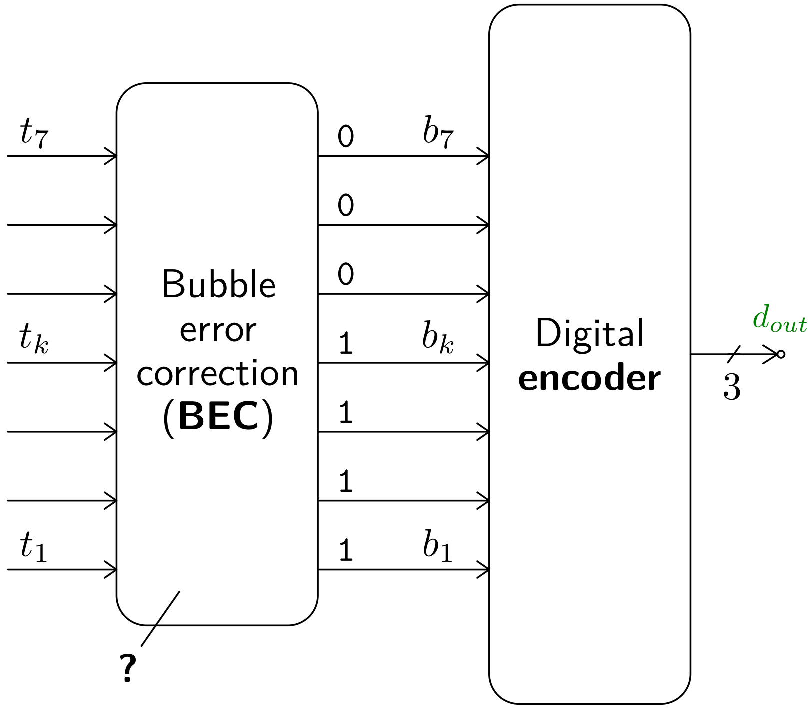

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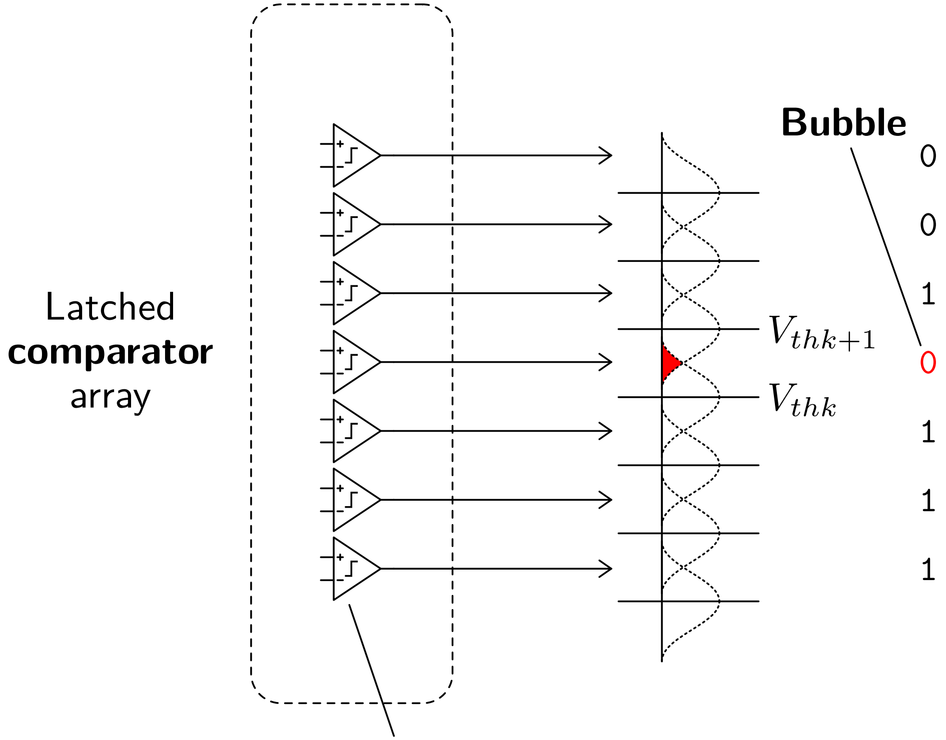

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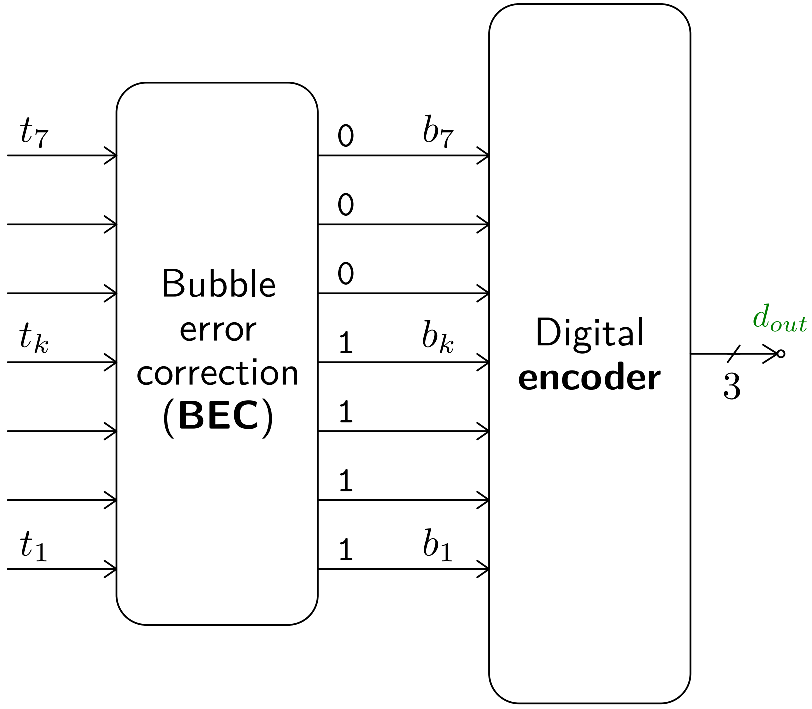


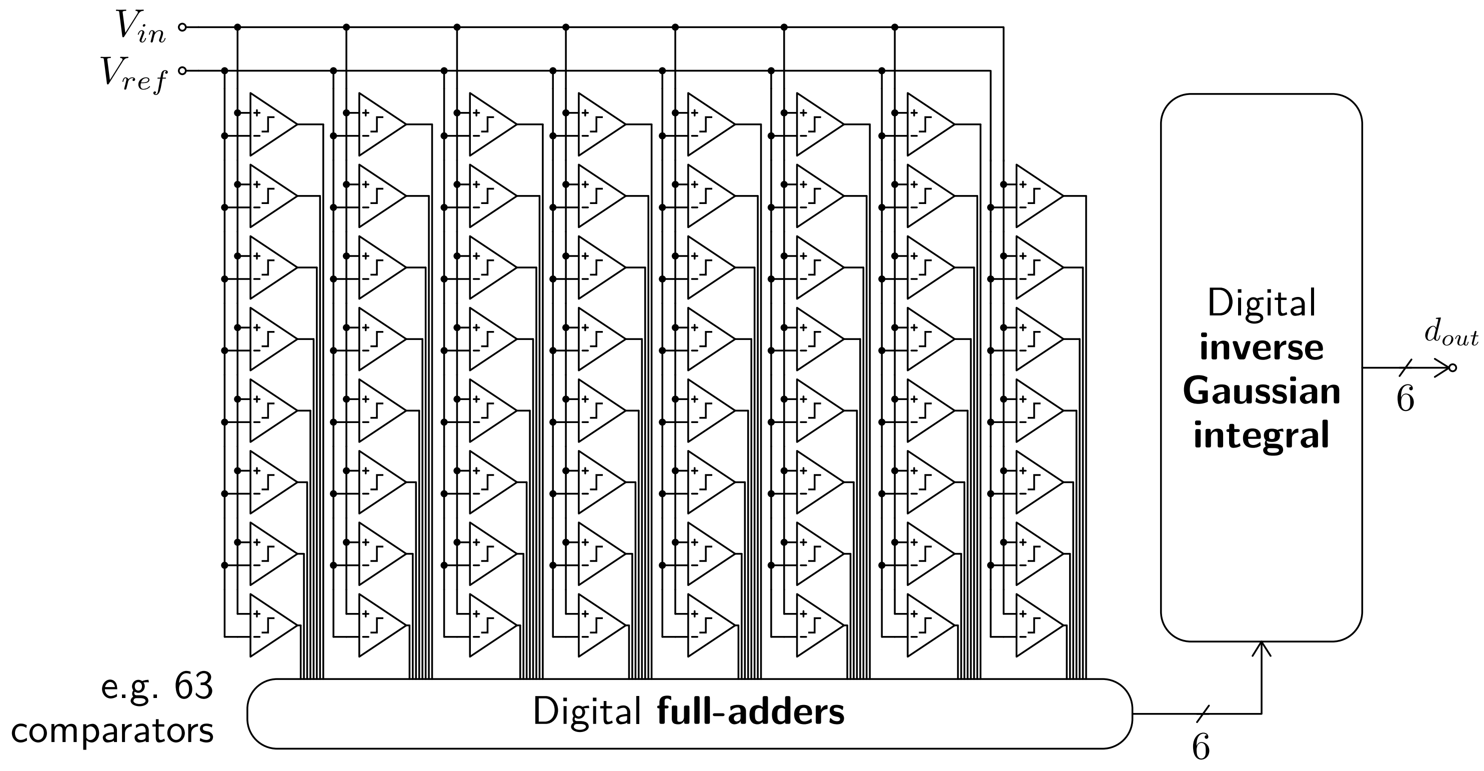
- **Analog:** (WL) large enough to limit bubble distance to 1 thermometer code
- **Digital:** compact combinational logic for BEC at each thermometer code

t_{k-1}	t_k	t_{k+1}	b_k
0	X	X	0
1	X	0	t_k
1	X	1	1

▲ Important **area** and **input capacitance** savings

Comparators Offset

- More on digitally assisted analog design: **an stochastic flash ADC**



S. Weaver, B. Hershberg and Un-Ku Moon
Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells
IEEE Transactions on Circuits and Systems I, 61(1):84-91, Jan 2014
doi.org/10.1109/TCSI.2013.2268571

Comparators Offset

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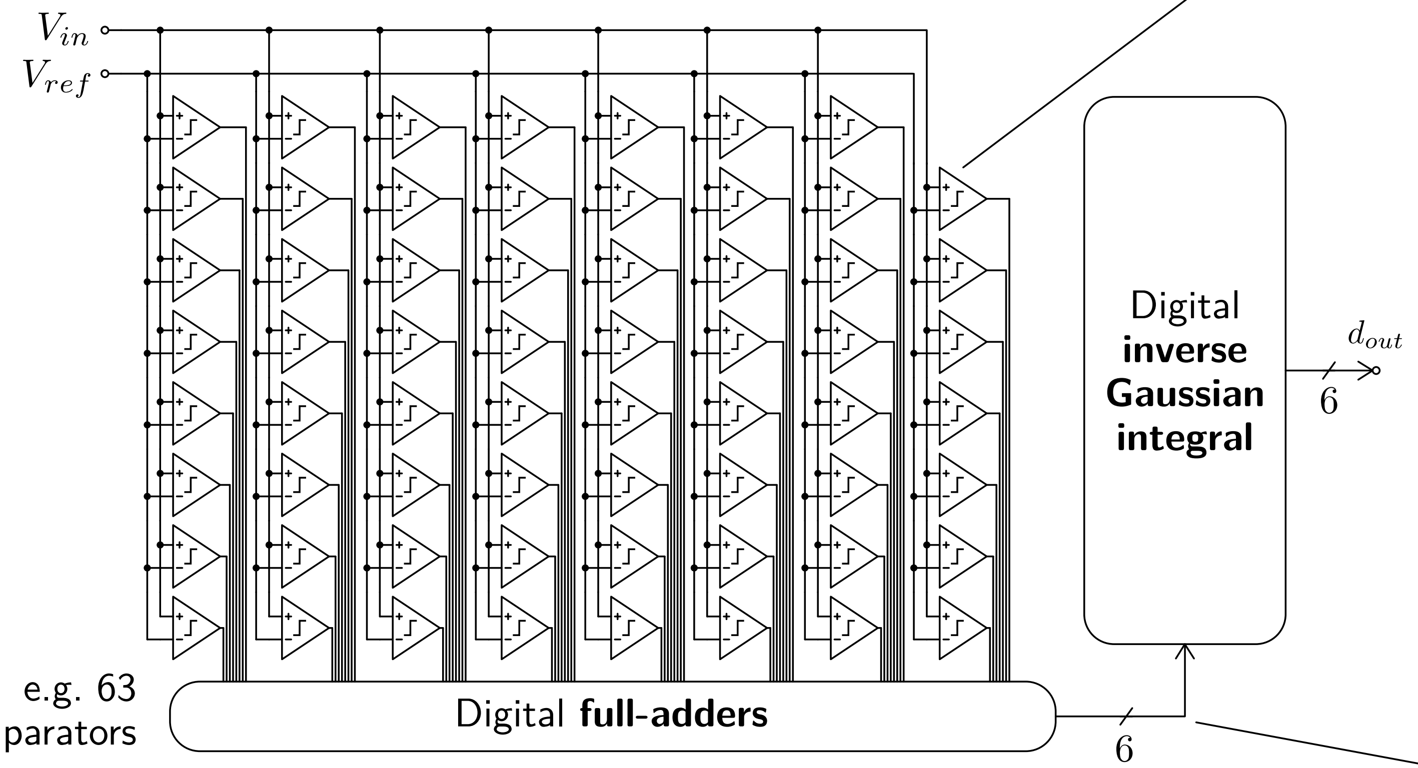
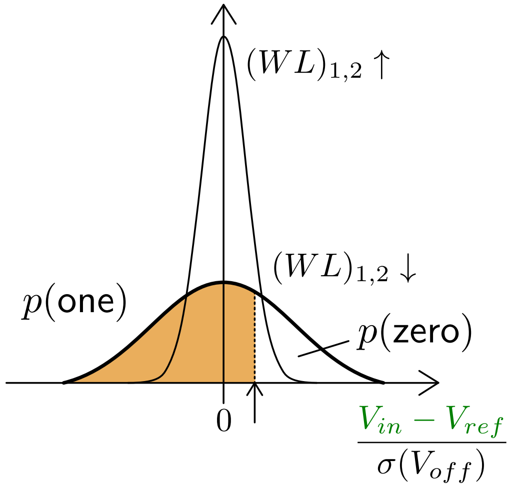


- ▲ Almost all **digital**
- ▲ **Compact** area (minimum-size transistors in comparators)
- ▼ **Non-linearity** compensation
- ▼ **Power** consumption



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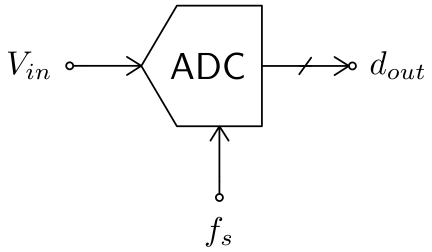
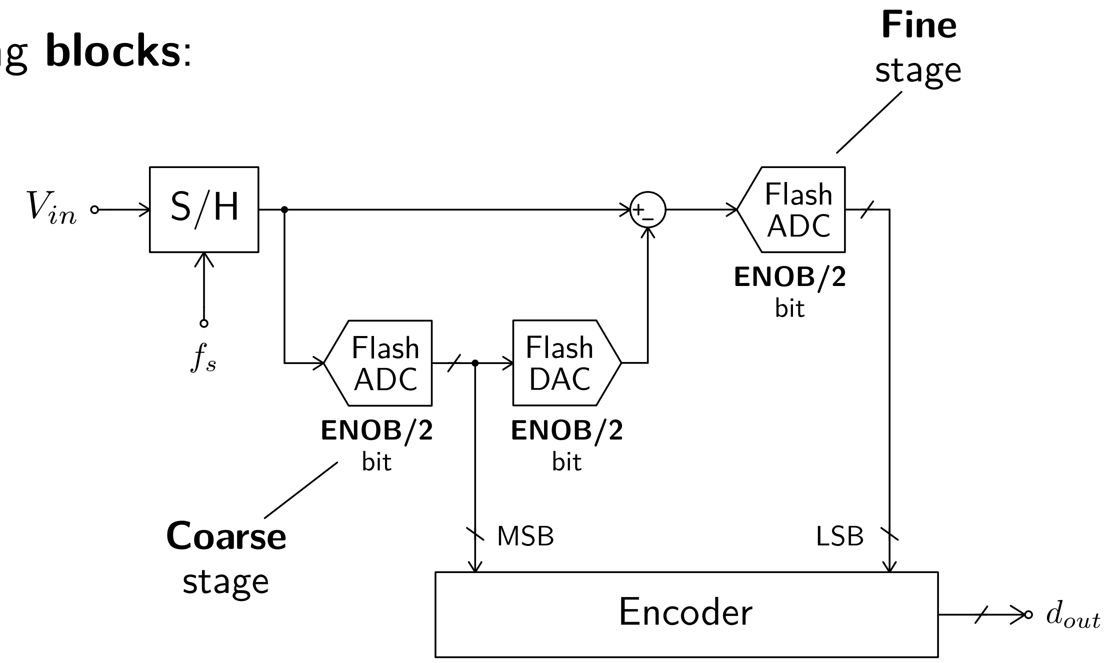
Sub-Range Flash ADC

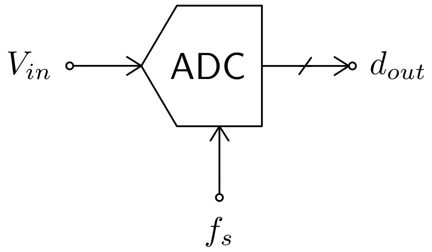


- Building **blocks**:



- **Two-step** coarse-fine data conversion scheme
- **ENOB splitting** can be chosen asymmetric depending on circuits...

Sub-Range Flash ADC



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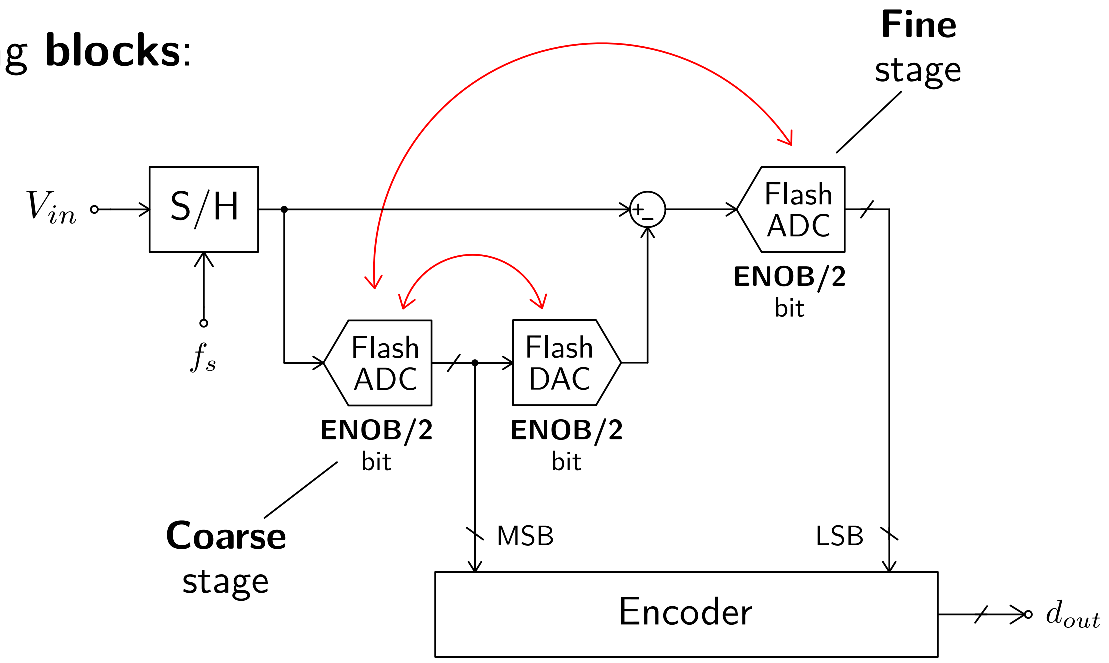


- **Two-step** coarse-fine data conversion scheme
- **ENOB splitting** can be chosen asymmetric depending on circuits...

▼ **Speed** reduction (x2)

▼ Non-linearity caused by **mismatching** between coarse ADC-DAC and between coarse-fine ADC

▲ Better **ENOB scaling** of comparators and passive components!

e.g. Number of comparators for **8-bit** flash ADC:

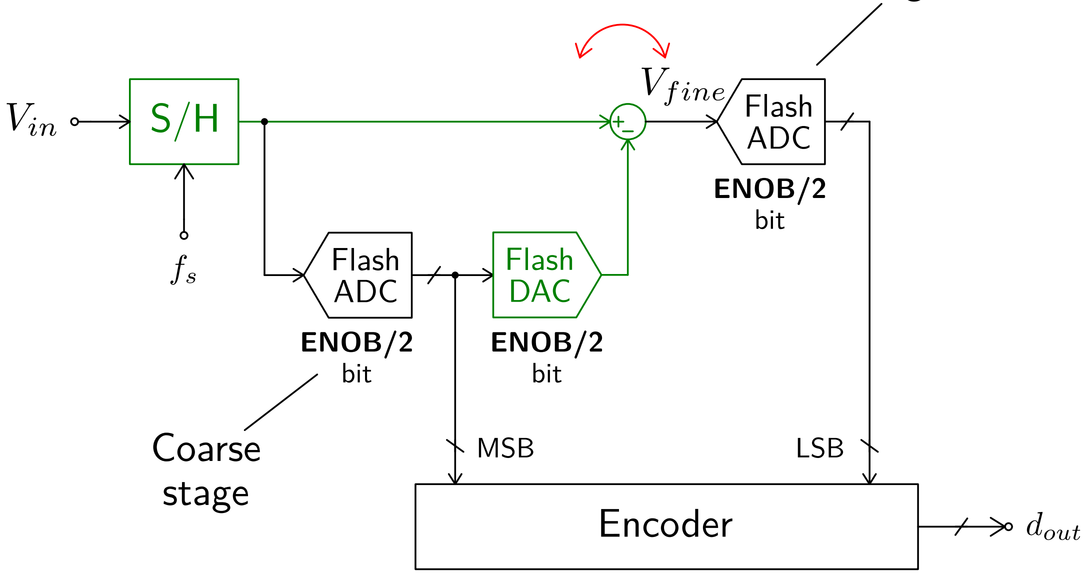
single-stage $\times(2^{ENOB} - 1) = 255 \quad \propto 2^{ENOB}$

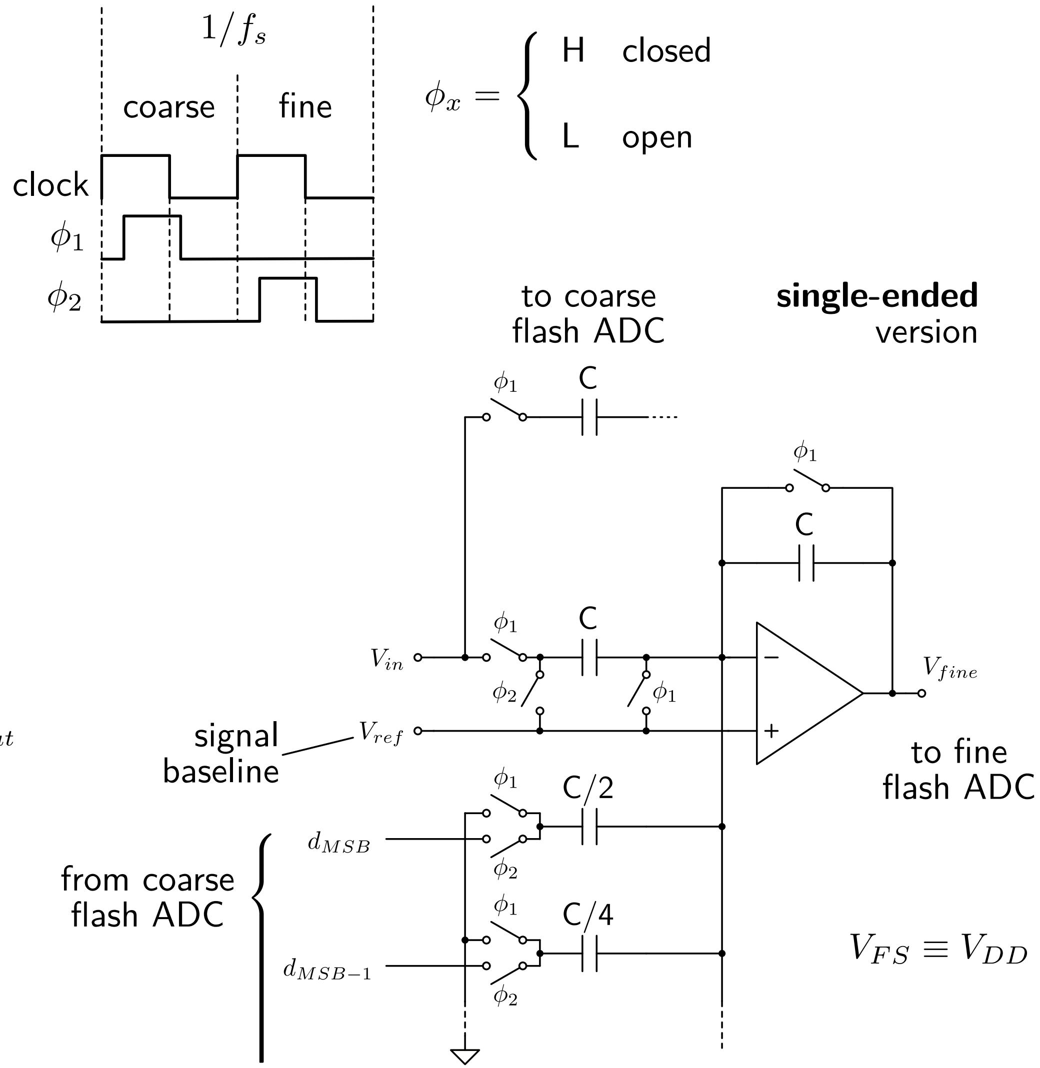
two-stage $\times 2(2^{\frac{ENOB}{2}} - 1) = 30 \quad \propto 2^{\frac{ENOB}{2}+1}$

$\div 2^{\frac{ENOB}{2}-1}$

Sub-Range Flash ADC

- **Circuit** implementation:

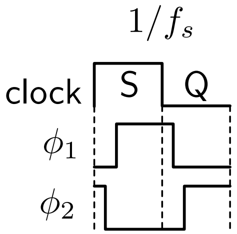




- ▼ Non-linearity cuased by **non-unitary gain** in MSB substraction
- ▲ **Compact** SC implementation

Time-Interleaved Flash ADC

- **Two-step** CMOS comparator:



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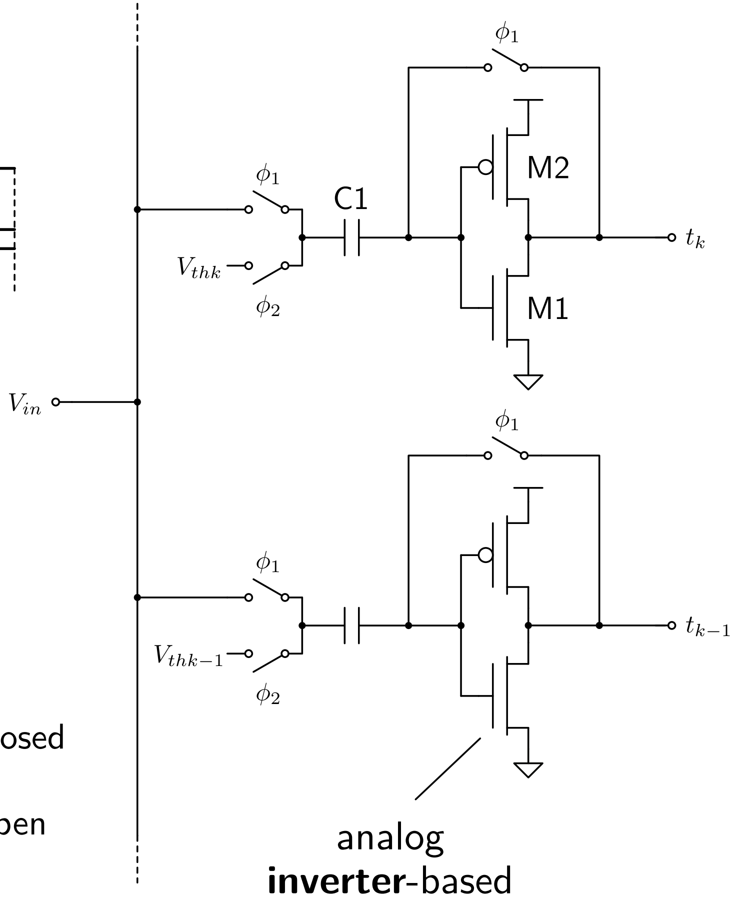
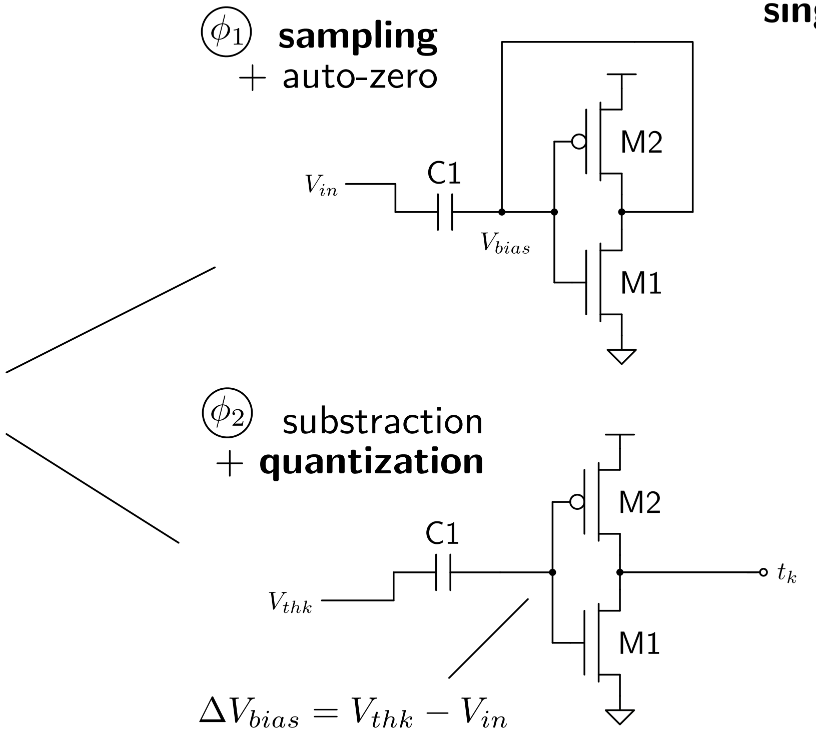


single-ended version



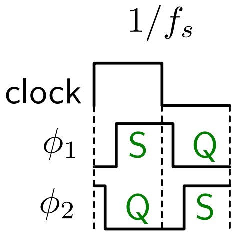
- ▲ **Offset** insensitive!
- ▲ Compact **area**
- ▼ Poor power supply rejection ratio (**PSRR**)

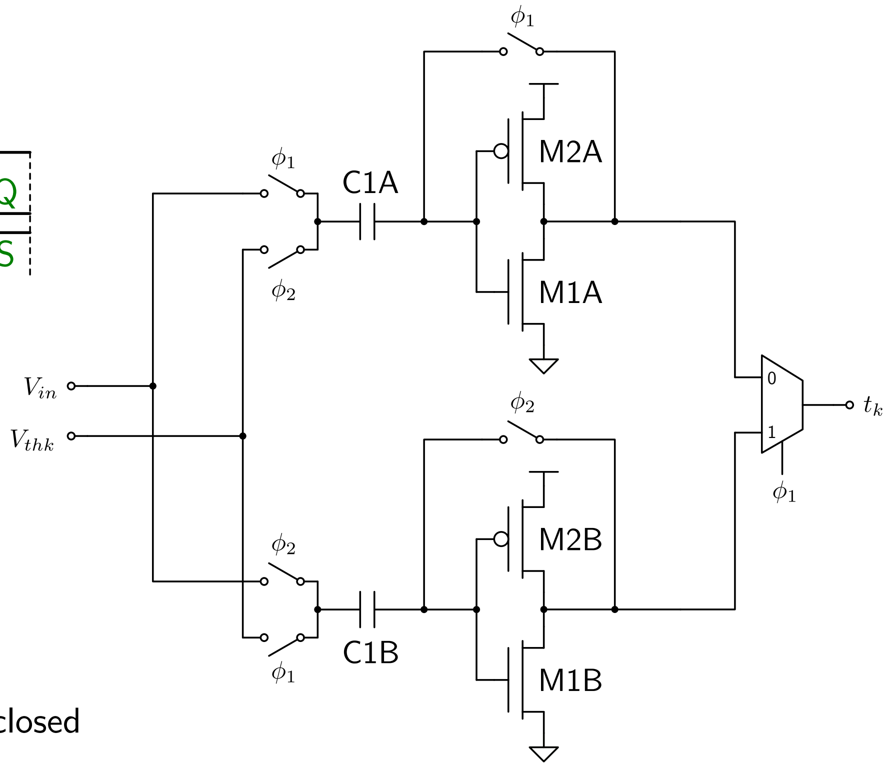
Time-Interleaved Flash ADC

- **Counter-phase** two-step CMOS comparator:

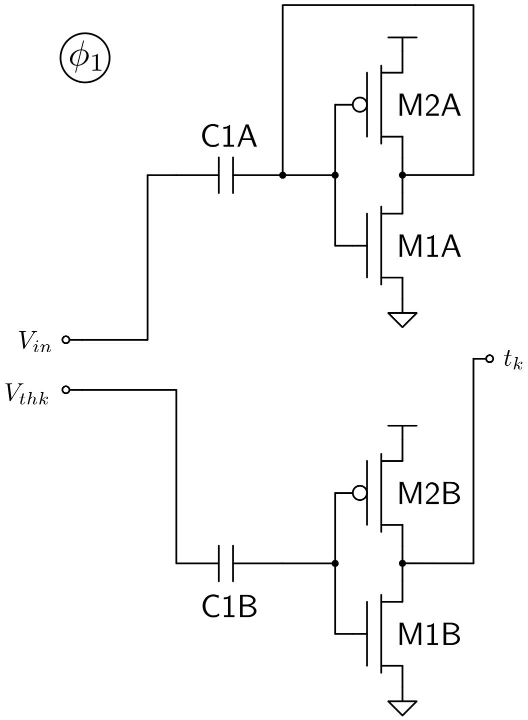
▼ Higher **jitter** sensitivity (both clock edges)

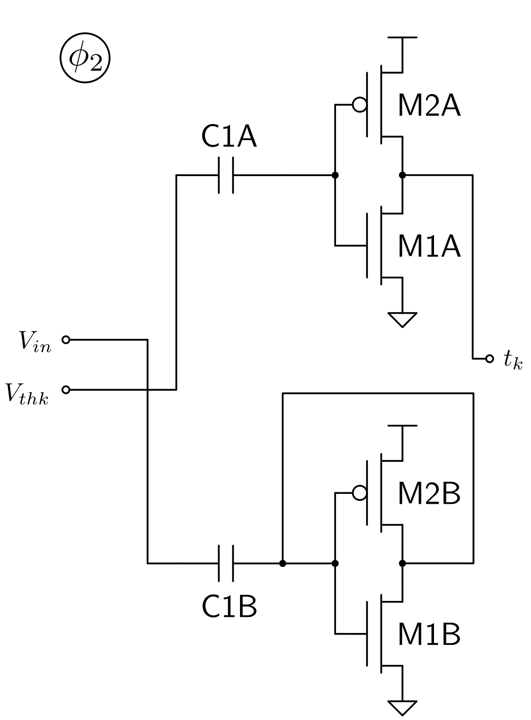
▲ Higher **speed** (x2)





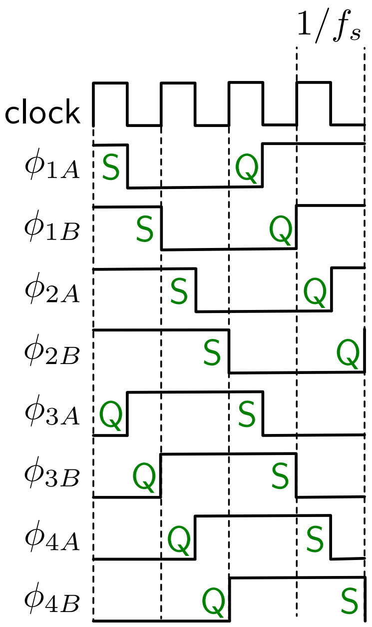
$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$





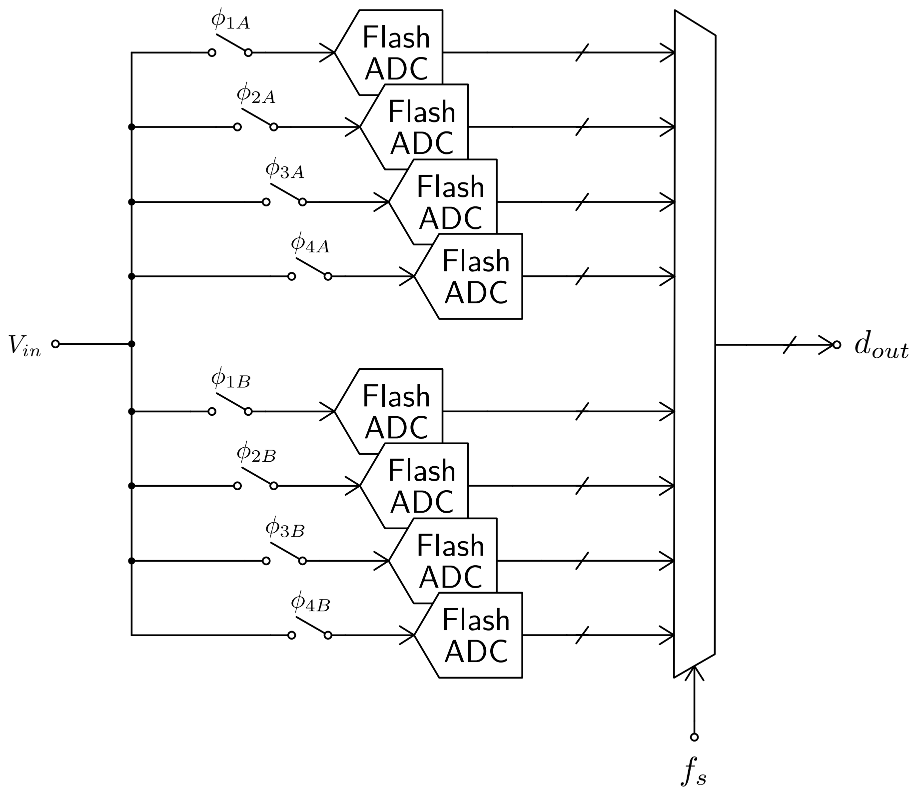
Time-Interleaved Flash ADC

- Extending the same idea to multiple **time-interleaving**:



$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

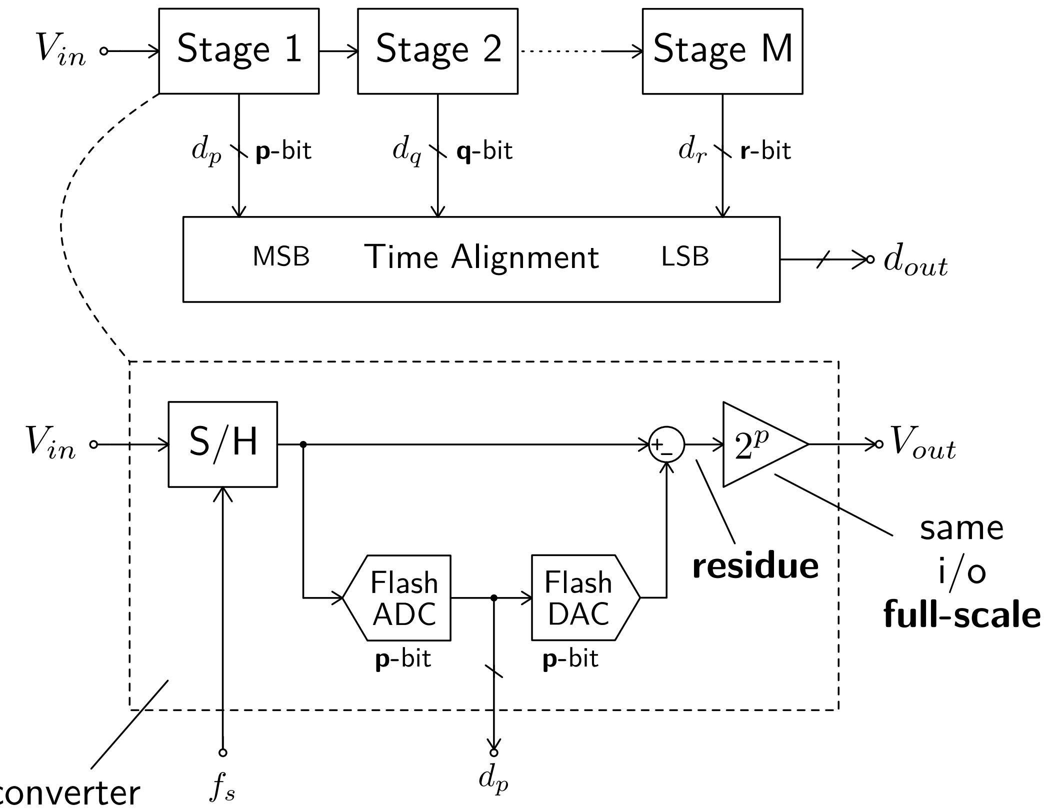
e.g. N=4

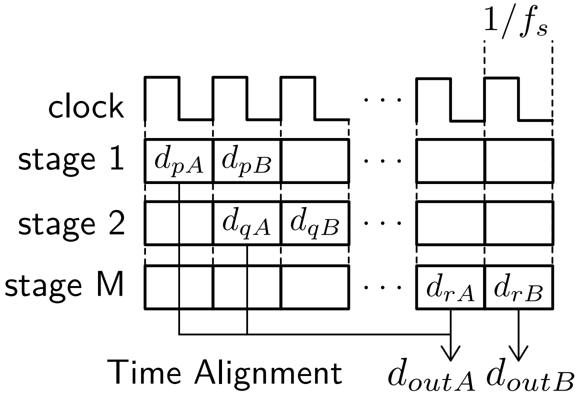


- ▲ Overall equivalent **high-speed** conversion
- ▲ Each flash ADC operates at **low-speed** (1/N)
- ▼ Large **area** (xN)
- ▼ High **latency** (xN)
- ▼ Complex **synchronization**

Pipeline ADC

- Combination of **cascaded sub-ranging** and **time-interleaving**:

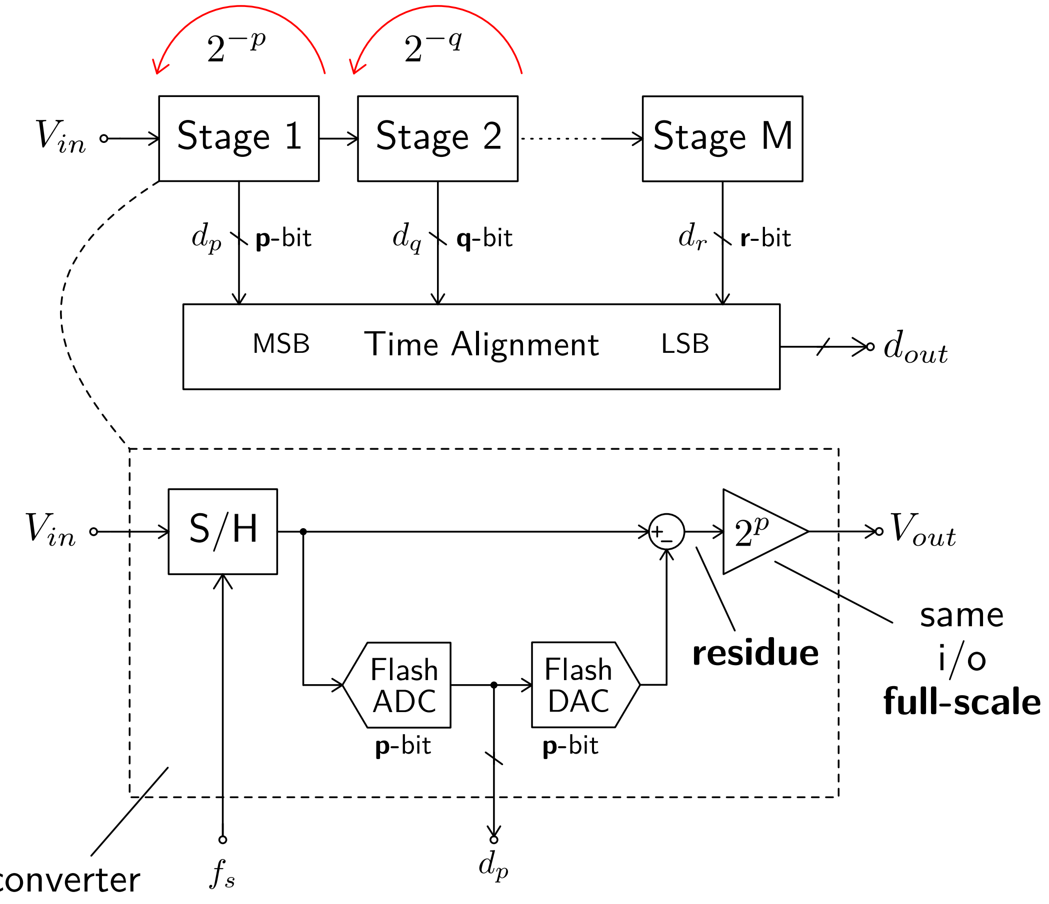


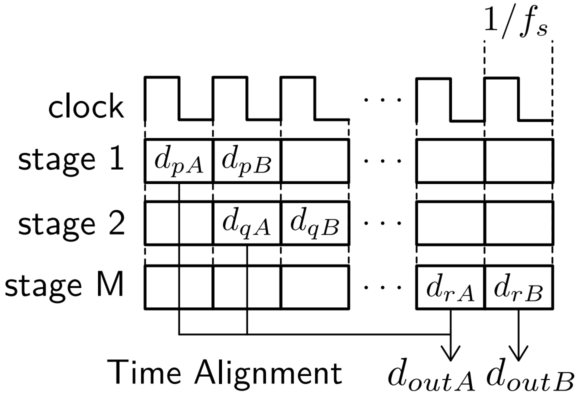


- Sub-converter functions:
  - Sampling and hold (**S/H**)
  - **Sub-range** quantization
  - **Residue** computation and scaling

Pipeline ADC

- Combination of **cascaded sub-ranging** and **time-interleaving**:



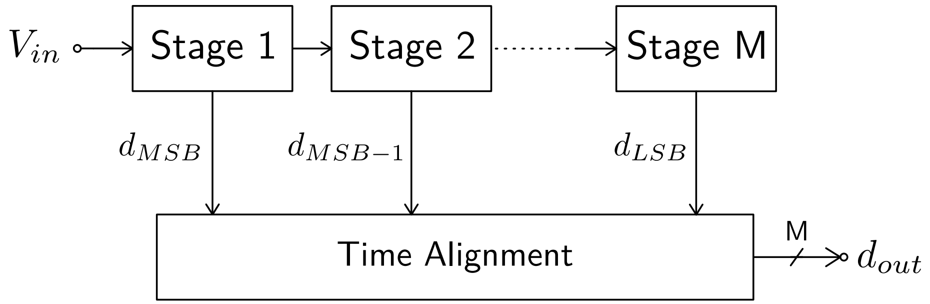


- ▲ **Simpler** flash sub-ADCs
- ▲ Performance depends on first-stage **only**
- ▲ No **speed** reduction
- ▼ High **latency** (xM)

$$SNR_{eq} = \frac{S_{in}}{2^{-2p}N_1 + 2^{-2(p+q)}N_2 + \cdots + 2^{-2(p+q+\cdots+r)}N_M}$$

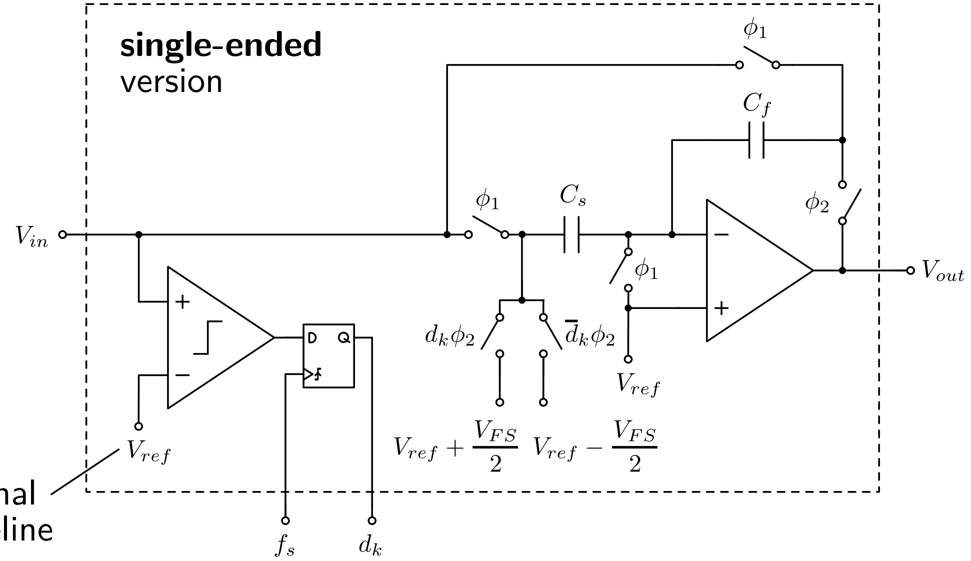
Pipeline ADC

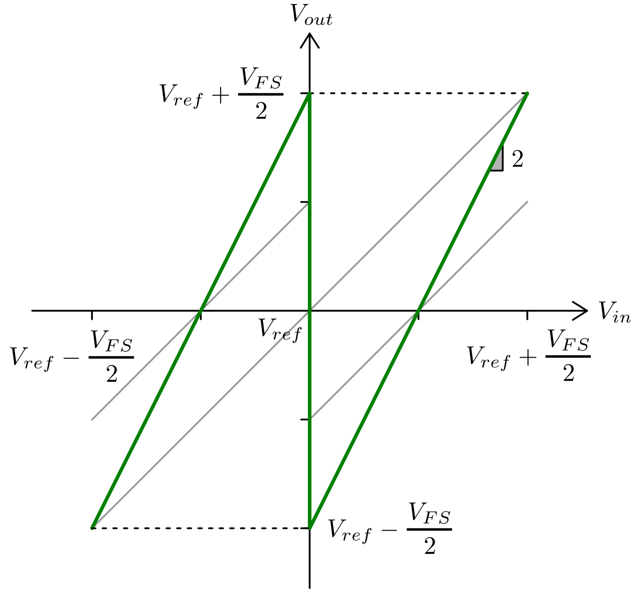
- Simple **1-bit stage** case study:



$$V_{out} = 2\underbrace{\left(V_{in} - V_{ref} + (-1)^{d_k}\frac{V_{FS}}{4}\right)}_{\text{residue}} + V_{ref}$$

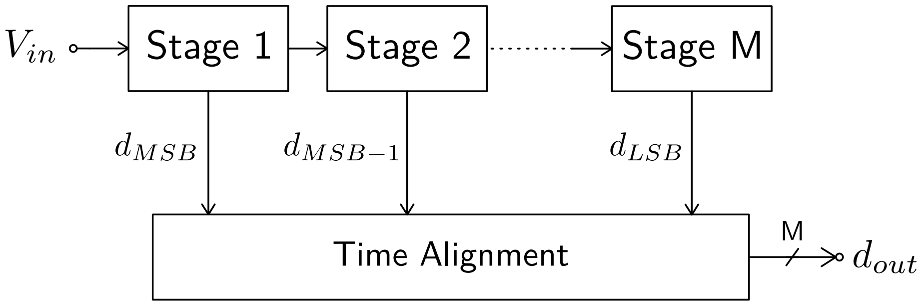
SC implementation of each stage:



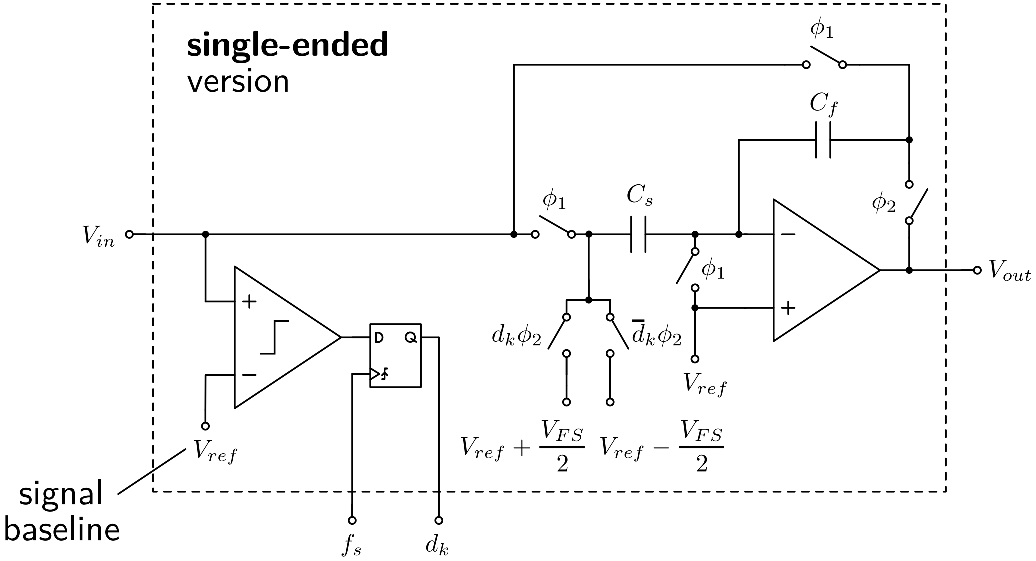


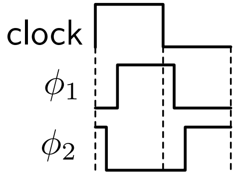
Pipeline ADC

- Simple **1-bit stage** case study:



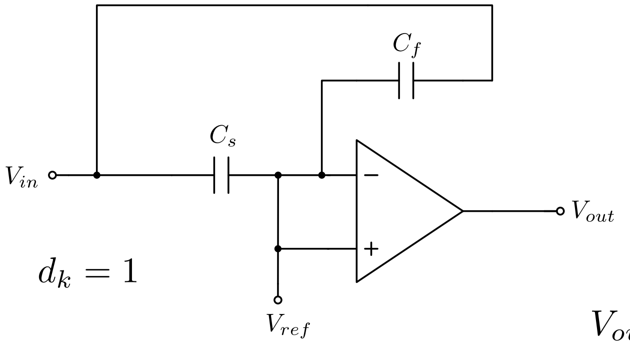
SC implementation of each stage:





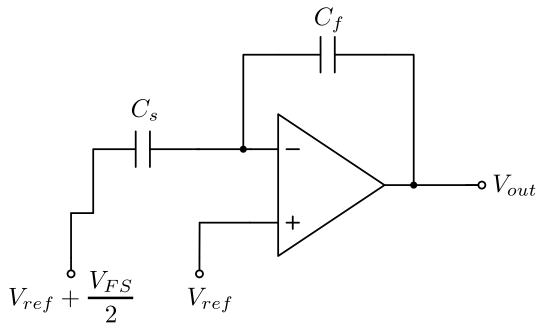
$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

ϕ_1 sampling + quantization (1)



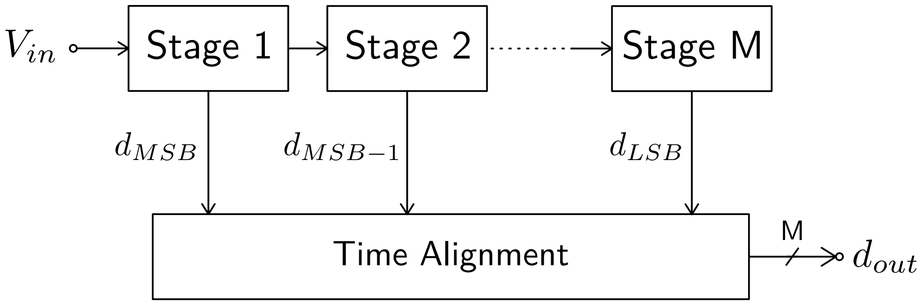
$$V_{out} = V_{in} - \frac{C_s}{C_f}\left(V_{ref} + (-1)^{\bar{d}_k}\frac{V_{FS}}{2} - V_{in}\right)$$

ϕ_2 residue (>0) + scaling

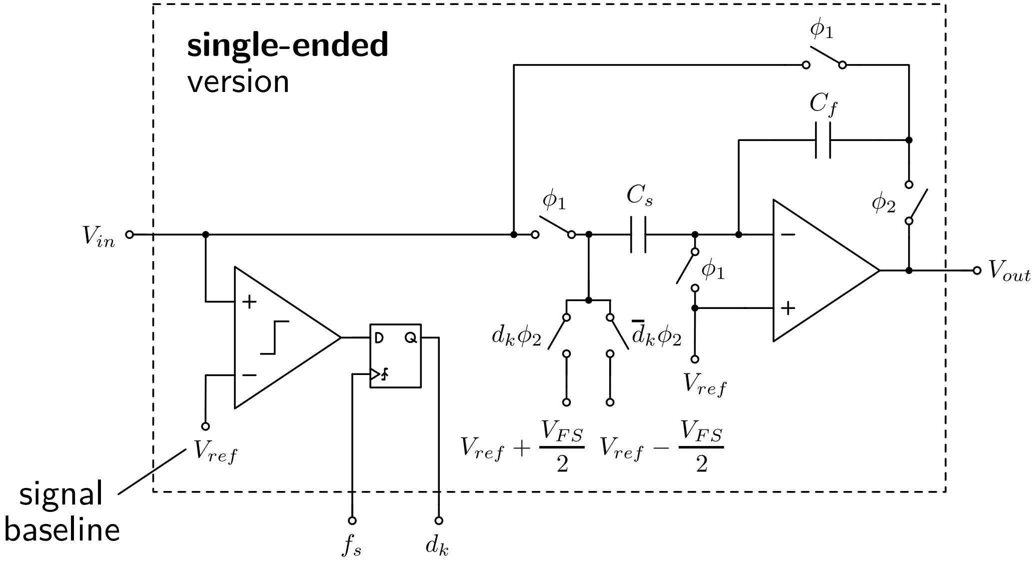


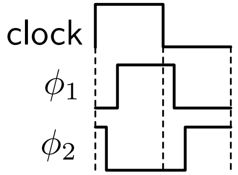
Pipeline ADC

- Simple **1-bit stage** case study:



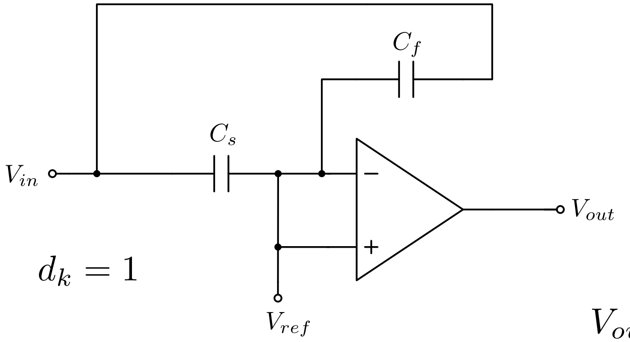
SC implementation of each stage:



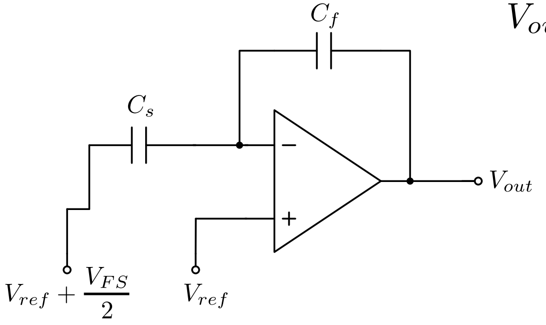


$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

ϕ_1 sampling + quantization (1)



ϕ_2 residue (>0) + scaling



- ▲ **Simplest** flash sub-ADCs
- ▲ Inherently **linear** single bit quantization
- ▼ **Noise** contributions from stage 2 → **multi-bit** first stage
- ▼ **Offset** sensitivity

$$V_{out} = V_{in} - \frac{C_s}{C_f}\left(V_{ref} + (-1)^{\bar{d}_k}\frac{V_{FS}}{2} - V_{in}\right)$$

$$V_{out} = 2\underbrace{\left(V_{in} - V_{ref} + (-1)^{d_k}\frac{V_{FS}}{4}\right)}_{\text{residue}} + V_{ref}$$

$C_f \equiv C_s$

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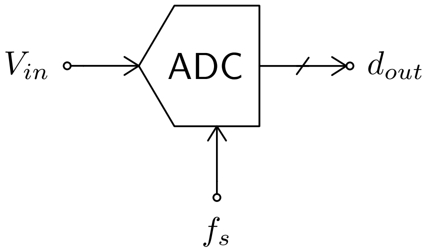
4 Successive-Approximation Converters

5 Integrating Techniques

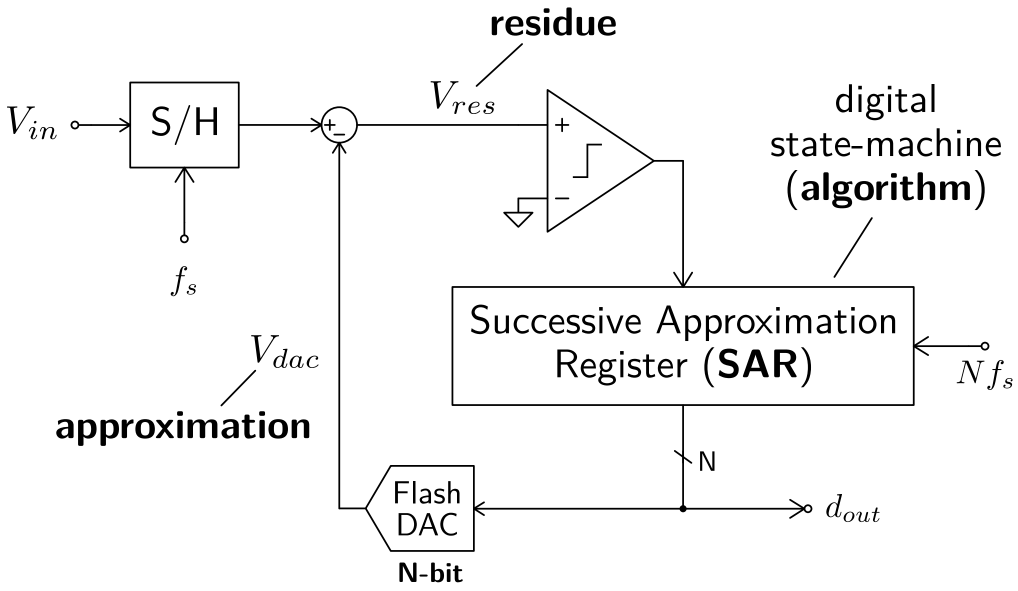
6 Delta-Sigma Modulation

7 Time-Domain Converters

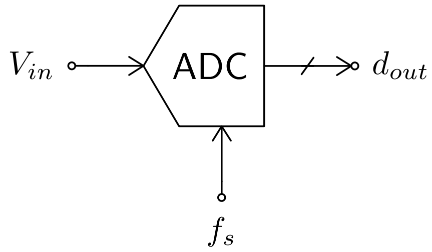
Successive Approximation ADC



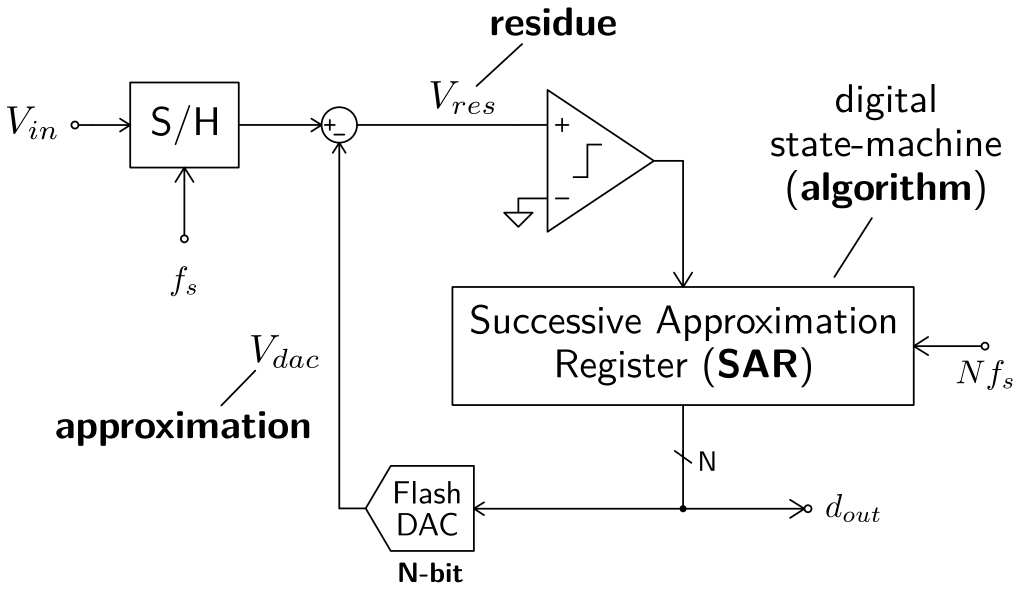
- Building **blocks**:



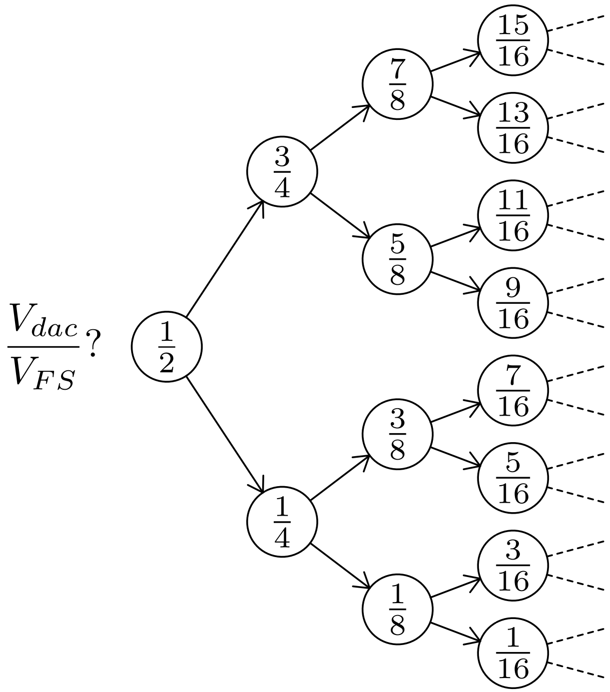
Successive Approximation ADC



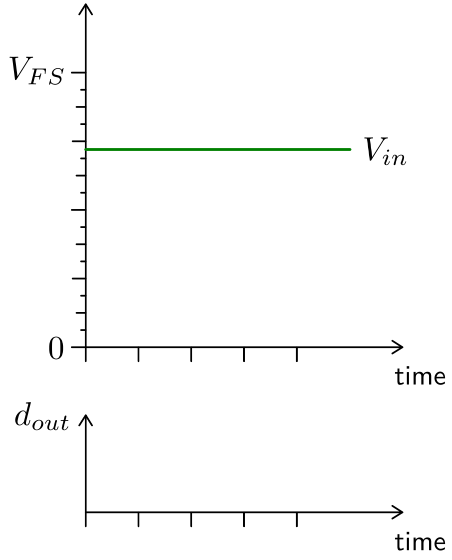
- Building **blocks**:



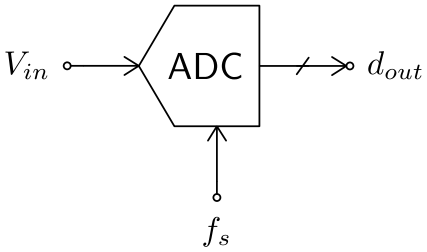
- **Symmetrical binary tree** search:



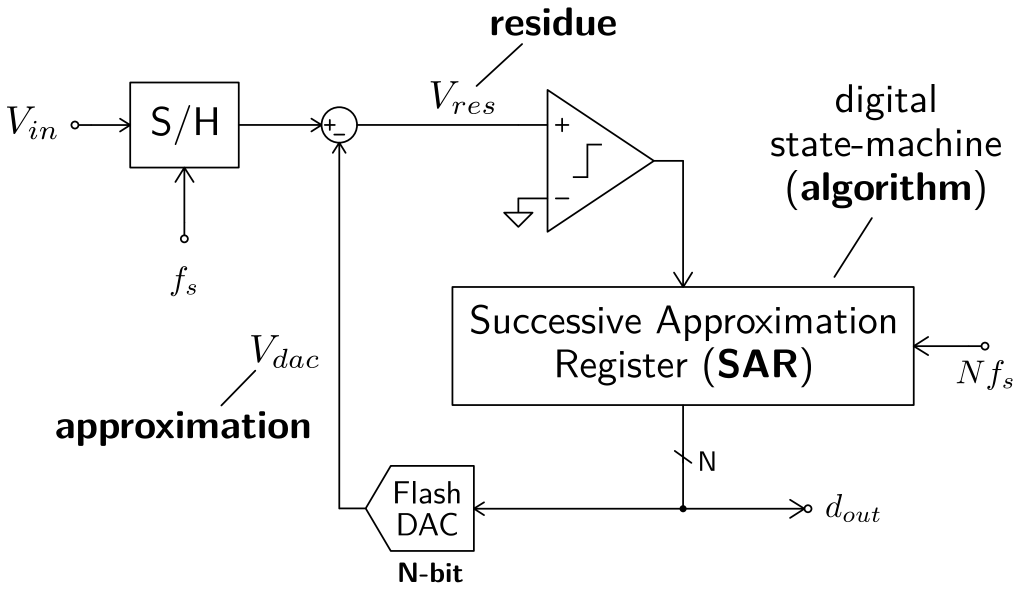
e.g. **4-bit** SAR ADC



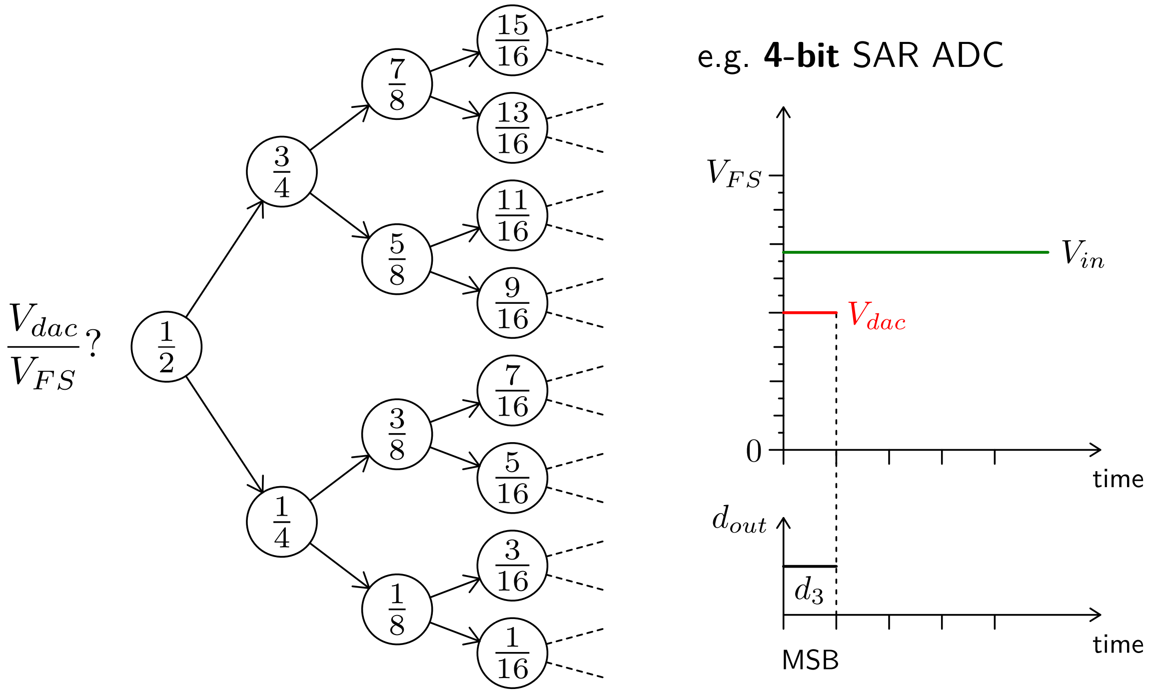
Successive Approximation ADC



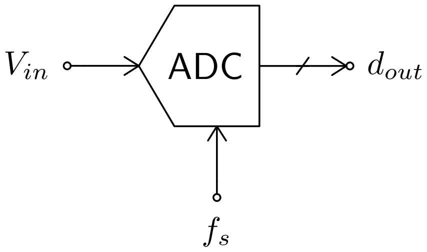
- Building **blocks**:



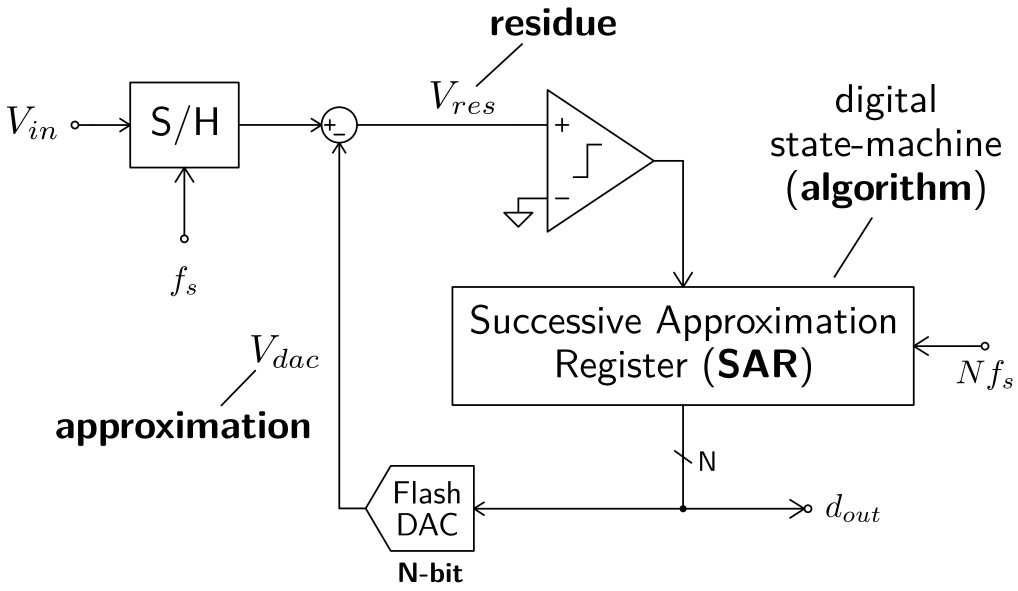
- **Symmetrical binary tree** search:



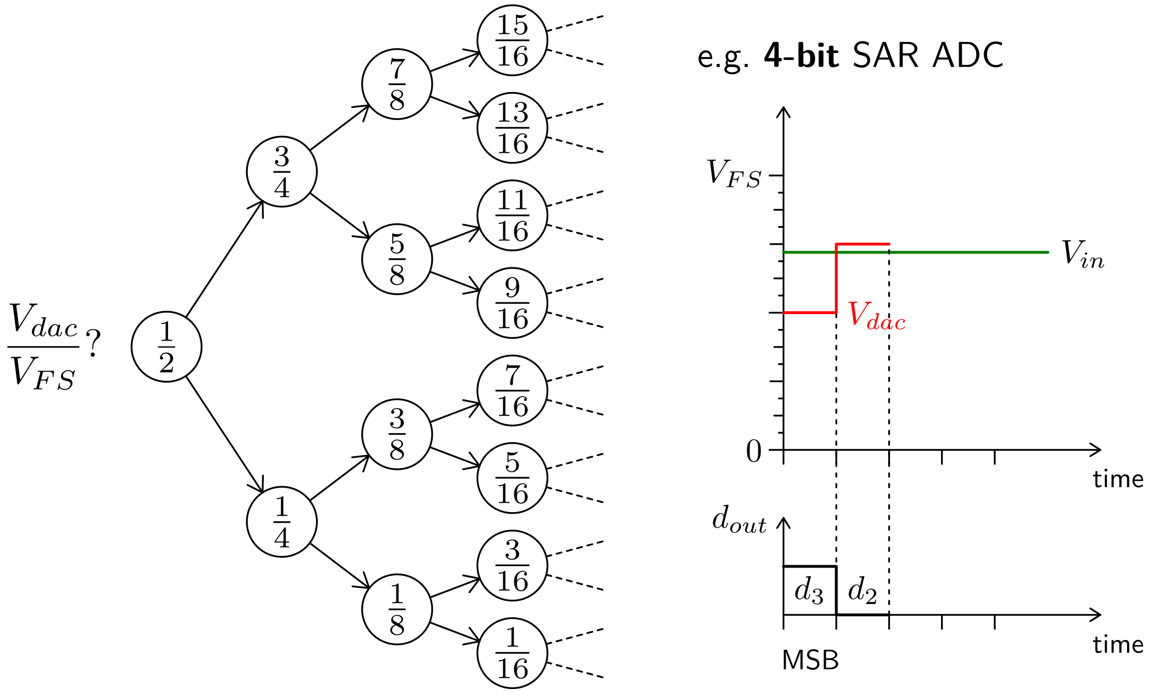
Successive Approximation ADC



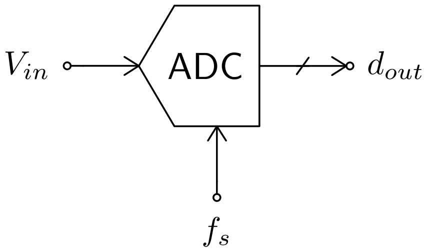
- Building **blocks**:



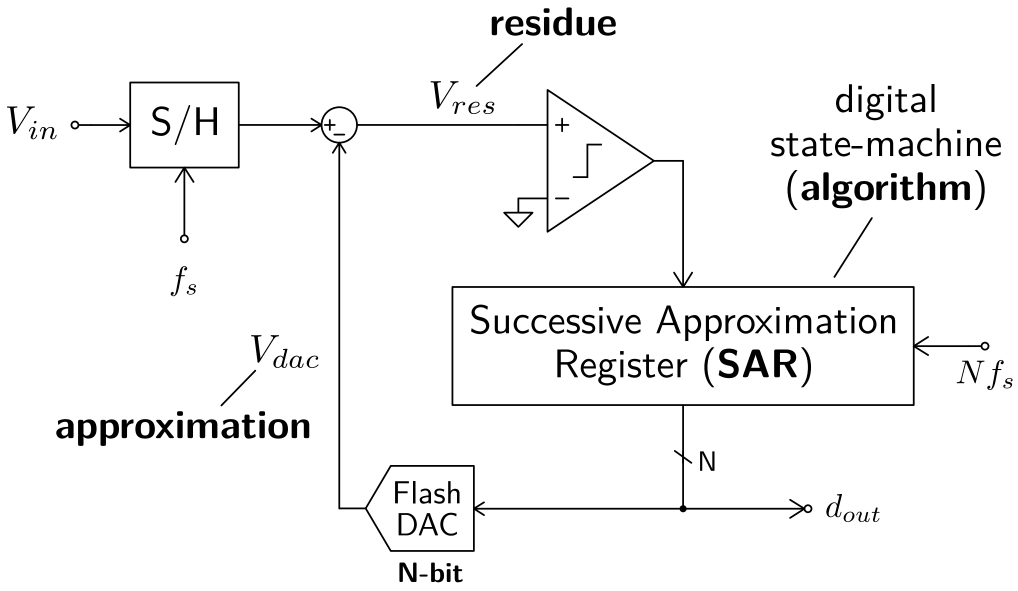
- **Symmetrical binary tree** search:



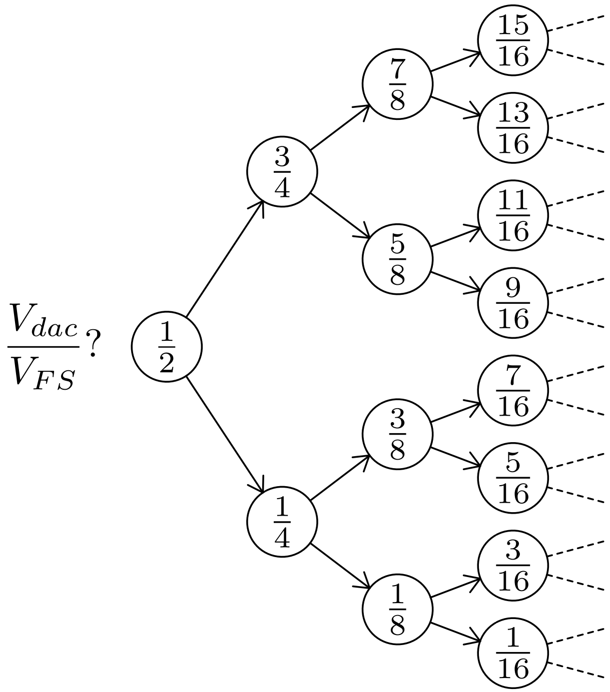
Successive Approximation ADC



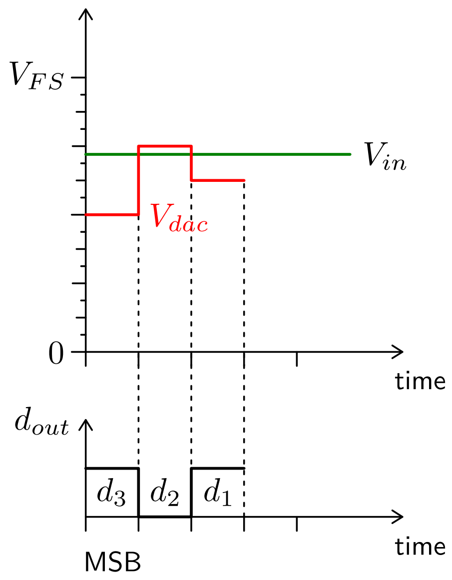
- Building **blocks**:



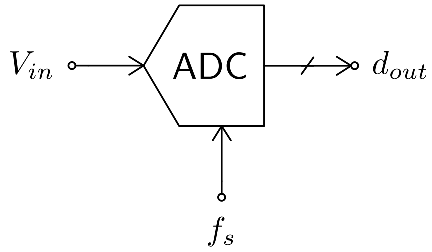
- **Symmetrical binary tree** search:



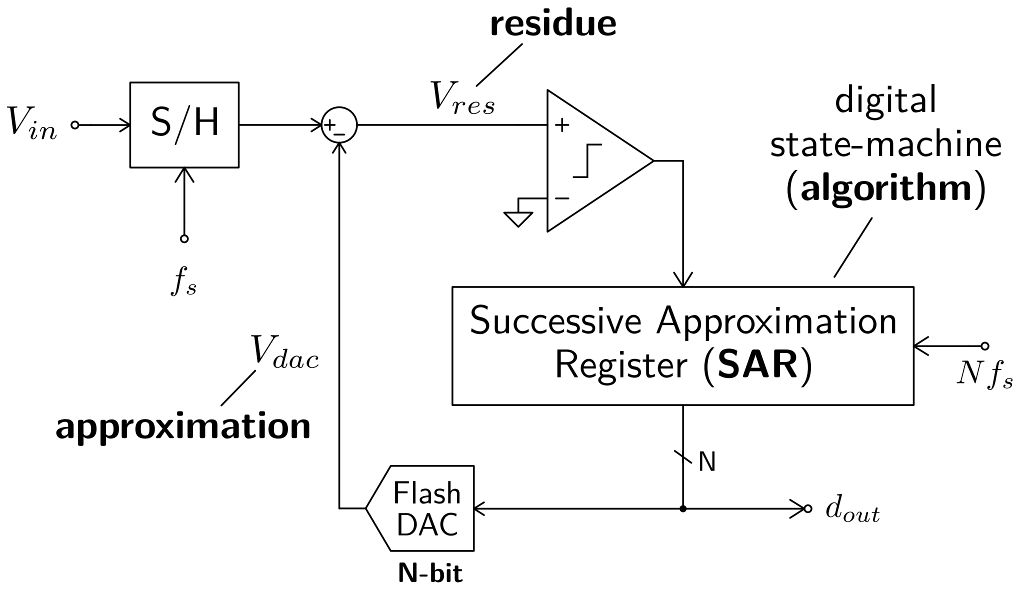
e.g. **4-bit** SAR ADC



Successive Approximation ADC



- Building **blocks**:



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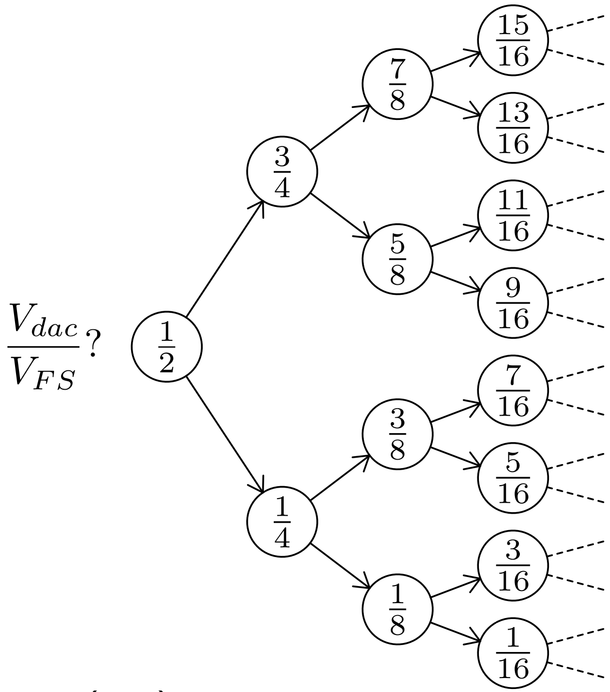
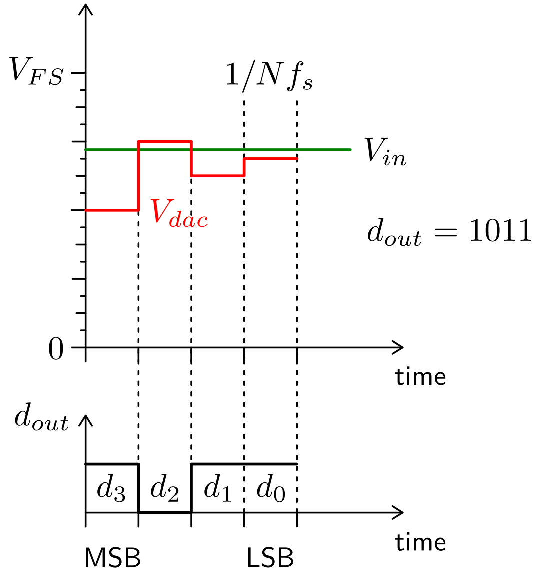


e.g. **4-bit** SAR ADC



▲ Analog **minimalist**

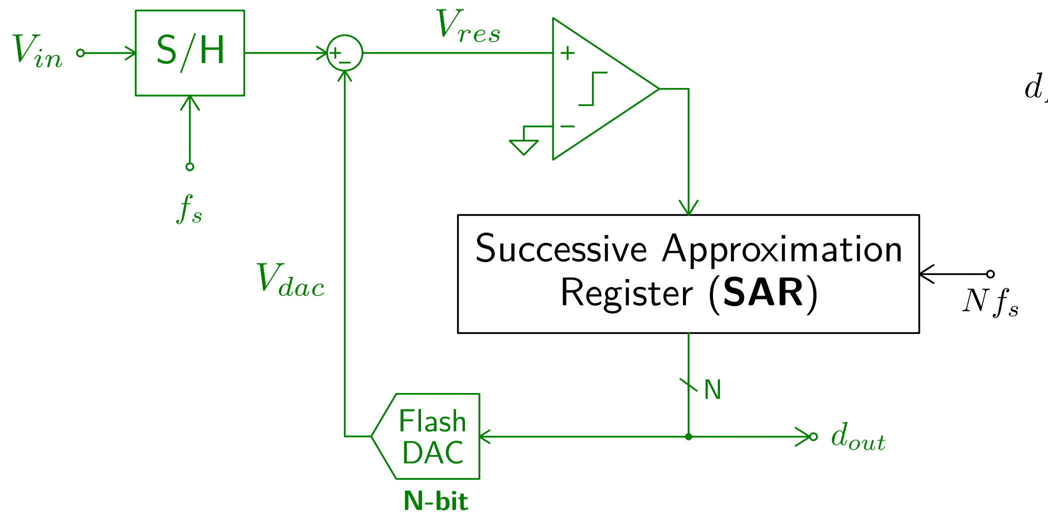
▲ Very **low-power** consumption

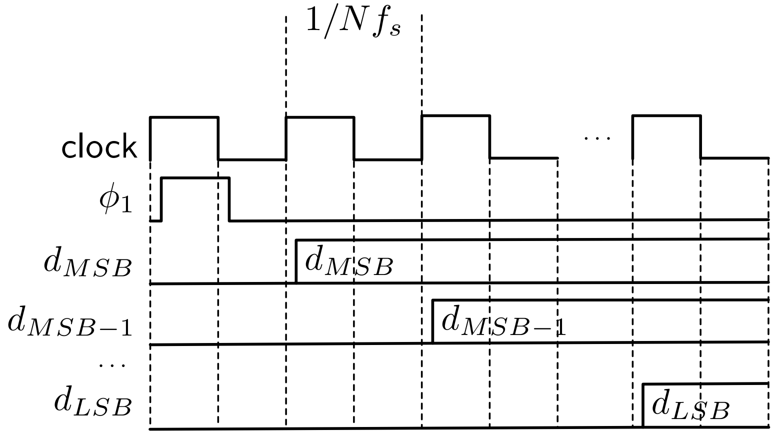
▼ **Speed** requirements (xN)

▼ Performance limited by **flash DAC**

Successive Approximation ADC

- **Circuit** implementation:

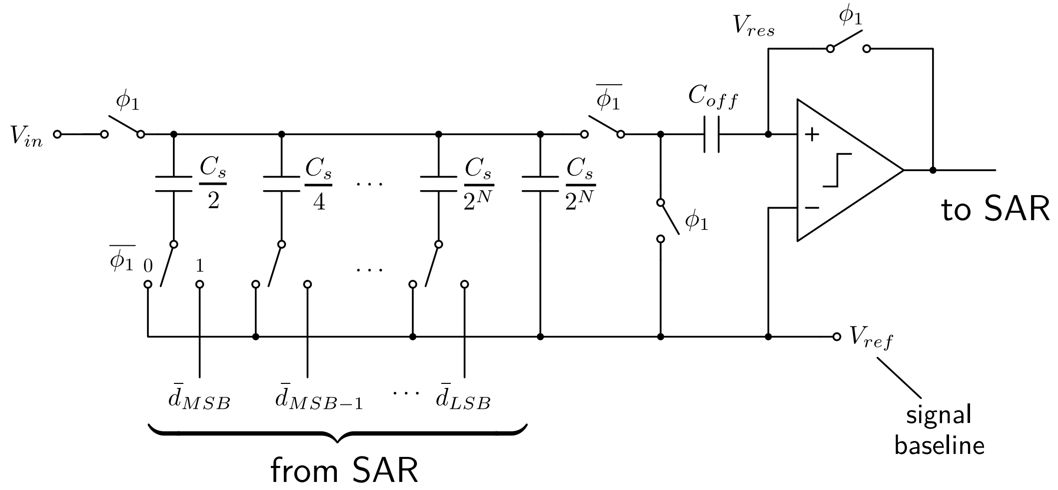




$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

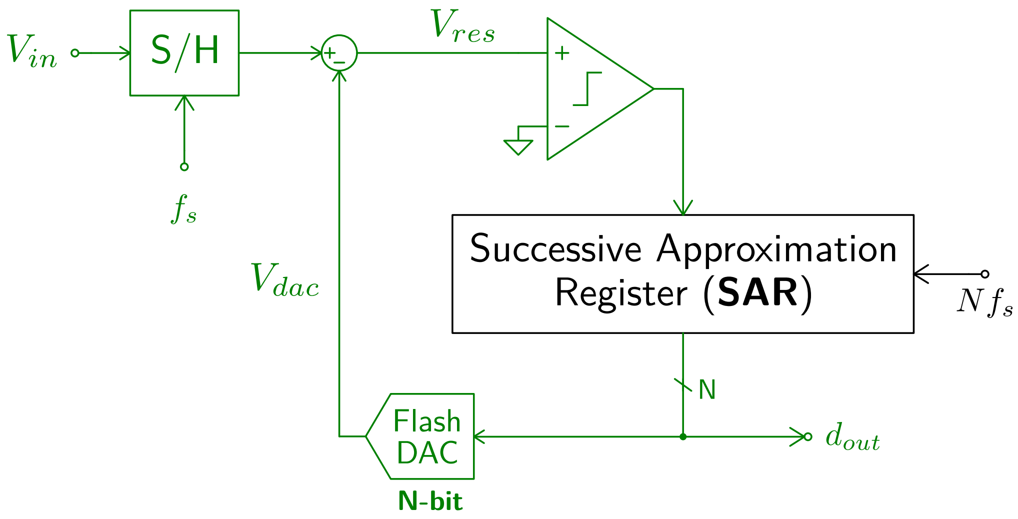
$$V_{FS} \equiv 2V_{ref}$$

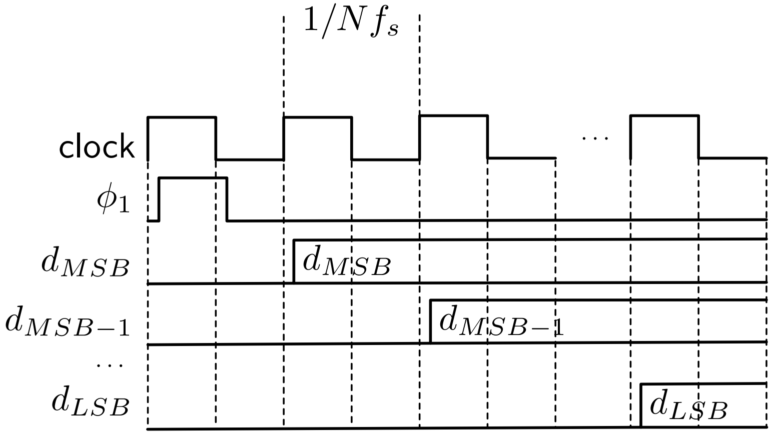
single-ended version



Successive Approximation ADC

- **Circuit** implementation:

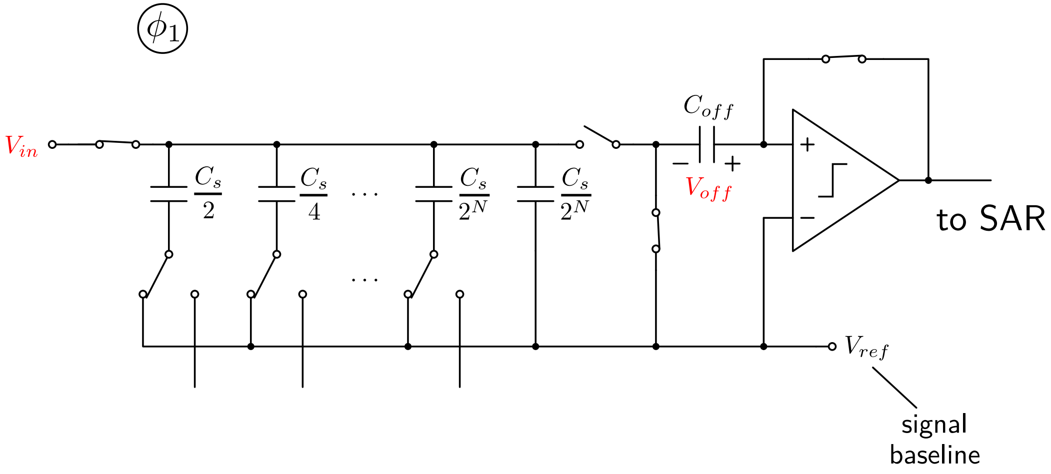




$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

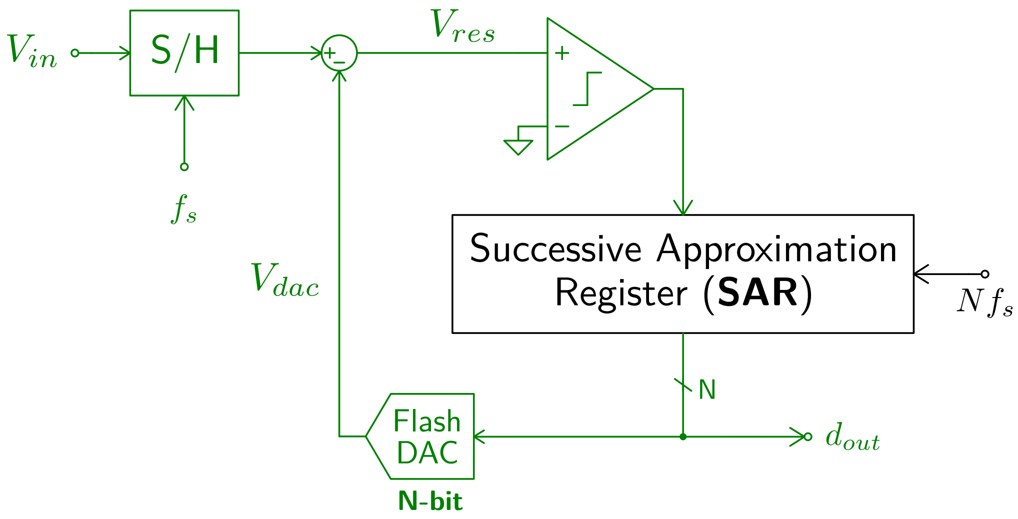
$$\frac{C_s}{2^N} + \sum_{i=1}^{N} \frac{C_s}{2^i} \equiv C_s$$

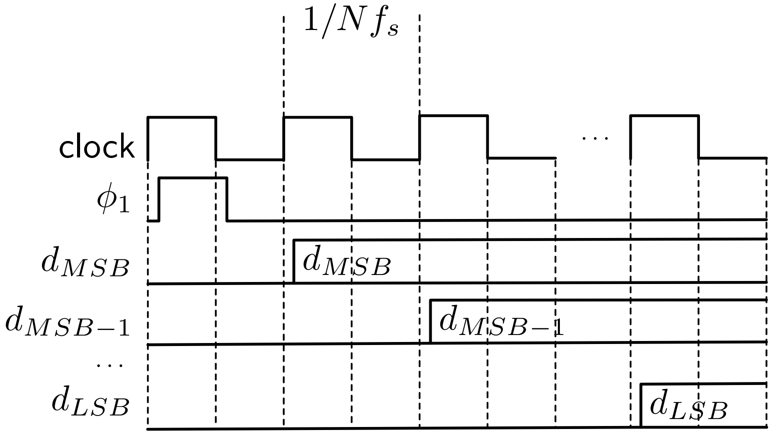
$V_{FS} \equiv 2V_{ref}$ **single-ended** version



Successive Approximation ADC

- **Circuit** implementation:



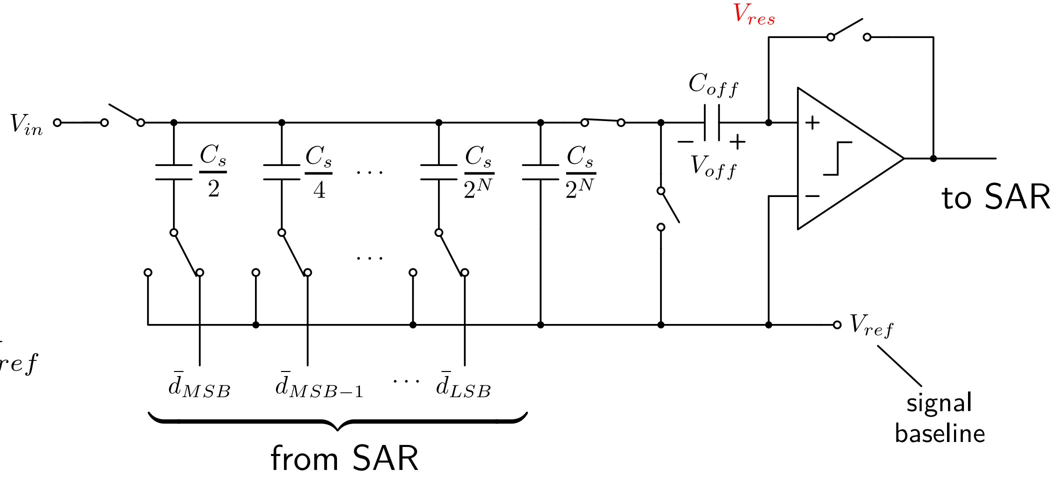


$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

$V_{FS} \equiv 2V_{ref}$ **single-ended** version

$$\frac{C_s}{2^N} + \sum_{i=1}^{N} \frac{C_s}{2^i} \equiv C_s$$

$$V_{res} = V_{in} - V_{off} + \left[\frac{(-1)^{d_{MSB}}}{2} + \frac{(-1)^{d_{MSB}}}{4} + \cdots + \frac{(-1)^{d_{LSB}}}{2^N} \right] V_{ref}$$



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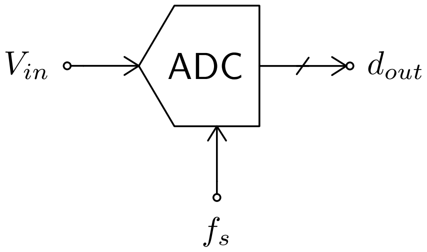
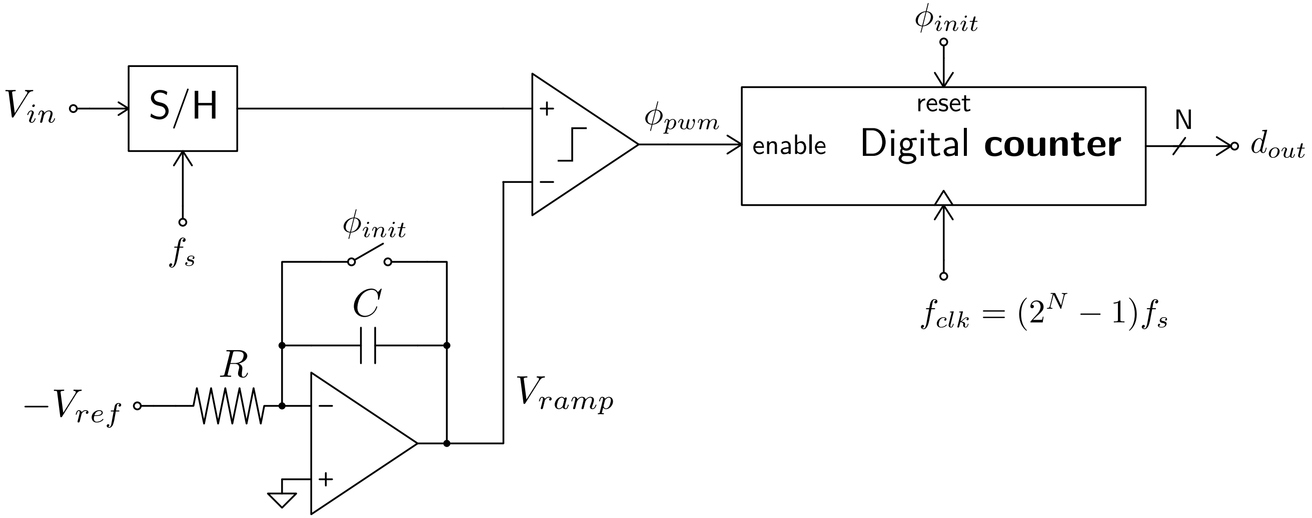
Single-Slope ADC

$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$



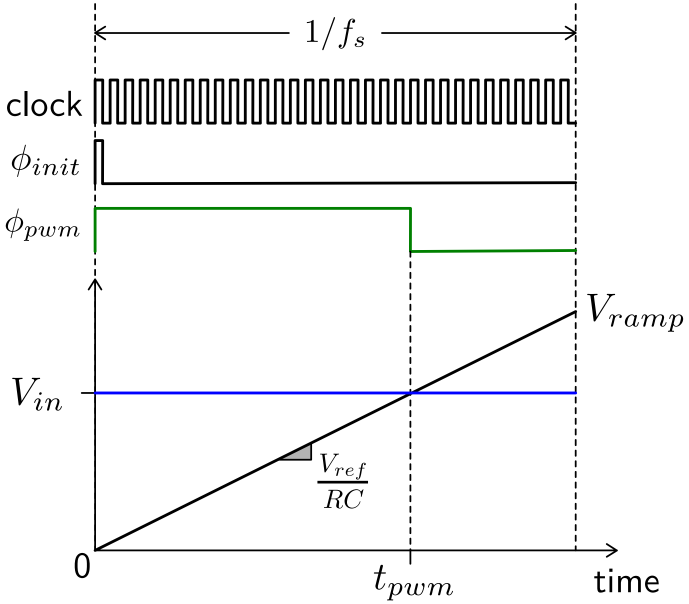
- Building **blocks**:



pulse-width modulation (**PWM**)

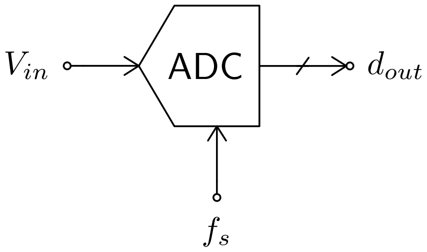
$$t_{pwm} = RC\frac{V_{in}}{V_{ref}}$$

$$d_{out} = t_{pwm}f_{clk} = (2^N - 1)f_sRC\frac{V_{in}}{V_{ref}}$$

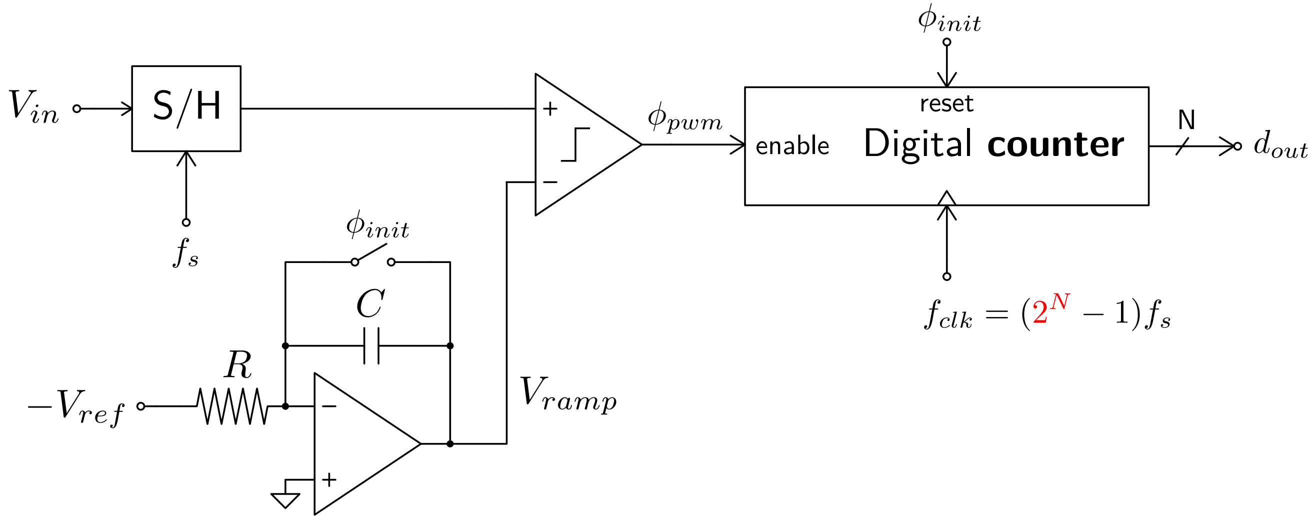


Single-Slope ADC

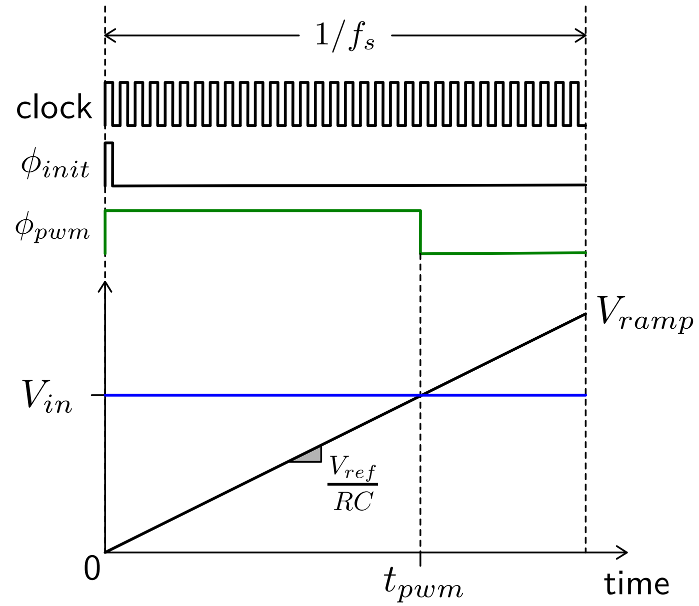
$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$



- Building **blocks**:



pulse-width modulation (**PWM**)



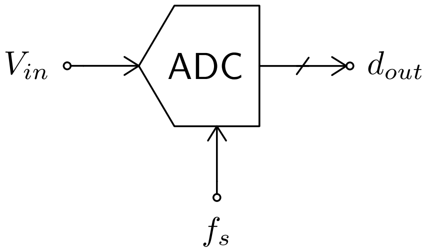
$$t_{pwm} = RC \frac{V_{in}}{V_{ref}}$$

$$d_{out} = t_{pwm} f_{clk} = (2^N - 1) f_s RC \frac{V_{in}}{V_{ref}}$$

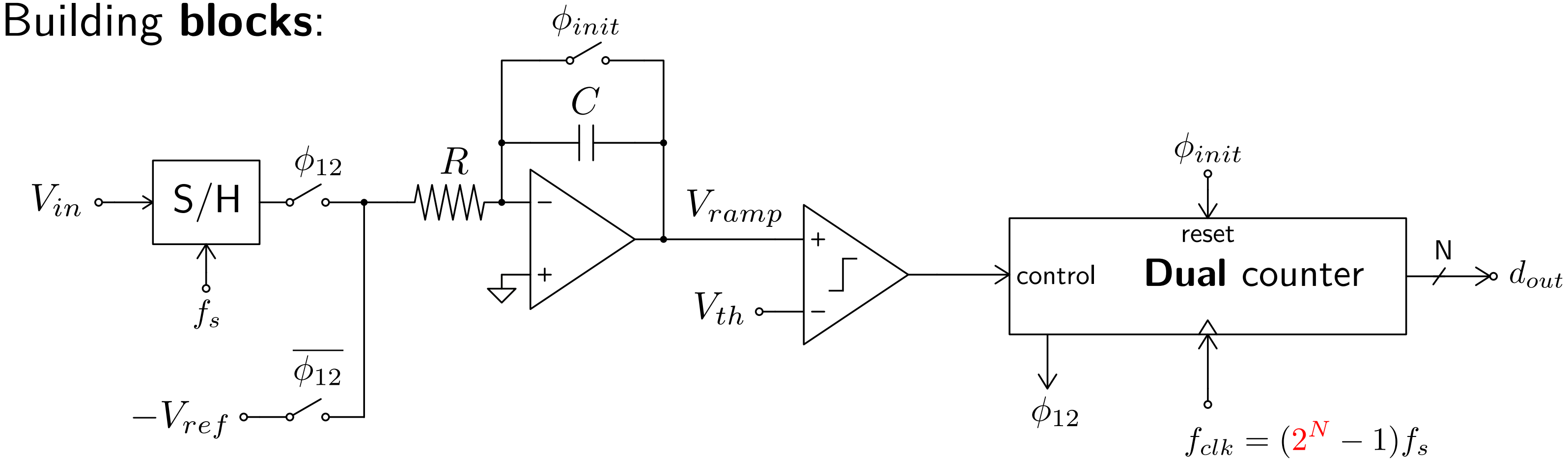
- ▲ Analog **minimalist**
- ▲ Very **low-power**
- ▼ **Speed** requirements (x$\mathbf{2^N}$)
- ▼ Technological sensitivity (**RC**)

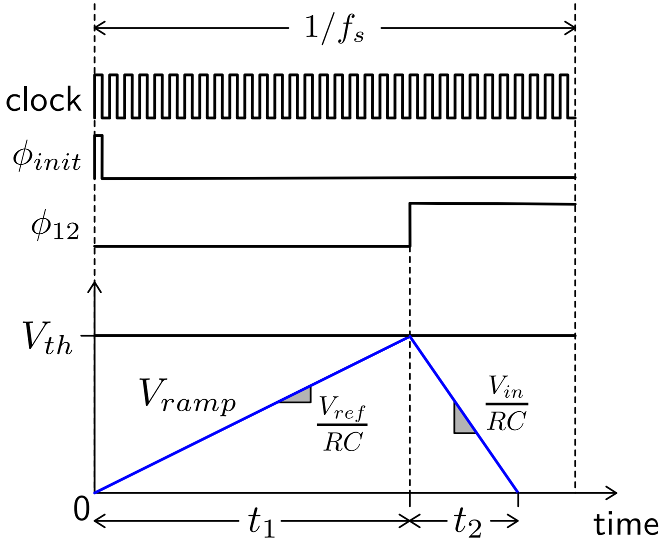
Dual-Slope ADC

$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$



- Building **blocks**:





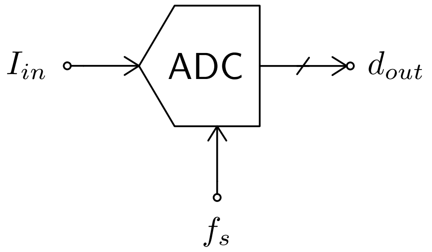
- ▲ Analog **minimalist**
- ▲ Very **low-power**

$$d_{out} = \frac{d_1}{d_2} \propto \frac{V_{in}}{V_{ref}}$$

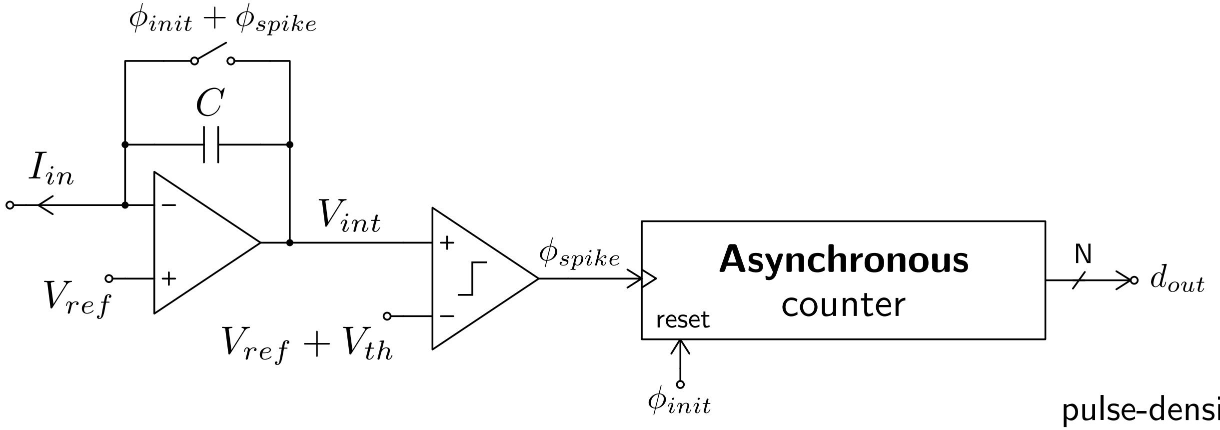
- ▼ **Speed** requirements (x**2$^{\mathbf{N}}$**)
- ▲ Technology independence (**RC**)

Integrate-and-Fire ADC

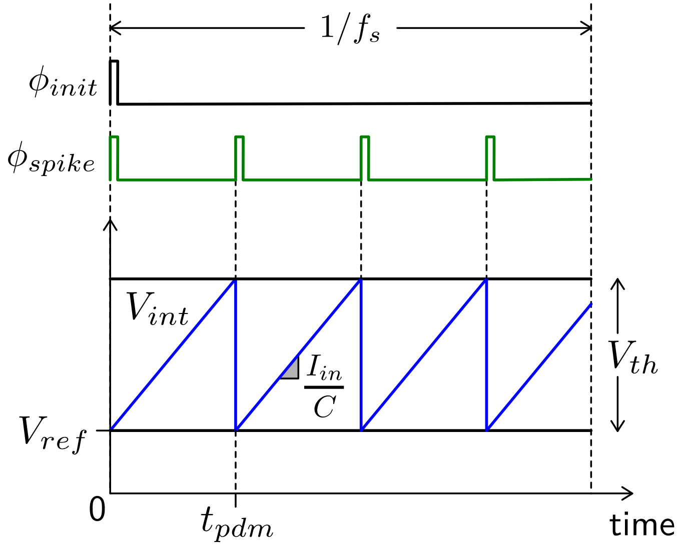
$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$



- Building **blocks**:



pulse-density modulation (**PDM**)



- ▲ Intrinsic **anti-aliasing** filtering
- ▲ **Current-mode** sensors (e.g. imagers)
- ▲ Very **low-power**

$$d_{out} = \frac{1/f_s}{t_{pdm}} = \frac{I_{in}}{C V_{th} f_s}$$

- **Speed** requirements adapted to signal
- ▼ Technology sensitivity (**C**)

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6 Delta-Sigma Modulation

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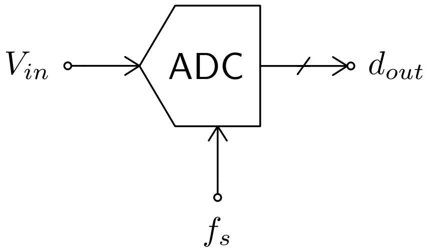
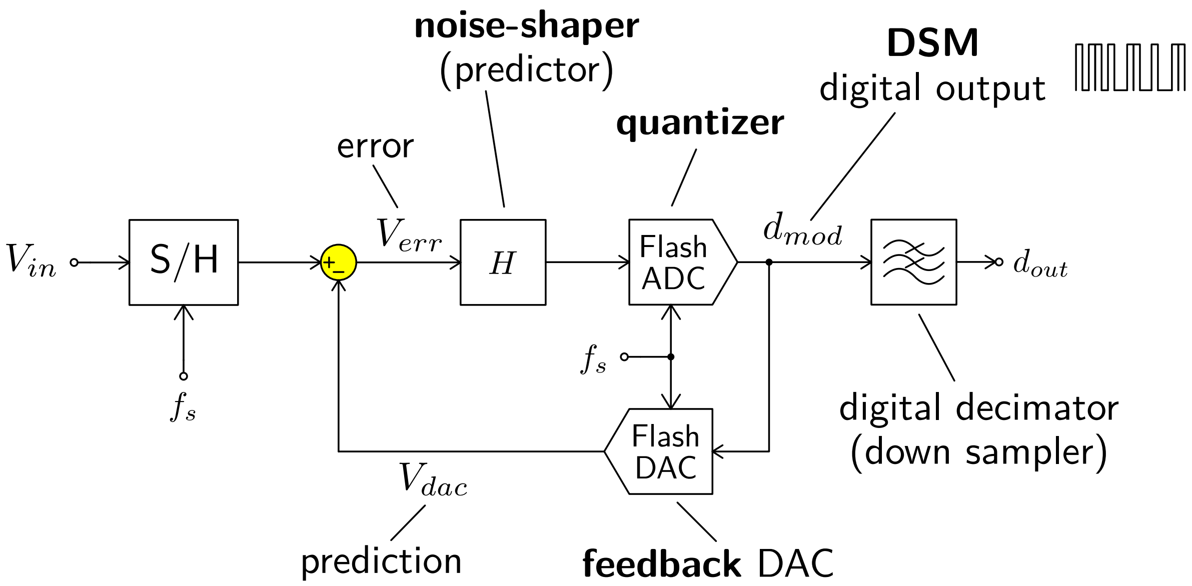
Delta-Sigma Modulator ADC



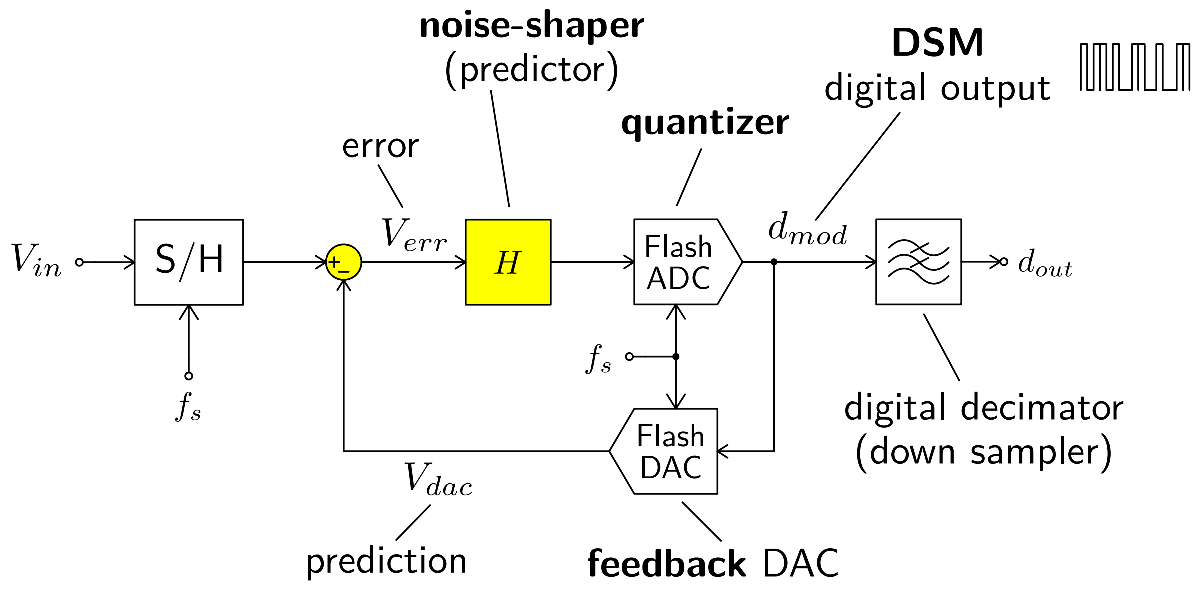
- General **single-loop DSM** architecture:



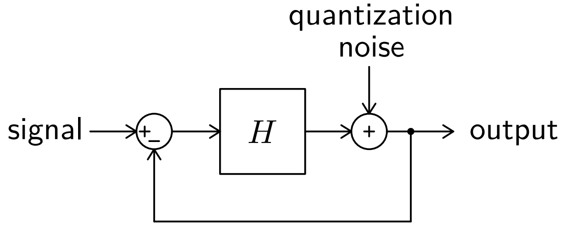
- Overall **negative feedback** tracks input signal

Delta-Sigma Modulator ADC

- General **single-loop DSM** architecture:



- Signal vs **quantization noise** behavior?

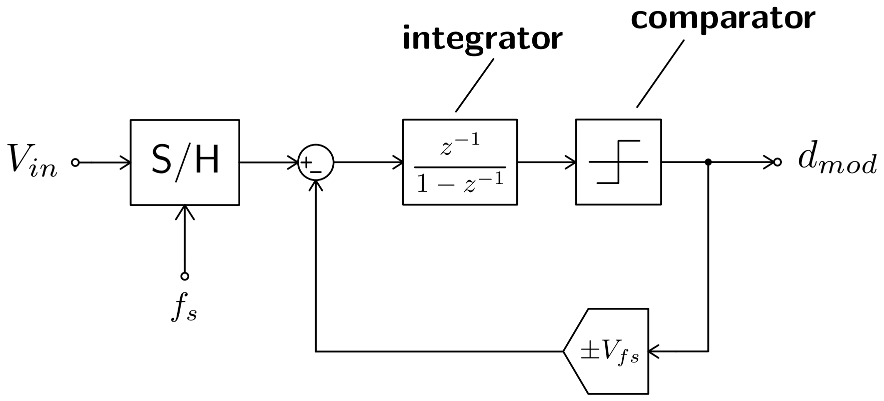


$$\begin{cases} STF = \dfrac{H}{1+H} & \to 1 \\ & H \to \infty \\ NTF = \dfrac{1}{1+H} & \to 0 \end{cases}$$

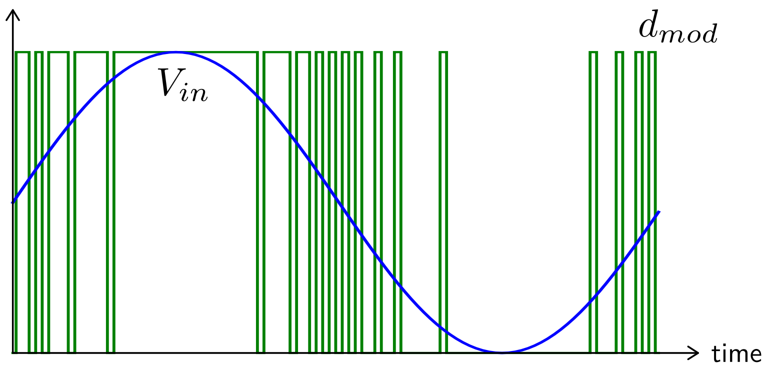
- Overall **negative feedback** tracks input signal
- Noise-shaper **filter**:
  - In-band **high-gain**
  - Either continuous- H(s) or **discrete-time H(z)**
- Peromance of flash ADC block can be strongly **relaxed**!

Delta-Sigma Noise Shaping

- **Simplest** architecture: **first-order** (N=1) **1-bit** (B=1) single-loop DSM



- Single-bit feedback DAC is **intrinsically linear**



Delta-Sigma Noise Shaping

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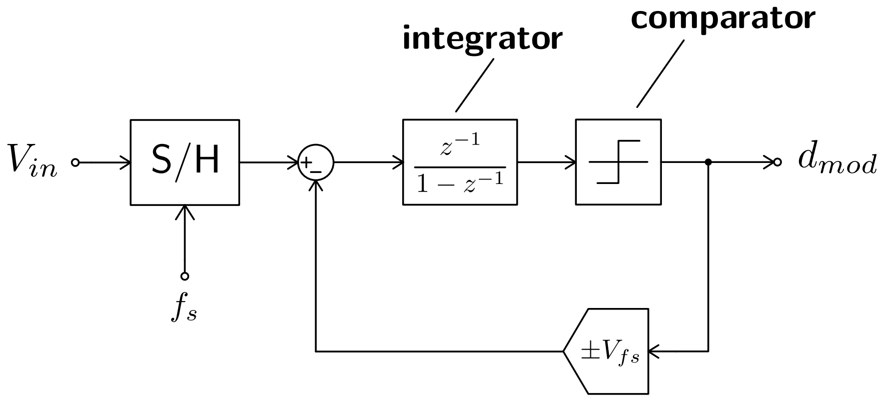


$$H(z) = \frac{z^{-1}}{1-z^{-1}}$$

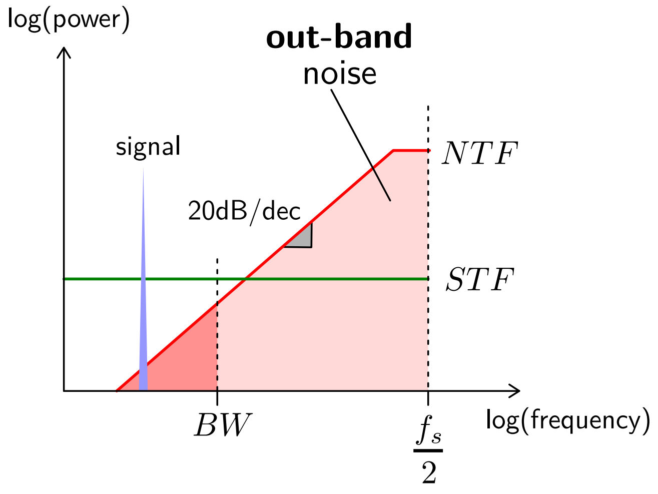
$$\begin{cases} STF = \dfrac{H}{1+H} \equiv z^{-1} & \text{(delay)} \\ NTF = \dfrac{1}{1+H} \equiv 1 - z^{-1} & \text{(differentiator)} \end{cases}$$

all-pass

high-pass shaping

- ▲ Single-bit feedback DAC is **intrinsically linear**
- ▼ **Oversampling** is needed

$$OSR \doteq \frac{f_s}{2BW} \gg 1$$



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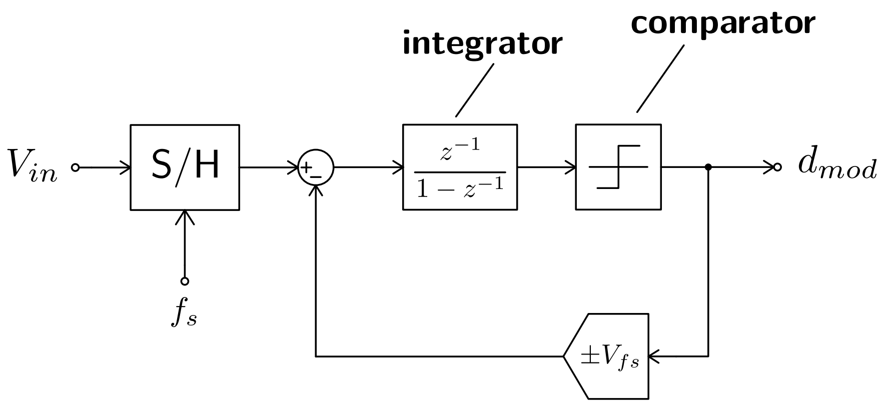


$$H(z) = \frac{z^{-1}}{1-z^{-1}}$$

$$\begin{cases} STF = \frac{H}{1+H} \equiv z^{-1} & \text{(delay)} \\ NTF = \frac{1}{1+H} \equiv 1 - z^{-1} & \text{(differentiator)} \end{cases}$$

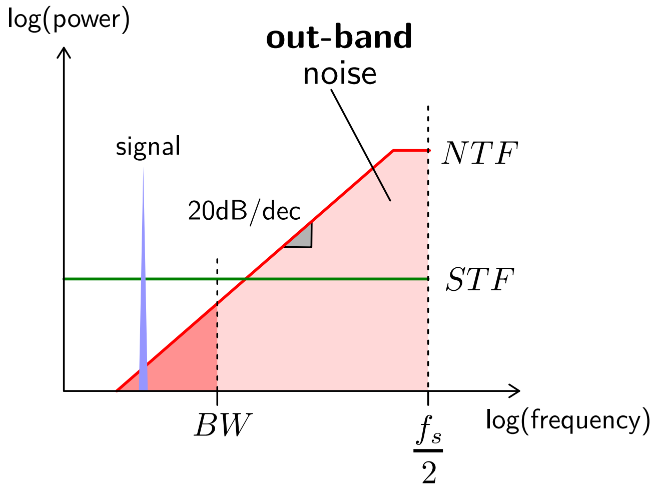
all-pass (z^{-1})

high-pass shaping ($1 - z^{-1}$)

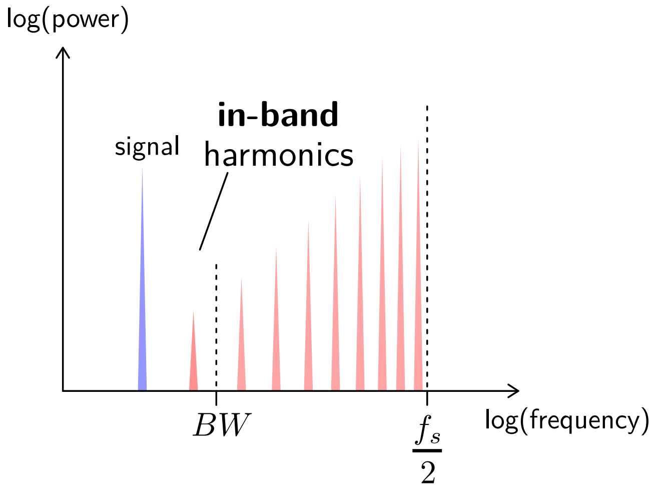
▲ Single-bit feedback DAC is **intrinsically linear**

▼ **Oversampling** is needed

$$OSR \doteq \frac{f_s}{2BW} \gg 1$$

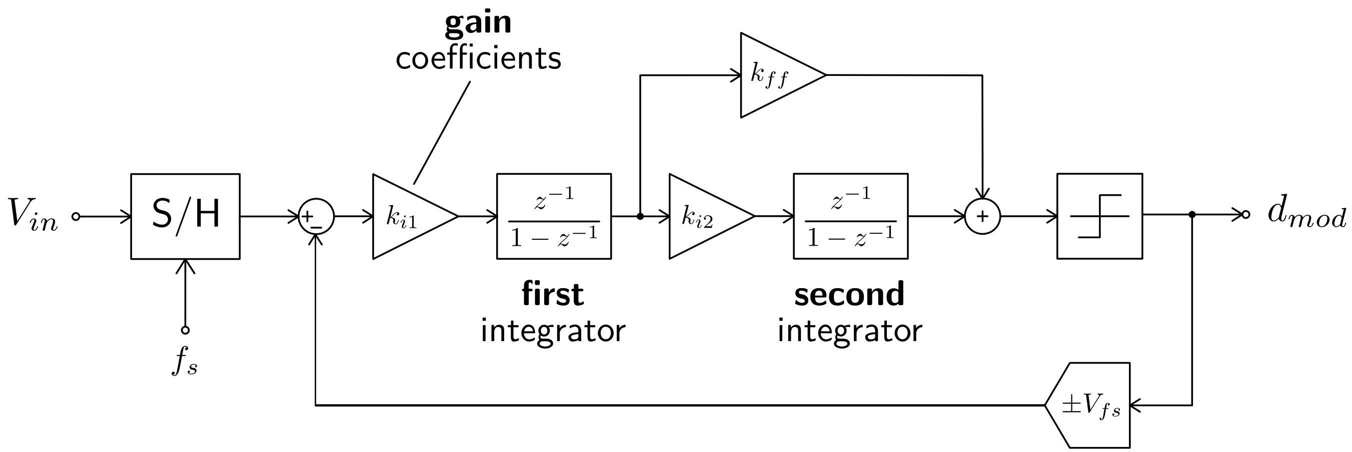


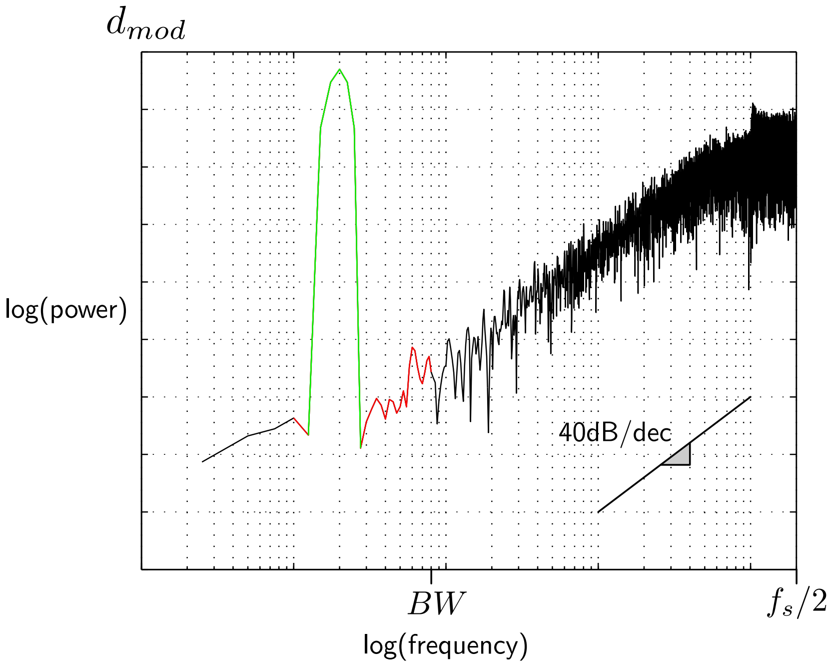
▼ Higher order (**N>1**) shaping to avoid signal to quantization noise correlation (harmonics)



Delta-Sigma Noise Shaping

- **Higher-order** noise shaping (e.g. N=2):

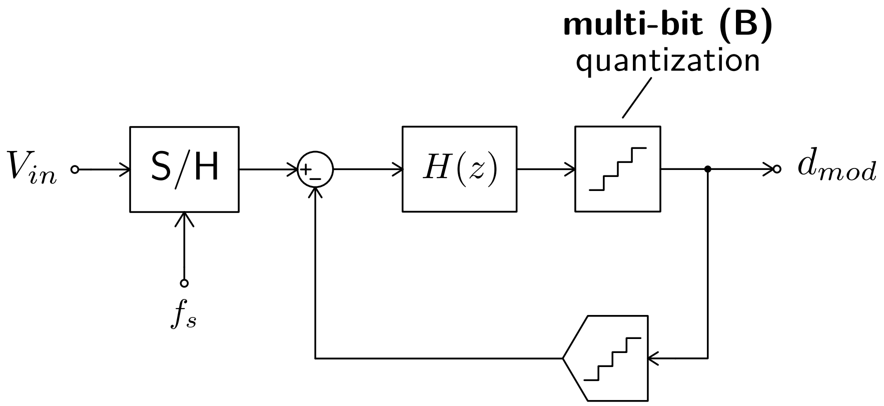




- ▲ **Sharper** noise shaping
- ▲ Signal to quantization noise **uncorrelation** (continuous spectra)
- ▼ Possibility of loop **instability** for N>2
- **Coefficients** optimization!

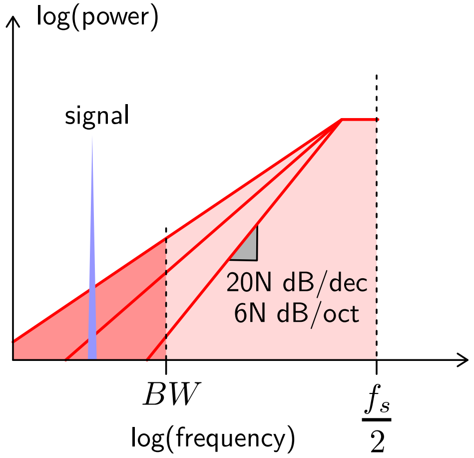
DSM ADC Design

- **N-order B-bit** single loop architecture:



- **Multi-bit** quantization:
  - Resolution added to overall **DR**
  - **Internal full-scale** reduction
  - Feedback DAC **not intrinsically linear**

- **High-order** filtering:
  - **Sharper** noise shaping
  - **Stability** issues



- **Ideal** dynamic range:

$$DR = \frac{3\pi}{2}\left(2^B-1\right)^2(2N+1)\left(\frac{OSR}{\pi}\right)^{2N+1}$$

shaping order — **oversampling** only

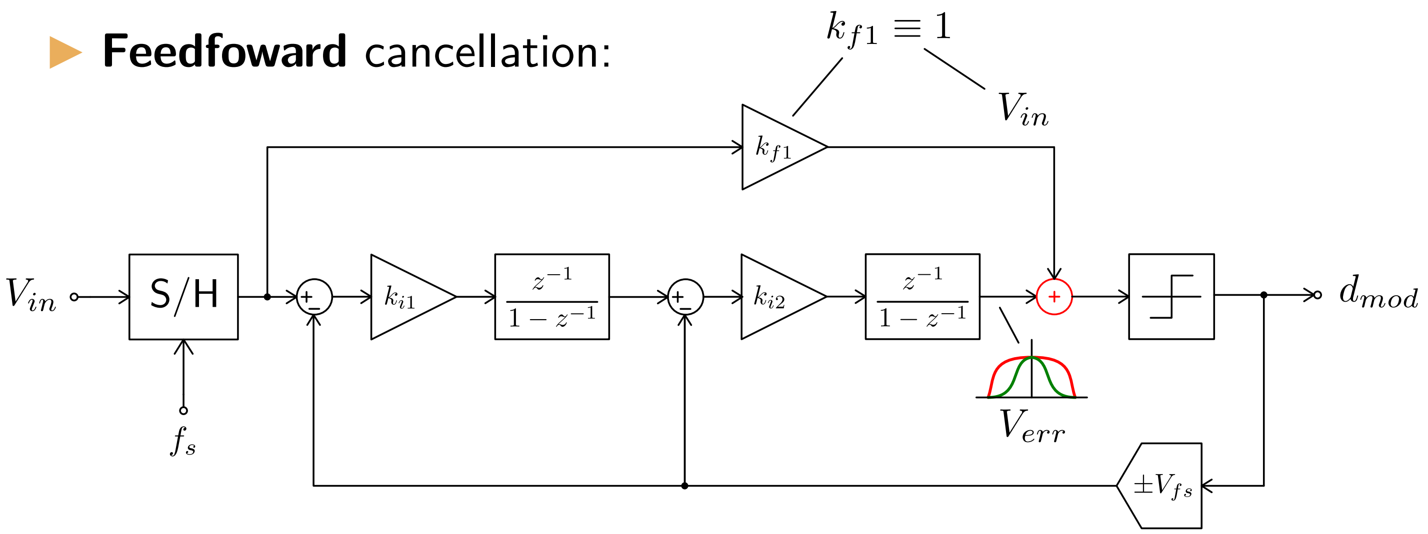
(N+0.5)-bit/oct(OSR)

$$DR[\text{dB}] = 6.7 + 20\log\left(2^B-1\right) + 10\log(2N+1) + 20(N+0.5)\log\frac{OSR}{\pi}$$

direct improvement

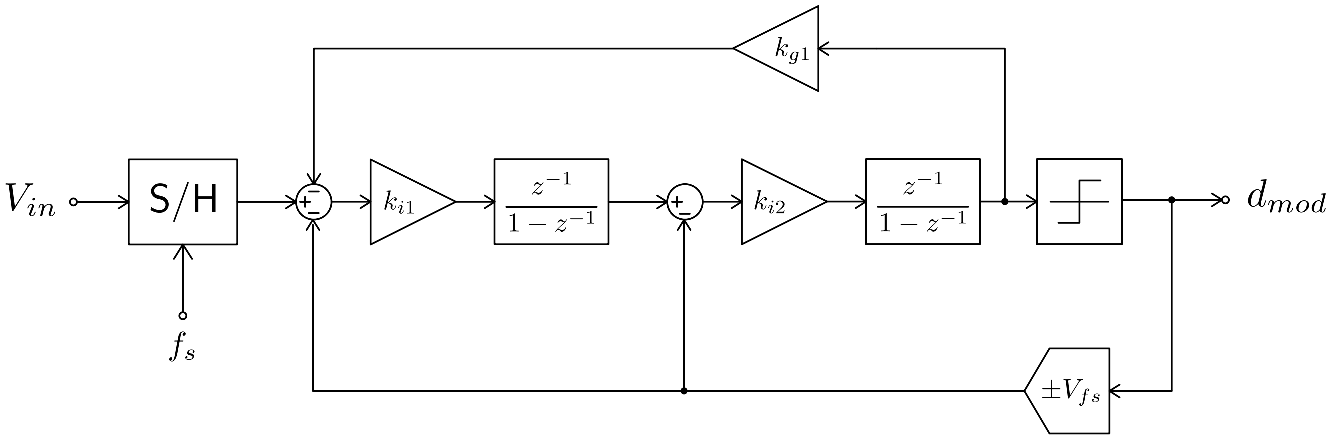
DSM ADC Design

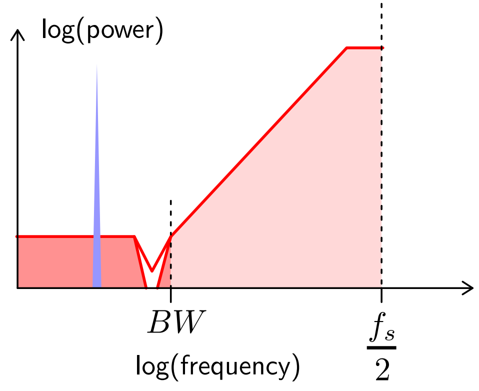
- **Feedfoward** cancellation:



- ▲ **Internal full scale** low occupancy
- ▼ Additional **adder stage** in front of quantizer

- **Resonator** attenuation:

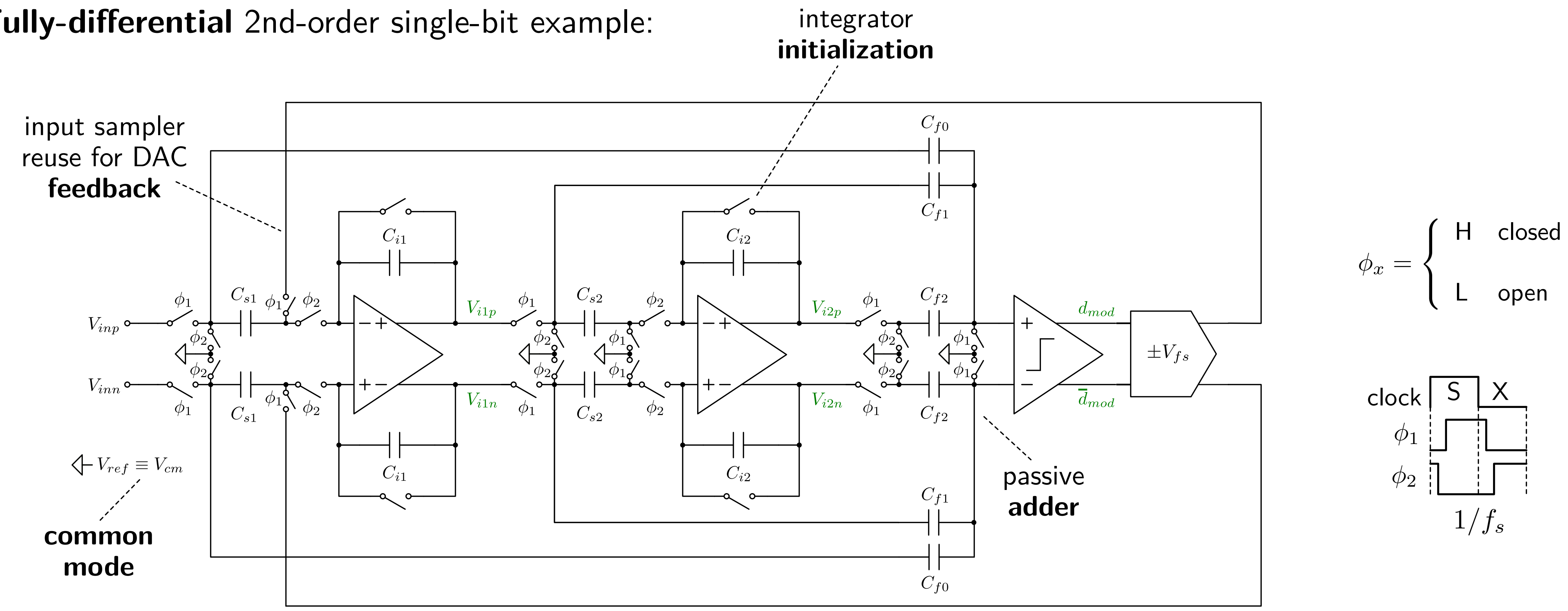




- ▲ Extra noise shaping at **band edge**
- ▼ Zero sensitivity to coefficient **mismatching**

DSM SC Circuits

- **Fully-differential** 2nd-order single-bit example:



$$k_{i1} \doteq \frac{C_{s1}}{C_{i1}} \qquad k_{i2} \doteq \frac{C_{s2}}{C_{i2}} \qquad k_{f1} \doteq \frac{C_{f1}}{C_{f2}} \equiv 1$$

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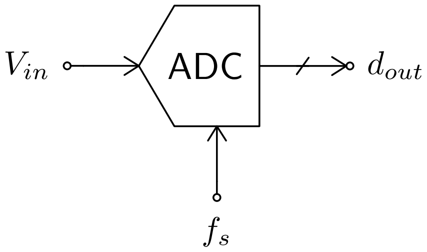
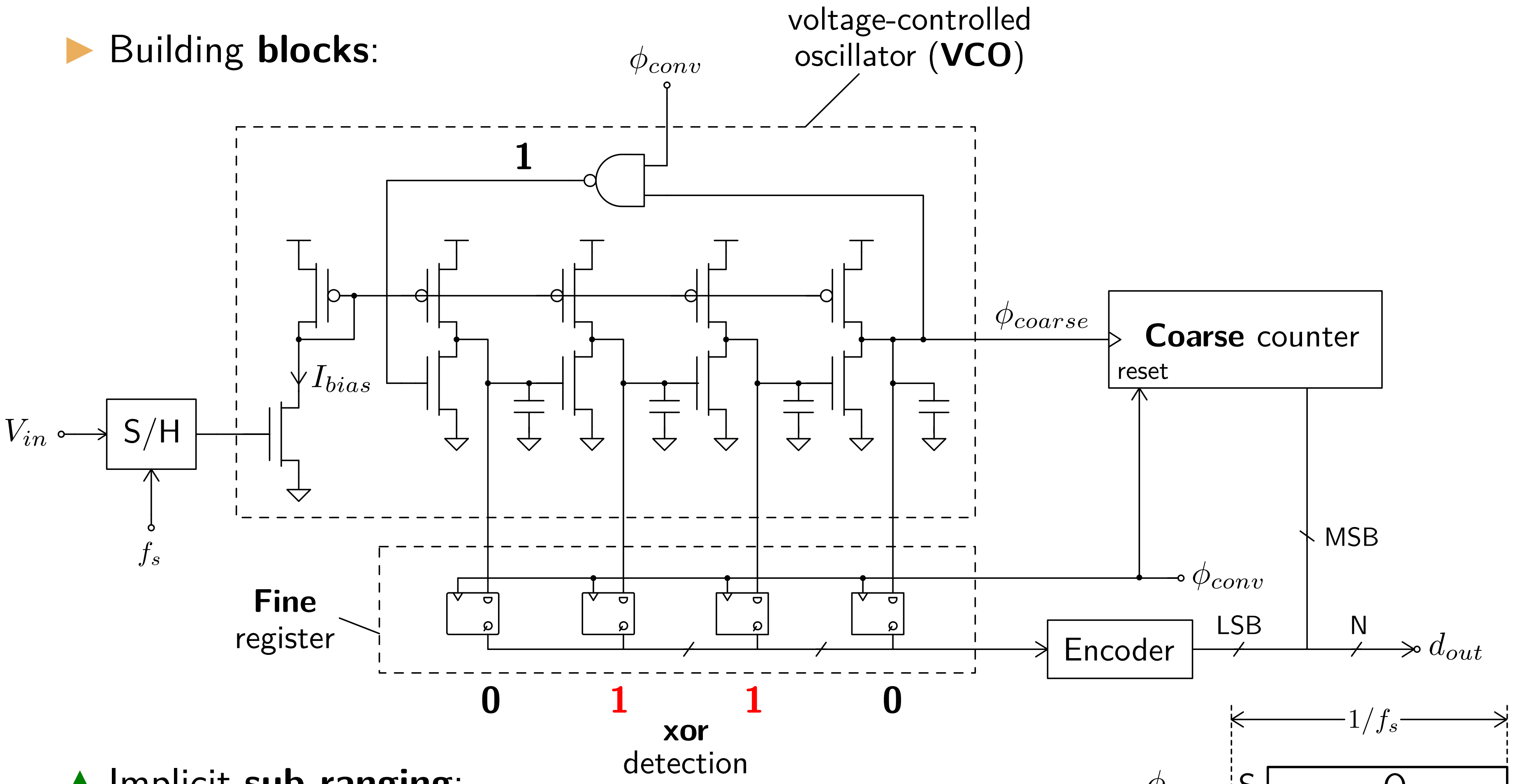
Voltage-to-Frequency ADC

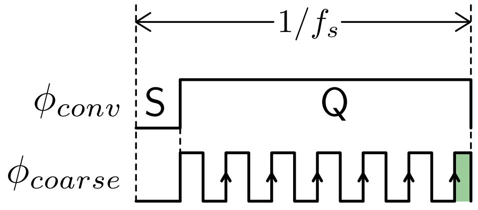


- Building **blocks**:

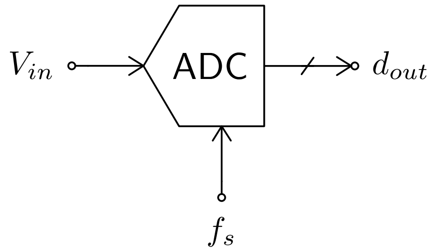


- Implicit **sub-ranging**:

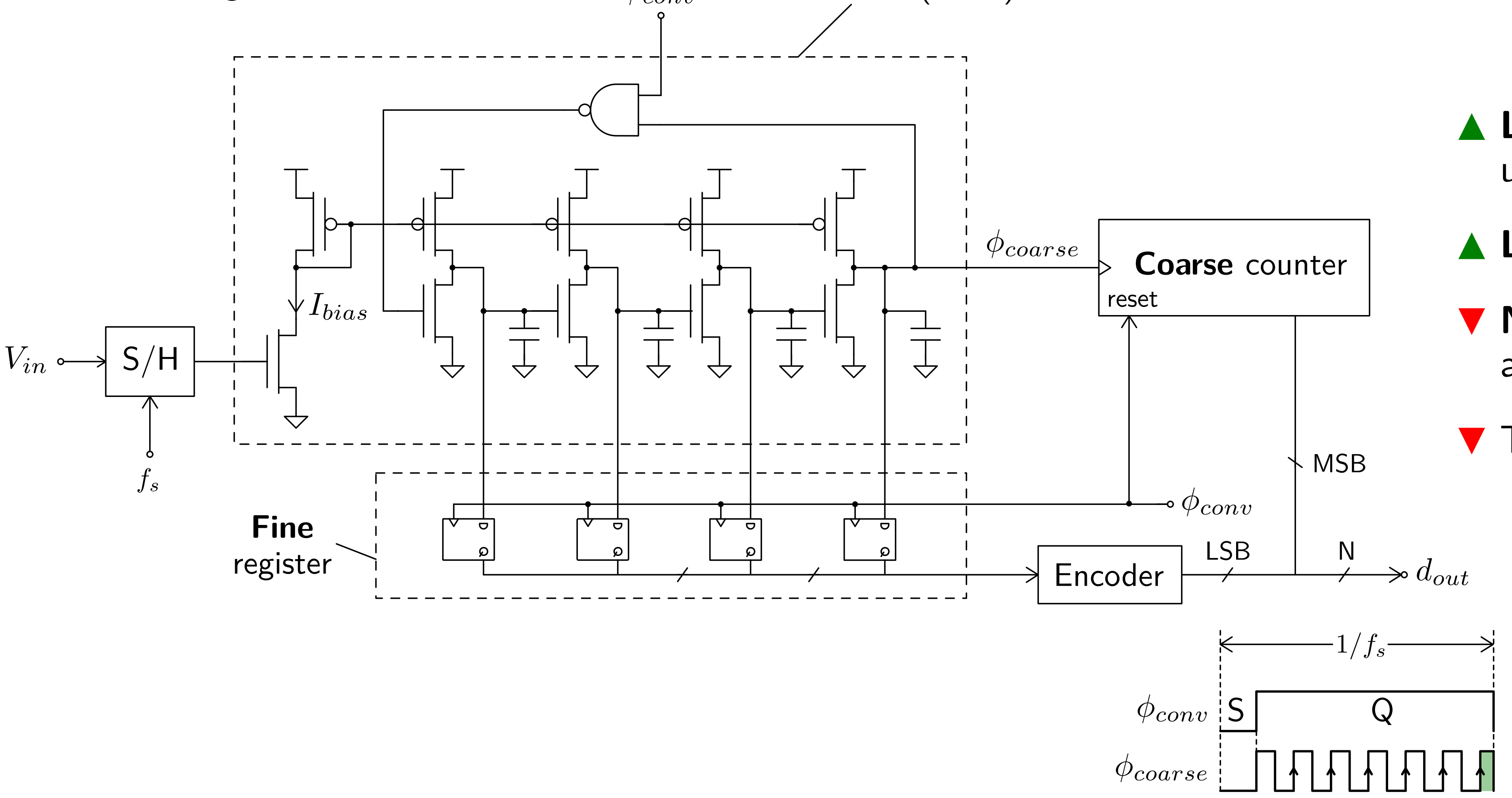
$$f_{VCO} = \left(2^{MSB} - 1\right) f_s \ll (2^N - 1) f_s$$



Voltage-to-Frequency ADC



- Building **blocks**:



- ▲ **Low frequecy** ($f_{coarse} << 2^{ENOB} f_s$), unlike integrating ADCs
- ▲ **Low-voltage** operation
- ▼ **Non-linearity** V_{in}-I_{bias} and I_{bias}-f_{VCO}
- ▼ Technology **sensitivity**