1. Introduction to Integrated Heterogeneous Systems

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Integrated Circuits and Systems
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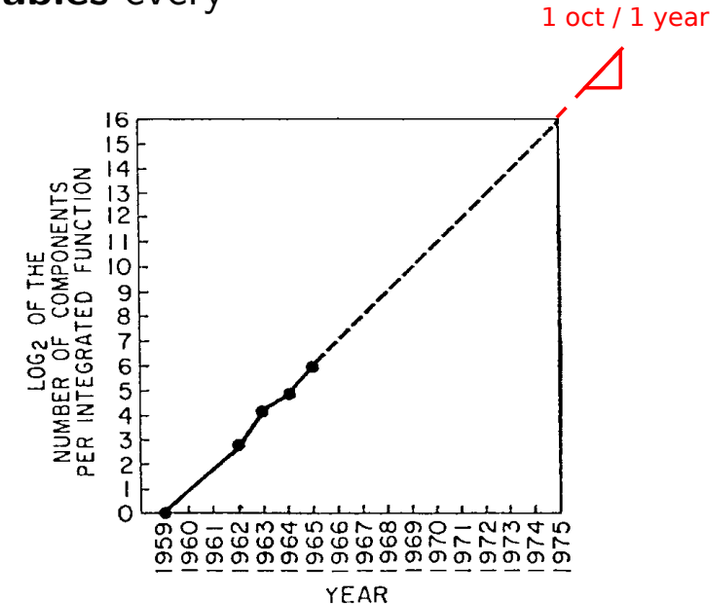
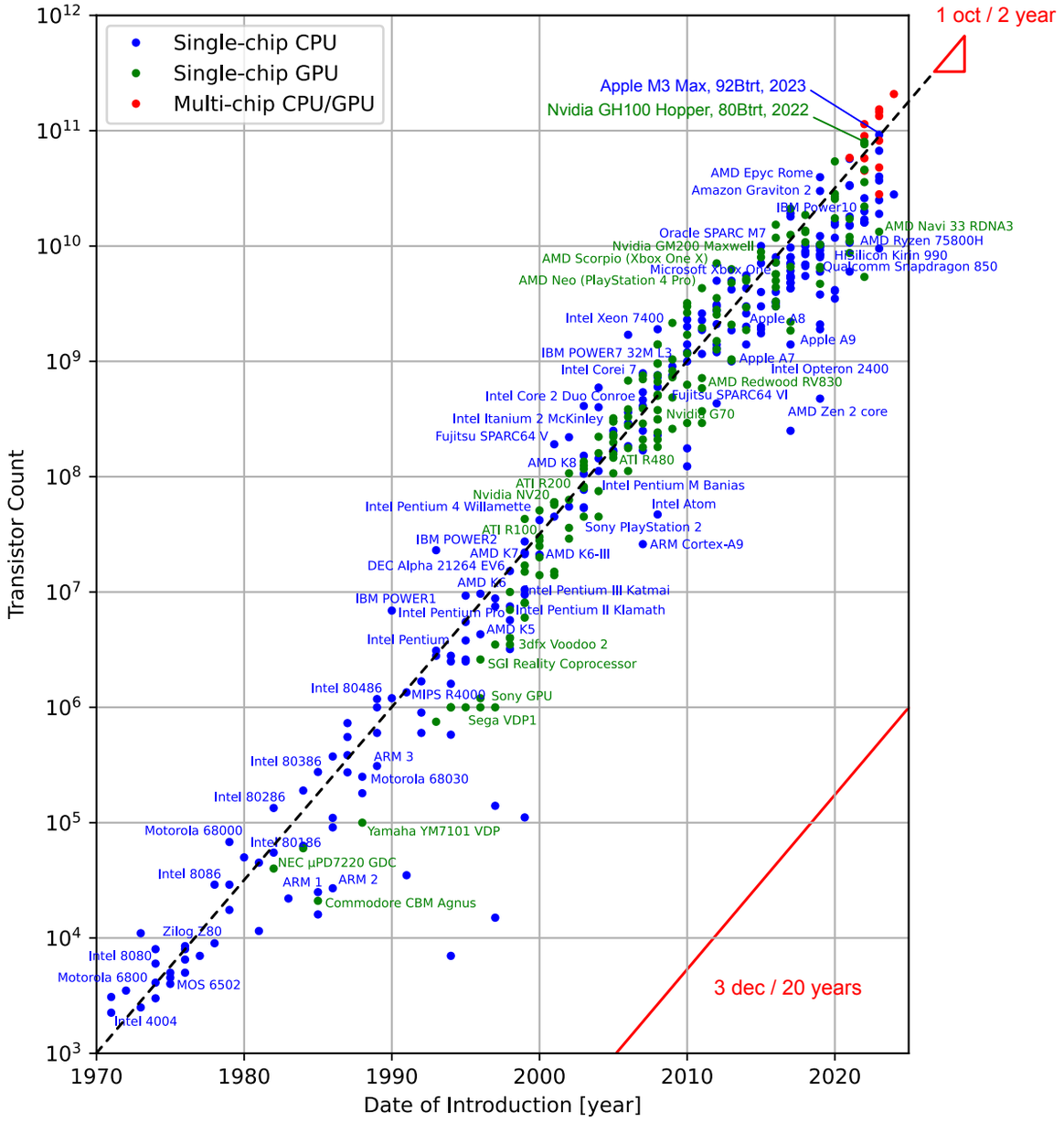
Moore's Law

- Number of transistors per chip **doubles** every **24** months



↗ Gordon E. Moore
Cramming More Components onto Integrated Circuits
Electronics Magazine, 38(8):114–117, Apr 1965
doi.org/10.1109/N-SSC.2006.4785860



↗ Plot built from tabulated data available in wikipedia.org/wiki/Transistor_count

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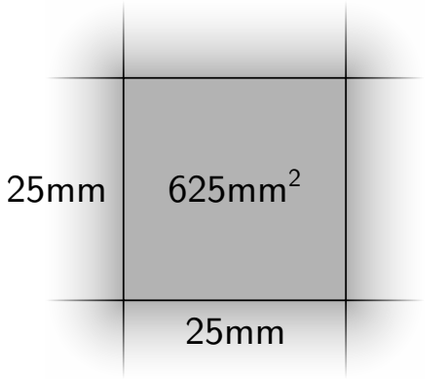
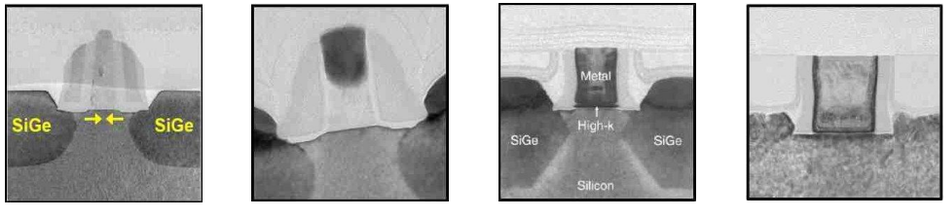
Typ. reticle size



Technology **nodes**

$\div\sqrt{2}$

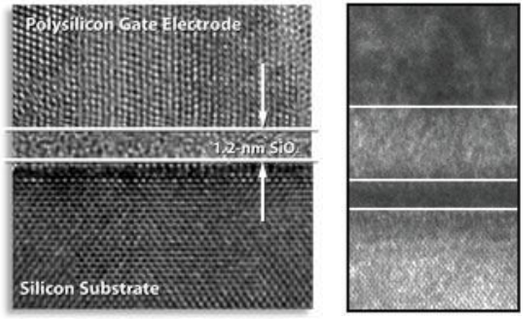
2004	2006	2008	2010
90nm	65nm	45nm	32nm



Front-end of line (**FEOL**)

GEN1 GEN2 GEN1 GEN2

SiGe-strained Silicon → High-k metal gate



1.2-nm SiO_2 dielectric (5 atomic layers!)

Low-resistance layer

Work-function metal

3nm-Hafnium dielectric

Silicon substrate

↗ intel.com

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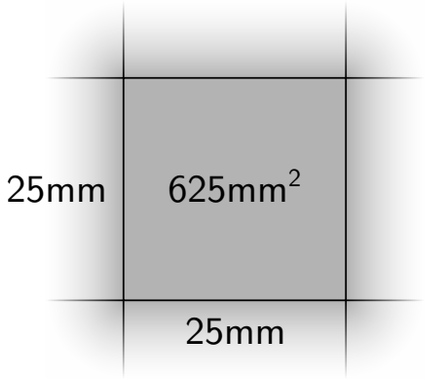

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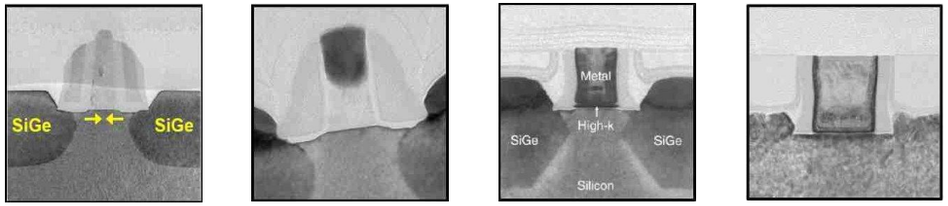

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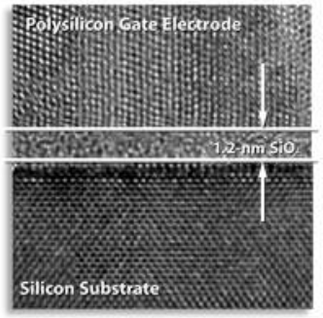
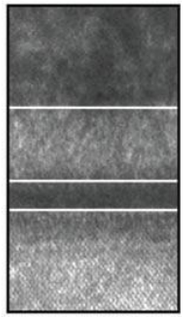




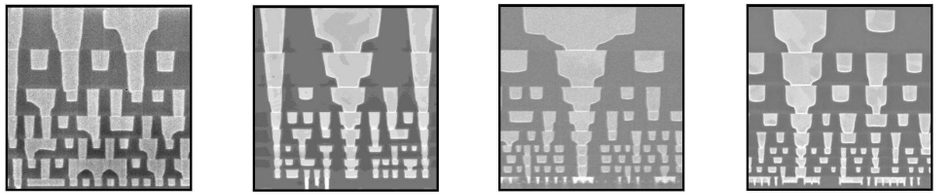
Low-resistance layer

Work-function metal

3nm-Hafnium dielectric

Silicon substrate

↗ intel.com



7M, **Al** 9M, low-k, **Cu**

Back-end of line (**BEOL**)

More Moore

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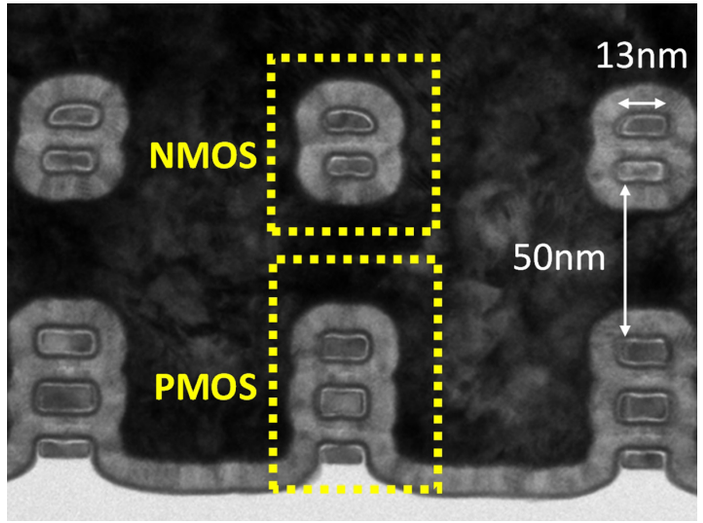
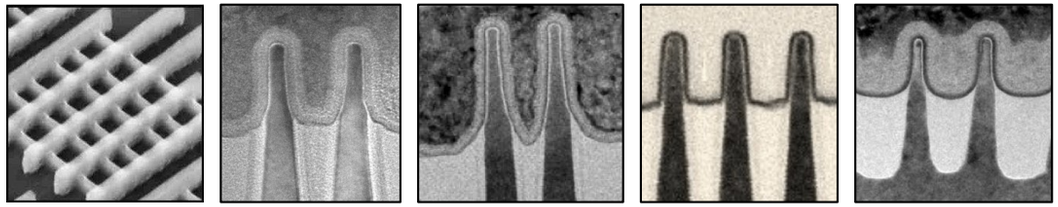


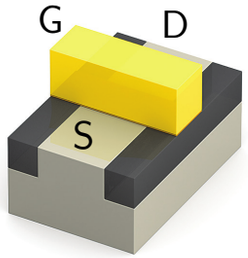
Technology **nodes**

2012	2014	2016	2018	2020
22nm	14nm	10nm	7nm	5nm

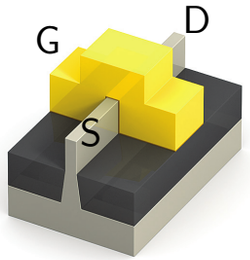


↗ tsmc.com

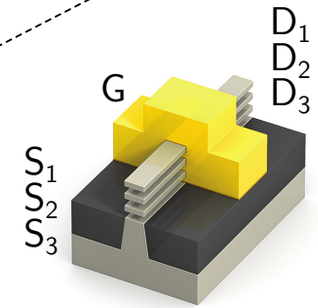
3D FinFET + SOI + multiple patterning



Planar FET

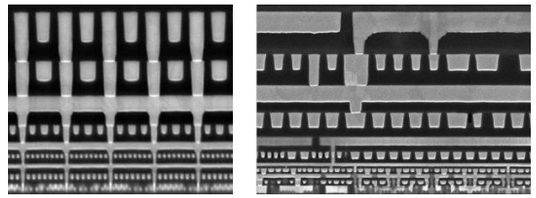


FinFET



Nanosheet/Gate-All-Around FET

↗ Samuel K. Moore
Intel's Stacked Nanosheet Transistors Could Be the Next Step in Moore's Law
IEEE Spectrum, Dec 2020
spectrum.ieee.org



>10M, ultra low-k

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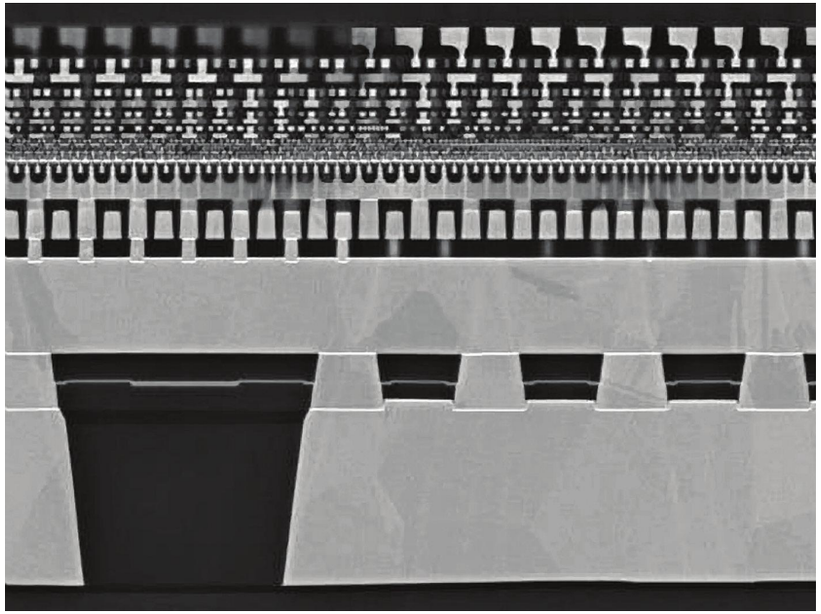

↗ Gwendolyn Rak
Intel Hopes to Leapfrog Its Competitors
IEEE Spectrum, Jan 2024
spectrum.ieee.org

Future **3D** technologies

↗ Luc Van den hove
20-Year Semiconductor Roadmap: Tearing Down the Walls
IMEC International Technology Forum, July 2022
imec-int.com

More Moore

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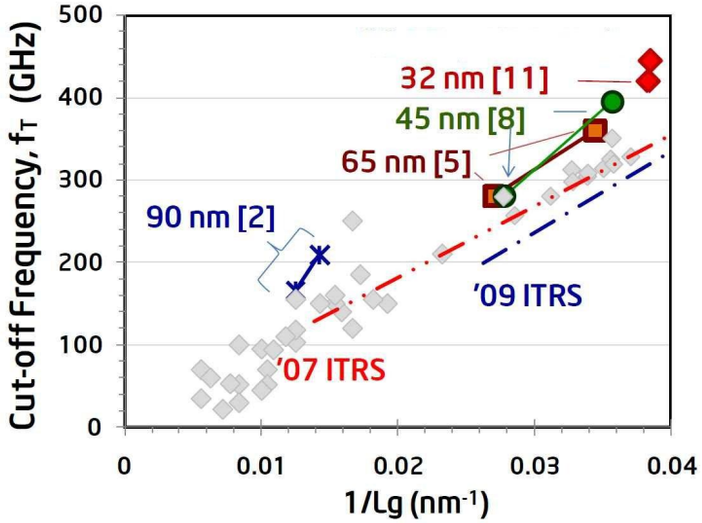
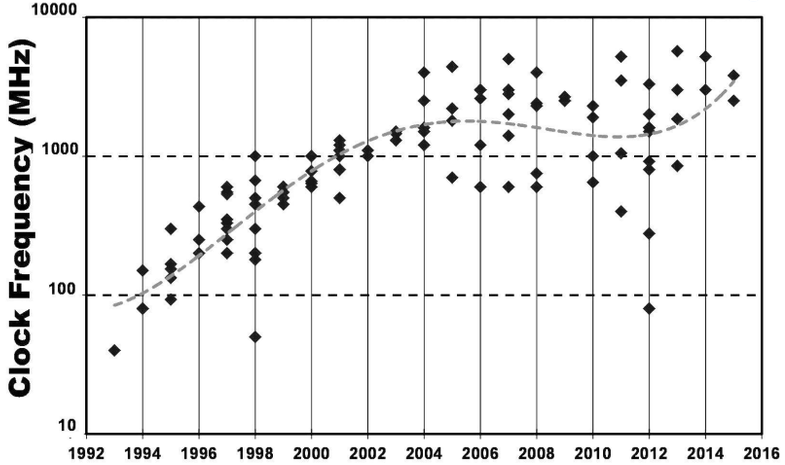
- **Cut-off frequency** increases, but not exploited due to RF and **power** limitations → parallelism

↗ intel.com

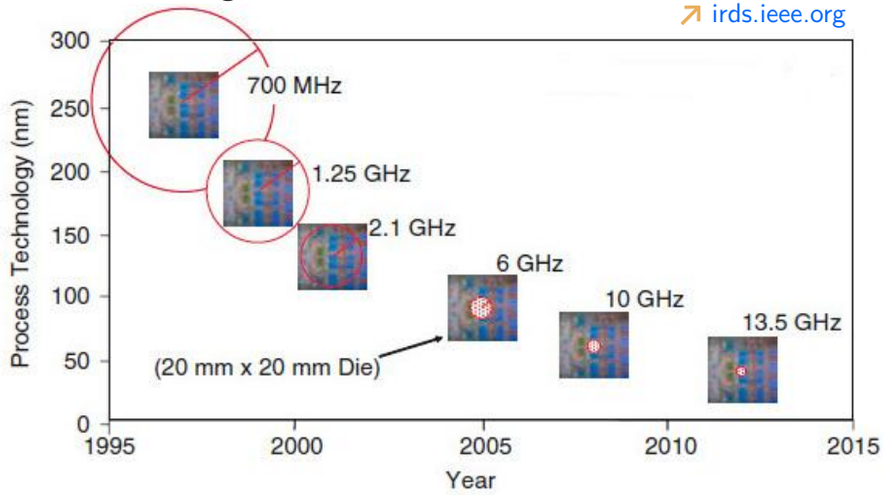


↗ isscc.org

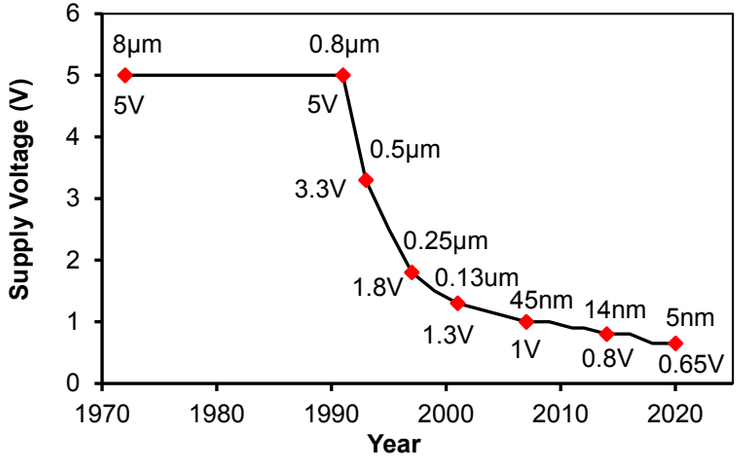


wavelength

↗ irds.ieee.org



↗ Zhang et al. (2022)



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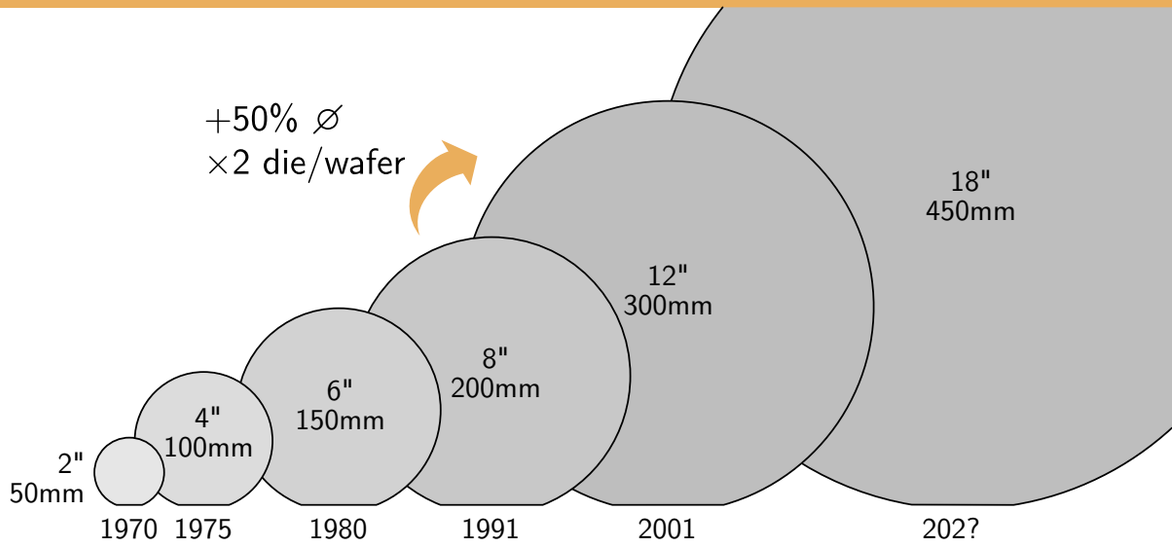

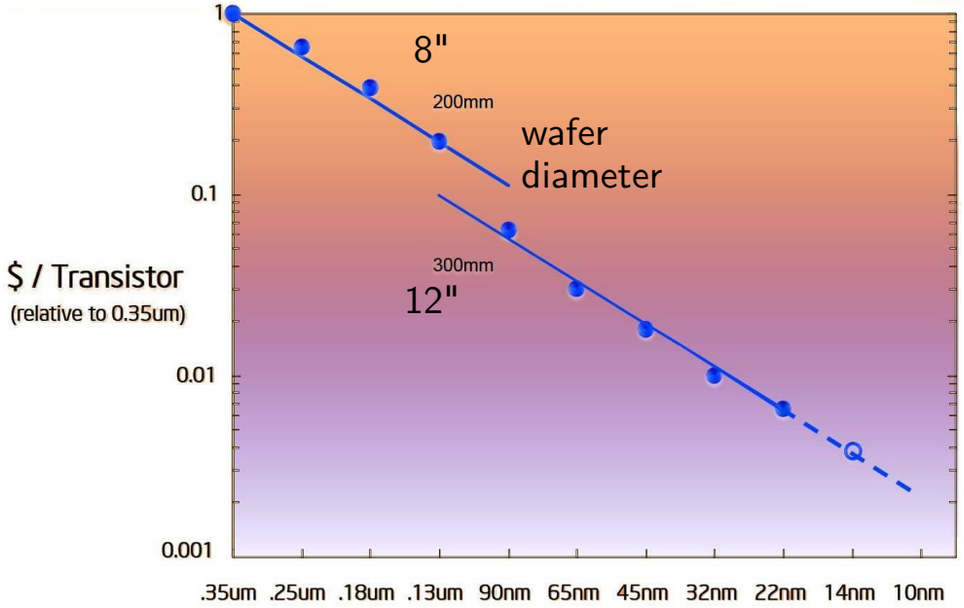

↗ intel.com

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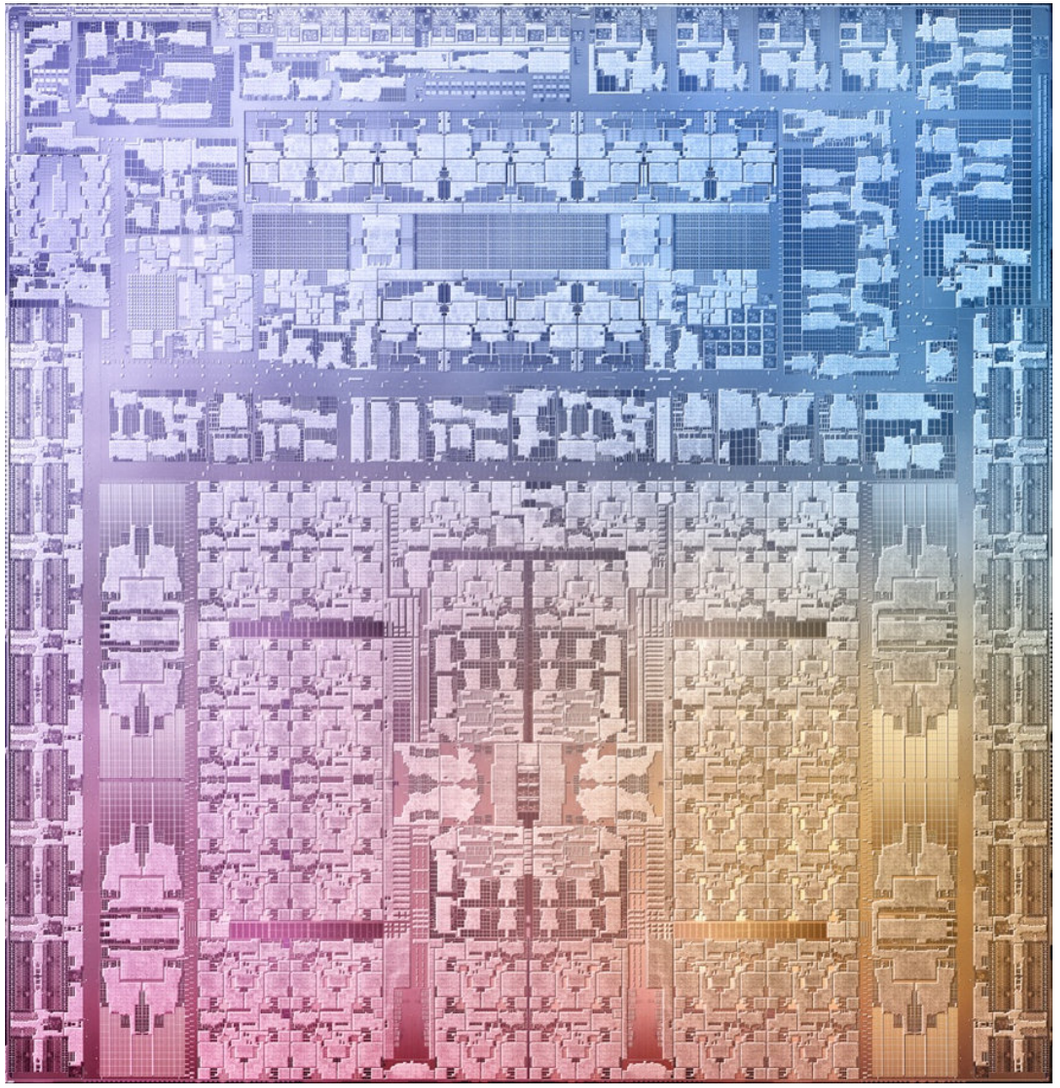
- ▲ **Cut-off frequency** increases, but not exploited due to RF and **power** limitations → parallelism
- ▲ **Cost/transistor** improved also due to wafer scaling (capacity)
- ▼ Small is beautiful, but what to do with so **many**, **inexpensive** and super **fast** devices?

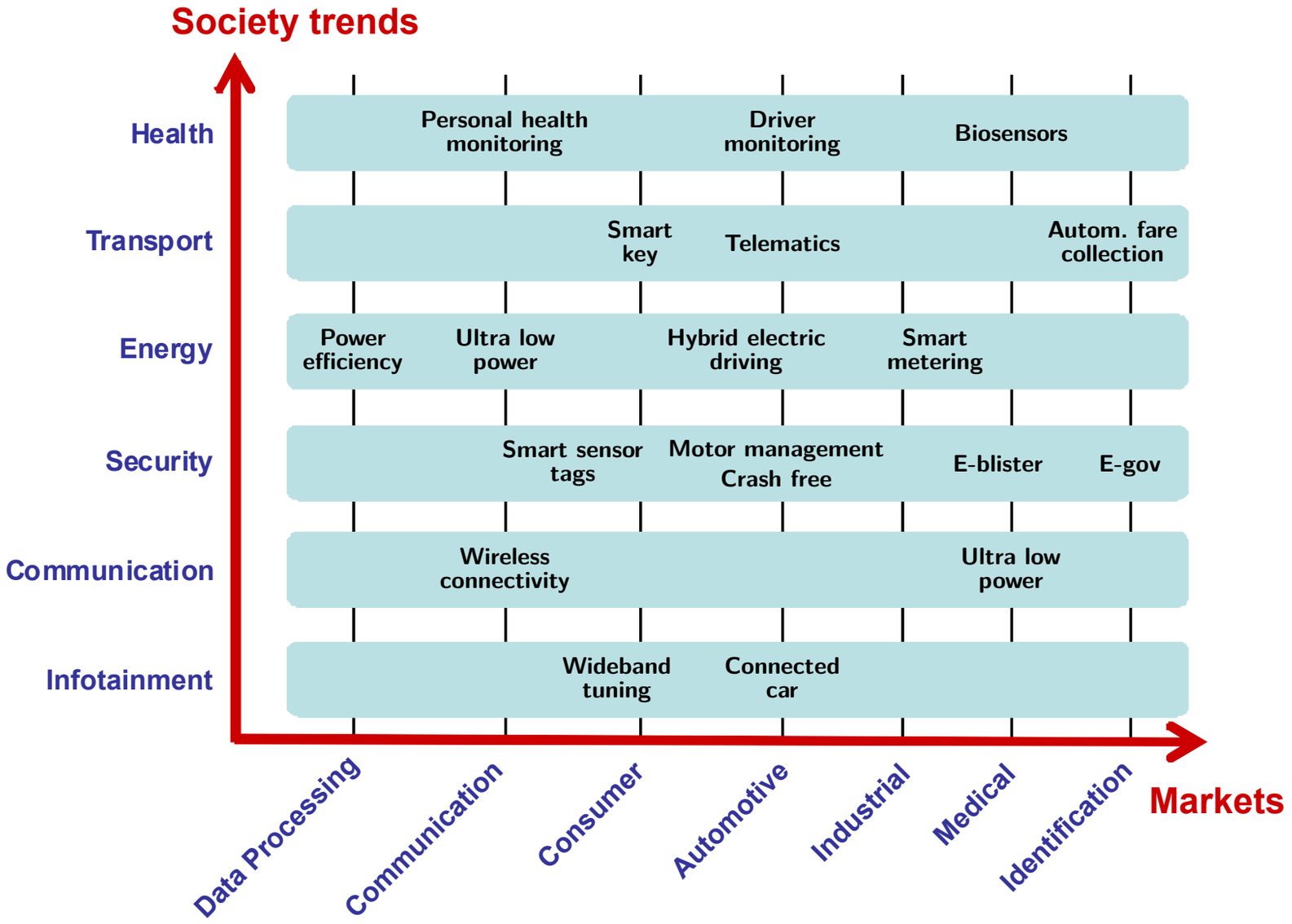
↗ apple.com



Apple M3 Max processor with 12 P-cores 4 E-cores and 40 GPU cores in 15-metal 3-nm FinFET TSMC technology featuring **92 billion transistors**

More than Moore

- Diversification of technology **applications**
- **Ubiquitous** computing
- Not only signal processing but:
  - Smart **sensing**
  - Wireless **communications**
  - **Power** control
- **Multi-domain** integrated systems:
  - Physics
  - Chemistry
  - Biology
  - Medicine



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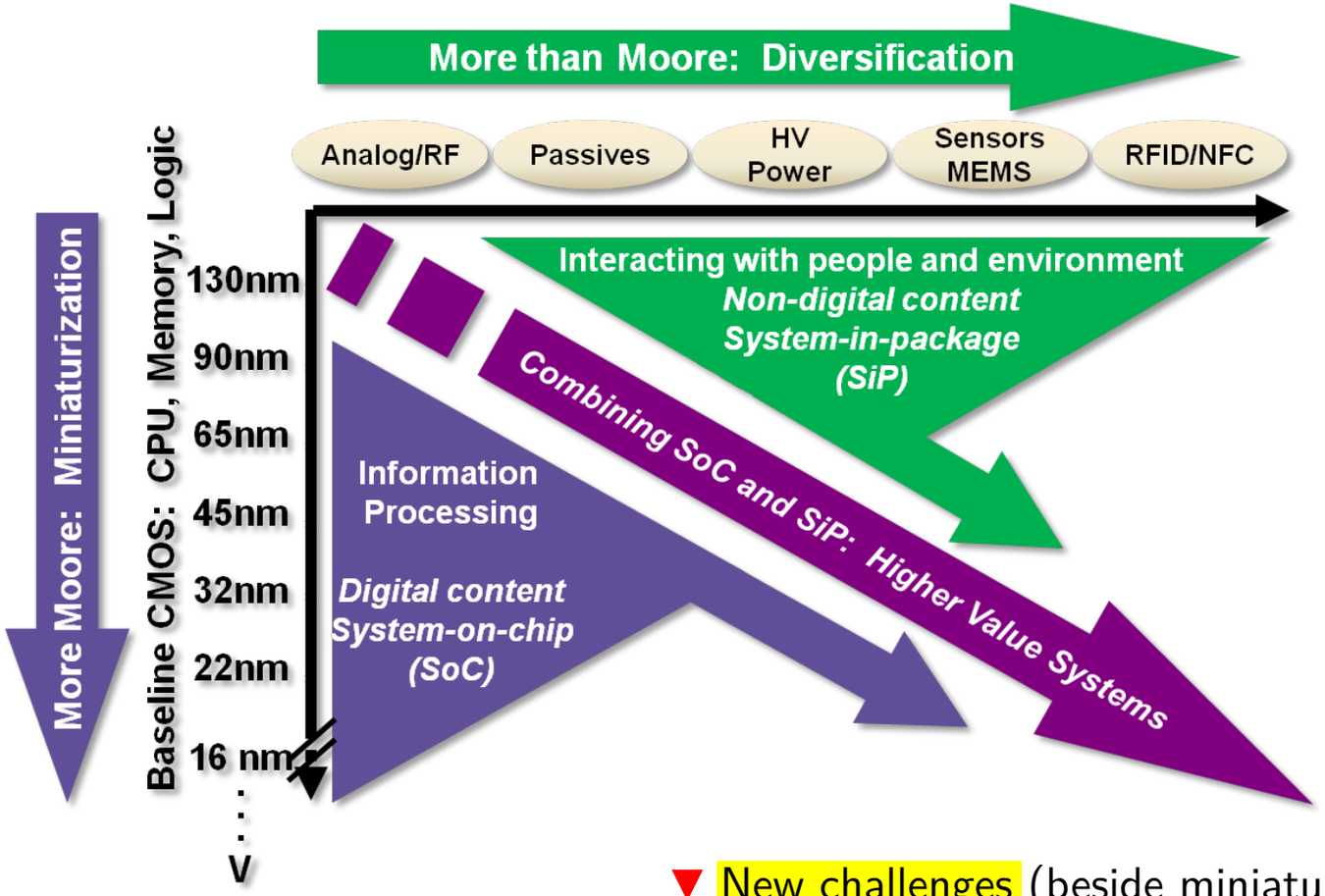
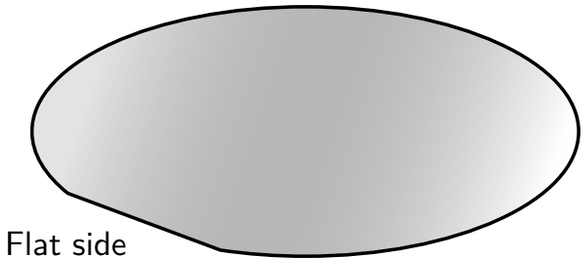
  - Chemistry
  - Biology
  - Medicine

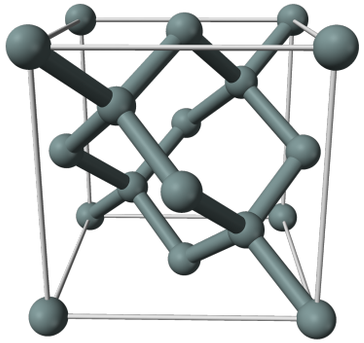


- New challenges (beside miniaturization):
  - CMOS technologies with extra process **modules**
  - **Hetereogeneous** circuit design (A/D/RF/MEMS/power...)
  - Application-specific **packaging**

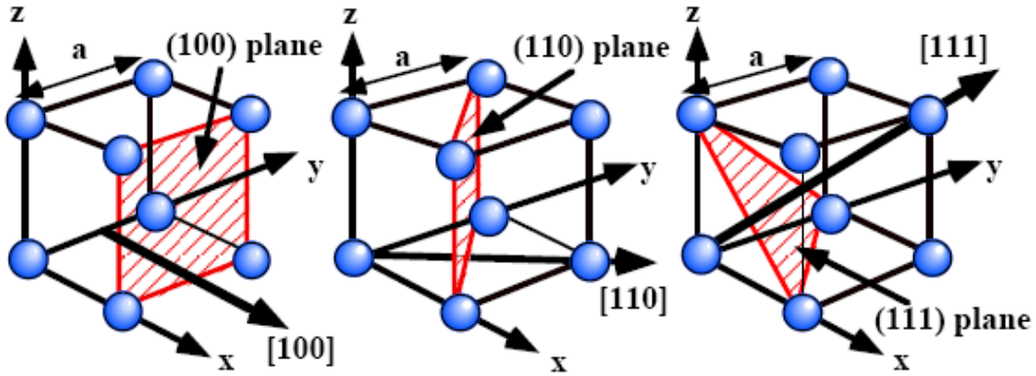
Silicon Wafer

- Polished **monocrystalline** slice
- **Periodic** atomic lattice



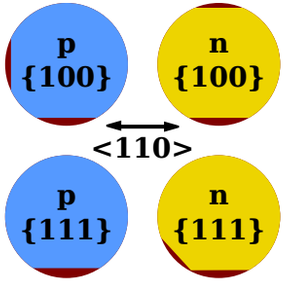


~5Å lattice spacing



CMOS technologies

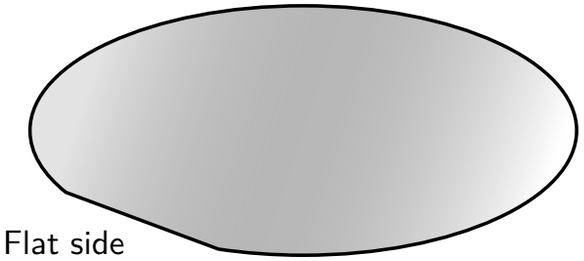
Bipolar technologies

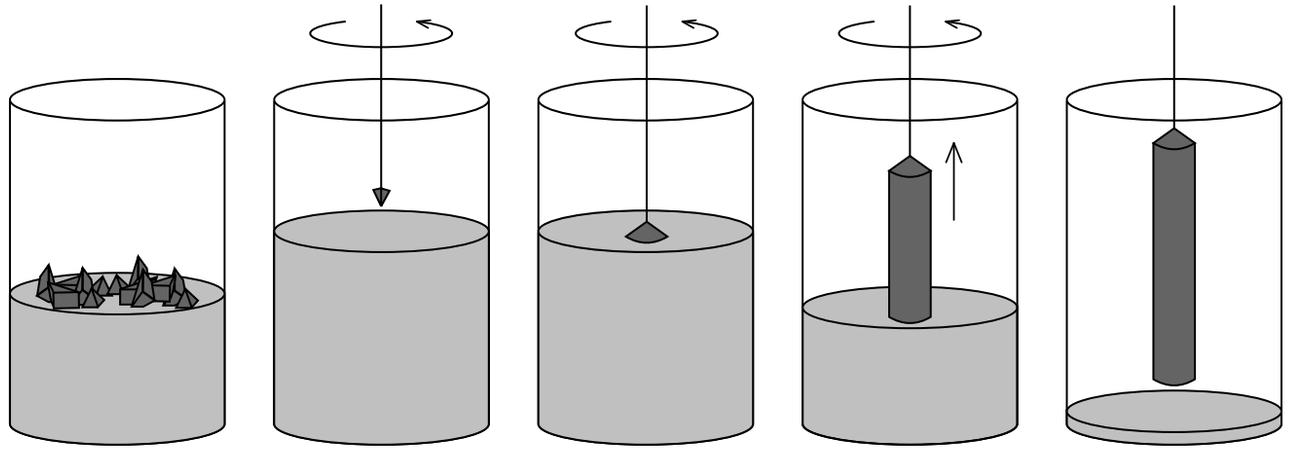


- Doping type
- Crystalline plane

Silicon Wafer

- Polished **monocrystalline** slice
- **Periodic** atomic lattice
- Obtained from cylindrical **ingots**

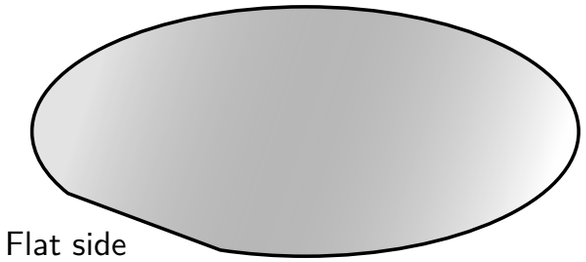




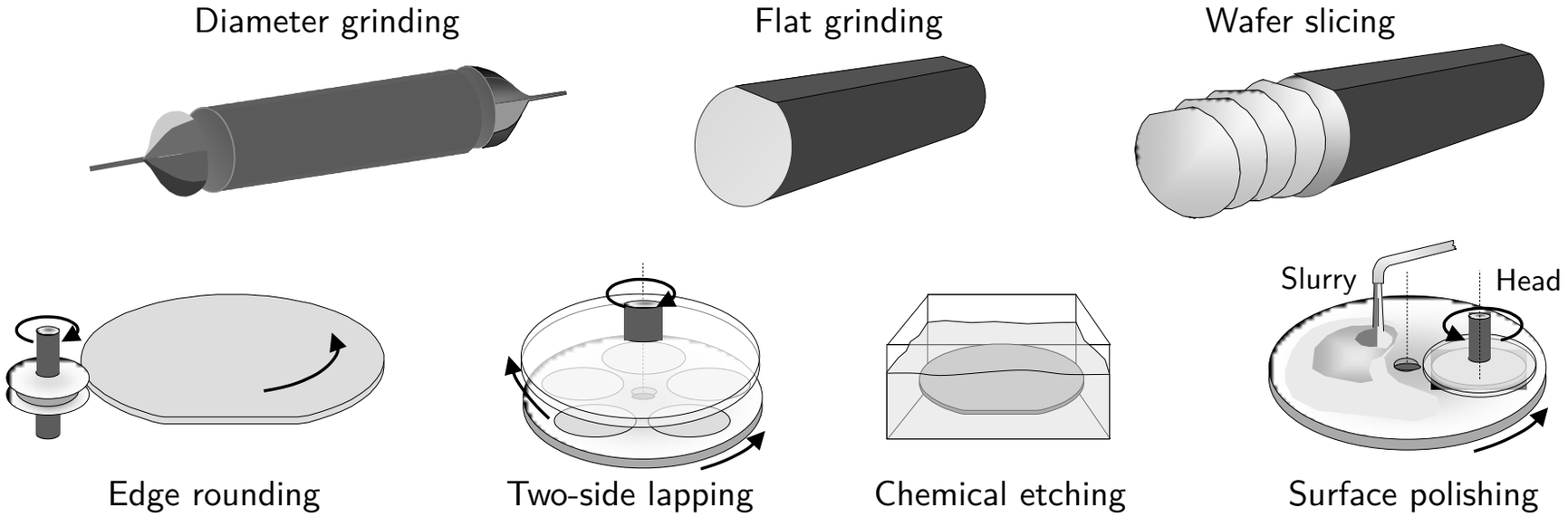
Czochralski method

Silicon Wafer

- Polished **monocrystalline** slice
- **Periodic** atomic lattice
- Obtained from cylindrical **ingots**
- Grinding, slicing and polishing

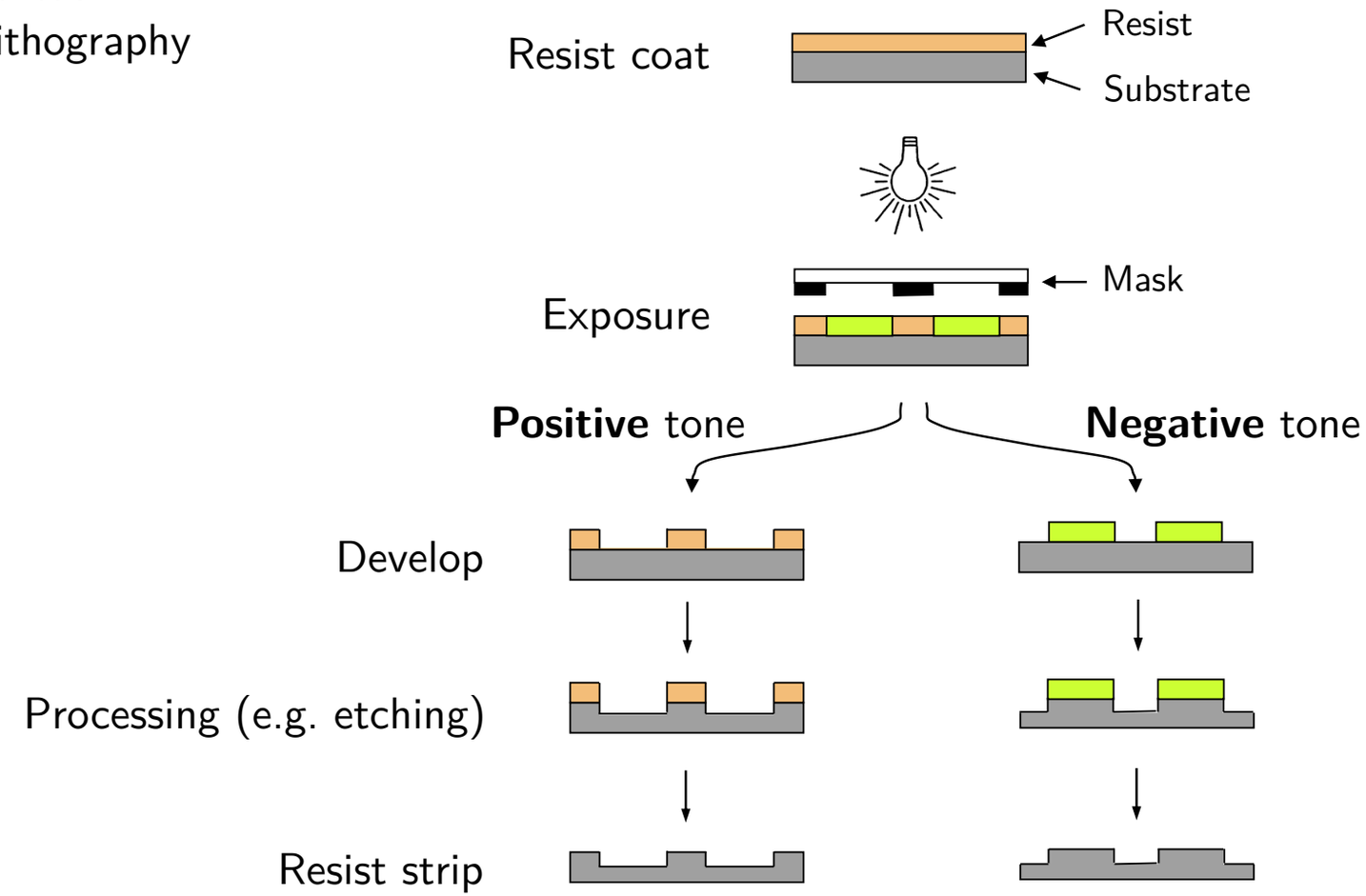


- 200-µm to 750-µm thicknesss
- Bulk, epitaxial, Silicon-on-insulator (SOI)



Wafer Processing

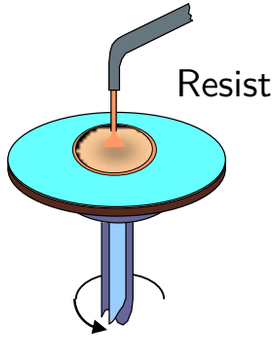
- **Patterning** areas using photolithography



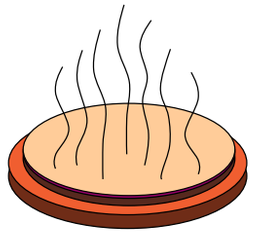
Wafer Processing

- **Patterning** areas using photolithography

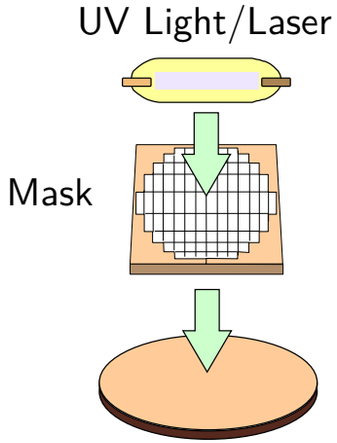
1. Vapor prime



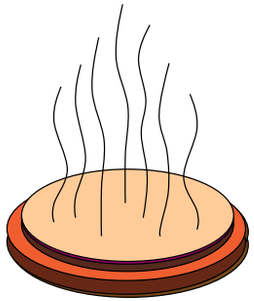
2. Spin coat



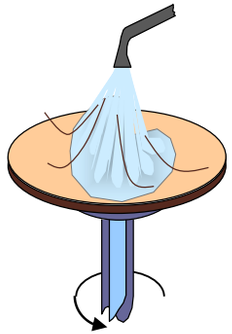
3. Soft bake



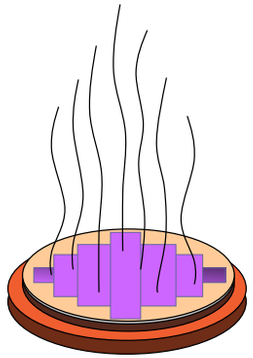
4. **Alignment** and exposure



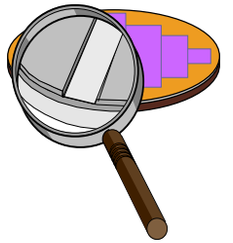
5. Post-expsure bake



6. Develop



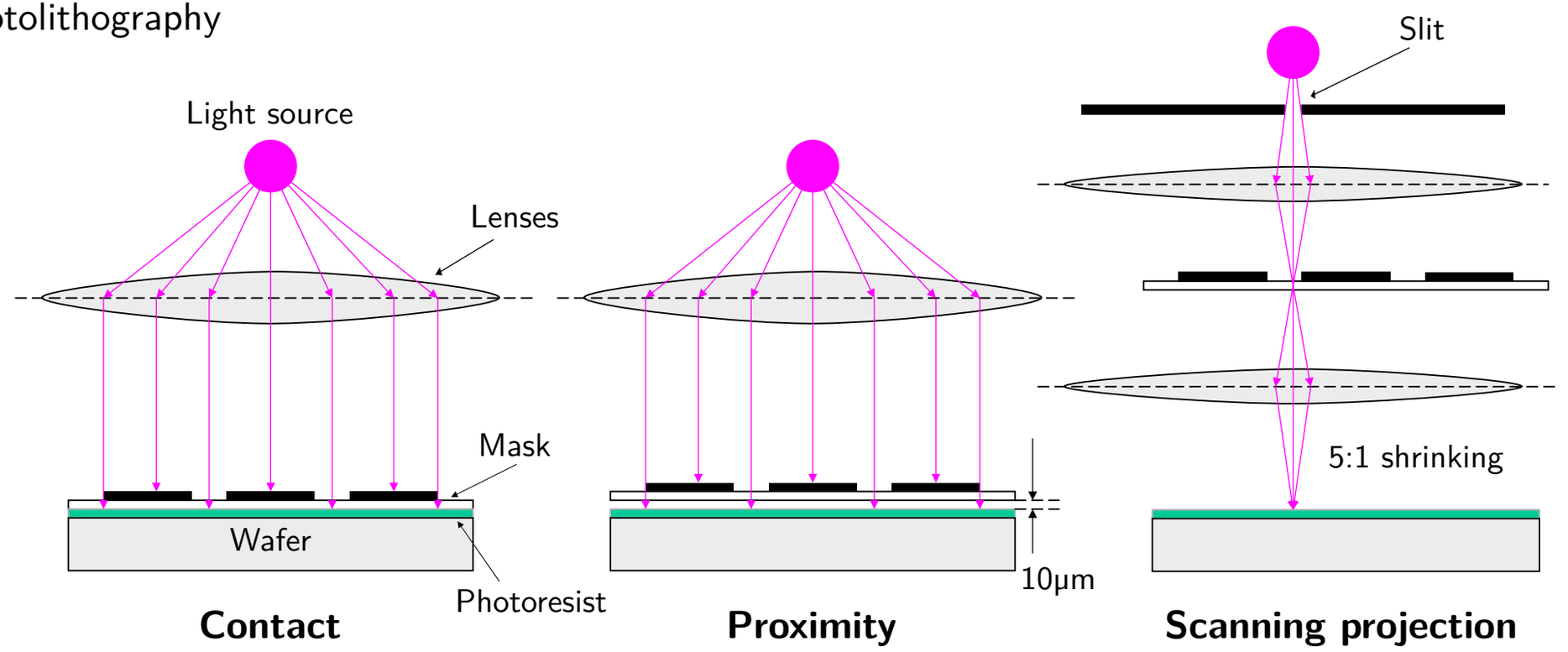
7. Hard bake



8. Inspection

Wafer Processing

- **Patterning** areas using photolithography



Contact

- ▲ Simple equipment
- ▼ Limited mask lifetime

Proximity

- ▲ No direct contact
- ▼ Resolution >3µm

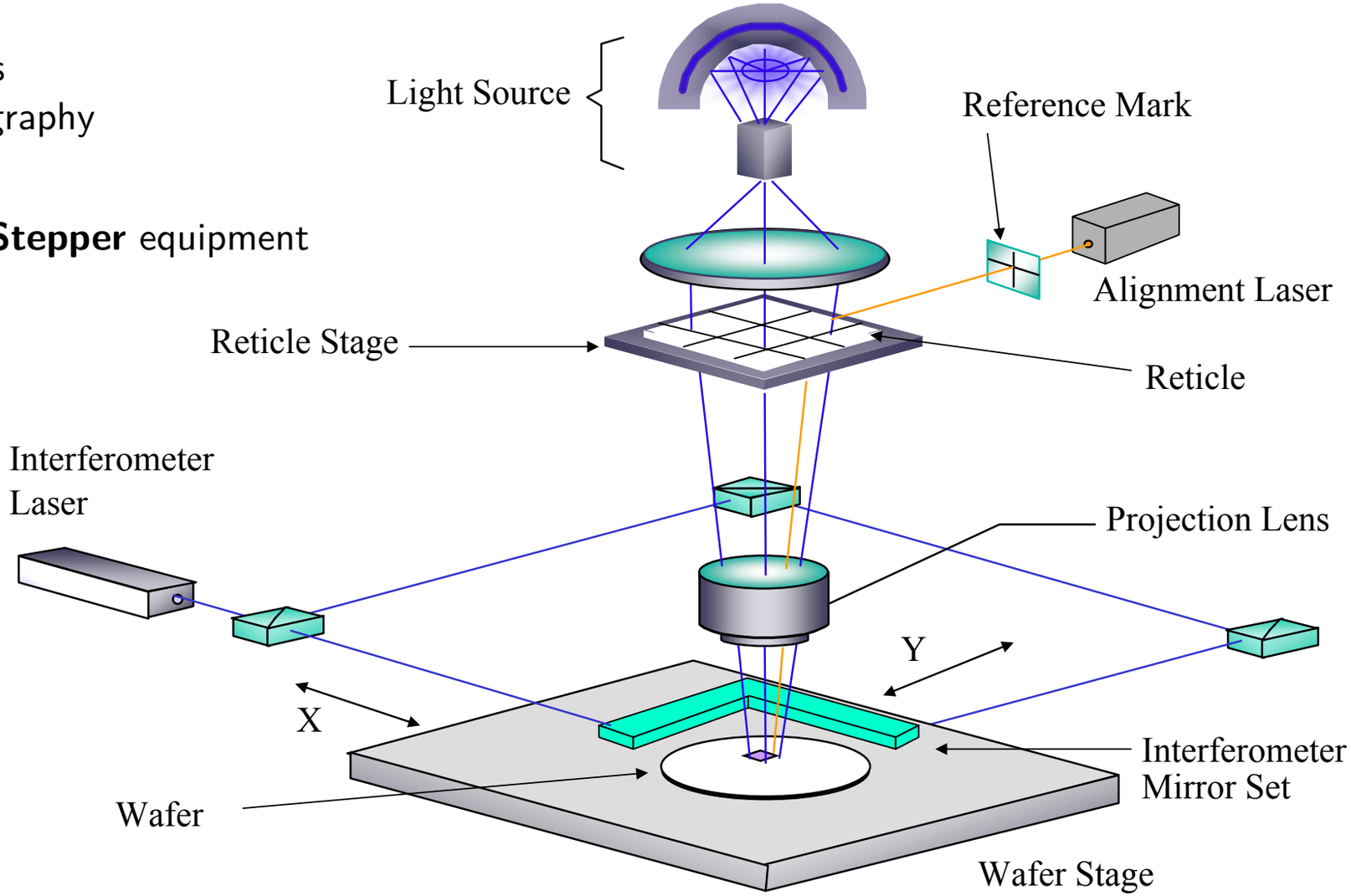
Scanning projection

- ▲ High resolution
- ▼ Expensive and slower

Wafer Processing

- **Patterning** areas using photolithography

Stepper equipment



Wafer Processing

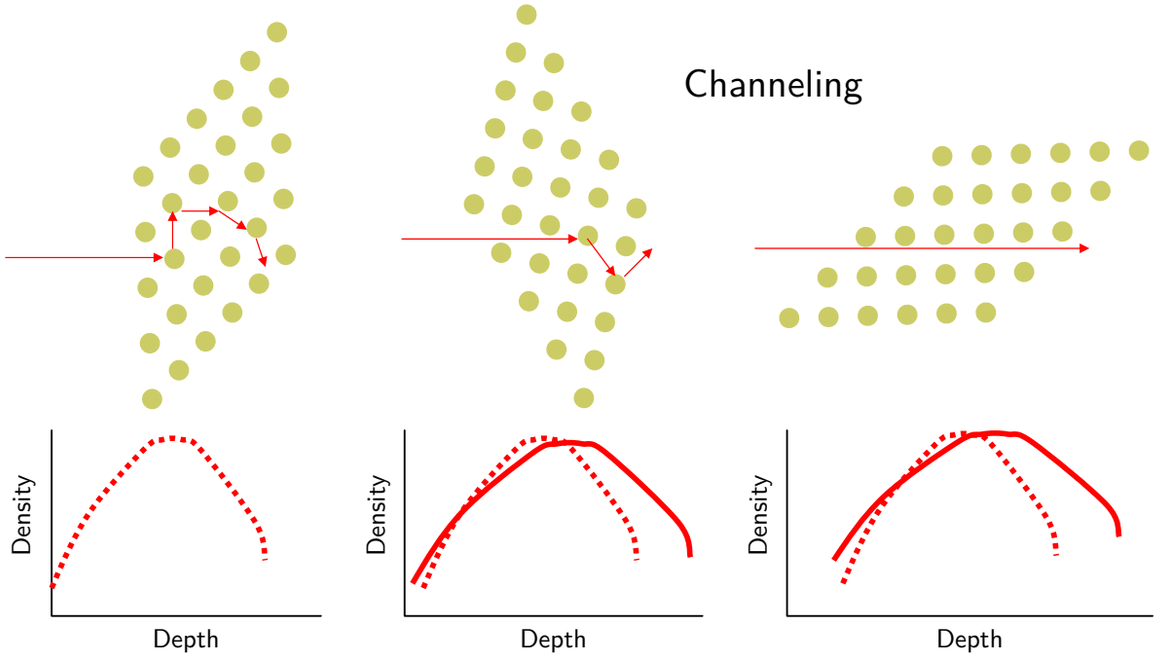
- **Patterning** areas
  using photolithography

UV Light source	Name	Wavelength (nm)	Application feature size (μm)
Mercury Lamp	G-line	436	0.50
	H-line	405	
	I-line	365	0.35 to 0.25
Excimer Laser	XeF	351	
	XeCl	308	
	KrF (DUV)	248	0.25 to 0.15
	ArF	193	0.18 to 0.13
Fluorine Laser	F_2	157	0.13 to 0.1
		124	
		10	

EUV

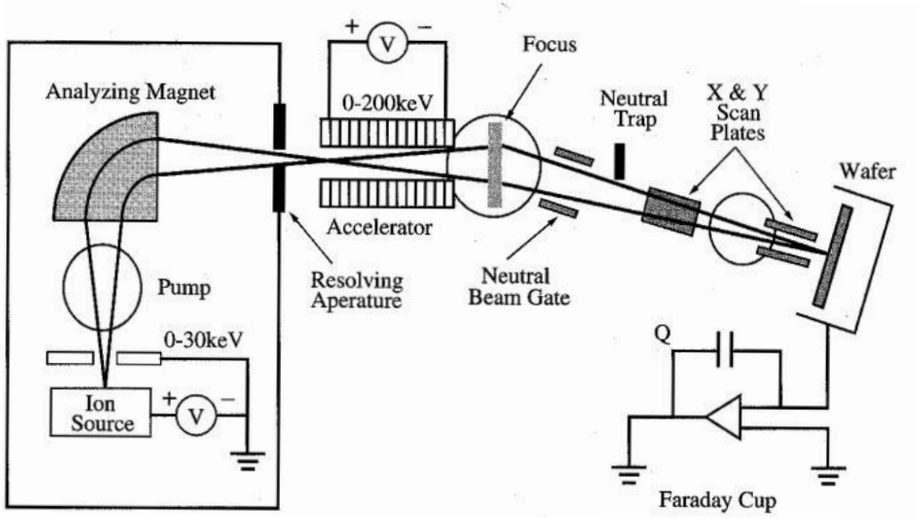
Wafer Processing

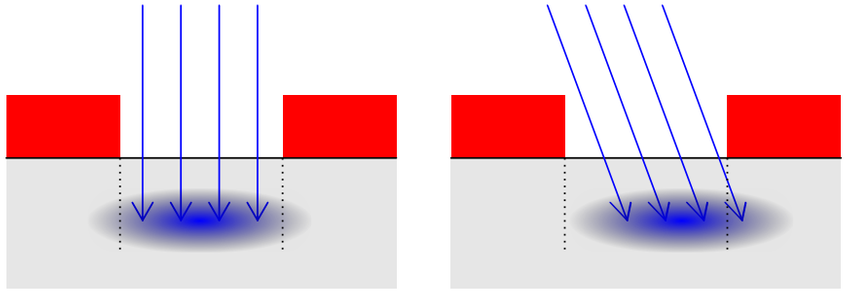
- **Patterning** areas using photolithography
- **Adding** materials:
  - Ion implantation



▲ Depth control

▼ Lattice damage



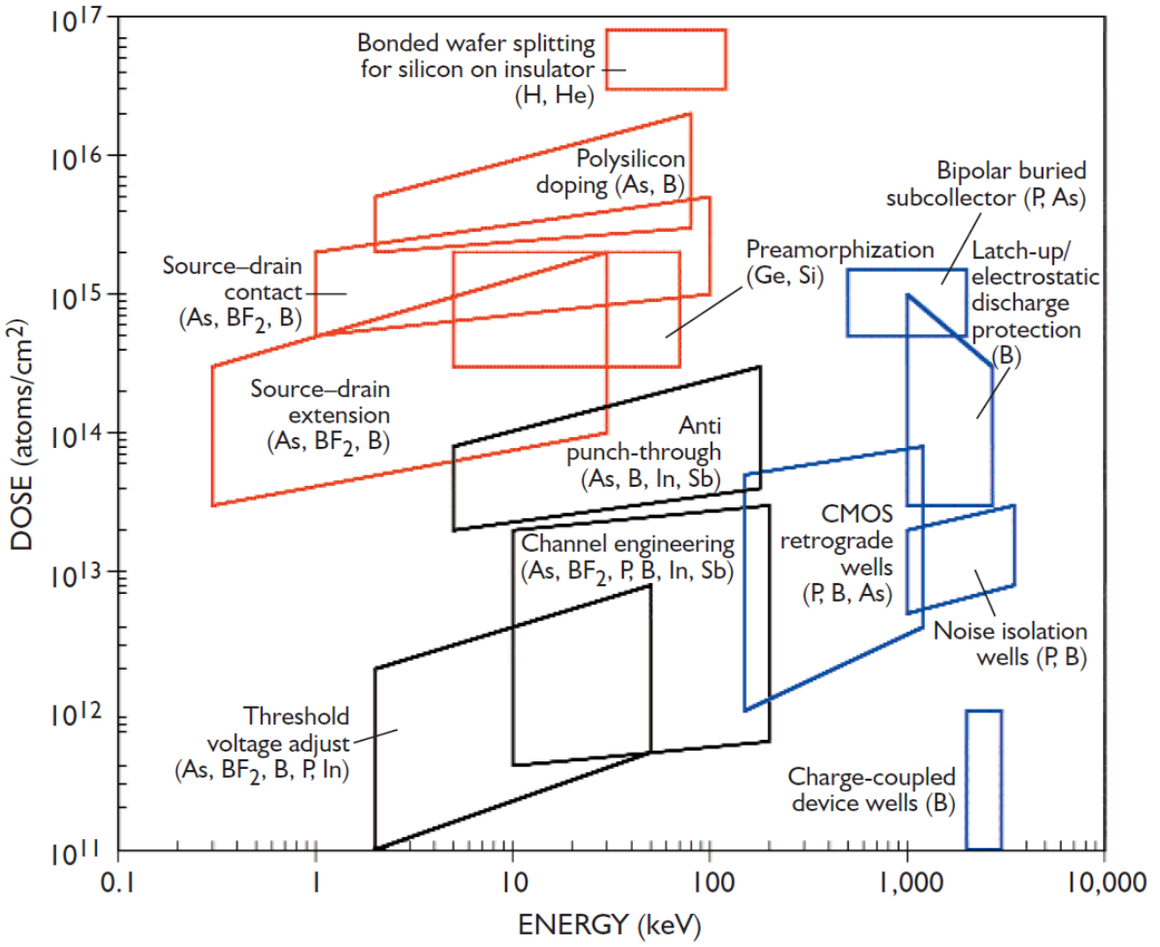


▼ Lateral effect ▼ Shadowing

Wafer Processing

- **Patterning** areas using photolithography
- **Adding** materials:
  - Ion implantation

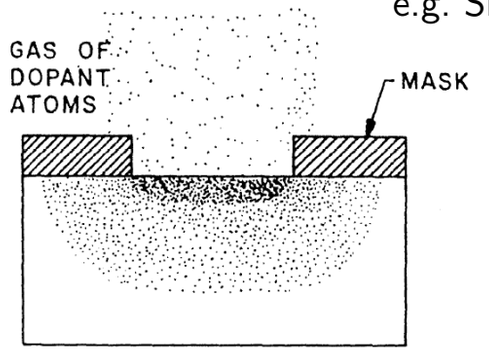
Doping applications

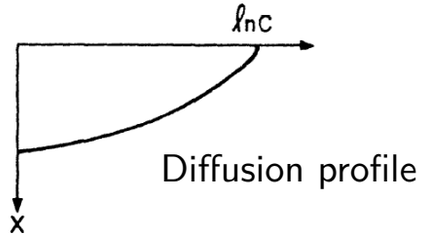


Wafer Processing

- **Patterning** areas using photolithography
- **Adding** materials:
  - Ion implantation
  - Diffusion
  - Thin-film growing
  - Thin-film deposition

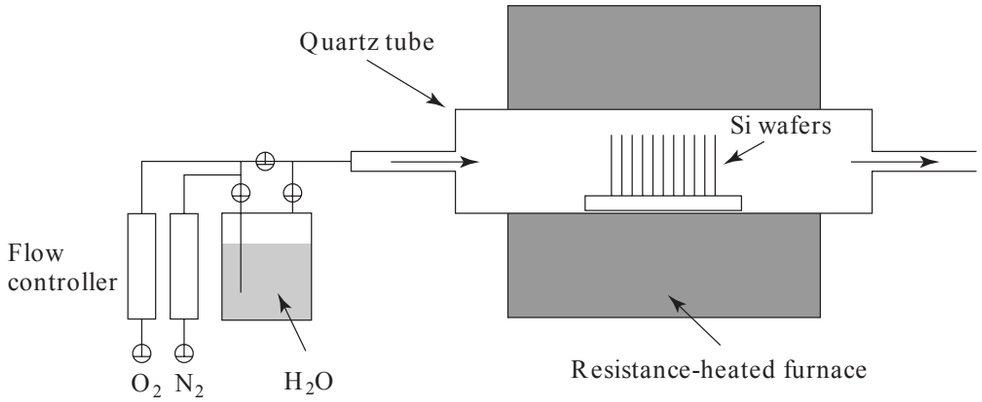
e.g. Si doping (hours, 800°C to 1200°C)

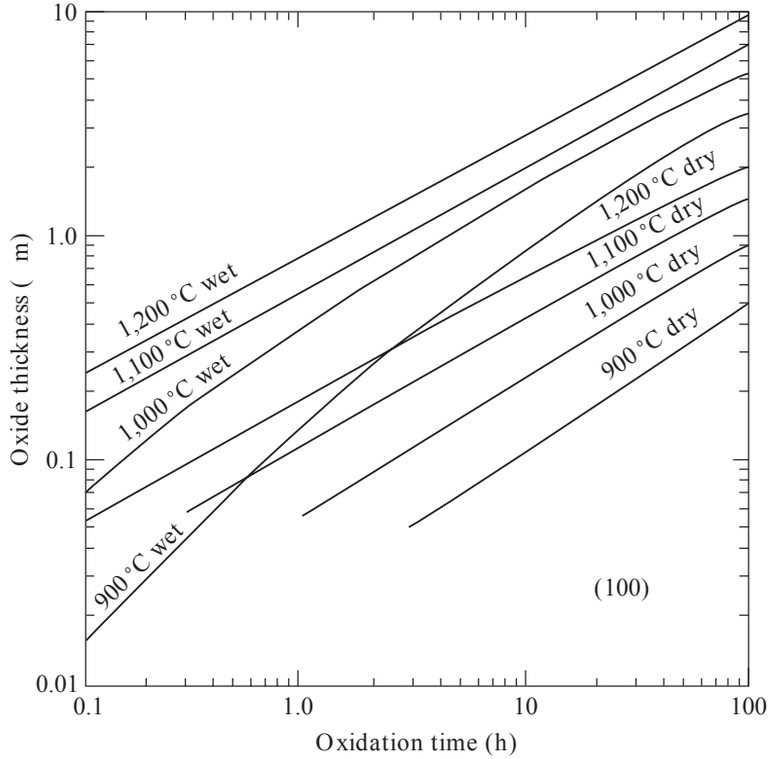




Diffusion profile

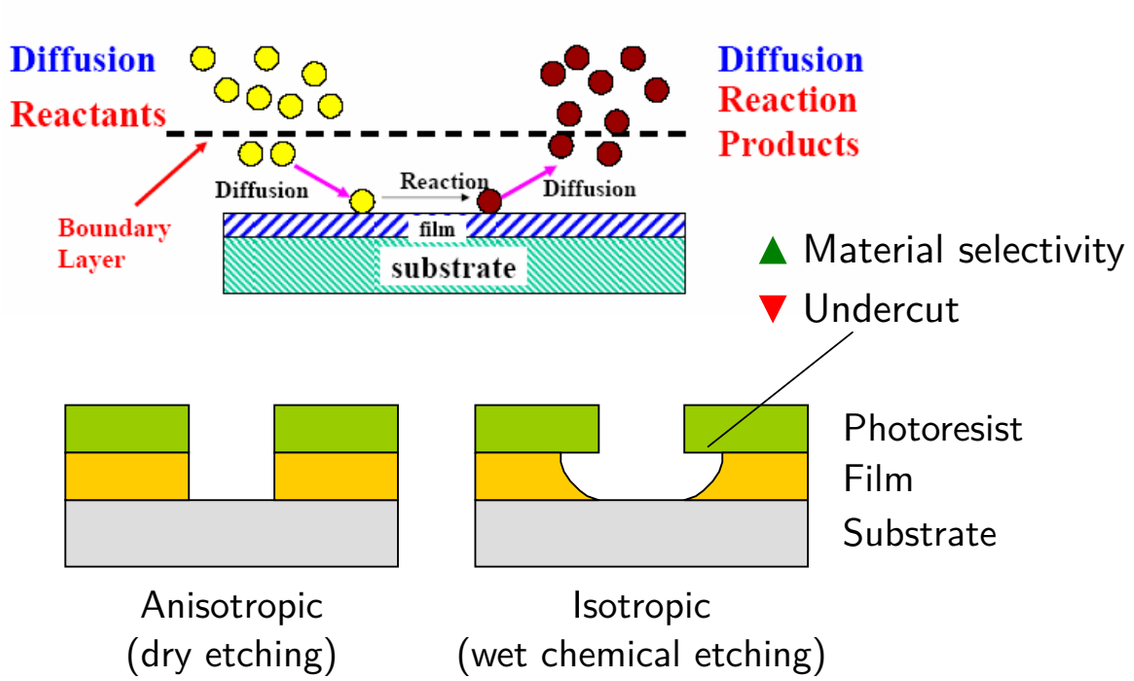
e.g. SiO_2 oxidation (hours, 700°C to 1200°C)



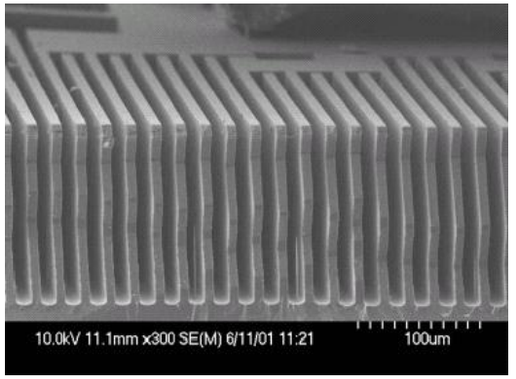


Wafer Processing

- **Patterning** areas using photolithography
- **Adding** materials:
  - Ion implantation
  - Diffusion
  - Thin-film growing
  - Thin-film deposition
- **Removing** materials:
  - Cleaning
  - Etching

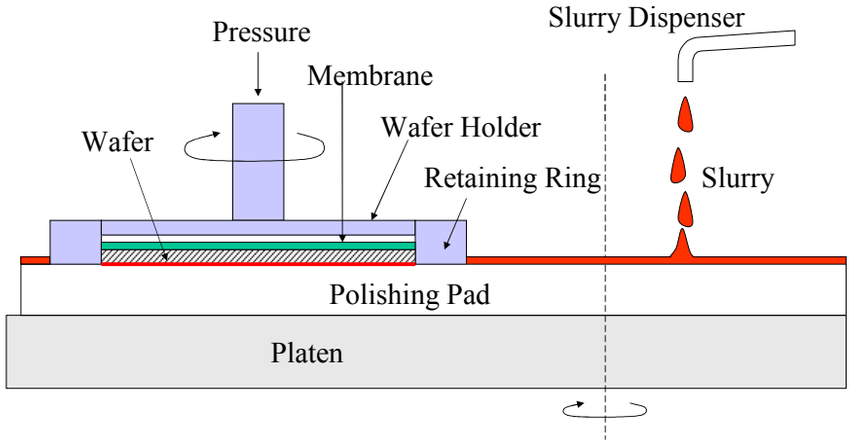


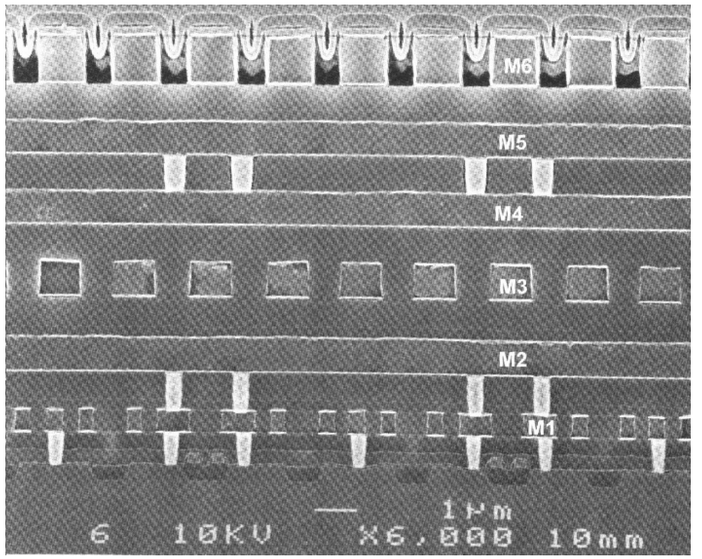
e.g. physical/chemical reactive ion etching (RIE) for micromachining



Wafer Processing

- **Patterning** areas using photolithography
- **Adding** materials:
  - Ion implantation
  - Diffusion
  - Thin-film growing
  - Thin-film deposition
- **Removing** materials:
  - Cleaning
  - Etching
  - Chemical-mechanical planarization (**CMP**)
- **Thermal** treatment:
  - Annealing
  - Reflowing
  - Alloying

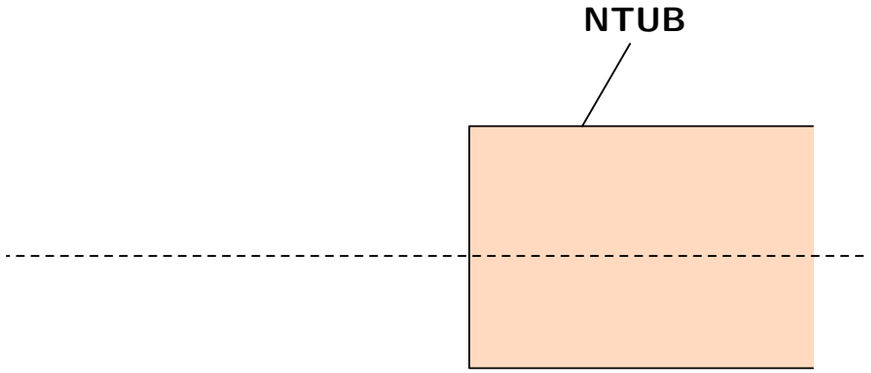


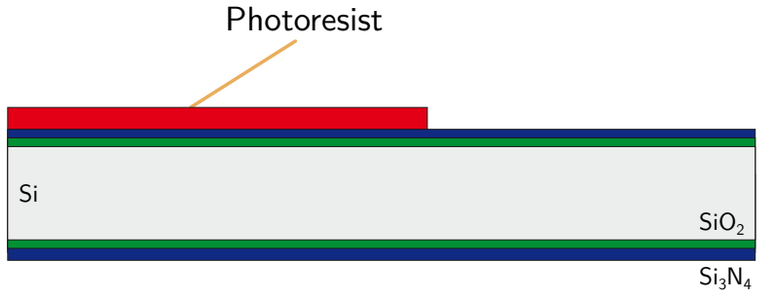


e.g. 6-metal 0.18μm BEOL

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
  - 4-inch wafers
  - 22-mm x 22-mm (484mm^2) stepper reticle
  - 8-mask layout design
- **FEOL** stages:
  - N and P wells





Initial pad oxidation (314Å to 415Å)
Nitride deposition (1050Å to 1300Å)
NTUB photolithography

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
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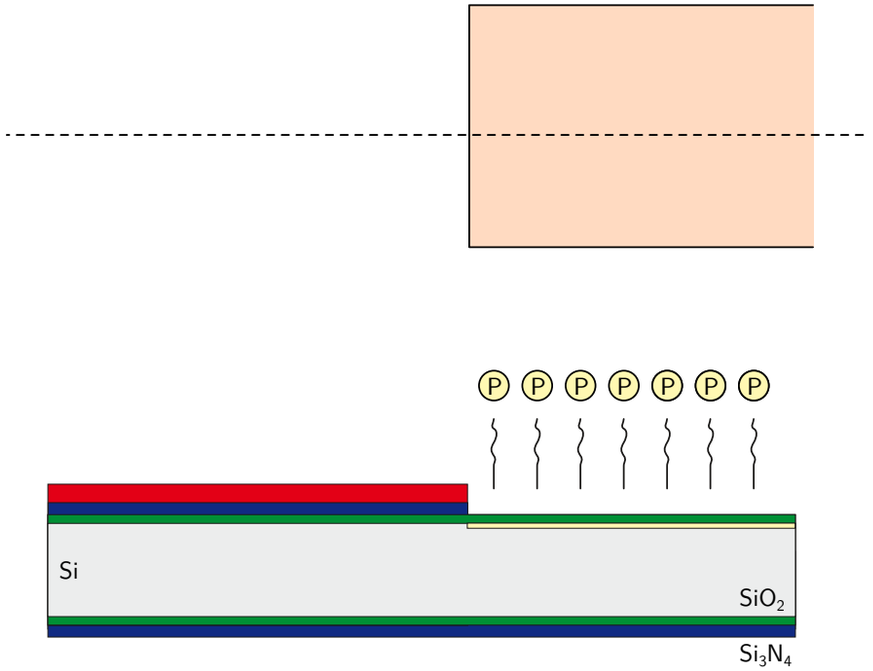

Nitride etching
N-well implantation

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
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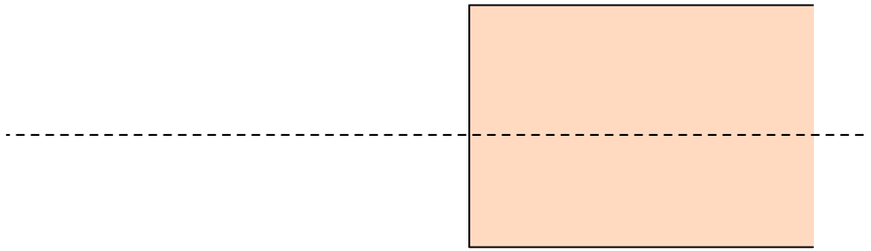

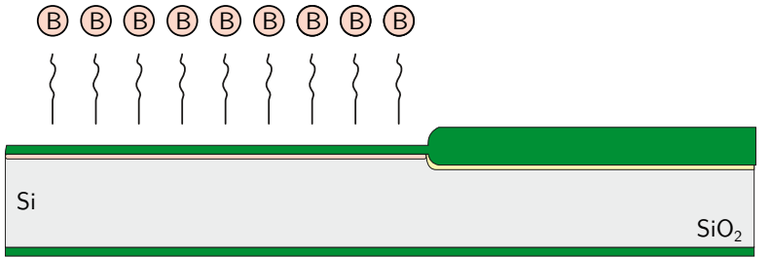

Well-oxide grow (3500Å to 4500Å)
Nitride stripping
P-well implantation

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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- **FEOL** stages:
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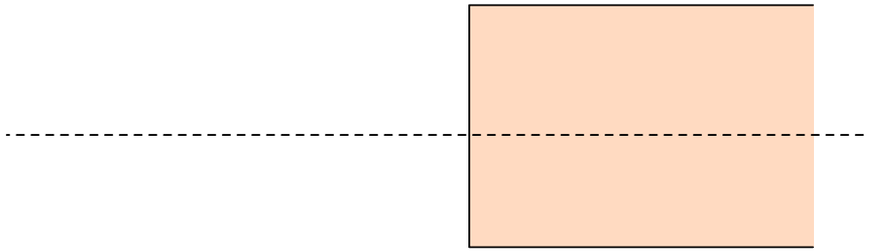

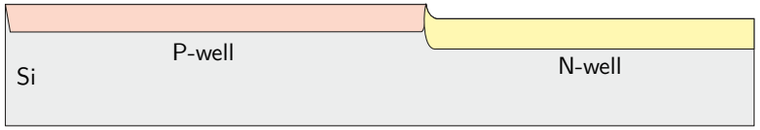

Oxide stripping
P-well (7µm) N-well (5µm) drive-in
and oxide grow (1500Å to 1750Å)
Oxide stripping

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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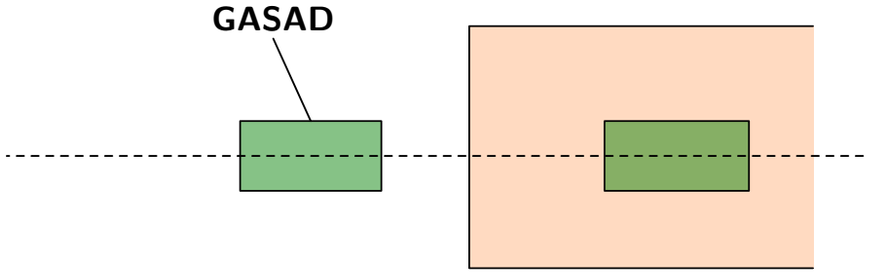
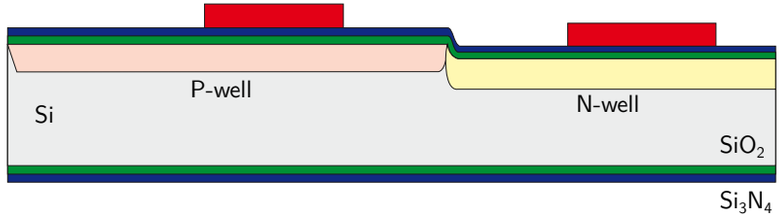
  - 22-mm x 22-mm (484mm^2) stepper reticle
  - 8-mask layout design
- **FEOL** stages:
  - N and P wells
  - Active areas





Pad oxidation (150Å to 225Å)
Nitride deposition (1050Å to 1300Å)
GASAD photolithography

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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  - 4-inch wafers
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  - 8-mask layout design
- **FEOL** stages:
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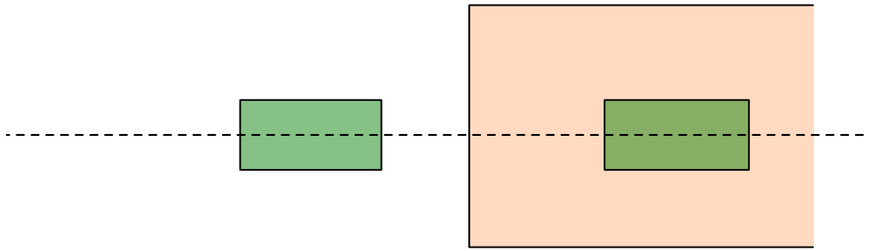
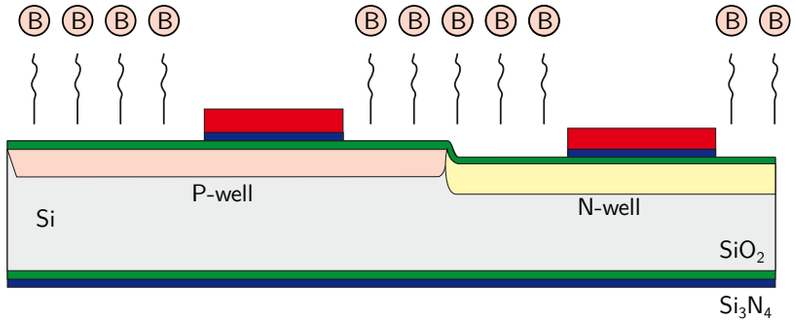
  - Active areas





Nitride etching
Field implantation

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
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  - 8-mask layout design
- **FEOL** stages:
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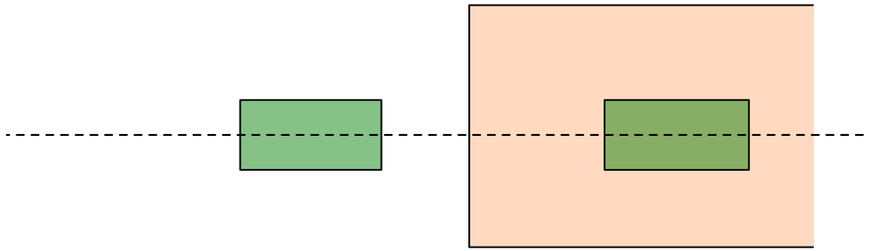
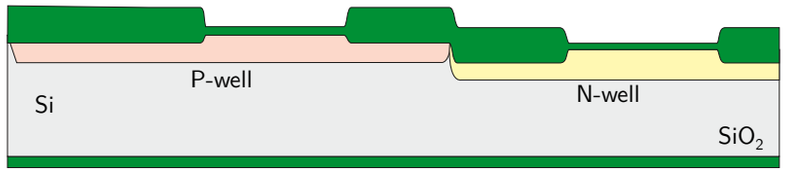
  - Active areas





LOCOS* (10000Å to 11200Å)
Nitride etching

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

*LOCal Oxidation of Silicon

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
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  - 8-mask layout design
- **FEOL** stages:
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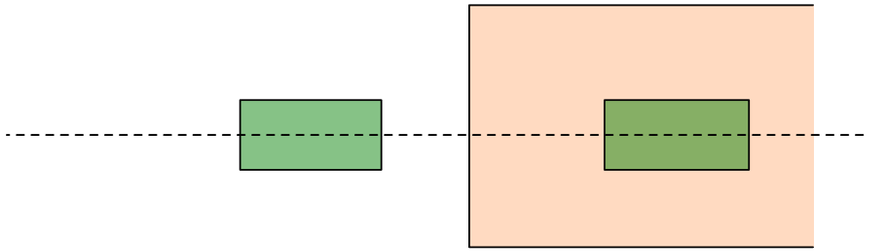
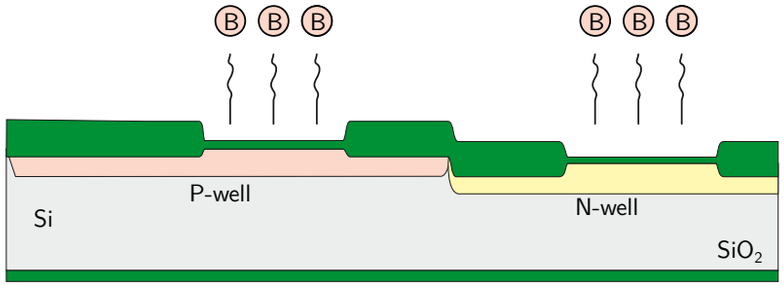
  - Active areas





Sacrifitial oxidation (850Å to 1050Å)
Gate implantation
Pre-poly cleaning

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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  - 4-inch wafers
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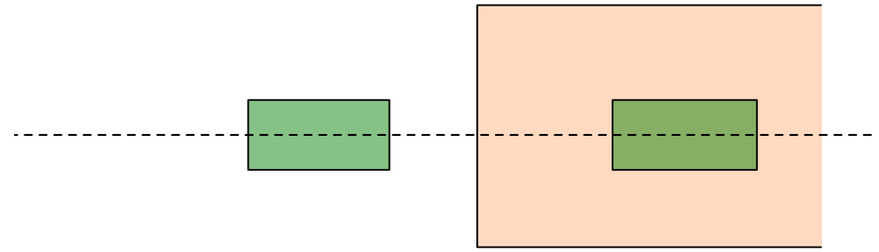
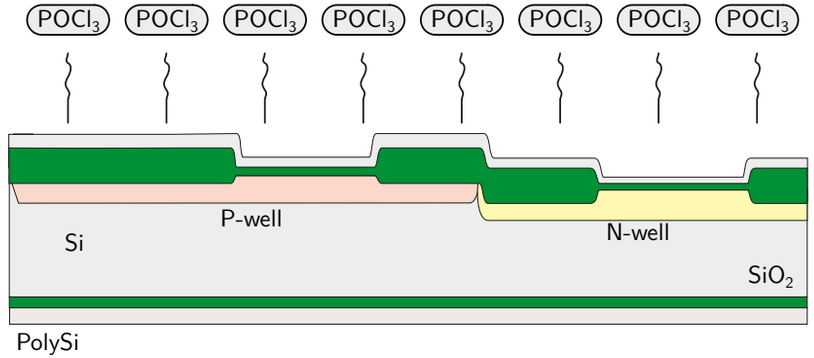
  - 8-mask layout design
- **FEOL** stages:
  - N and P wells
  - Active areas
  - PiP capacitor





PolySi deposition
(3200Å to 3800Å)
N-type doping

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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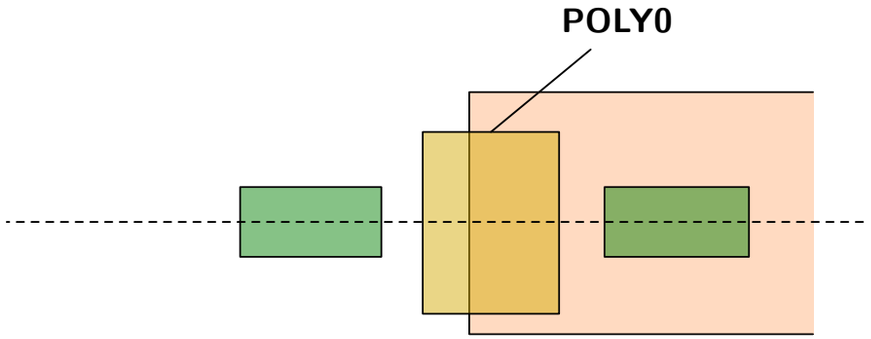
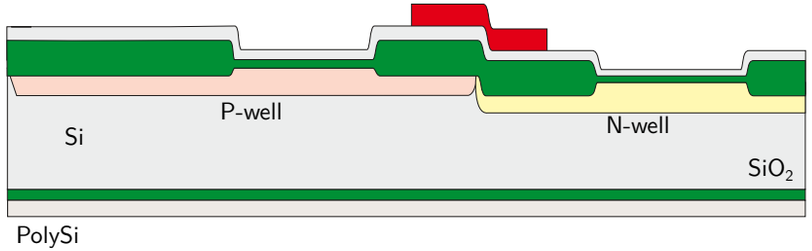
  - Active areas
  - PiP capacitor





POLY0 photolithography

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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- **FEOL** stages:
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  - Active areas
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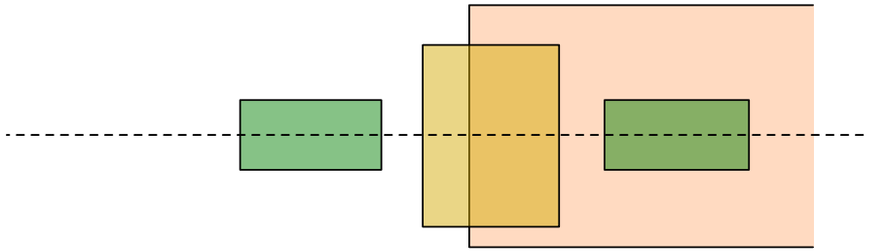
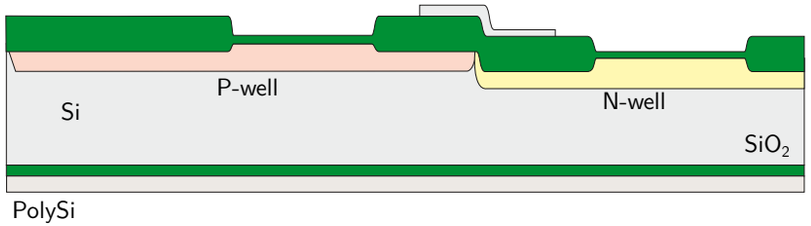


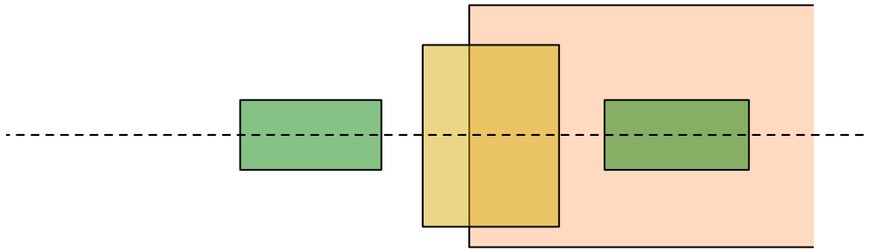


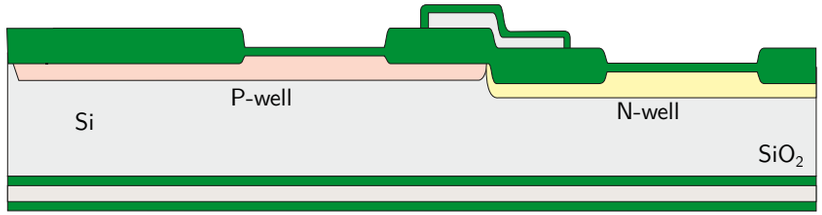
PolySi etching
Sacrifitial oxide stripping

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
  - 4-inch wafers
  - 22-mm x 22-mm (484mm^2) stepper reticle
  - 8-mask layout design
- **FEOL** stages:
  - N and P wells
  - Active areas
  - PiP capacitor
  - MOS gate





Gate-oxide growing (340Å to 390Å)

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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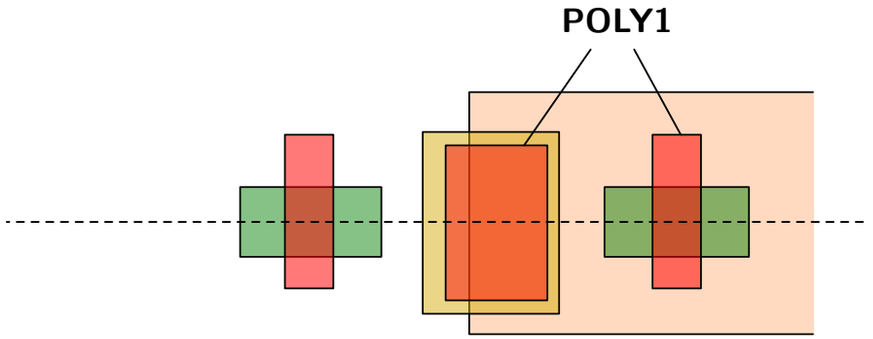

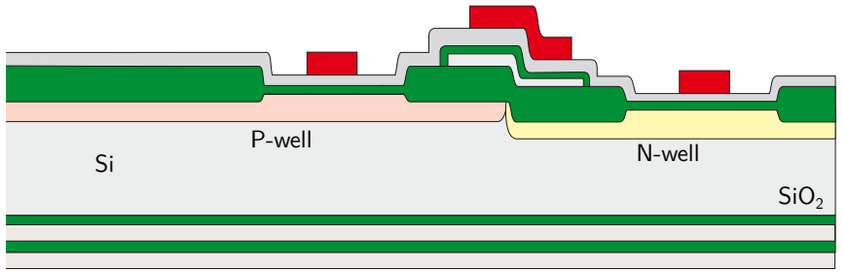

PolySi deposition (4500Å to 5100Å)
POLY1 photolithography

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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  - PiP capacitor
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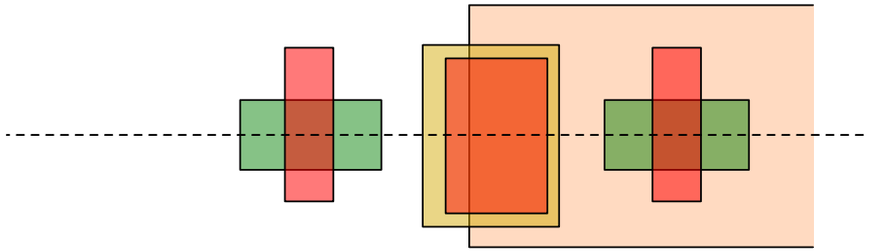

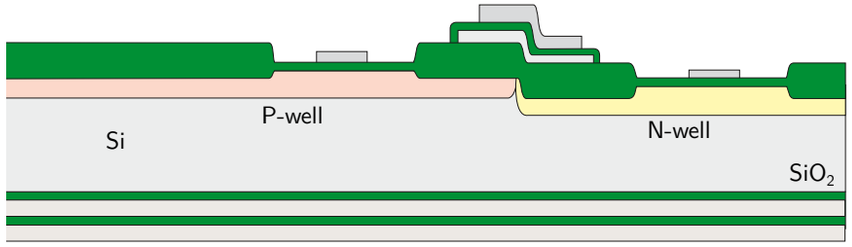

PolySi etching

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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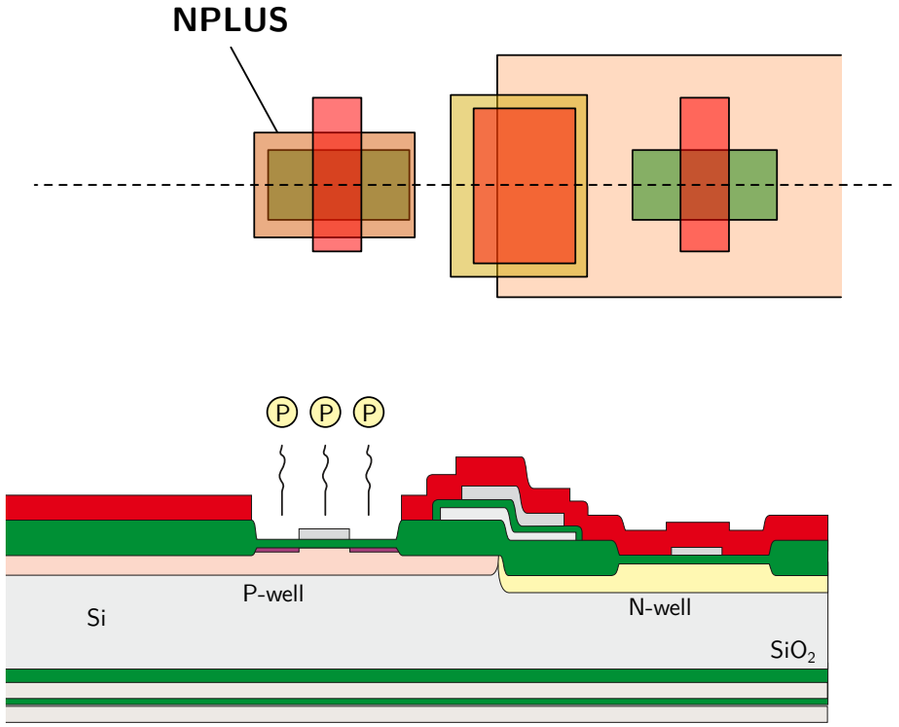
  - 8-mask layout design
- **FEOL** stages:
  - N and P wells
  - Active areas
  - PiP capacitor
  - MOS gate
  - MOS source and drain



NPLUS photolithography
N-type doping

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

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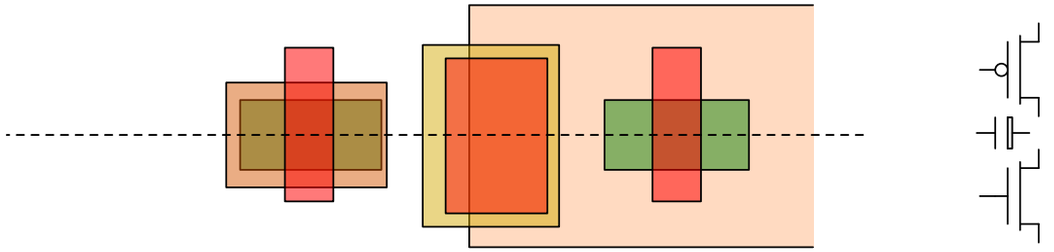
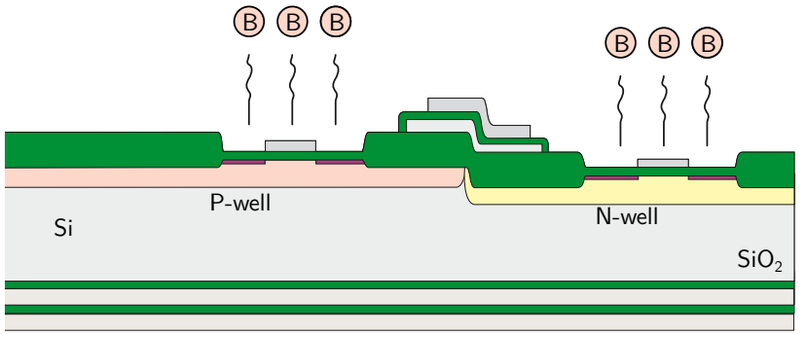
  - N and P wells
  - Active areas
  - PiP capacitor
  - MOS gate
  - MOS source and drain





P-type doping

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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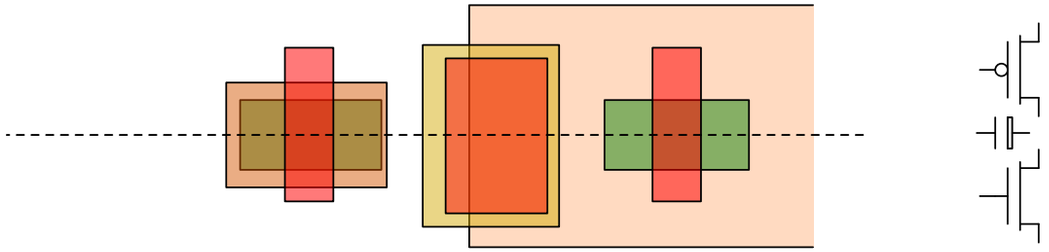
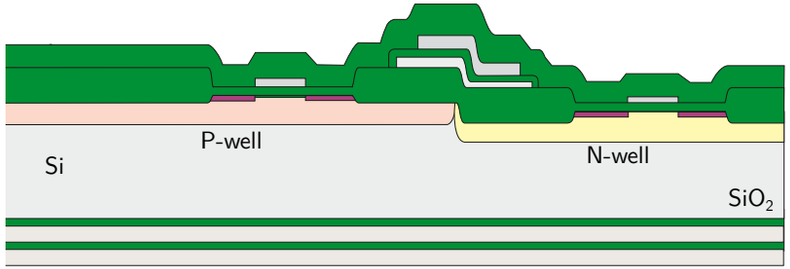
  - 22-mm x 22-mm (484mm^2) stepper reticle
  - 8-mask layout design

- **FEOL** stages:
  - N and P wells
  - Active areas
  - PiP capacitor
  - MOS gate
  - MOS source and drain



- **BEOL** stages:
  - Interlevel oxide



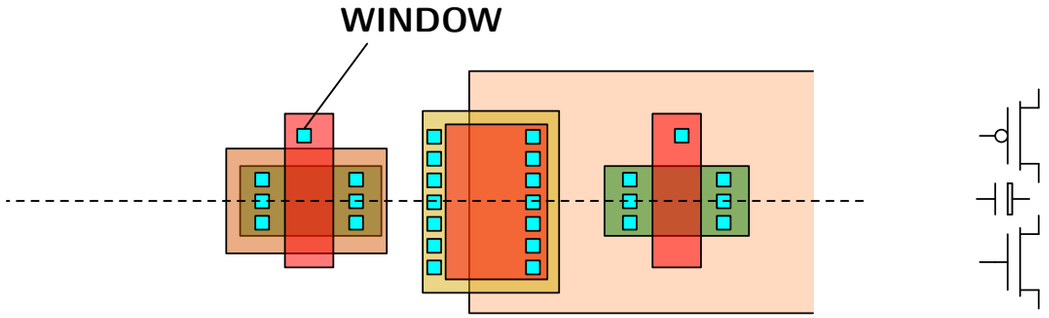
TEOS* deposition (12000Å to 13000Å)
N^{++}(1µm) and P^{++}(3µm) D/S diffusion

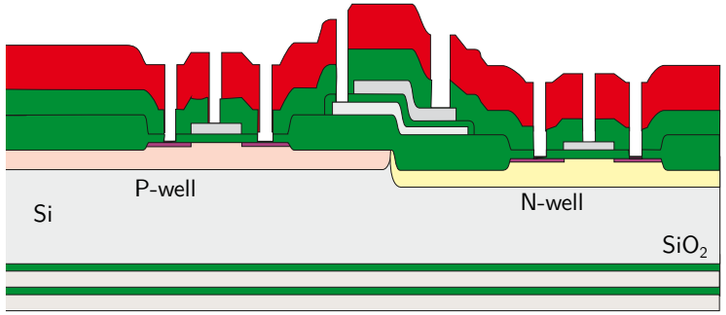
↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

*TEtraethyl OrthoSilicate

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
  - 4-inch wafers
  - 22-mm x 22-mm (484mm^2) stepper reticle
  - 8-mask layout design
- **FEOL** stages:
  - N and P wells
  - Active areas
  - PiP capacitor
  - MOS gate
  - MOS source and drain
- **BEOL** stages:
  - Interlevel oxide
  - Contacts





WINDOW photolithography

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

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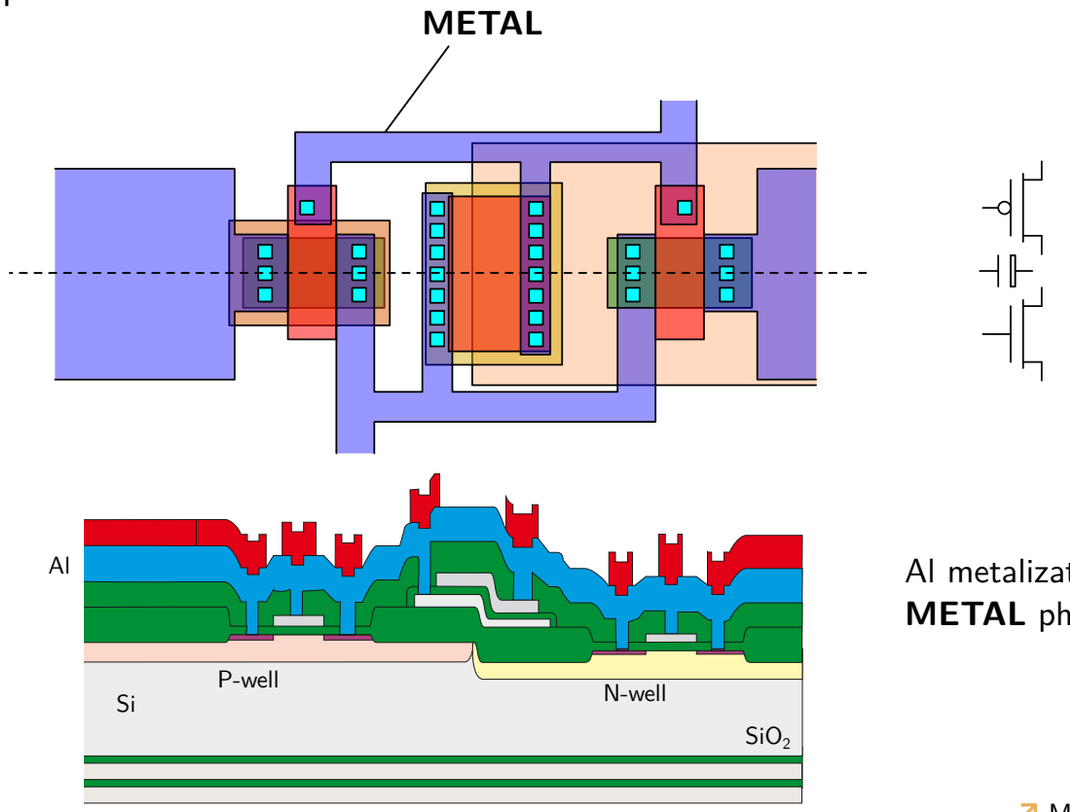
  - Active areas
  - PiP capacitor
  - MOS gate
  - MOS source and drain
- **BEOL** stages:
  - Interlevel oxide
  - Contacts
  - Metal



Al metalization
METAL photolithography

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
  - 4-inch wafers
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  - PiP capacitor
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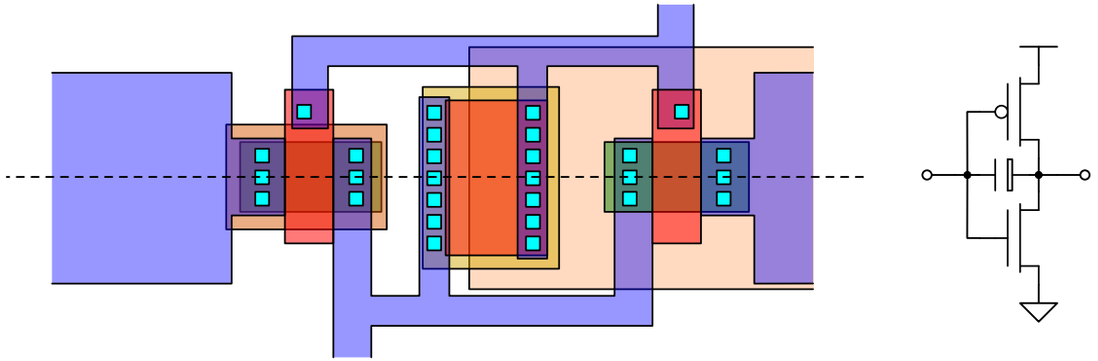
  - MOS source and drain
- **BEOL** stages:
  - Interlevel oxide
  - Contacts
  - Metal

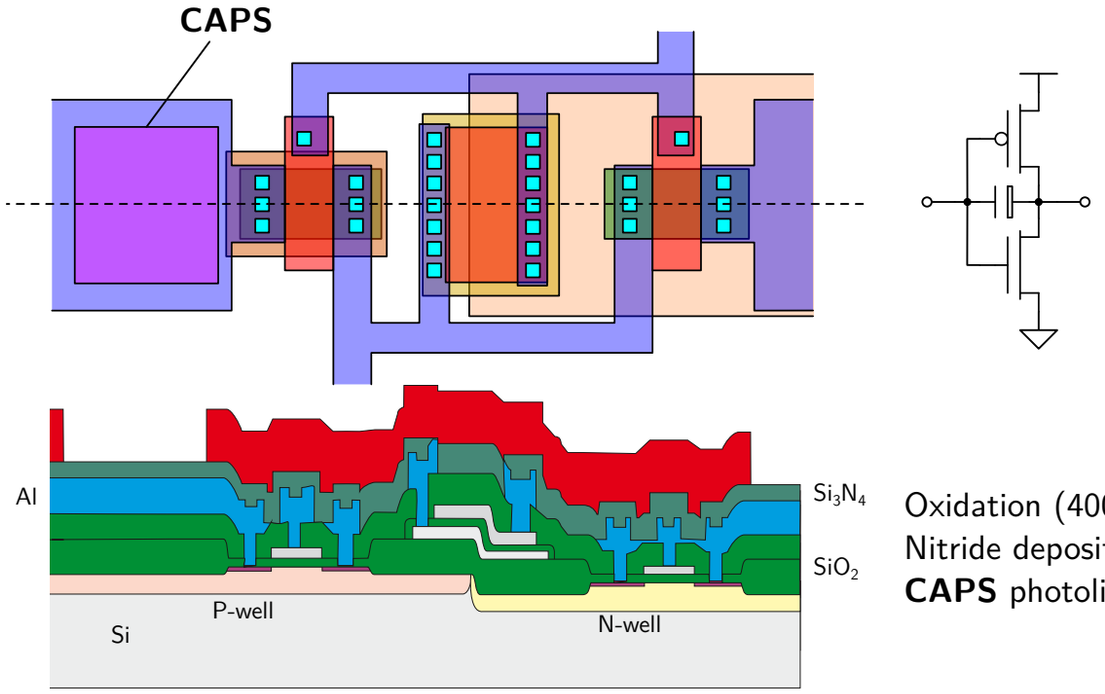


Al etching

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
  - 4-inch wafers
  - 22-mm x 22-mm (484mm^2) stepper reticle
  - 8-mask layout design
- **FEOL** stages:
  - N and P wells
  - Active areas
  - PiP capacitor
  - MOS gate
  - MOS source and drain
- **BEOL** stages:
  - Interlevel oxide
  - Contacts
  - Metal
  - Passivation and pads

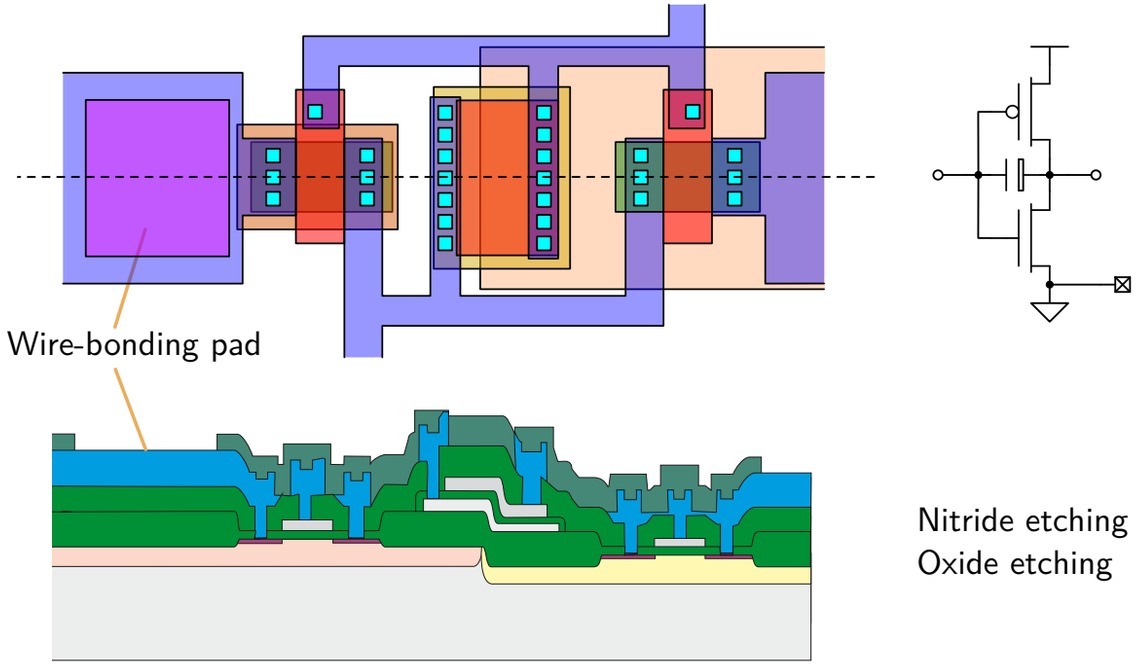


Oxidation (4000Å)
Nitride deposition (4000Å)
CAPS photolithography

↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

CNM25 Technology Example

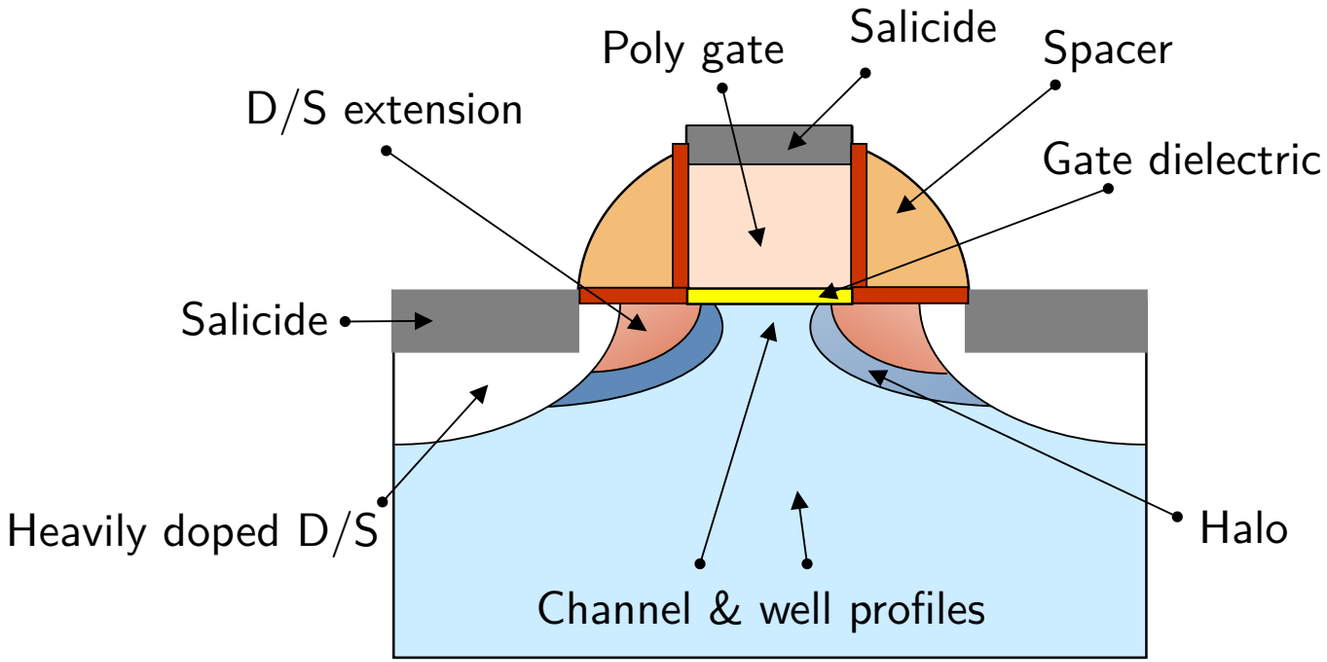
- **2.5-µm** polySi-insulator-polySi (**PiP**) **1M** twin-well CMOS process:
  - 4-inch wafers
  - 22-mm x 22-mm (484mm^2) stepper reticle
  - 8-mask layout design
- **FEOL** stages:
  - N and P wells
  - Active areas
  - PiP capacitor
  - MOS gate
  - MOS source and drain
- **BEOL** stages:
  - Interlevel oxide
  - Contacts
  - Metal
  - Passivation and pads



↗ M. Zabala and A. Sánchez, IMB-CNM(CSIC)

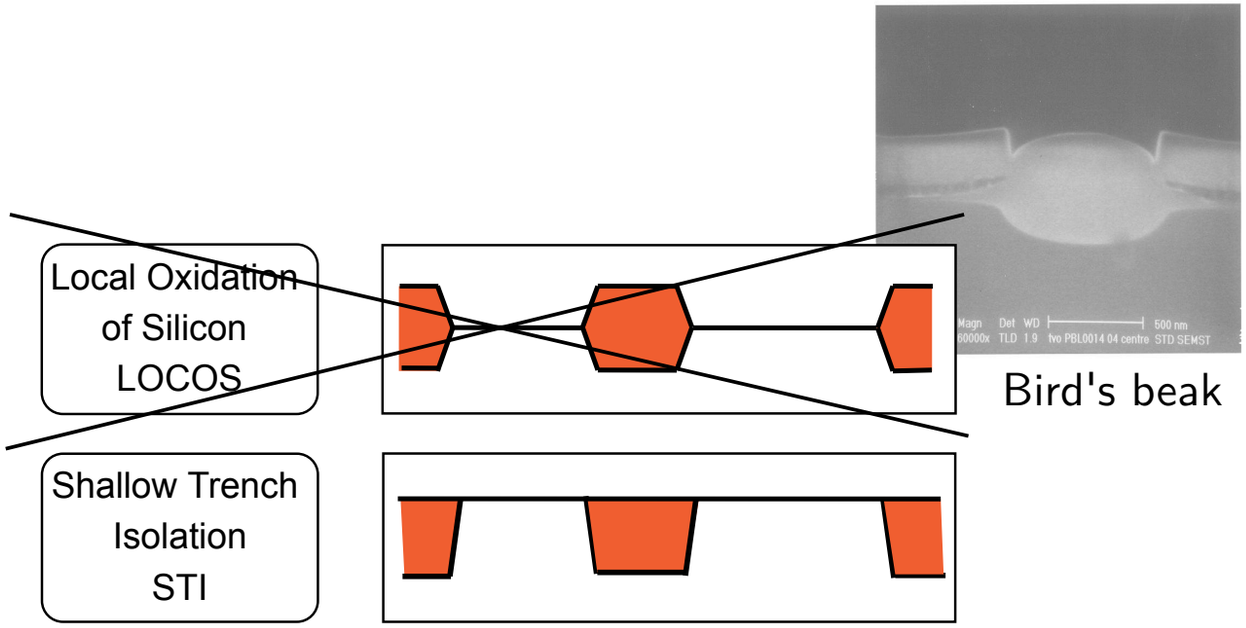
Modern Technologies

- Advanced **MOSFET** device structure



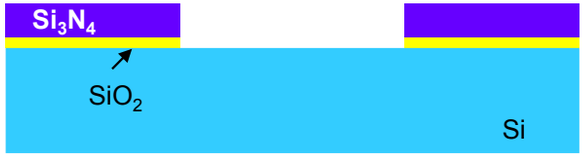
Modern Technologies

- Advanced **MOSFET** device structure
- Device **isolation**

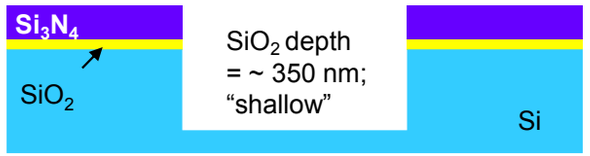


Pad oxide growth + nitride deposition

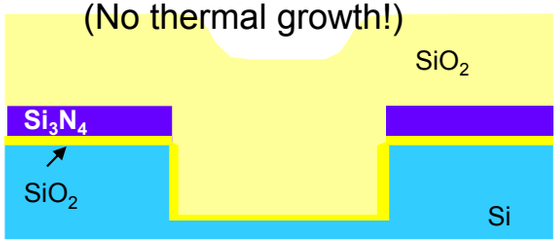
Pattern and etch Si_3N_4 and SiO_2



Trench etch into Si



Deposition of trench filling oxide
(No thermal growth!)



Oxide CMP polish step with stop on nitride

Field oxide recess (HF dip)
Removal of nitride layer (H_3PO_4)

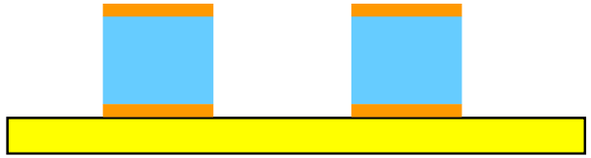
Modern Technologies

- Advanced **MOSFET** device structure
- Device **isolation**
- **Cu** interconnections
  - Lower resistivity
  - Higher melting point
  - Lower thermal expansion
  - Lower electromigration

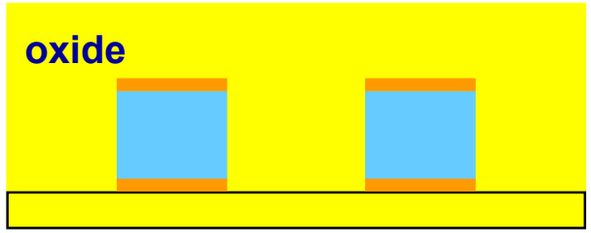
Classical Al metallisation

1) metal deposition

2) etching of metal lines



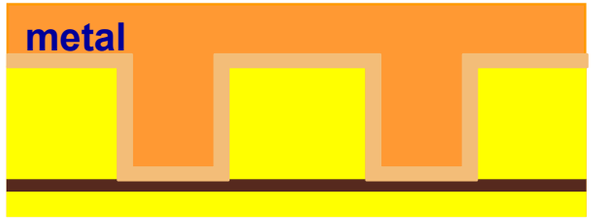
3) oxide gapfill + oxide CMP



Damascene Cu metallisation

1) etching of oxide trenches

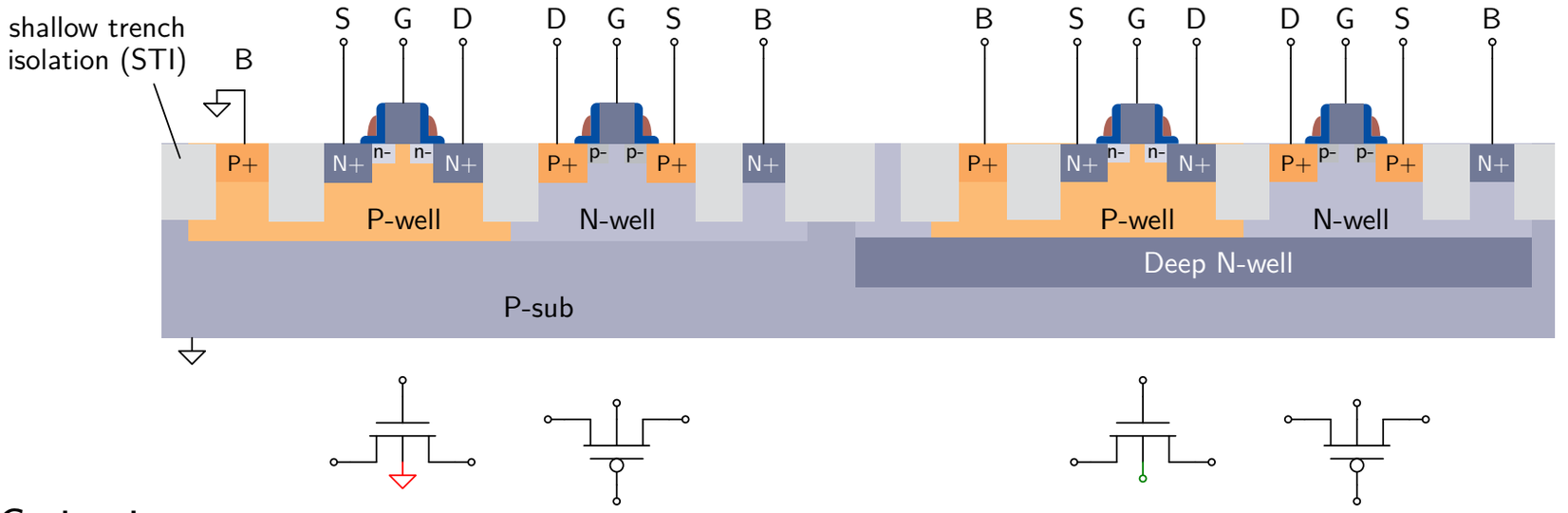
2) metal deposition



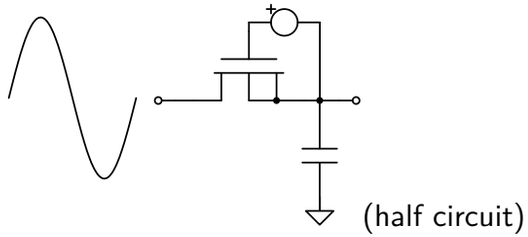
3) metal CMP

Mixed-Signal Technology Modules

- CMOS process **options** for each IC application:
  - Twin vs **triple** well



- **Gate-bootstrapping** in SC circuits (e.g. input samplers, charge pumps)
- **Isolation** against substrate noise



Mixed-Signal Technology Modules

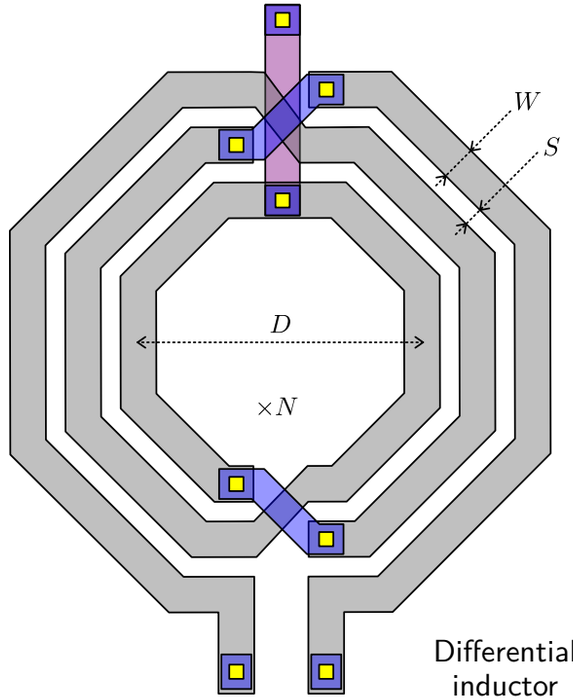
- CMOS process **options** for each IC application:
  - Twin vs **triple** well
  - Several MOSFET **threshold-voltage** families

Family	V_{TN} [V]	V_{TP} [V]	**Purpose**
LP	0.50	-0.55	+1.8-V low-leakage core
LV	0.33	-0.33	Low-voltage supply
TH	0.70	-0.63	+3.3-V I/O interface

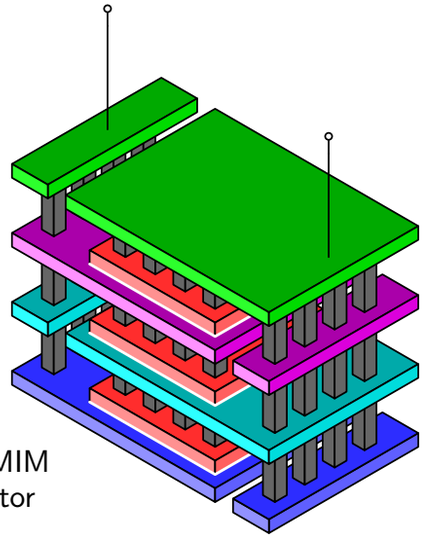
e.g. 0.18-μm 1P6M CMOS technology

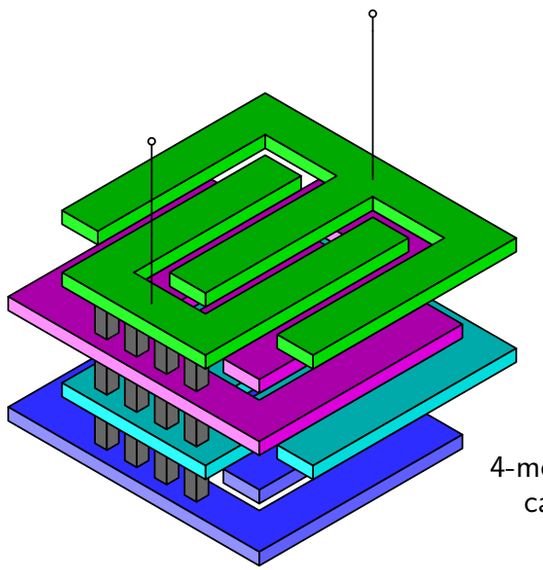
Mixed-Signal Technology Modules

- CMOS process **options** for each IC application:
  - Twin vs **triple** well
  - Several MOSFET **threshold-voltage** families
  - Metal-insulator-metal (**MIM**) and metal-oxide-metal (**MOM**) linear capacitors
  - High-resistance polySi (**HIPO**) linear and low-TC resistors
  - **Thick top metal** for high-Q RF inductors



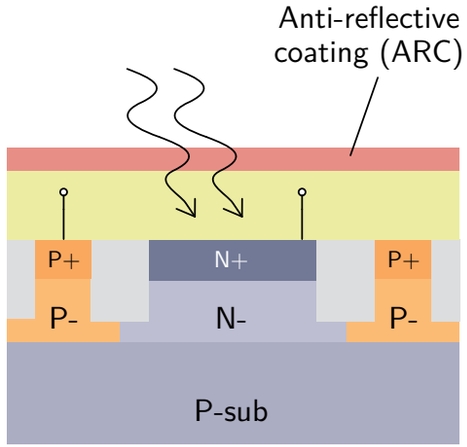
Differential inductor


Triple MIM capacitor


4-metal MOM capacitor

Mixed-Signal Technology Modules

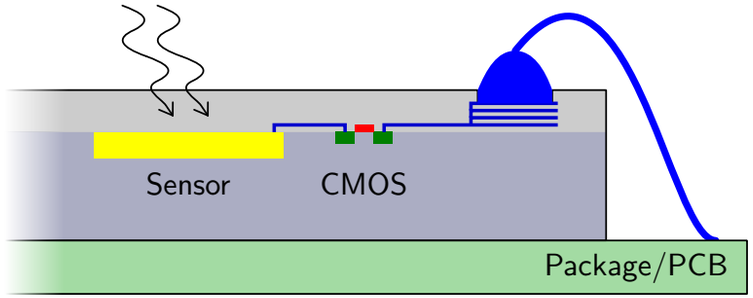
- CMOS process **options** for each IC application:
  - Twin vs **triple** well
  - Several MOSFET **threshold-voltage** families
  - Metal-insulator-metal (**MIM**) and metal-oxide-metal (**MOM**) linear capacitors
  - High-resistance polySi (**HIPO**) linear and low-TC resistors
  - **Thick top metal** for high-Q RF inductors
  - Linear **varactors** for continuous RF tuning
  - High-voltage (**HV**) and **LDMOS** transistors for power management
  - Lateral and vertical **bipolar** transistors for bandgap references
  - **Anti-reflective** coating and optimum **doping profiles** for CMOS image sensors (**CIS**)
  - Non-volatile memory (**NVM**) for chip ID, configuration, tunning...



- **Many** modules = higher mask/process **costs** + difficult circuit design **migration**

Hybrid-Packaging Alternatives

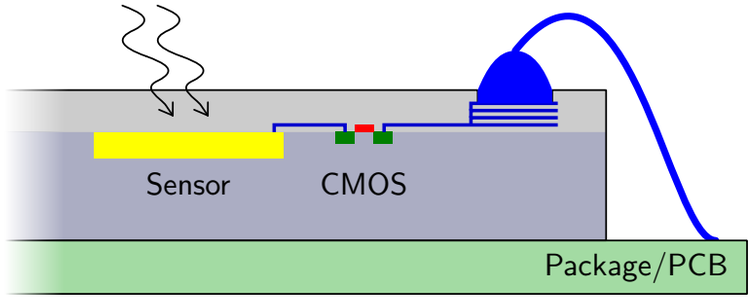
- Classic **wire-bonding** approach:



- **Monolithic** solution (signal integrity, production)
- Sensor needs to be CMOS **compatible**
- **Area** costs
- Wire-bonding costs for **large arrays**

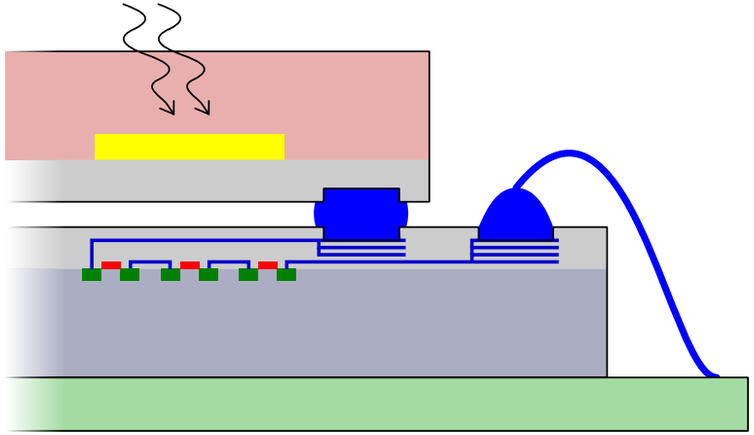
Hybrid-Packaging Alternatives

- Classic **wire-bonding** approach:



- **Monolithic** solution (signal integrity, production)
- Sensor needs to be CMOS **compatible**
- **Area** costs
- Wire-bonding costs for **large arrays**

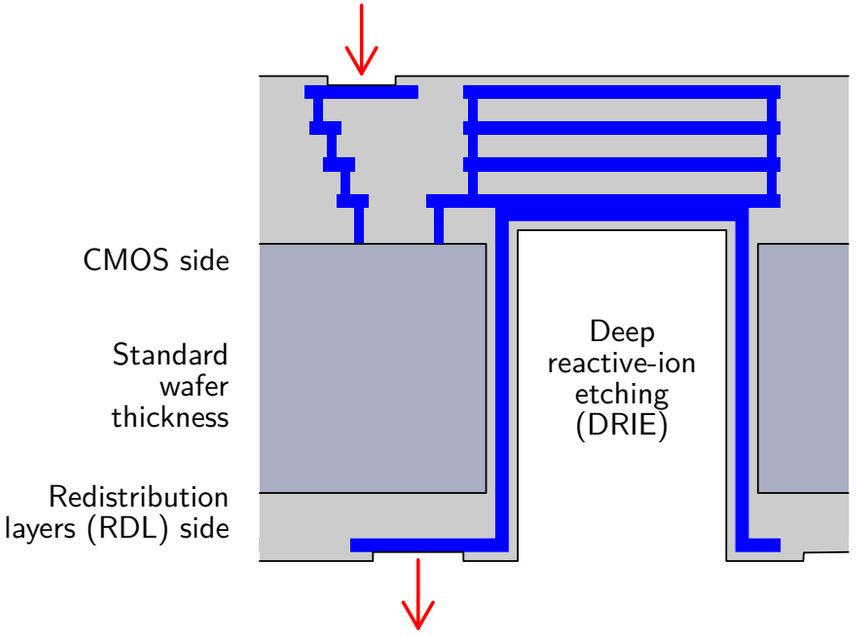
- **Bump-bonding** flip-chip:



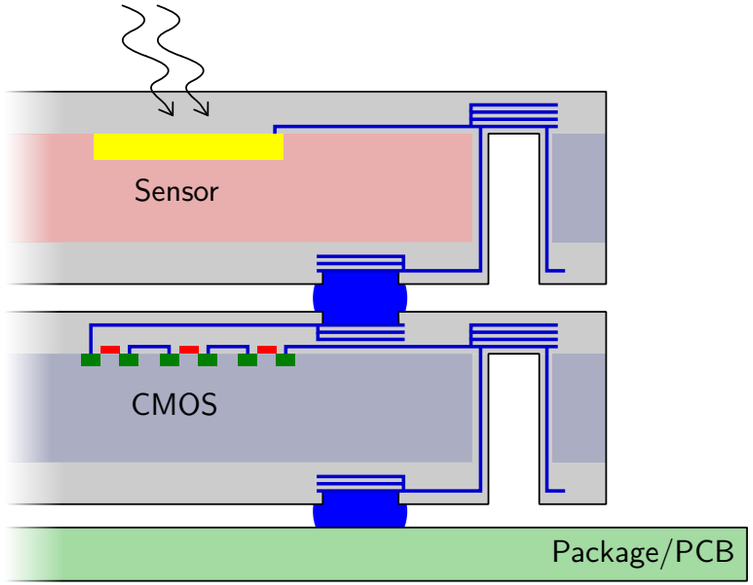
- **Heterogeneous** sensor/CMOS technologies
- Sensor **area** can be reused for circuits
- **Back-side** sensing
- Wire-bonding costs for **large arrays**

Hybrid-Packaging Alternatives

- 3D stacking with through-Silicon vias (**TSV**):



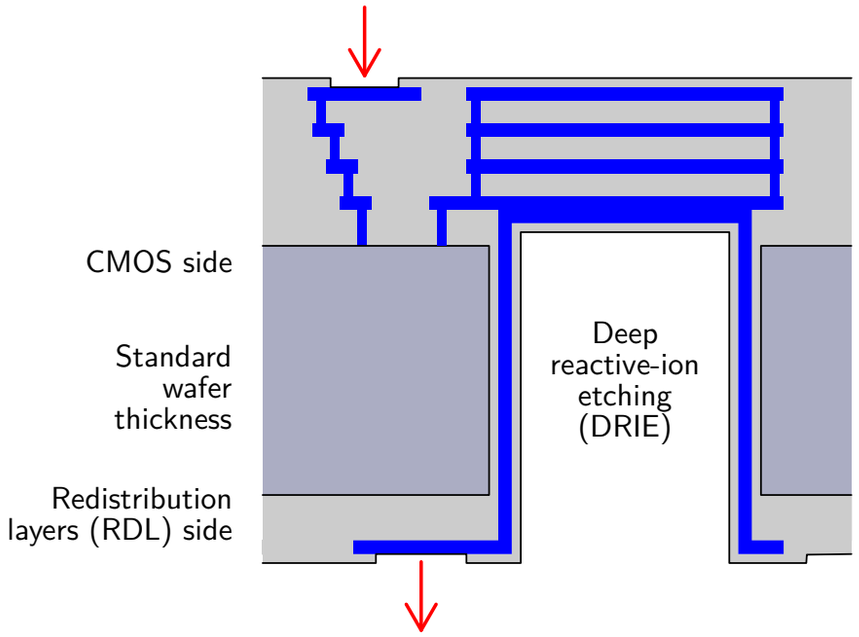
- Height/diameter < 20
- Typ. diameter 50µm to 100µm
- pF-range parasitic capacitance
- $<$ 1-Ω series resistance



- **Heterogeneous** sensor/CMOS technologies
- Sensor **area** can be reused for circuits
- **Front-side** sensing
- Wire-bonding free

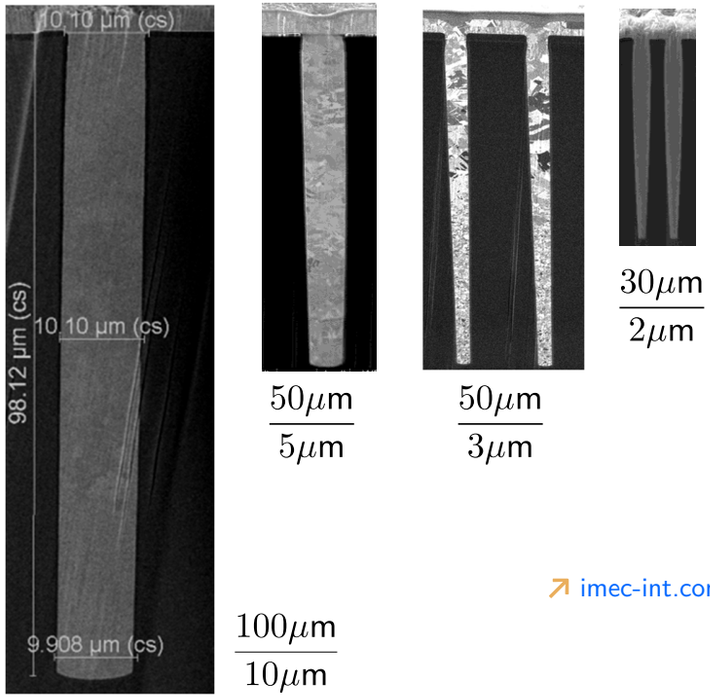
Hybrid-Packaging Alternatives

- 3D stacking with through-Silicon vias (**TSV**):



  - Height/diameter < 20
  - Typ. diameter 50µm to 100µm
  - pF-range parasitic capacitance
  - $<$ 1-Ω series resistance

- TSV downscaling by wafer chemical-mechanical polishing (**CMP**):

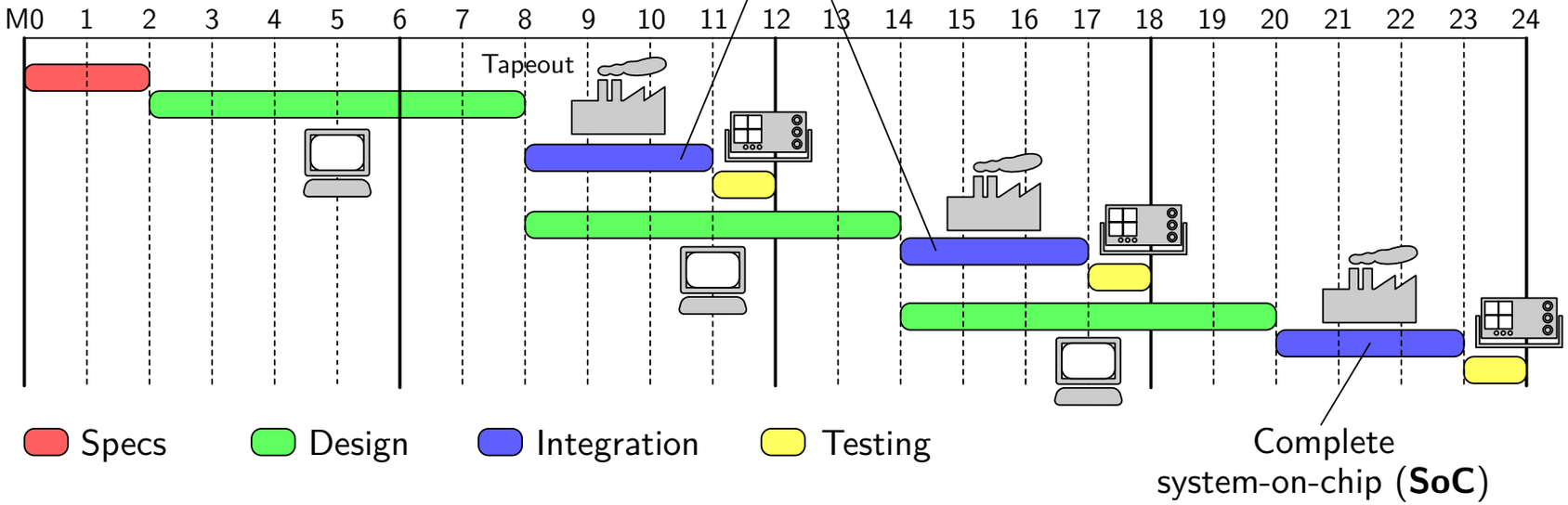


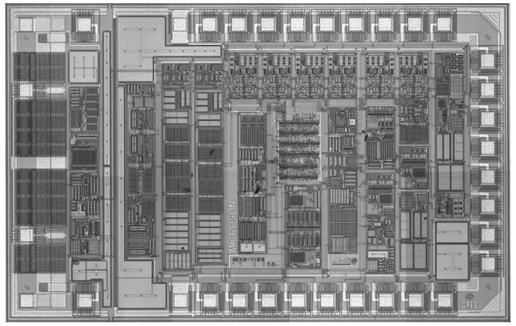
$\frac{100\mu m}{10\mu m}$ $\frac{50\mu m}{5\mu m}$ $\frac{50\mu m}{3\mu m}$ $\frac{30\mu m}{2\mu m}$

↗ imec-int.com

IC Development

- Typical project **scheduling**:

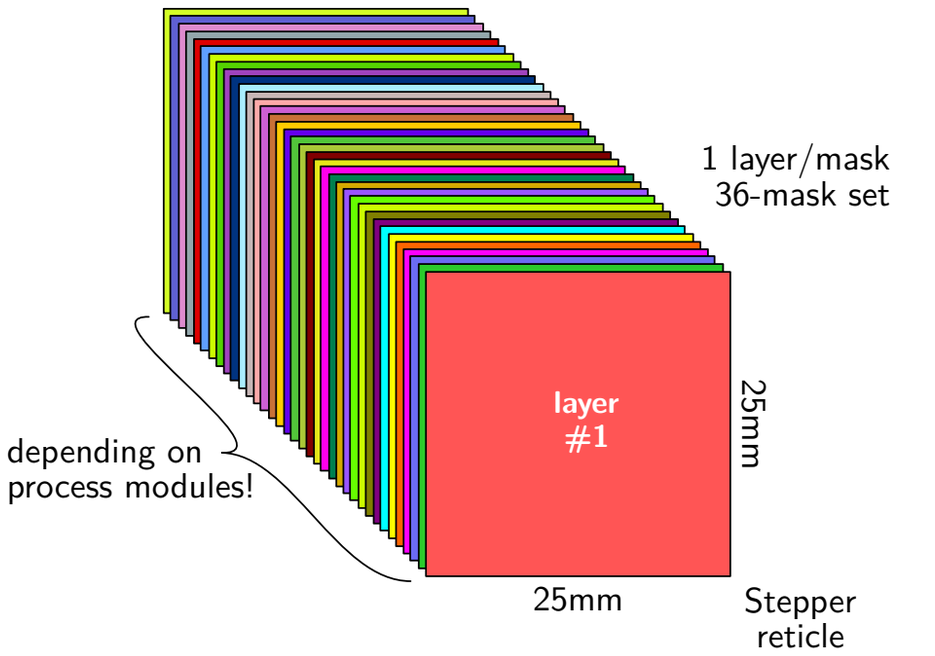




- Alignment with foundry fixed **run calendar**
- Long design **iterations** (typ. **6M**)
- **First** complete prototype >**18M**

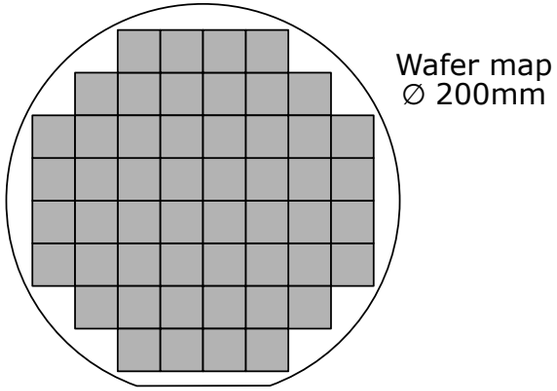
CMOS Technology Costs

- **Full-mask** regular run



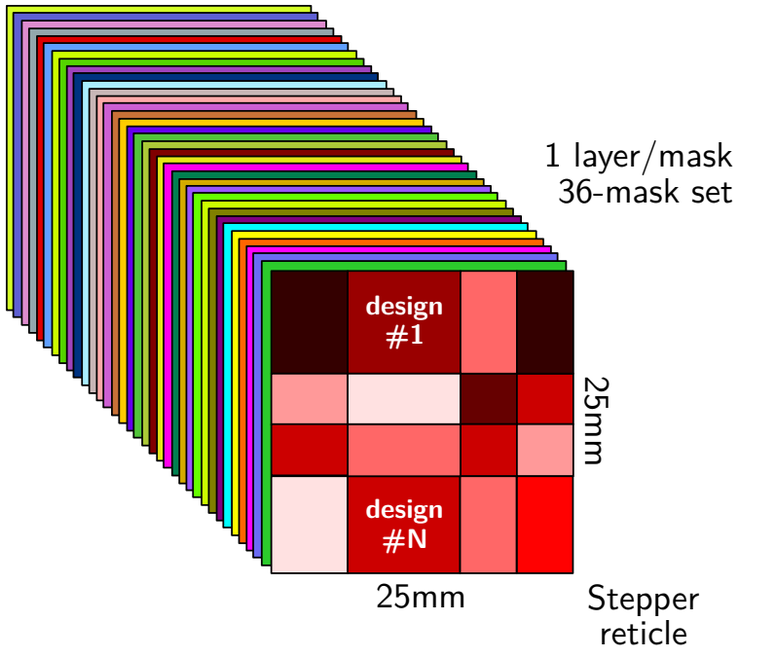
e.g. 0.15-µm 1P6M CMOS technology

- Die size: $<$ **625 mm^2**
- Mask costs: **100 k€**
- Processing costs: **2 k€/wafer**
- Samples: $>$ **50 die/wafer**
- Intended for **full production** ($>$ 200 wafer/year)



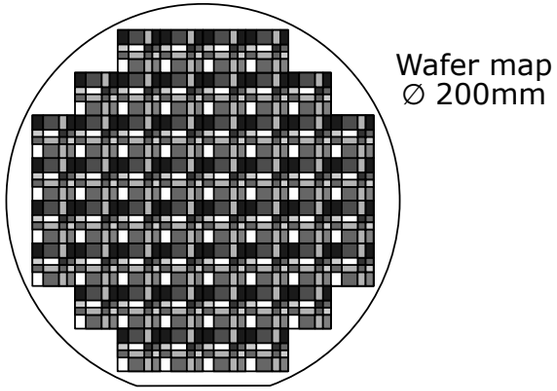
CMOS Technology Costs

- **Full-mask** regular run
- Multi-project wafer (**MPW**) run



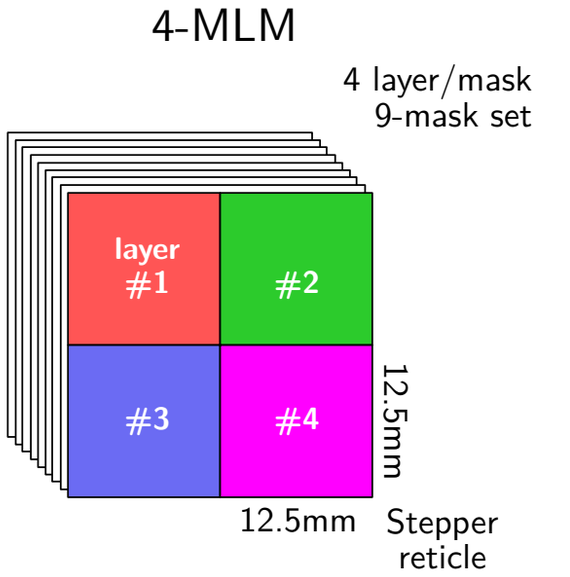
e.g. 0.15-µm 1P6M CMOS technology

- Die size: $>$ **4 mm^2**
- Mask and processing costs: **1 k€/mm^2**
- Samples: $<$ **100 die**
- Intended for **prototyping**



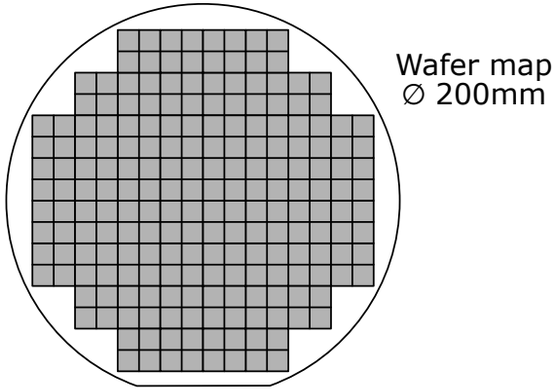
CMOS Technology Costs

- **Full-mask** regular run
- Multi-project wafer (**MPW**) run
- Multi-layer mask (**MLM**) engineering run



e.g. 0.15-µm 1P6M CMOS technology

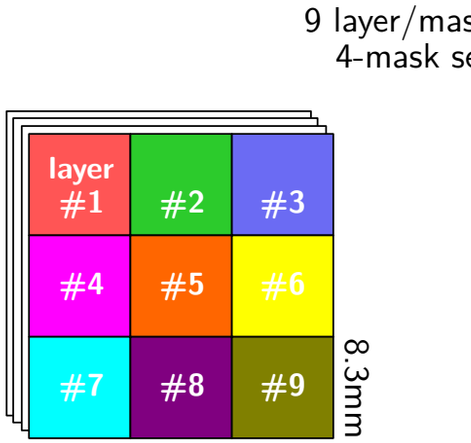
- Die size: $<$ **156 mm^2**
- Mask costs: **25 k€**
- Processing costs: **2 k€/wafer** (6-wafer lots)
- Samples: $>$ **200 die/wafer**
- Intended for **small series** ($<$ 100 wafer/year)



CMOS Technology Costs

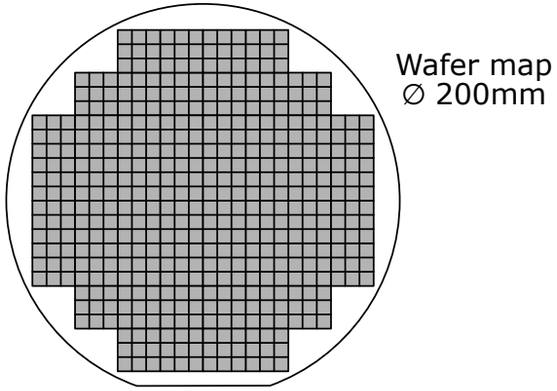
- **Full-mask** regular run
- Multi-project wafer (**MPW**) run
- Multi-layer mask (**MLM**) engineering run

9-MLM



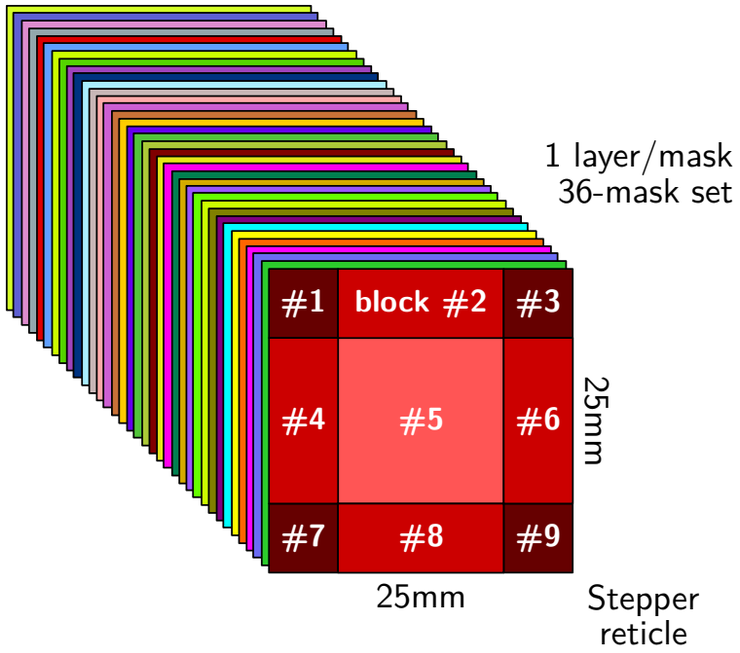
e.g. 0.15-µm 1P6M CMOS technology

- Die size: $<$ **69 mm^2**
- Mask costs: **12 k€**
- Processing costs: **2 k€/wafer** (6-wafer lots)
- Samples: $>$ **450 die/wafer**
- Intended for **small series** ($<$ 100 wafer/year)



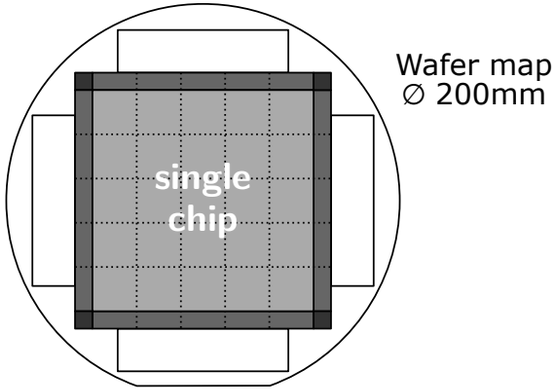
CMOS Technology Costs

- **Full-mask** regular run
- Multi-project wafer (**MPW**) run
- Multi-layer mask (**MLM**) engineering run
- Wafer-scale **stitching** run

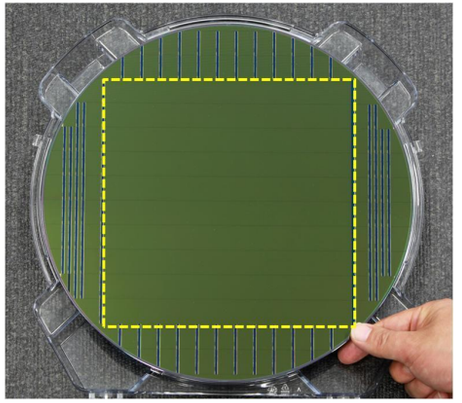


e.g. 0.15-µm 1P6M CMOS technology

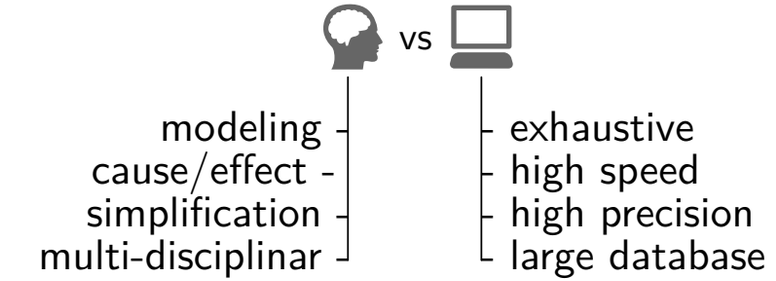
- Die size: **150x150 mm^2**
- Mask costs: **100 k€**
- Processing costs: **2 k€/wafer**
- Samples: **1 die/wafer**
- Intended for **limited series**
- **Low yield** (acceptable for imagers)



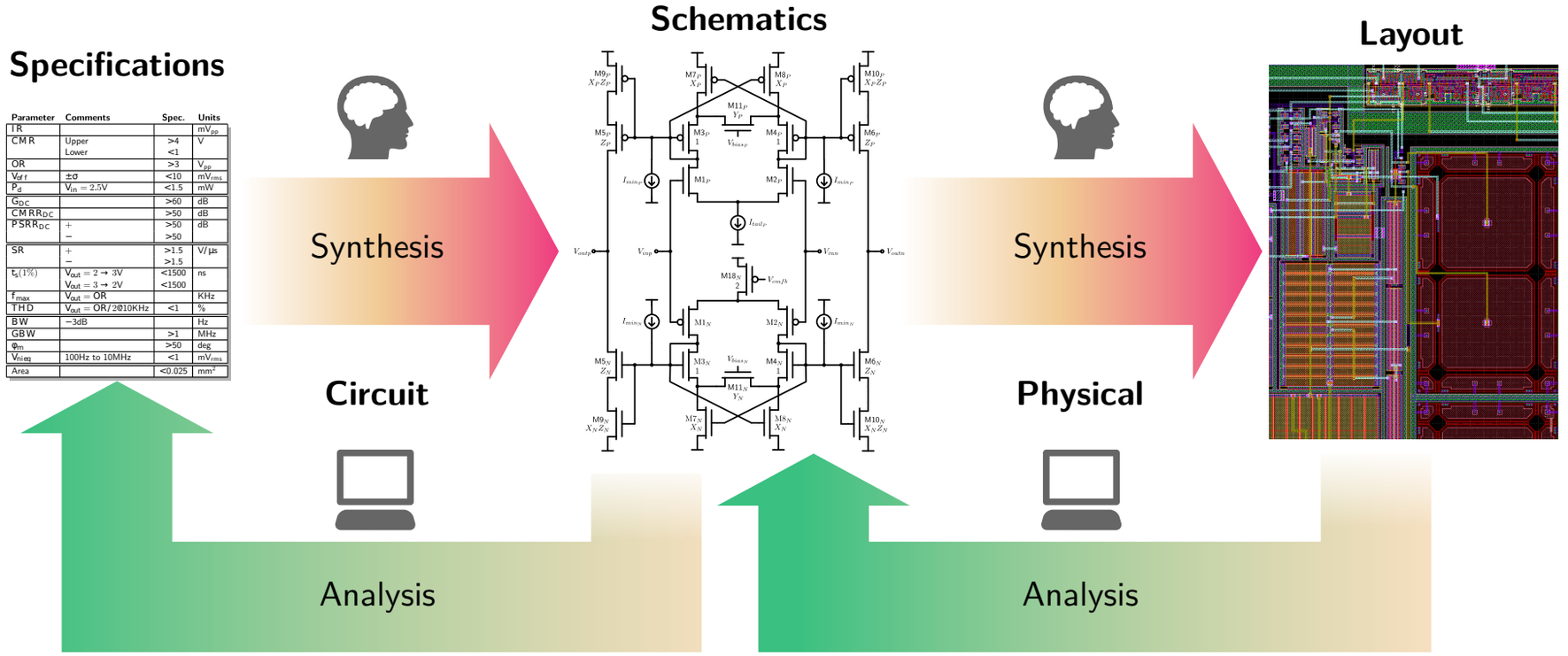
↗ imagesensors.org



IC Design Scenario



- **Synthesis** vs **analysis**:

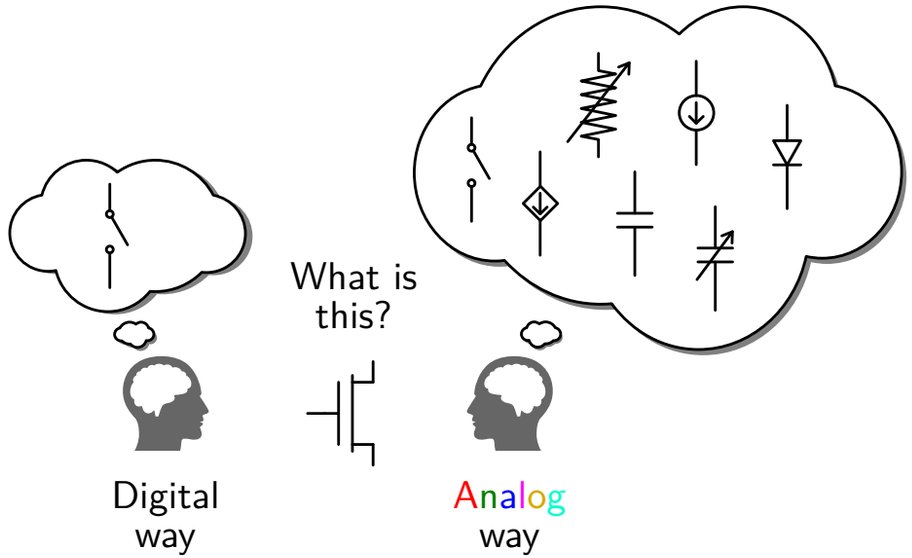


Parameter	Comments	Spec.	Units
IR			mV_{pp}
CMR	Upper Lower	>4 <1	V
OR		>3	V_{pp}
V_{off}	$\pm\sigma$	<10	mV_{rms}
P_d	$V_{in} = 2.5V$	<1.5	mW
G_{DC}		>60	dB
$CMRR_{DC}$		>50	dB
$PSRR_{DC}$	+ −	>50 >50	dB
SR	+ −	>1.5 >1.5	V/µs
$t_s(1\%)$	$V_{out} = 2 \rightarrow 3V$ $V_{out} = 3 \rightarrow 2V$	<1500 <1500	ns
f_{max}	$V_{out} = OR$		KHz
THD	$V_{out} = OR/2@10KHz$	<1	%
BW	−3dB		Hz
GBW		>1	MHz
ϕ_m		>50	deg
V_{nieq}	100Hz to 10MHz	<1	mV_{rms}
Area		<0.025	mm^2

▼ EDA tools do **not** design ICs!

Analog vs Digital

- *If it can be done by digital, don't use analog!*
- Analog IC design is **complex**...
  - **Background** in physics, electronics, information and control theory, signal processing, communications
  - Variety of **state-of-the-art** solutions
  - High dependence from **technology**
  - **Modeling** skills
  - Complex **EDA** tools



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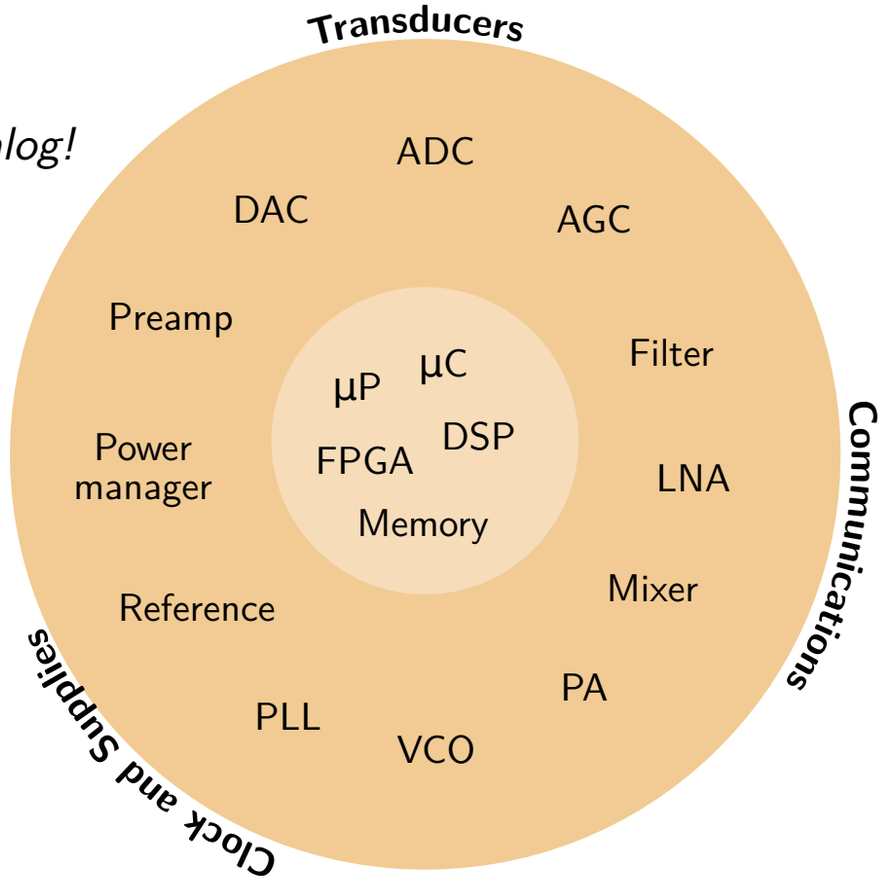
- ...but still **necessary**!



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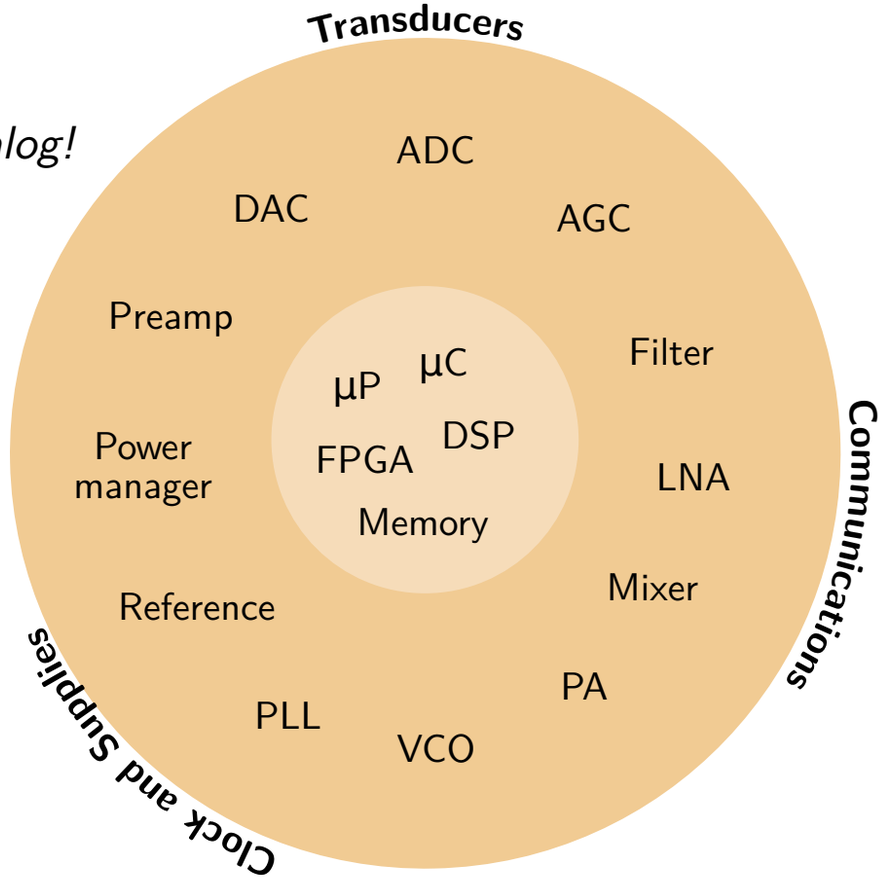
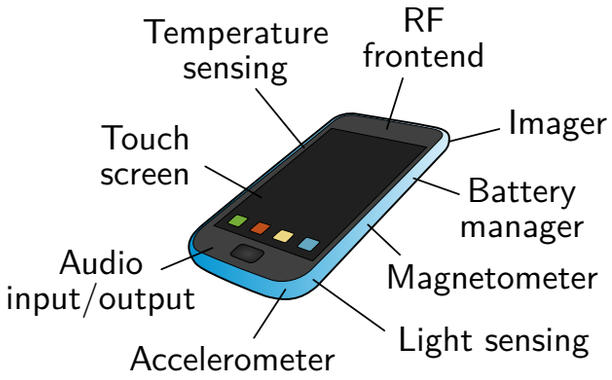
  - **Modeling** skills
  - Complex **EDA** tools
- ...but still **necessary**!
- Most modern ICs are really **mixed-signal**





IC vs PCB

- What can mixed IC design offer compared to PCB?

Good	Bad

IC vs PCB

- What can mixed IC design offer compared to PCB?

Good	Bad
▲ Small **size** and high **density**	
▲ **Complex** systems	
▲ High **speed** operation	
▲ Low **power** consumption	
▲ **Heterogeneous** SoC (A/D/RF/MEMS/Power)	
▲ Low **production costs**	

IC vs PCB

- What can mixed IC design offer compared to PCB?

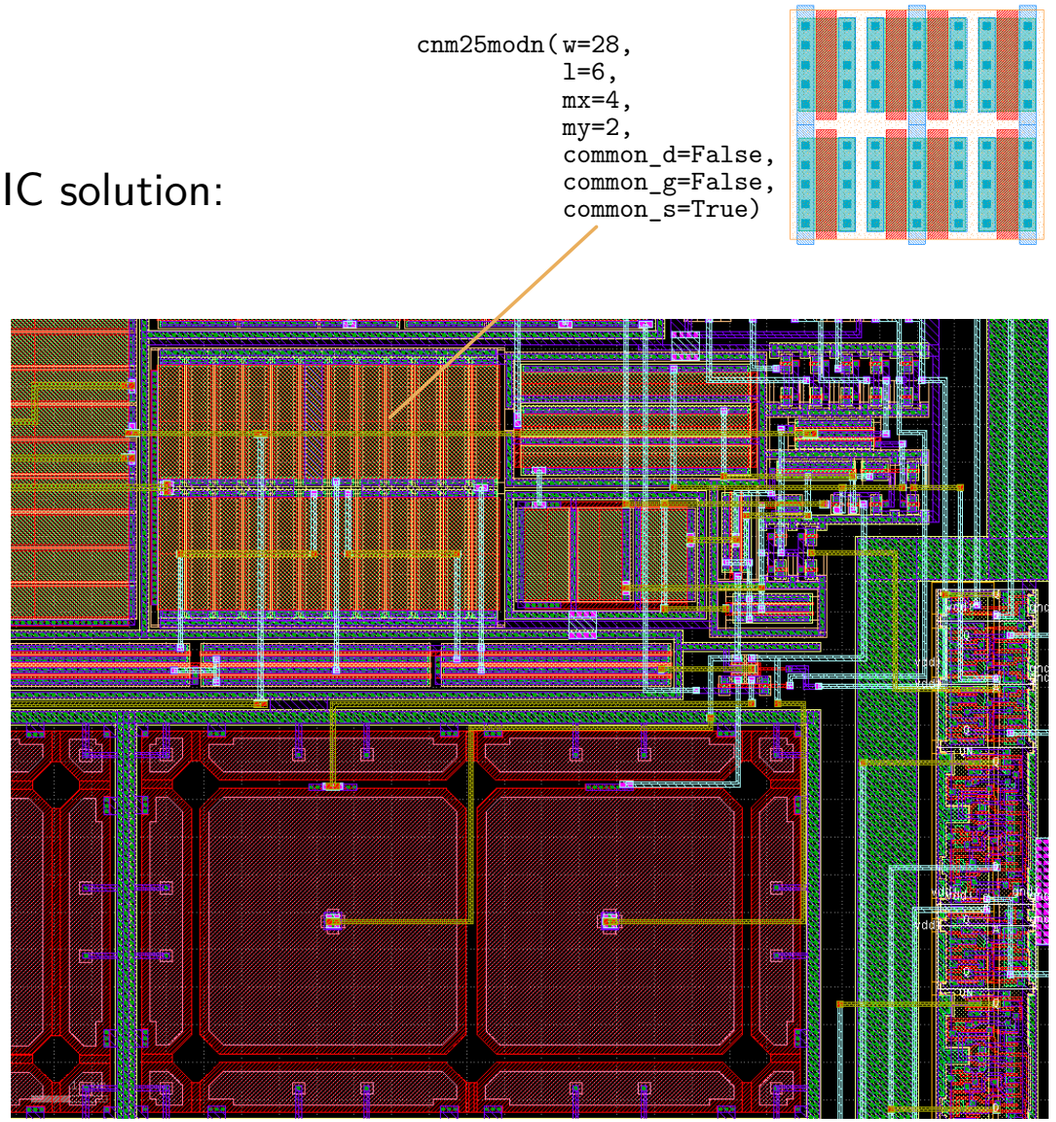
Good	Bad
▲ Small **size** and high **density**	▼ Low **observability**/**controllability**
▲ **Complex** systems	▼ Few device **primitives**
▲ High **speed** operation	▼ Technology **variability** (process and mismatching)
▲ Low **power** consumption	▼ Complex **modeling**
▲ **Heterogeneous** SoC (A/D/RF/MEMS/Power)	▼ High **design costs** (EDA/personnel)
▲ Low **production costs**	▼ High **prototyping costs**
	▼ Long **design cycles**

IC Flavors

- Each **application** may require a different IC solution:

	Full-custom
Density	
Flexibility	
Performance	
Design time	
EDA tools	
Prototype costs	
Target volume	High
Mixed-mode	A and D

- **Hand-drawn** geometry
- **All** layers customized
- Application-specific IC (**ASIC**) result

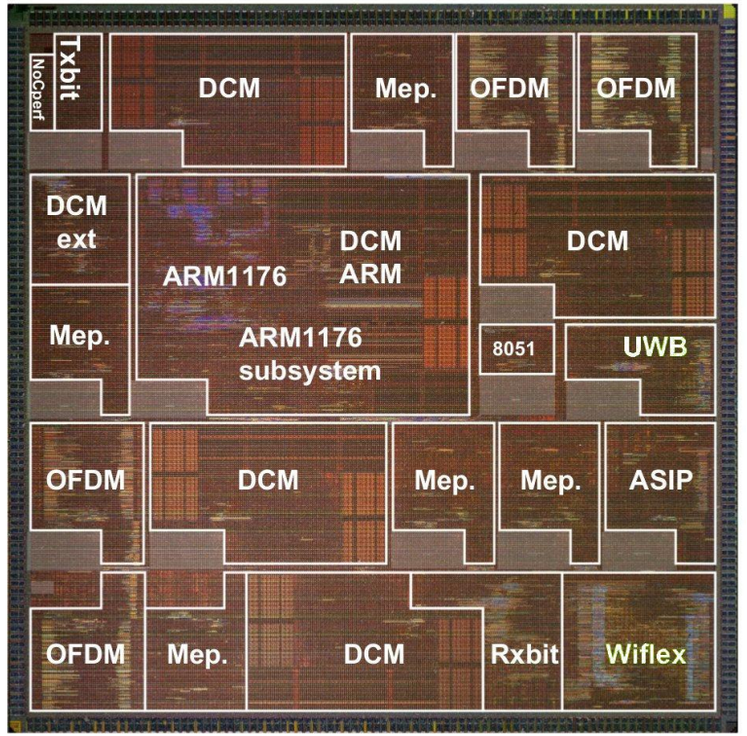


IC Flavors

- Each **application** may require a different IC solution:

	Full-custom	**Macro-cell**
Density		
Flexibility		
Performance		
Design time		
EDA tools		
Prototype costs		
Target volume	High	High
Mixed-mode	A and D	A and D

- Configurable **IP** blocks (ADC, memory...)
- Automated **routing**
- **All** layers customized
- Still an **ASIC**



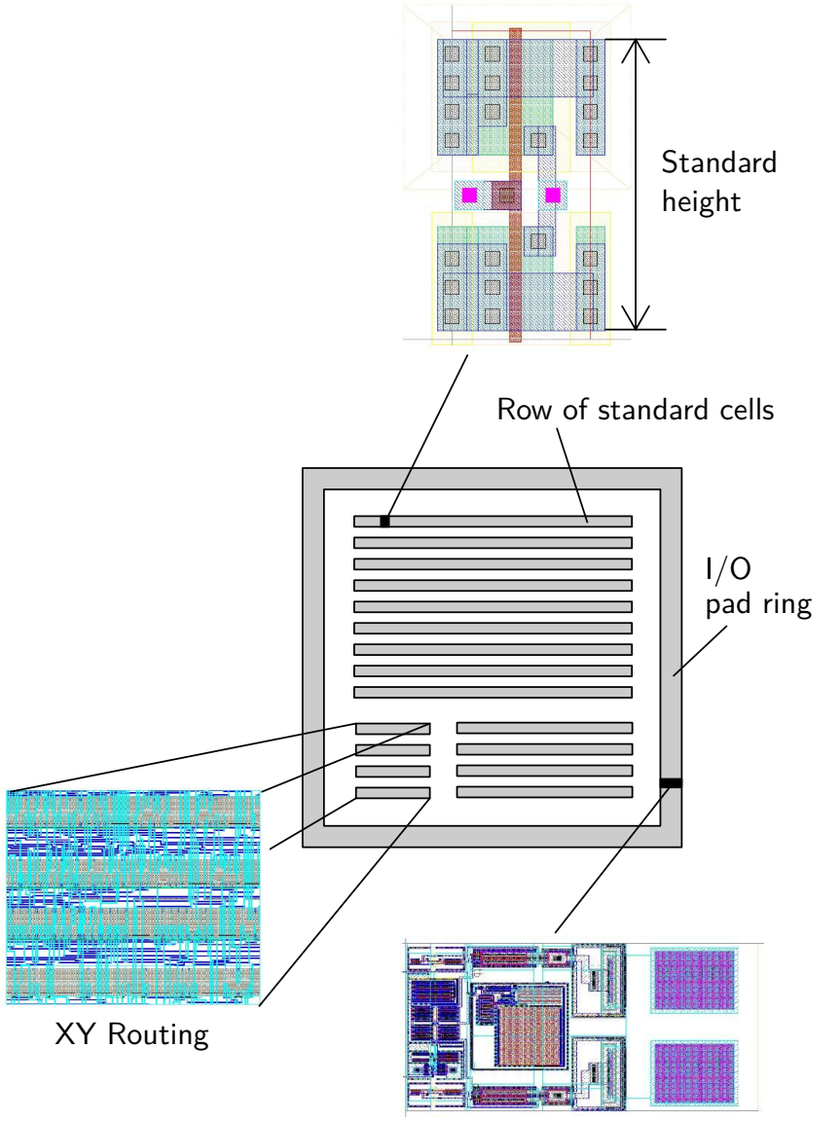
Magali 65-nm SoC for 4G communication with 22 IPs

IC Flavors

- Each **application** may require a different IC solution:

	Full-custom	Macro-cell	**Standard-cell**
Density			
Flexibility			
Performance			
Design time			
EDA tools			
Prototype costs			
Target volume	High	High	High
Mixed-mode	A and D	A and D	D

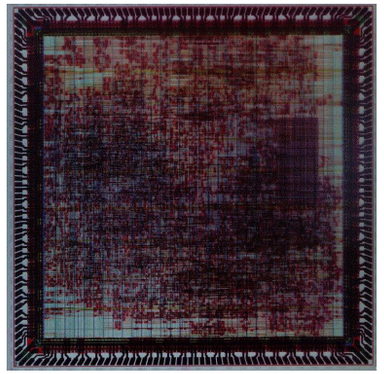
- **Gate** level cells + automated **routing**
- Regular **floorplan**
- **All** layers customized
- Still an **ASIC**

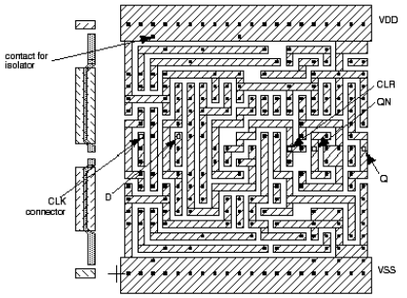


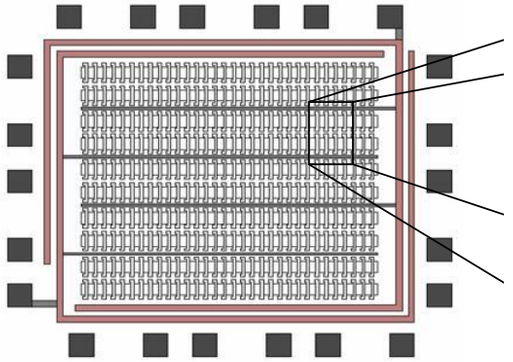
IC Flavors

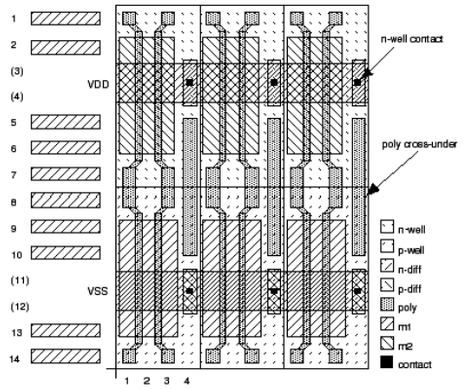
- Each **application** may require a different IC solution:

	Full-custom	Macro-cell	Standard-cell	**Gate-array**
Density				
Flexibility				
Performance				
Design time				
EDA tools				
Prototype costs				
Target volume	High	High	High	Medium
Mixed-mode	A and D	A and D	D	D









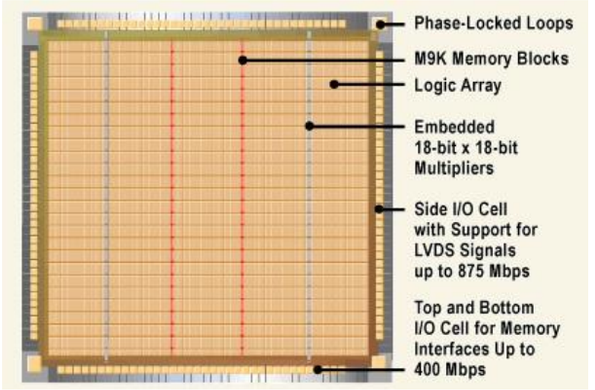
- **Pre-built** transistors/gates/IPs
- **Only routing** layers customized
- **Structured** ASIC

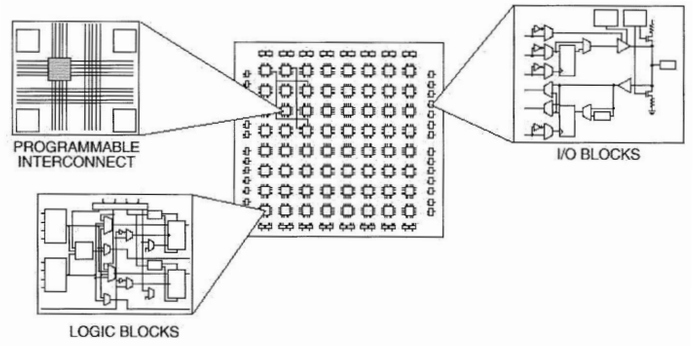
IC Flavors

- Each **application** may require a different IC solution:

	Full-custom	Macro-cell	Standard-cell	Gate-array	**FPGA**
Density					
Flexibility					
Performance					
Design time					
EDA tools					
Prototype costs					
Target volume	High	High	High	Medium	Low
Mixed-mode	A and D	A and D	D	D	D (A)

Altera
Cyclone III





- **Programmable** logic blocks
- **Programmable** routing
- Not an **ASIC**

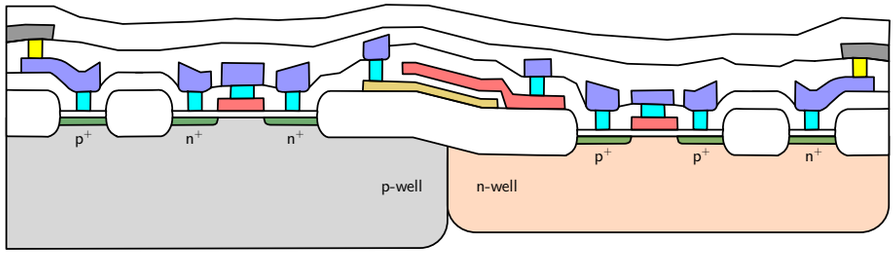
IC Flavors

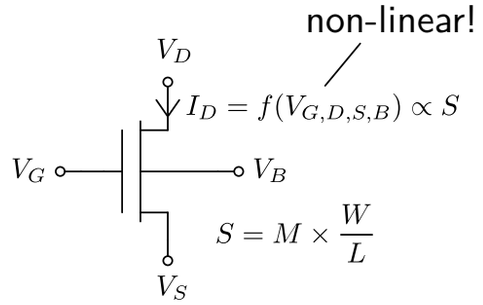
- Each **application** may require a different IC solution:

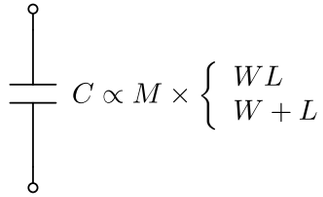
	Full-custom	Macro-cell	Standard-cell	Gate-array	FPGA
Density					
Flexibility					
Performance					
Design time					
EDA tools					
Prototype costs					
Target volume	High	High	High	Medium	Low
Mixed-mode	A and D	A and D	D	D	D (A)

Full-Custom Design

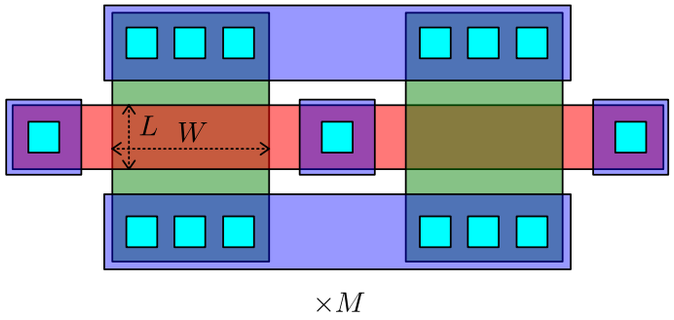
- ▼ **Fixed** CMOS technology:
  - Materials and processes
  - Vertical dimensions
- ▲ Mixed design space:
  - Circuit **topology**
  - Device **horizontal sizing**
  - Device **biasing**

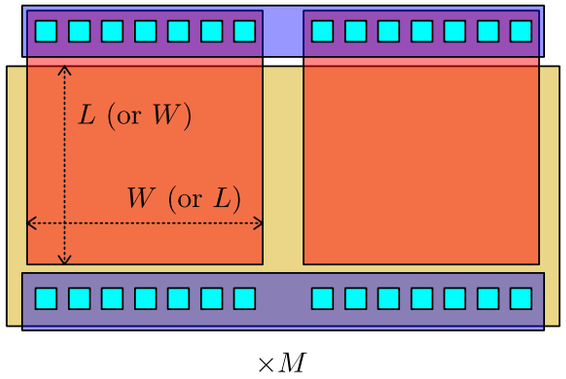






Width
Length
Multiplicity





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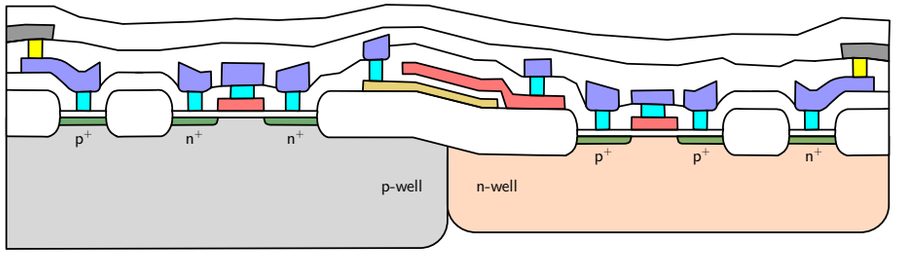
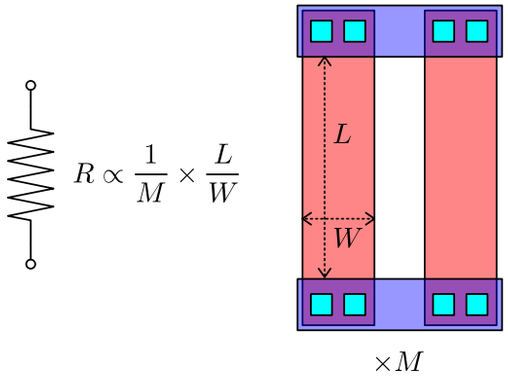
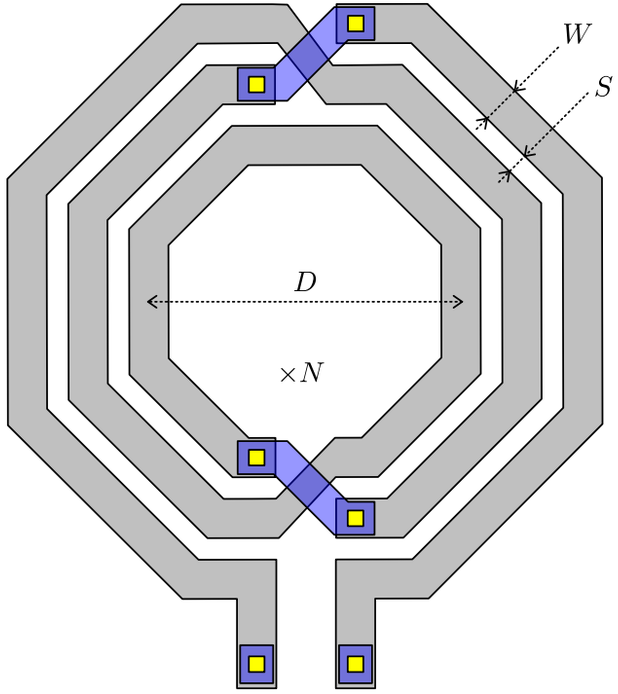
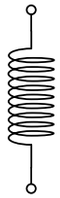






other device cases:

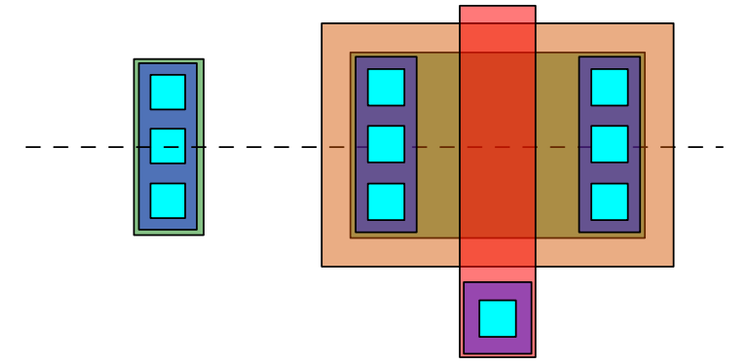
Number of turns
Inner **D**iameter
Spacing
Width

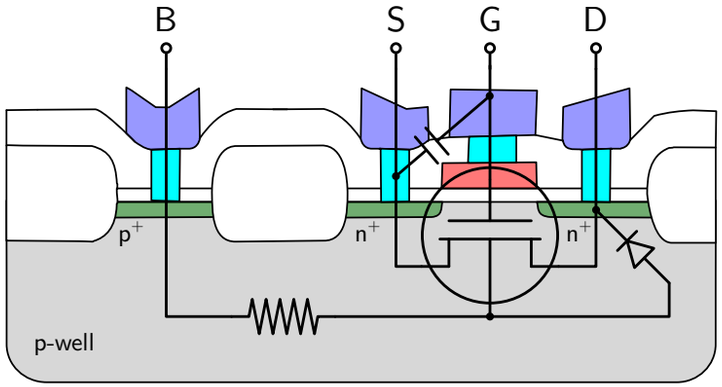


$L = f(N, D, S, W)$

Bulk Enhancement MOSFET

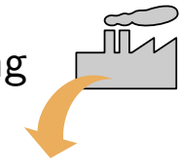
- **Intrinsic** and **extrinsic** model parts





- ▲ **Accurate** results from electrical simulation
- ▼ Too **complex** for hand design!

- **Analytical** (physical) vs **numerical** (fitting) modeling



```
.MODEL MY_NMOS BSIM3V3 TYPE=N
+ VERSION=3.2 PARAMCHK=1
```

Process
```
+ NSUB=2.161E+19 NCH=1.280E+17 XJ=1.500E-07 LINT=7.639E-04
+ WINT=3.669E-04 LL=0 LLN=0 LW=0 LWN=0 LWL=0 WL=-1.253E-10
+ WLN=1 WW=-2.595E-07 WWN=4.475E-01 WWL=0 DWG=0 DWB=0
+ TOX=3.800E-08 TOXM=3.800E-08 XT=1.000E-07 RDSW=3.580E+02
+ PRWB=6.678E-03 PRWG=4.740E-04 WR=4.148E-01
```

Threshold voltage
```
+ VTH0=7.874E-01 K1=1.233E+03 K2=-6.791E-02 K3=8.227E+03
+ K3B=-5.071E-01 W0=2.500E-06 NLX=0 DVT0=5.820E+00 DVT1=5.168E-01
+ DVT2=-2.594E-01 DVT0W=0 DVT1W=5.300E+06 DVT2W=-3.200E-02
+ A0=8.010E-01 B0=0 B1=0 A1=0 A2=1 AGS=1.006E-01 KETA=-1.385E-02
```

Mobility
```
+ MOBMOD=1 U0=6.020E+02 VSAT=1.746E+08
+ UA=9.395E-07 UB=2.828E-15 UC=5.191E-08
```

Output resistance
```
+ DROUT=5.600E-01 PCLM=3.178E+03 PDIBLC1=4.811E+03
+ PDIBLC2=8.600E-03 PDIBLCB=0 PSCBE1=4.240E+08
+ PSCBE2=1.000E-05 PVAG=0 DELTA=1.000E-02
```

Subthreshold
```
+ CDSC=2.953E-02 CDSCB=7.380E-03 CDSCD=-2.864E-03
+ NFACTOR=6.727E-01 CIT=0 VOFF=-6.277E-02
+ DSUB=5.600E-01 ETA0=0 ETAB=-1.653E-01
```

SPICE

Charge model
```
+ CAPMOD=3 DWC=3.669E-04 DLC=0 CLC=1.000E-07
+ CLE=6.000E-01 CF=0 ELM=2 ACDE=1 MOIN=15
+ NOFF=1 VOFFCV=0 XPART=6.000E-01 LLC=0
+ LWC=0 LWLC=0 WLC=-1.253E-10 WWC=-2.595E-07 WWLC=0
```

Substrate
```
+ ALPHA0=2.725E-03 ALPHA1=-7.804E-01 BETA0=3.180E+01
```

Junction diode
```
+ JS=1.000E-04 JSW=0 NJ=1 IJTH=1.000E-01
+ CJ=5.000E-04 MJ=5.000E-01 PB=1
+ CJSW=5.000E-10 MJSW=3.300E-01 PBSW=1
+ CJSWG=5.000E-10 MJSWG=3.300E-01 PBSWG=1
```

Overlap cap.
```
+ CGSO=0 CGDO=0 CGBO=0 CGSL=0 CGDL=0 CKAPPA=6.000E-01
```

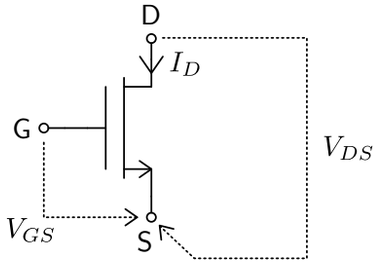
Thermal model
```
+ TNOM=27 KT1=-1.100E-01 KT1L=0 KT2=2.200E-02 AT=3.300E+04
+ UA1=4.310E-09 UB1=-7.610E-18 UC1=-5.600E-11 PRT=0 UTE=-1.5
+ XTI=3 TPB=0 TPBSW=0 TPBSWG=0 TCJ=0 TCJSW=0 TCJSWG=0
```

Noise model
```
+ NOIMOD=1 KF=1.000E-17 AF=1.5 EF=1.5 NOIA=2.000E+29
+ NOIB=2.000E+29 NOIC=2.000E+29 EM=4.100E+07
```

Scaling
```
+ XL=0 XW=0 PK1=1.711E-01 PK2=-6.688E-02
+ PUA=6.246E-04 PUB=-3.418E-12 LUC=1.519E-05
+ PUC=-5.063E-05 PAGS=2.532E-01 PRDSW=-1.071E+04
+ WVSAT=0 PVSAT=-1.800E+05 PVTH0=-1.644E-01
```

Bulk Enhancement MOSFET

- Classic **large signal I/V** model:



Non linear

$$I_D = \begin{cases} \beta\left[(V_{GS}-V_{TH})\,V_{DS} - \frac{1}{2}V_{DS}^2\right] & V_{DS} \le V_{DSsat} \\ \frac{\beta}{2}(V_{GS}-V_{TH})^2\left[1+\lambda\,(V_{DS}-V_{DSsat})\right] & V_{DS} \ge V_{DSsat} \end{cases}$$

Channel length modulation (**CLM**): negligible for large signal, but critical in **small signal**

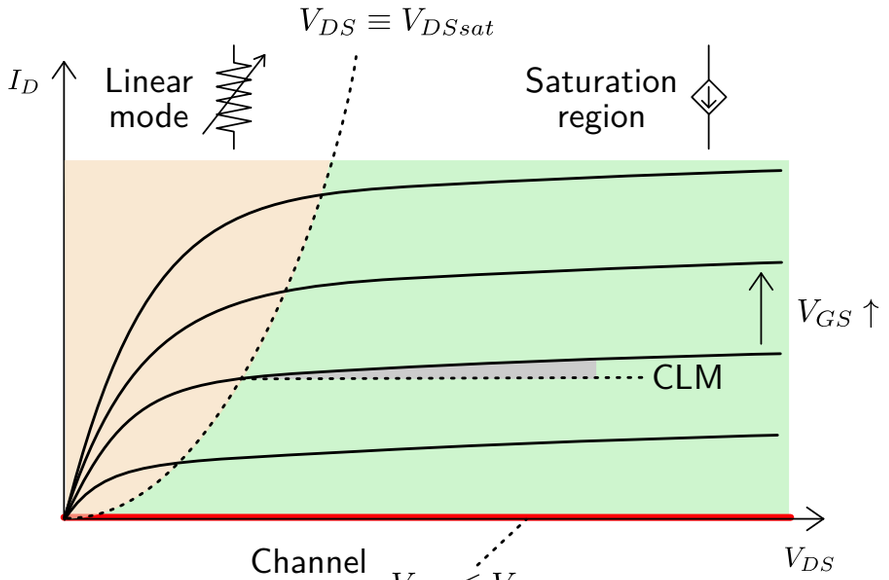
$$\lambda \propto \frac{1}{L}$$

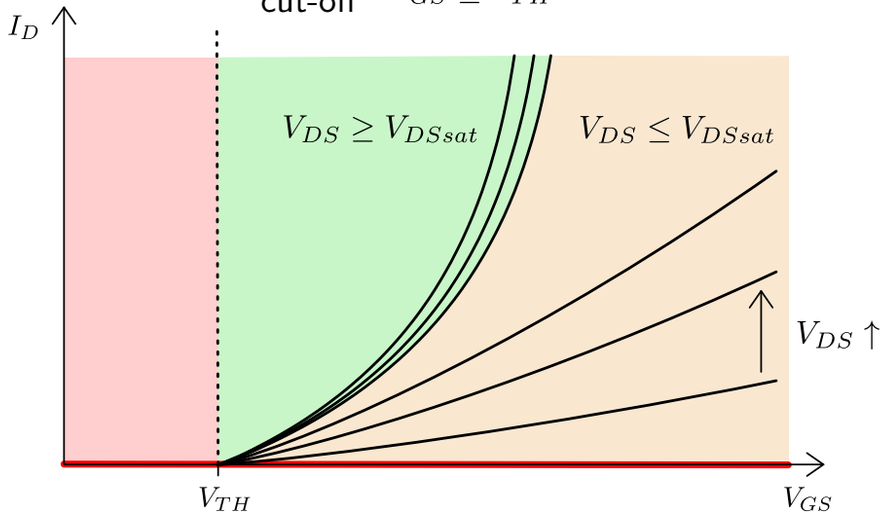
$$\beta \doteq M\frac{W}{L}K \qquad K = \mu C_{ox}$$

Current factor

$$V_{DSsat} \doteq V_{GS} - V_{TH}$$

Pinch-off voltage





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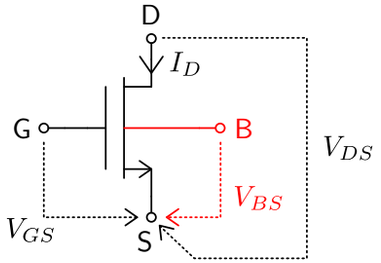

Non linear

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$$\lambda \propto \frac{1}{L}$$

$$\beta \doteq M\frac{W}{L}K \qquad K = \mu C_{ox}$$

Current factor

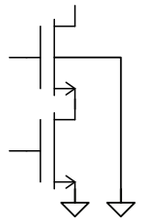
$$V_{DSsat} \doteq V_{GS} - V_{TH}$$

Pinch-off voltage

▲ **Simple** enough for hand design

▼ **Body effect** in stacked circuits?

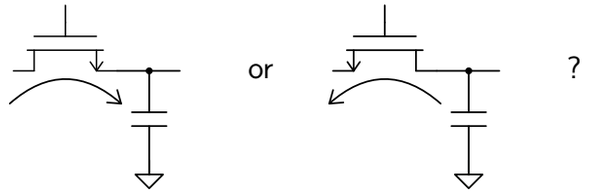
$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|}\right)$$



$$\gamma = \frac{\sqrt{2q\epsilon_{Si}N_{sub}}}{C_{ox}}$$

Body effect coefficient

▼ **Asymmetrical** D/S model!



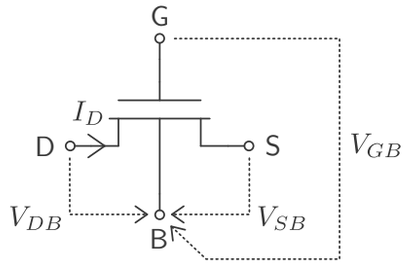
▼ **Subthreshold** operation?

▼ **Single expression** wanted for all regions with continuous derivatives (small signal)...

Bulk Enhancement MOSFET

- EKV **large signal I/V** model:

↗ ekv.epfl.ch
Enz
Krummenacher
Vittoz



$$F(x) \doteq \ln^2\left(1+e^{\frac{x}{2}}\right) \equiv \begin{cases} e^x & x \ll 0 \\ \left(\frac{x}{2}\right)^2 & x \gg 0 \end{cases}$$

$$I_D = I_{DF} - I_{DR} = I_S\left[F\left(\frac{V_P - V_{SB}}{U_t}\right) - F\left(\frac{V_P - V_{DB}}{U_t}\right)\right]$$

Forward Reverse

- **Specific current**

$$I_S \doteq 2n\beta U_t^2$$

Subthreshold slope (1<n<2)

$$M\frac{W}{L}\underbrace{\mu C_{ox}}_{K}$$

- Pinch-off voltage

$$V_P \doteq \frac{V_{GB} - V_{TH}}{n} \equiv V_{sat}$$

- **Inversion coefficient**

$$IC \doteq \frac{I_D}{I_S}$$

	Weak inversion (subthreshold) V_{SB} and $V_{DB} \gg \frac{V_{GB}-V_{TH}}{n}$	**Strong inversion** V_{SB} or $V_{DB} \ll \frac{V_{GB}-V_{TH}}{n}$
Conduction	$I_S e^{\frac{V_{GB}-V_{TH}}{nU_t}}\left(e^{-\frac{V_{SB}}{U_t}} - e^{-\frac{V_{DB}}{U_t}}\right)$ $\lvert V_{DB} - V_{SB}\rvert \ll U_t$	$\beta\left[(V_{GB}-V_{TH}) - \frac{n}{2}(V_{DB}+V_{SB})\right](V_{DB}-V_{SB})$ V_{SB} and $V_{DB} \ll \frac{V_{GB}-V_{TH}}{n}$
Saturation (forward)	$I_S e^{\frac{V_{GB}-V_{TH}}{nU_t}} e^{-\frac{V_{SB}}{U_t}}\left[1+\lambda(V_{DB}-V_{SB})\right]$ $(V_{DB}-V_{SB}) \gg U_t$	$\frac{\beta}{2n}(V_{GB}-V_{TH}-nV_{SB})^2\left[1+\lambda(V_{DB}-V_{sat})\right]$ $V_{SB} \ll \frac{V_{GB}-V_{TH}}{n}$ and $V_{DB} \gg V_{sat}$

Bulk Enhancement MOSFET

- EKV **large signal I/V** model:

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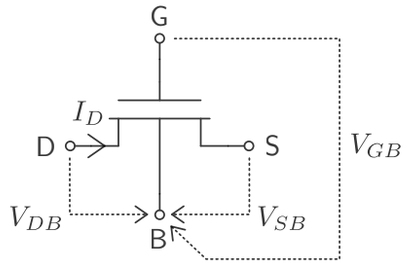
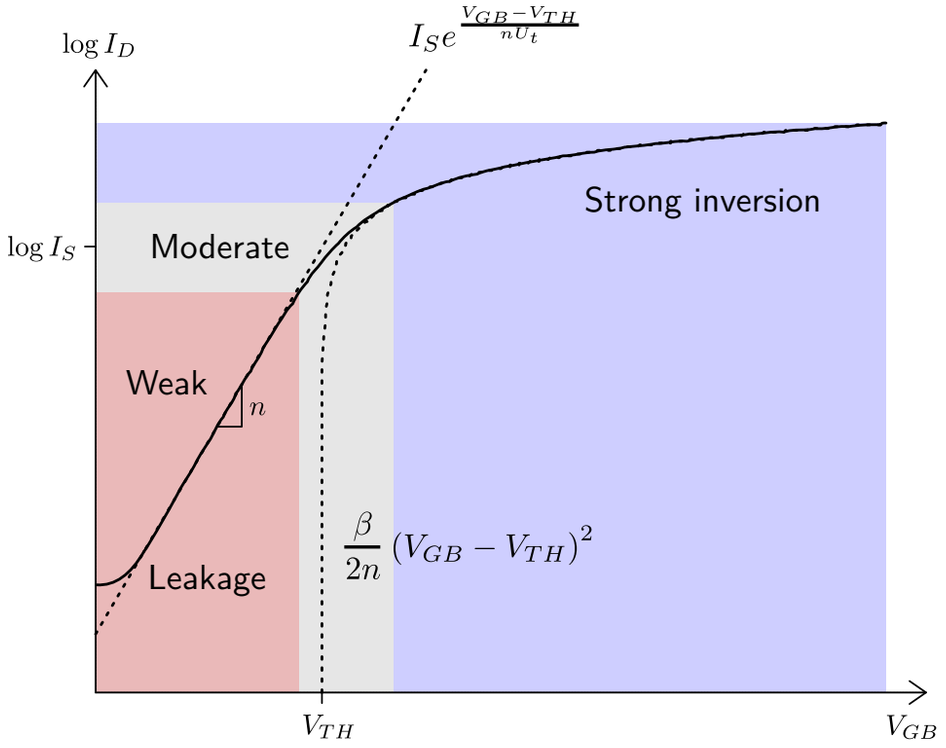


- ▲ **Simple** enough for hand design
- ▲ **Symmetrical** D/S expressions
- ▲ Explicit **body effect**
- ▲ **Single expression** from strong to weak inversion and from conduction to saturation
- ▲ **Continuous derivatives** for small signal parameters

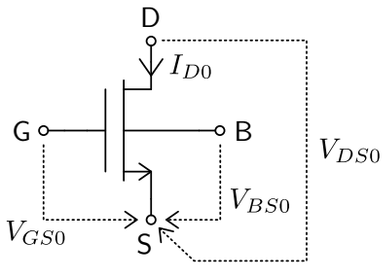
Forward saturation example (neglecting CLM):



$$I_D\left(V_{GB}, V_{SB}, V_{DB}\right)|_{\text{PMOS}} \equiv -\, I_D\left(-V_{GB}, -V_{SB}, -V_{DB}\right)|_{\text{NMOS}}$$

Bulk Enhancement MOSFET

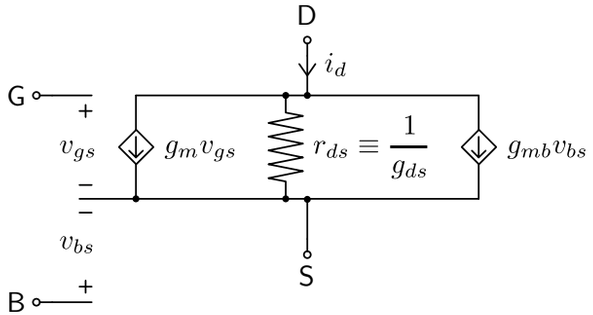
- Classic **small signal transconductance** model:



Non-linear
operating point

Small signal
increments only

$$V_{GS} = V_{GS0} + v_{gs}$$
$$V_{DS} = V_{DS0} + v_{ds}$$
$$V_{BS} = V_{BS0} + v_{bs}$$
$$I_D = I_{D0} + i_d$$



Linear
equivalent circuit

$$I_D = \begin{cases} \beta\left[(V_{GS} - V_{TH})\,V_{DS} - \frac{1}{2}V_{DS}^2\right] & V_{DS} \le V_{DSsat} \\ \frac{\beta}{2}(V_{GS} - V_{TH})^2\left[1 + \lambda\,(V_{DS} - V_{DSsat})\right] & V_{DS} \ge V_{DSsat} \end{cases}$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|}\right)$$

$$g_m \doteq \frac{\partial I_D}{\partial V_{GS}} \equiv \left.\frac{i_d}{v_{gs}}\right|_{v_{ds}=v_{bs}=0}$$

$$g_{ds} \doteq \frac{\partial I_D}{\partial V_{DS}} \equiv \left.\frac{i_d}{v_{ds}}\right|_{v_{gs}=v_{bs}=0}$$

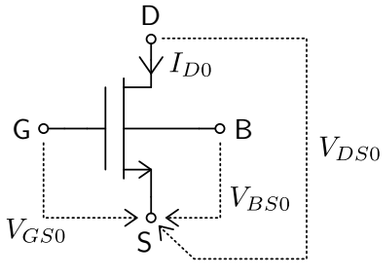
$$g_{mb} \doteq \frac{\partial I_D}{\partial V_{BS}} \equiv \left.\frac{i_d}{v_{bs}}\right|_{v_{gs}=v_{ds}=0}$$

$$g_m \simeq \begin{cases} \beta V_{DS} & V_{DS} \le V_{DSsat} \\ \beta\,(V_{GS} - V_{TH}) \equiv \sqrt{2\beta I_D} & V_{DS} \ge V_{DSsat} \end{cases}$$

- Analog circuits biased through current sources → **op** as a function of **drain current**

Bulk Enhancement MOSFET

- Classic **small signal transconductance** model:



Non-linear
operating point

Small signal
increments only

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$$V_{DS} = V_{DS0} + v_{ds}$$
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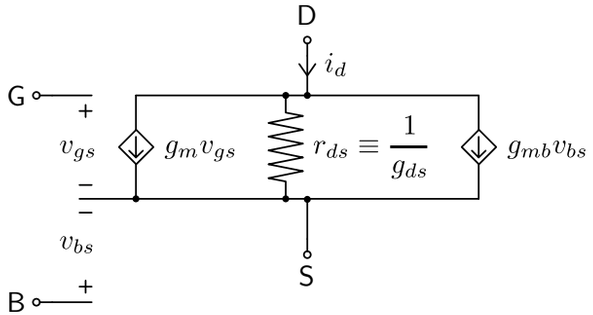


Linear
equivalent circuit

$$I_D = \begin{cases} \beta\left[(V_{GS} - V_{TH})\, V_{DS} - \frac{1}{2} V_{DS}^2\right] & V_{DS} \leq V_{DSsat} \\ \frac{\beta}{2}(V_{GS} - V_{TH})^2 \left[1 + \lambda (V_{DS} - V_{DSsat})\right] & V_{DS} \geq V_{DSsat} \end{cases}$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|}\right)$$

$$g_m \doteq \frac{\partial I_D}{\partial V_{GS}} \equiv \left.\frac{i_d}{v_{gs}}\right|_{v_{ds}=v_{bs}=0}$$

$$g_{ds} \doteq \frac{\partial I_D}{\partial V_{DS}} \equiv \left.\frac{i_d}{v_{ds}}\right|_{v_{gs}=v_{bs}=0}$$

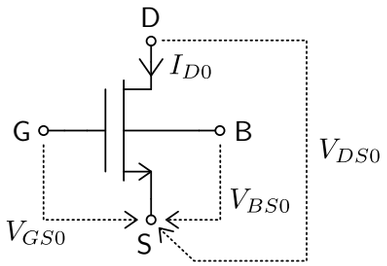
$$g_{mb} \doteq \frac{\partial I_D}{\partial V_{BS}} \equiv \left.\frac{i_d}{v_{bs}}\right|_{v_{gs}=v_{ds}=0}$$

$$g_{ds} \simeq \begin{cases} \beta\,(V_{GS} - V_{TH}) & V_{DS} \leq V_{DSsat} \\ \frac{\beta}{2}(V_{GS} - V_{TH})^2 \lambda \equiv \lambda I_D & V_{DS} \geq V_{DSsat} \end{cases}$$

- Analog circuits biased through current sources $\rightarrow$ **op** as a function of **drain current**

Bulk Enhancement MOSFET

- Classic **small signal transconductance** model:



Non-linear
operating point

Small signal
increments only

$$V_{GS} = V_{GS0} + v_{gs}$$
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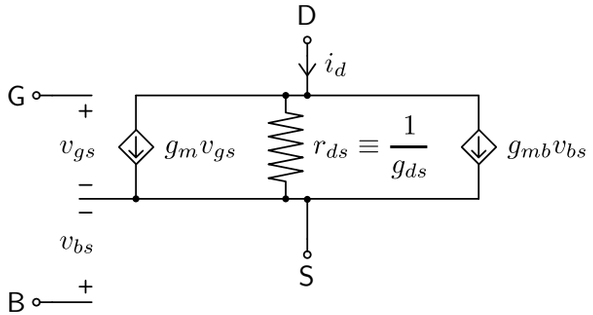
$$V_{BS} = V_{BS0} + v_{bs}$$
$$I_D = I_{D0} + i_d$$



Linear
equivalent circuit

$$I_D = \begin{cases} \beta\left[(V_{GS} - V_{TH})\,V_{DS} - \frac{1}{2}V_{DS}^2\right] & V_{DS} \le V_{DSsat} \\ \frac{\beta}{2}(V_{GS} - V_{TH})^2\left[1 + \lambda\,(V_{DS} - V_{DSsat})\right] & V_{DS} \ge V_{DSsat} \end{cases}$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|}\right)$$

$$g_m \doteq \frac{\partial I_D}{\partial V_{GS}} \equiv \left.\frac{i_d}{v_{gs}}\right|_{v_{ds}=v_{bs}=0}$$

$$g_{ds} \doteq \frac{\partial I_D}{\partial V_{DS}} \equiv \left.\frac{i_d}{v_{ds}}\right|_{v_{gs}=v_{bs}=0}$$

$$g_{mb} \doteq \frac{\partial I_D}{\partial V_{BS}} \equiv \left.\frac{i_d}{v_{bs}}\right|_{v_{gs}=v_{ds}=0}$$

$$g_{mb} \equiv \eta g_m$$

$$\eta = \frac{\gamma}{2\sqrt{|2\Phi_F - V_{BS}|}}$$

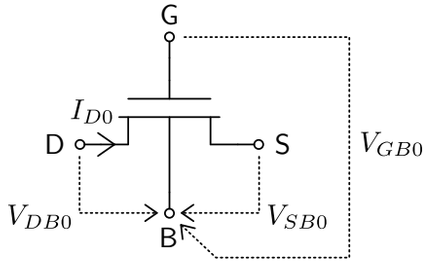
- **Asymmetrical** parameters and non-explicit expressions...

Bulk Enhancement MOSFET

- EKV **small signal transconductance** model:

$$g_{mg} \doteq \frac{\partial I_D}{\partial V_{GB}} \equiv \left.\frac{i_d}{v_{gb}}\right|_{v_{sb}=v_{db}=0} \qquad g_{md} \doteq \frac{\partial I_D}{\partial V_{DB}} \equiv \left.\frac{i_d}{v_{db}}\right|_{v_{gb}=v_{sb}=0}$$

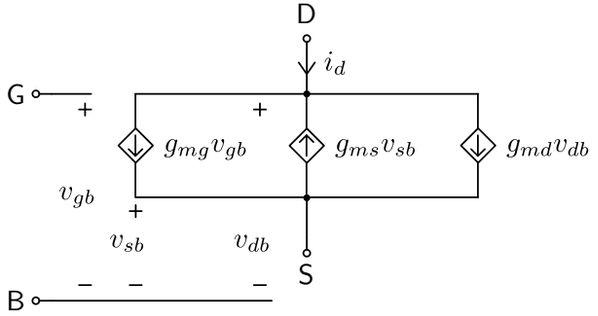
$$g_{ms} \doteq -\frac{\partial I_D}{\partial V_{SB}} \equiv -\left.\frac{i_d}{v_{sb}}\right|_{v_{gb}=v_{db}=0} \equiv n g_{mg}$$



Non-linear
operating point

Small signal
increments only

$$V_{GB} = V_{GB0} + v_{gb}$$
$$V_{DB} = V_{DB0} + v_{db}$$
$$V_{SB} = V_{SB0} + v_{sb}$$
$$I_D = I_{D0} + i_d$$

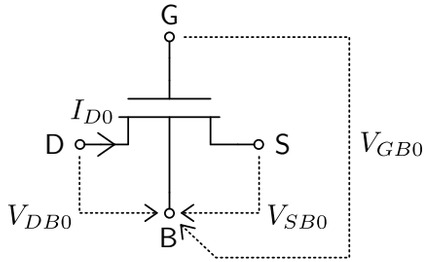


Linear
equivalent circuit

	Weak inversion (subthreshold)	**Strong inversion**
Conduction	$g_{mg} = \frac{I_D}{nU_t}$ $g_{ms} = \frac{I_{DF}}{U_t}$ $g_{md} = \frac{I_{DR}}{U_t}$	$g_{mg} = \beta\,(V_{DB} - V_{SB})$ $g_{ms} = \sqrt{2n\beta I_{DF}}$ $g_{md} = \sqrt{2n\beta I_{DR}}$
Saturation (forward)	$g_{mg} = \frac{I_D}{nU_t}$ $g_{ms} = \frac{I_D}{U_t}$ $g_{md} = \lambda I_D$	$g_{mg} = \sqrt{\frac{2\beta I_D}{n}}$ $g_{ms} = \sqrt{2n\beta I_D}$ $g_{md} = \lambda I_D \propto \frac{1}{L}$

Bulk Enhancement MOSFET

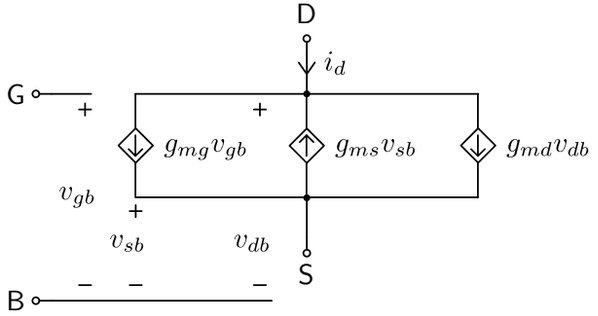
- EKV **small signal transconductance** model:



Non-linear
operating point

Small signal
increments only

$$V_{GB} = V_{GB0} + v_{gb}$$
$$V_{DB} = V_{DB0} + v_{db}$$
$$V_{SB} = V_{SB0} + v_{sb}$$
$$I_D = I_{D0} + i_d$$



Linear
equivalent circuit

$$g_{mg} \doteq \frac{\partial I_D}{\partial V_{GB}} \equiv \left.\frac{i_d}{v_{gb}}\right|_{v_{sb}=v_{db}=0} \qquad g_{md} \doteq \frac{\partial I_D}{\partial V_{DB}} \equiv \left.\frac{i_d}{v_{db}}\right|_{v_{gb}=v_{sb}=0}$$

$$g_{ms} \doteq -\frac{\partial I_D}{\partial V_{SB}} \equiv -\left.\frac{i_d}{v_{sb}}\right|_{v_{gb}=v_{db}=0} \equiv n g_{mg}$$

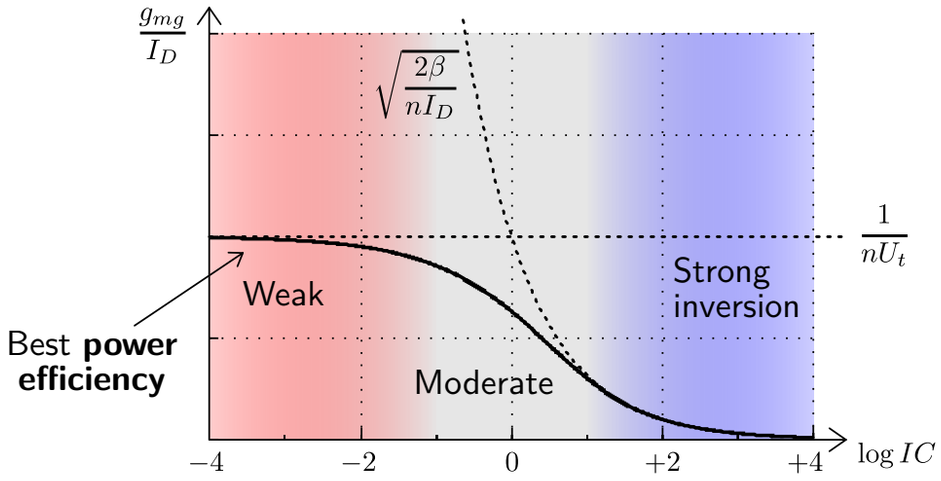
- **Equivalence** between models:

$$g_m \doteq \frac{\partial I_D}{\partial V_{GS}} \equiv g_{mg}$$

$$g_{mb} \doteq \frac{\partial I_D}{\partial V_{BS}} \equiv g_{ms} - g_{mg} - g_{md}$$

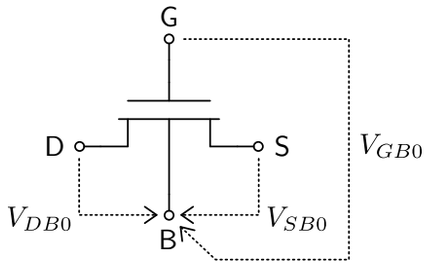
$$g_{ds} \doteq \frac{\partial I_D}{\partial V_{DS}} \equiv g_{md}$$

- **Continuity** between operating regions:



Bulk Enhancement MOSFET

- **Quasi-static transcapacitance** model:



Small signal **increments** only

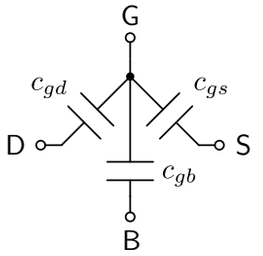
$$V_{GB} = V_{GB0} + v_{gb}$$
$$V_{DB} = V_{DB0} + v_{db}$$
$$V_{SB} = V_{SB0} + v_{sb}$$

$$c_{xy} \doteq \left.\frac{\partial Q_X}{\partial V_Y}\right|_{v_{rest}=0}$$

$$c_{xy} \neq c_{yx}$$

Non-reciprocal!

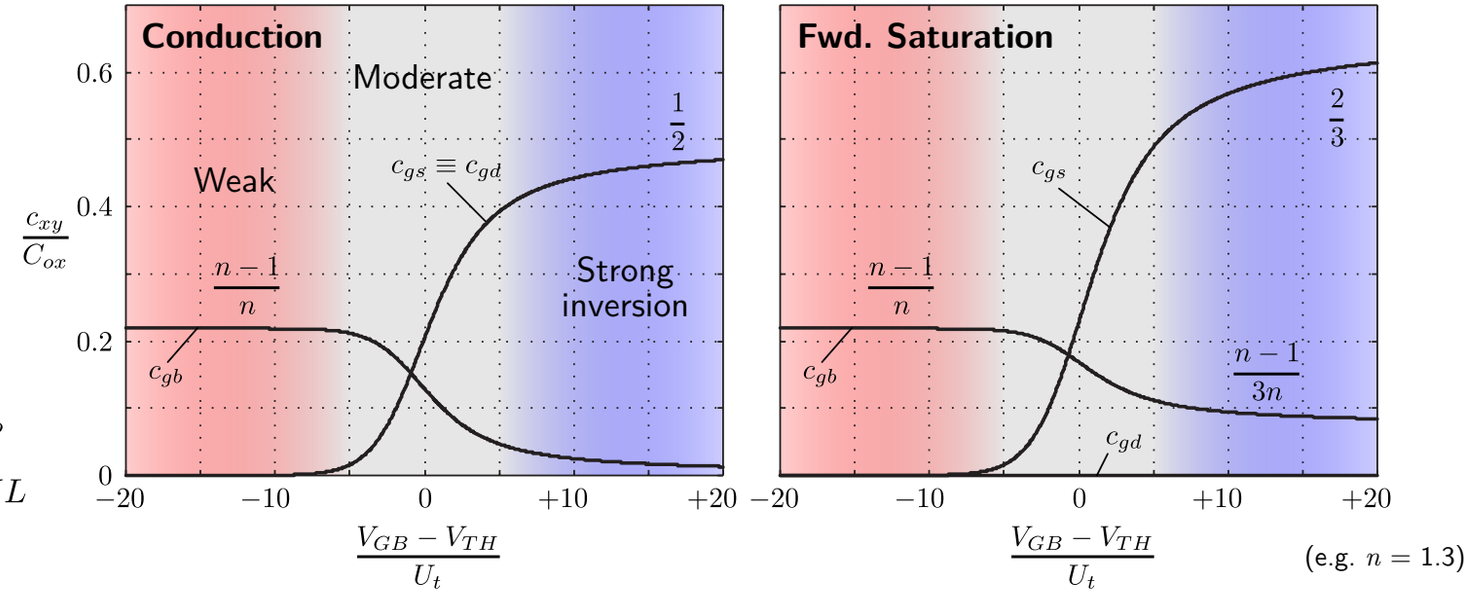
- **Input** only elements:



- Gate **oxide** cap.

3.9 (SiO_2) $\epsilon_r \epsilon_o$

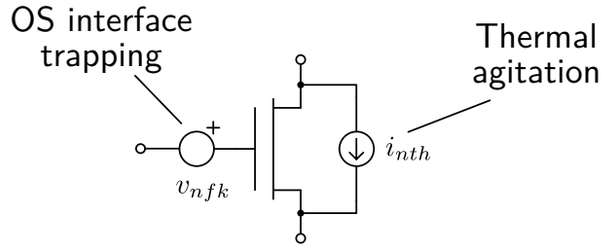
$$C_{ox} \doteq \frac{\epsilon_{ox}}{t_{ox}} WL$$



(e.g. $n = 1.3$)

Bulk Enhancement MOSFET

- Small signal **noise model**:



- **Thermal** (white) component:

$$\frac{di_{nth}^2}{df} = 4KTg_{ms}K_{th} \qquad U_t = \frac{KT}{q}$$

$$K_{th} = \begin{cases} 1 & \text{w.i. and s.i. conduction} \\ \frac{1}{2} \text{ or } \frac{2}{3} & \text{w.i. or s.i. saturation} \end{cases}$$

- **Flicker** (pink) component:

$$\frac{dv_{nfk}^2}{df} = \frac{K_{fk}}{WL}\frac{1}{f}$$

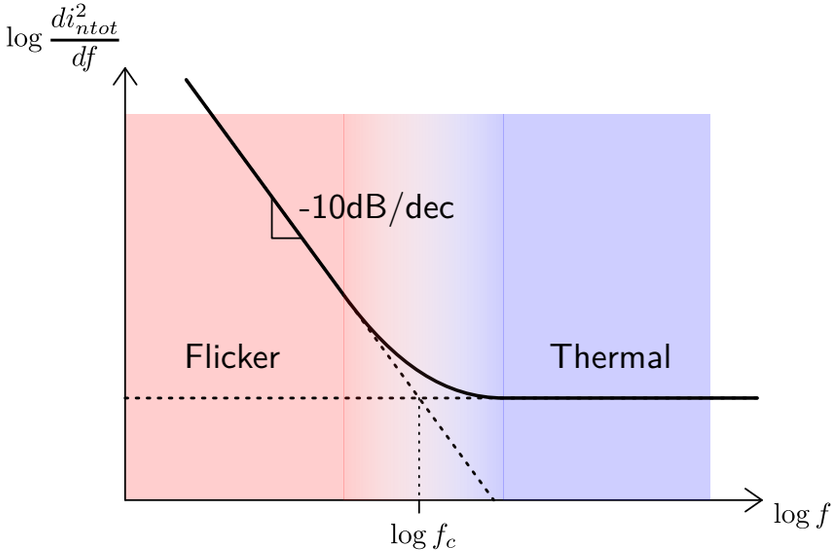
Technology dependent (NMOS >> PMOS)

Memory effect

- **Uncorrelated** phenomena:

$$\frac{di_{ntot}^2}{df} = 4KTg_{ms}K_{th} + g_{mg}^2\frac{K_{fk}}{WL}\frac{1}{f}$$

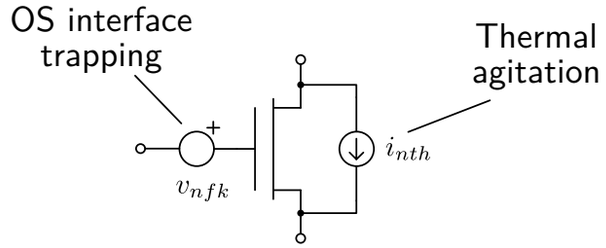
- Power spectral density (**PSD**) statistics:



$$f_c \doteq \frac{g_{mg}^2}{g_{ms}}\frac{K_{fk}}{K_{th}}\frac{1}{4KTWL}$$

Bulk Enhancement MOSFET

- Small signal **noise model**:



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$$U_t = \frac{KT}{q}$$

- **Flicker** (pink) component:

$$\frac{dv_{nfk}^2}{df} = \frac{K_{fk}}{WL}\frac{1}{f}$$

Technology dependent (NMOS >> PMOS)

Memory effect

- **Noise-aware** analog IC design:

Signal-to-noise ratio

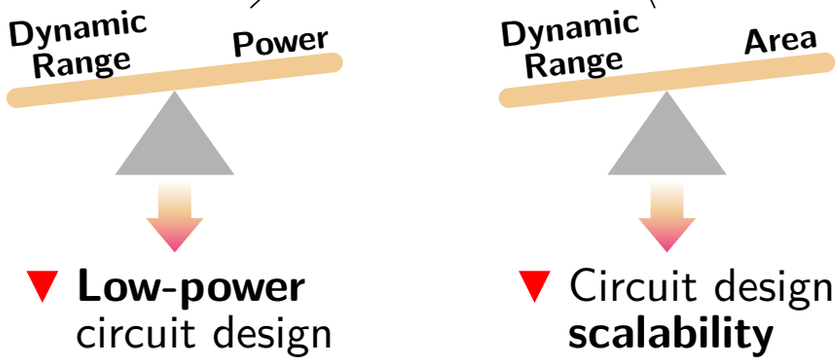
$$SNR \doteq \frac{V_{max}^2}{\int_{BW} \frac{dv_{ntot}^2}{df} df}$$

Signal full scale

$$\frac{di_{ntot}^2}{df} = 4KTg_{ms}K_{th} + g_{mg}^2\frac{K_{fk}}{WL}\frac{1}{f}$$

$$\frac{dv_{ntot}^2}{df} = \frac{4KTnK_{th}}{g_{mg}} + \frac{K_{fk}}{WL}\frac{1}{f}$$

$\propto I_D$ or $\sqrt{I_D}$

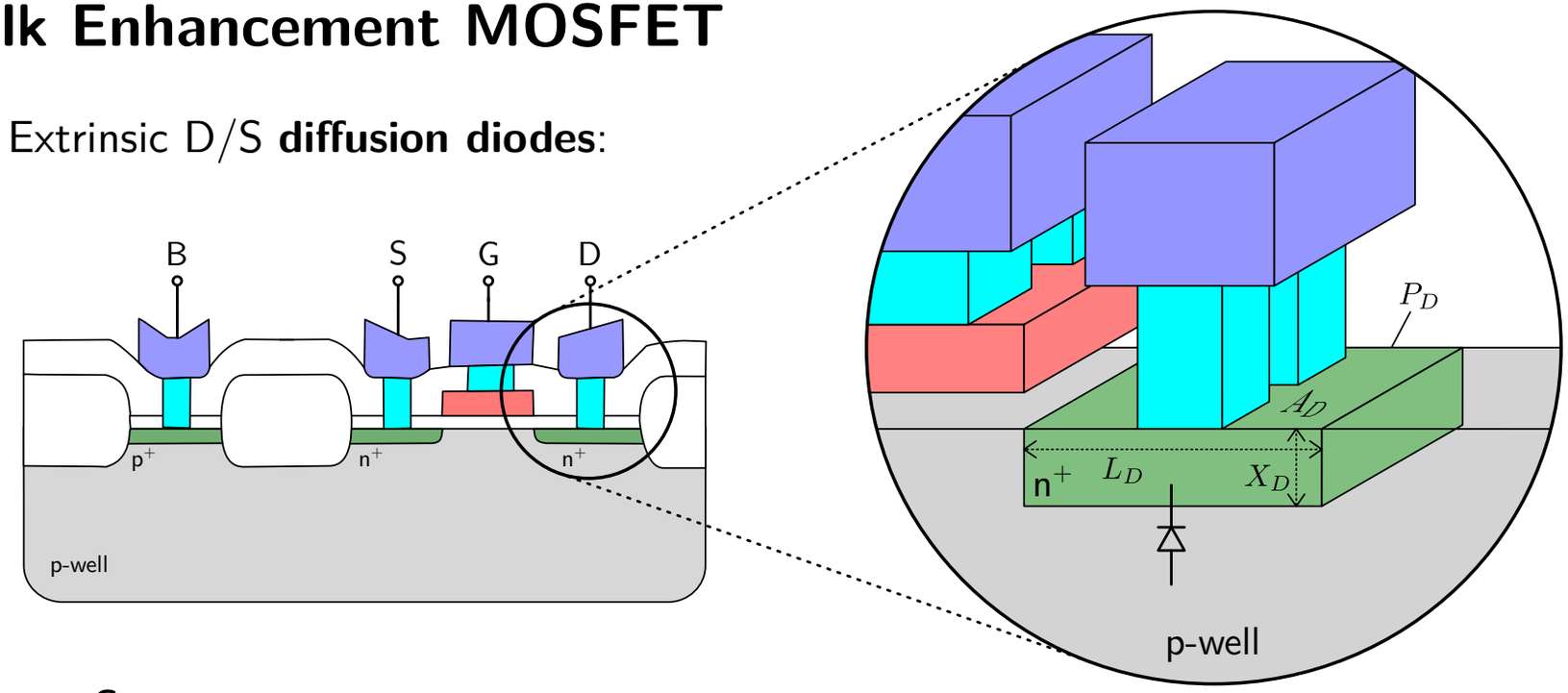


▼ **Low-power** circuit design

▼ Circuit design **scalability**

Bulk Enhancement MOSFET

- Extrinsic D/S **diffusion diodes**:



- **Geometry** parameters:

$$\begin{cases} A_D = W L_D & \text{Area} \\ P_D = 2\,(W + L_D) & \text{Perimeter} \end{cases}$$

$$A_J = A_D + P_D X_D$$

Bottom plate — Side walls

- Reverse **leakage current**:

$$I_D = A_D \texttt{JS}\left(e^{-\frac{V_{DB}}{U_t}} - 1\right) + P_D X_D \texttt{JSW}\left(e^{-\frac{V_{DB}}{U_t}} - 1\right)$$

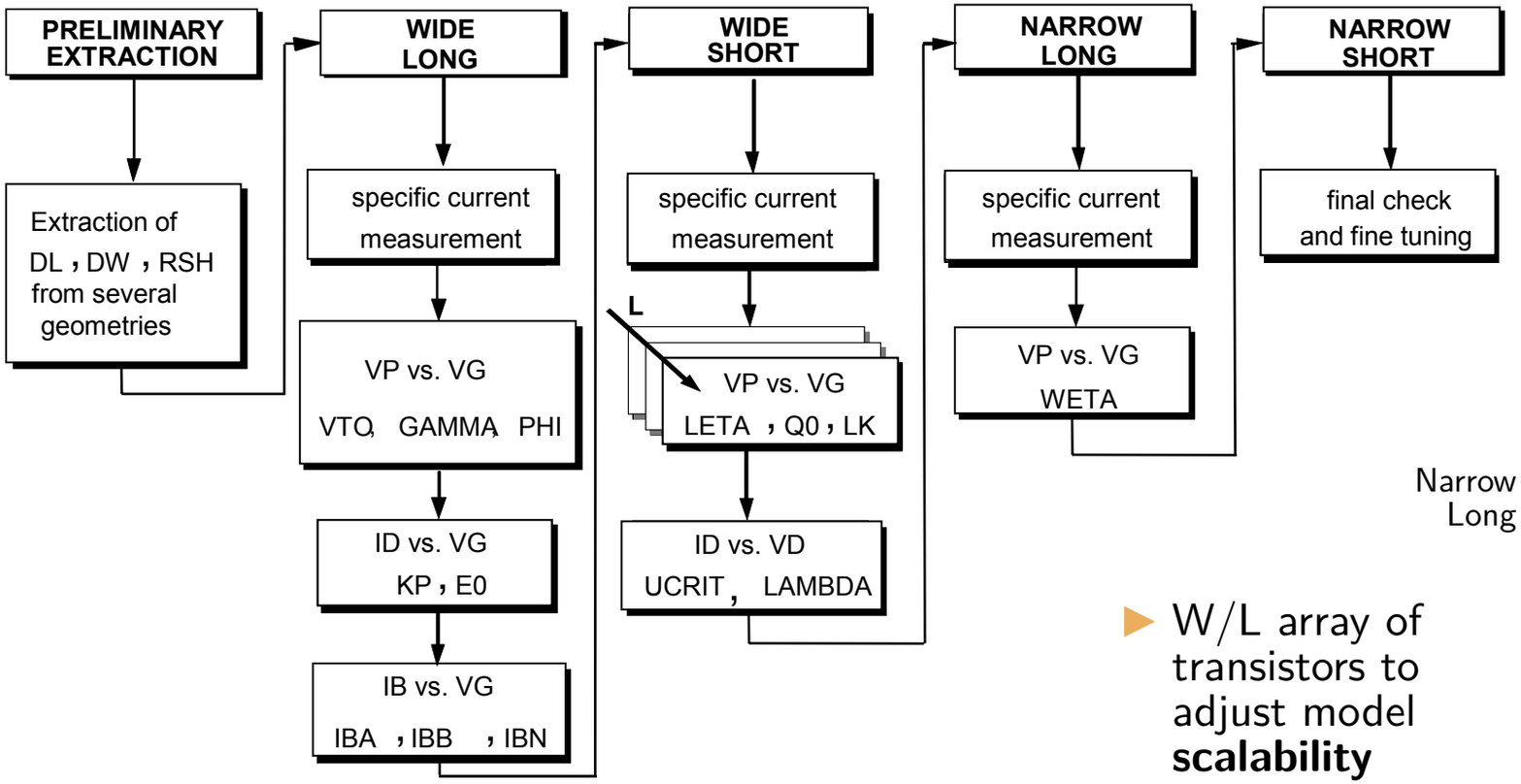
- Depletion **capacitance**:

$$C_D = A_D \frac{\texttt{CJ}}{\left(1 - \frac{V_{DB}}{\texttt{PB}}\right)^{\texttt{MJ}}} + P_D X_D \frac{\texttt{CJSW}}{\left(1 - \frac{V_{DB}}{\texttt{PBSW}}\right)^{\texttt{MJSW}}}$$

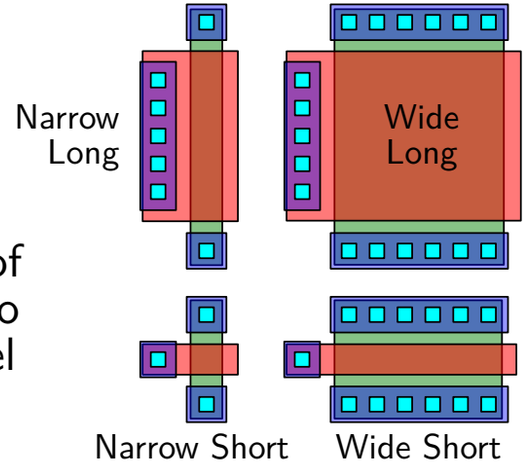
EKV Model Extraction

↗ M.Baucher et al.
An Efficient Parameter Extraction Methodology for the EKV MOST Model
IEEE ICMTS, Mar 1996
doi.org/10.1109/ICMTS.1996.535636

- **Sequential** methodology to minimize errors:



- W/L array of transistors to adjust model **scalability**



EKV Model Extraction

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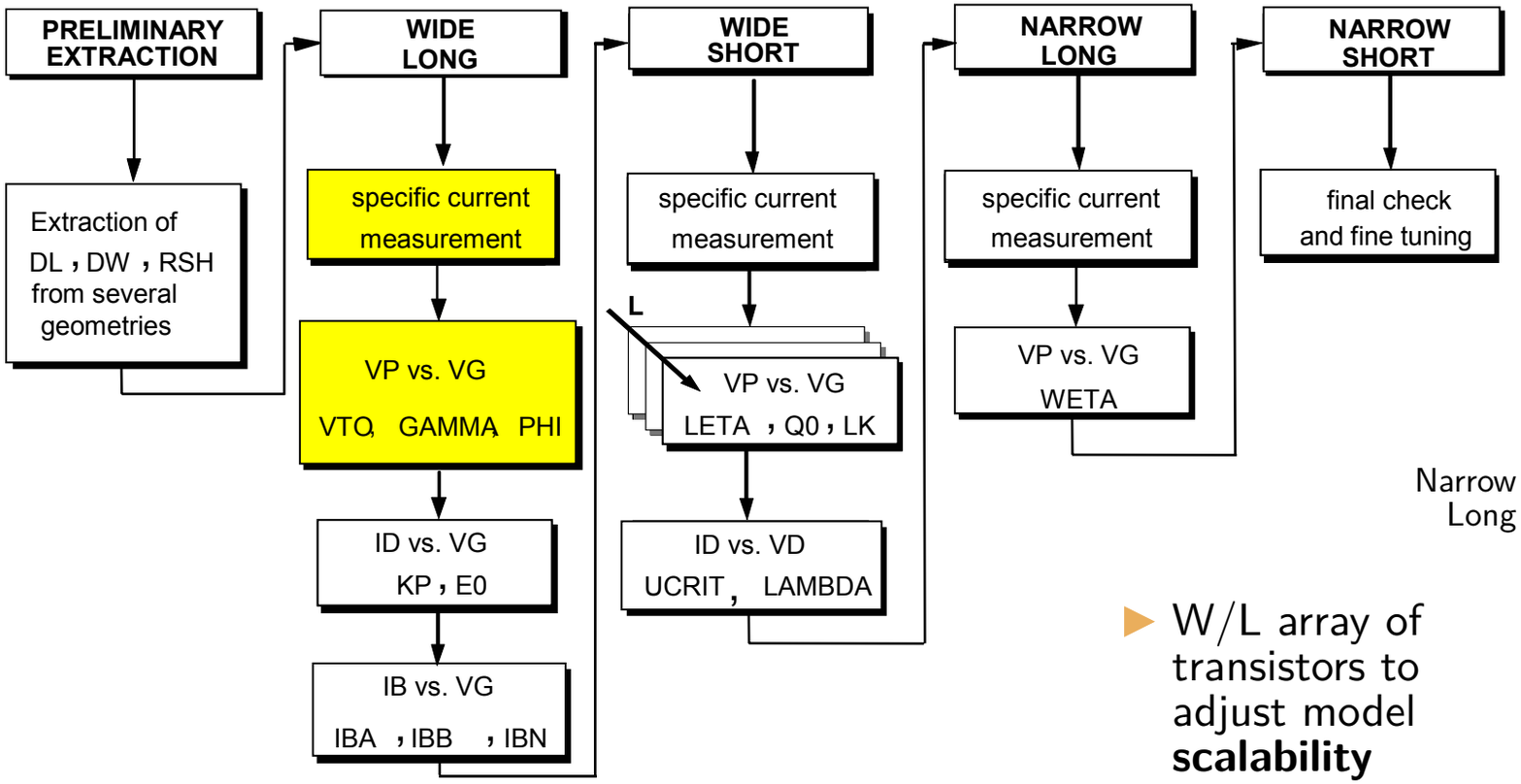
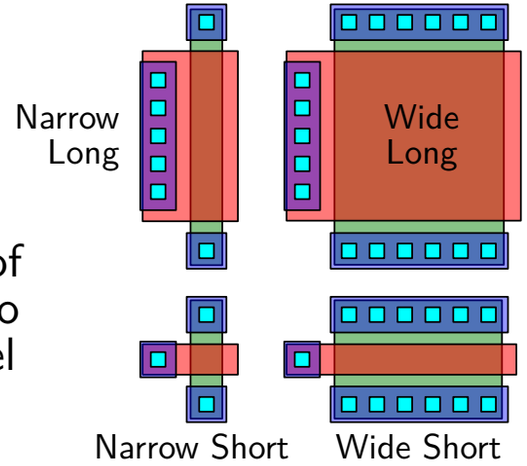
doi.org/10.1109/ICMTS.1996.535636

- **Sequential** methodology to minimize errors:



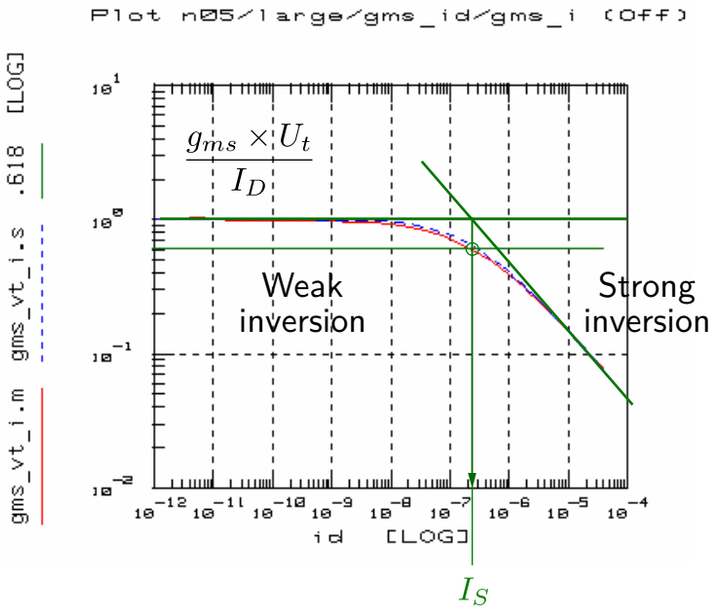
- W/L array of transistors to adjust model **scalability**



EKV Model Extraction

↗ M.Baucher et al.
An Efficient Parameter Extraction Methodology for the EKV MOST Model
IEEE ICMTS, Mar 1996
doi.org/10.1109/ICMTS.1996.535636

- e.g. **specific-current** estimation:



$$\frac{g_{ms} \times U_t}{I_D} = \frac{1}{\sqrt{\frac{1}{4} + IC} + \frac{1}{2}} = \begin{cases} 1 & IC \ll 1 \\ 0.618 & IC \equiv 1 \end{cases}$$

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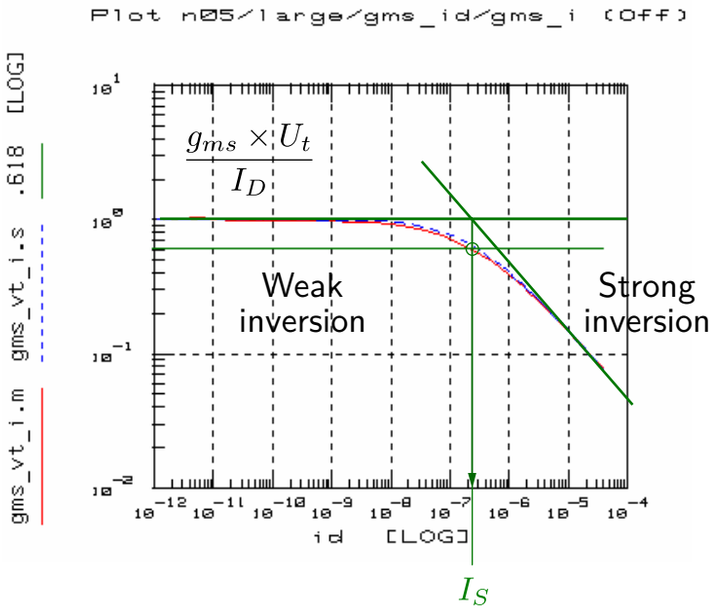

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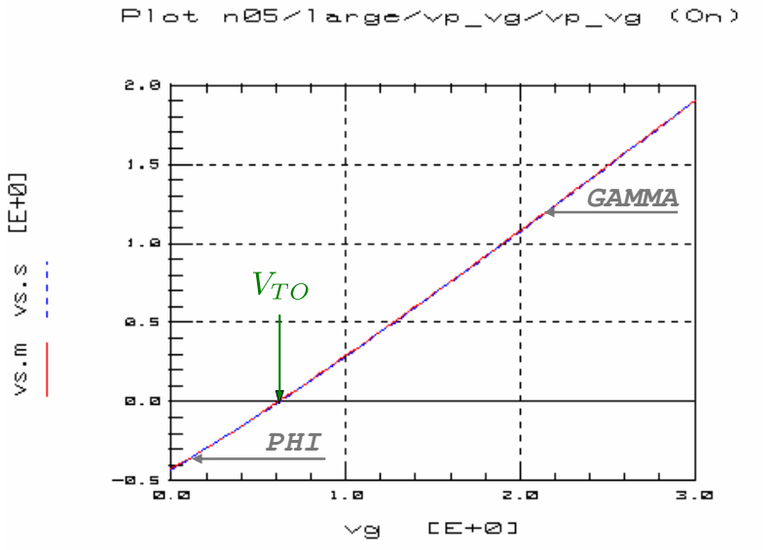
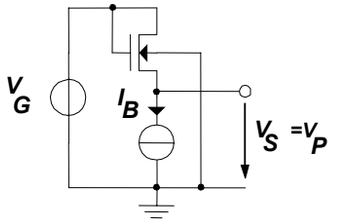
- e.g. **threshold-voltage** estimation:

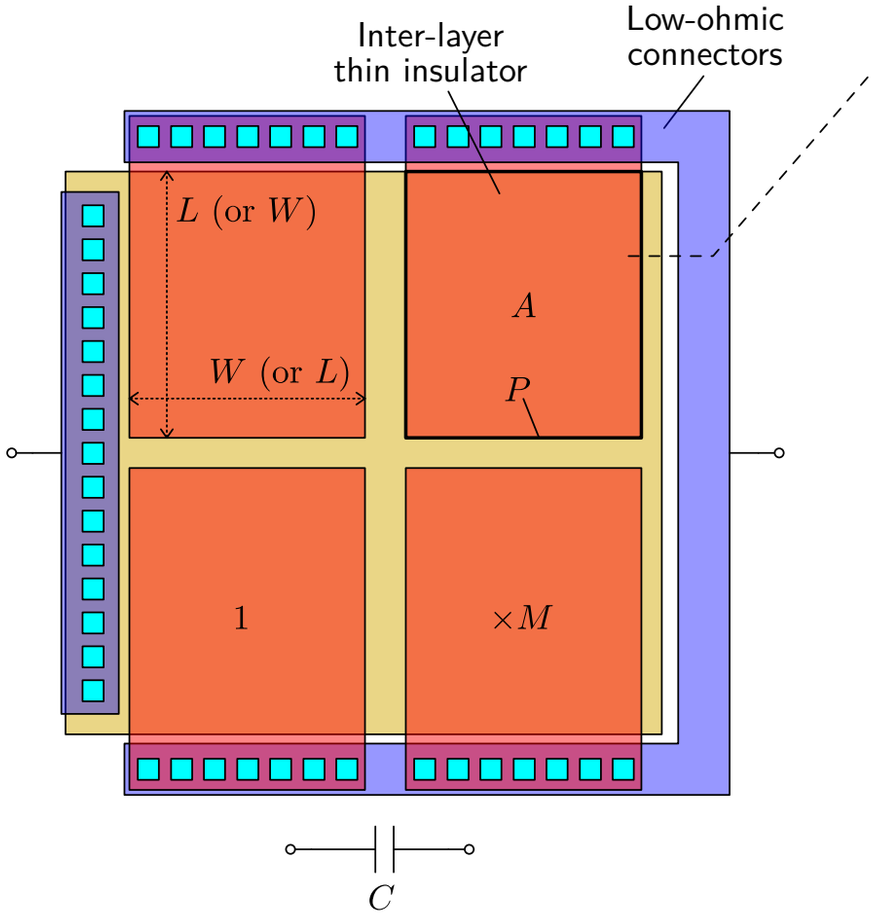


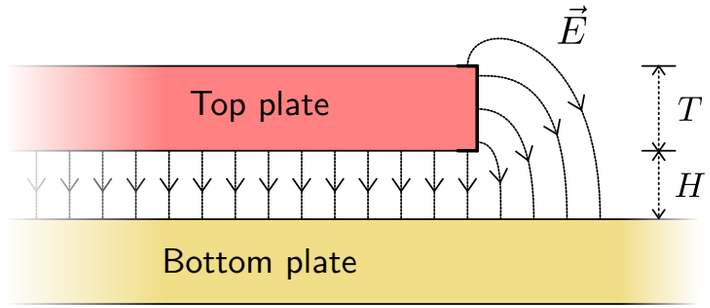


$$I_B = \frac{I_S}{2} = n\beta U_t^2$$

Passive Components

- Coplanar **capacitors**:





Not stretchable!

↗ C.P.Yuan and T.N.Trick
A Simple Formula for the Estimation of the Capacitance of Two-Dimensional Interconnects in VLSI Circuits
IEEE Electron Device Letters, 3(12):391-3, Dec 1982
doi.org/10.1109/EDL.1982.25610

- **Overlap** + **fringing** capacitance:

Electrical permittivity [F/m]

$$C = M\left[\frac{\epsilon}{H}WL + \frac{4\pi\epsilon(W+L)}{\ln\left(1+\frac{2H}{T}+\sqrt{\frac{2H}{T}\left(\frac{2H}{T}+2\right)}\right)}\right]$$

$$C = M\left[C_{ua}A + C_{up}P\right] \qquad \begin{cases} C_{ua}\ [\mathrm{F/m^2}] \\ C_{up}\ [\mathrm{F/m}] \end{cases}$$ Process dependent

- Typ. available **CMOS structures**:

	C_{ua} [fF/μm^2]	Voltage linearity	Temp. indep.
MOS	>1		
PiP or **MiM**	1~10		

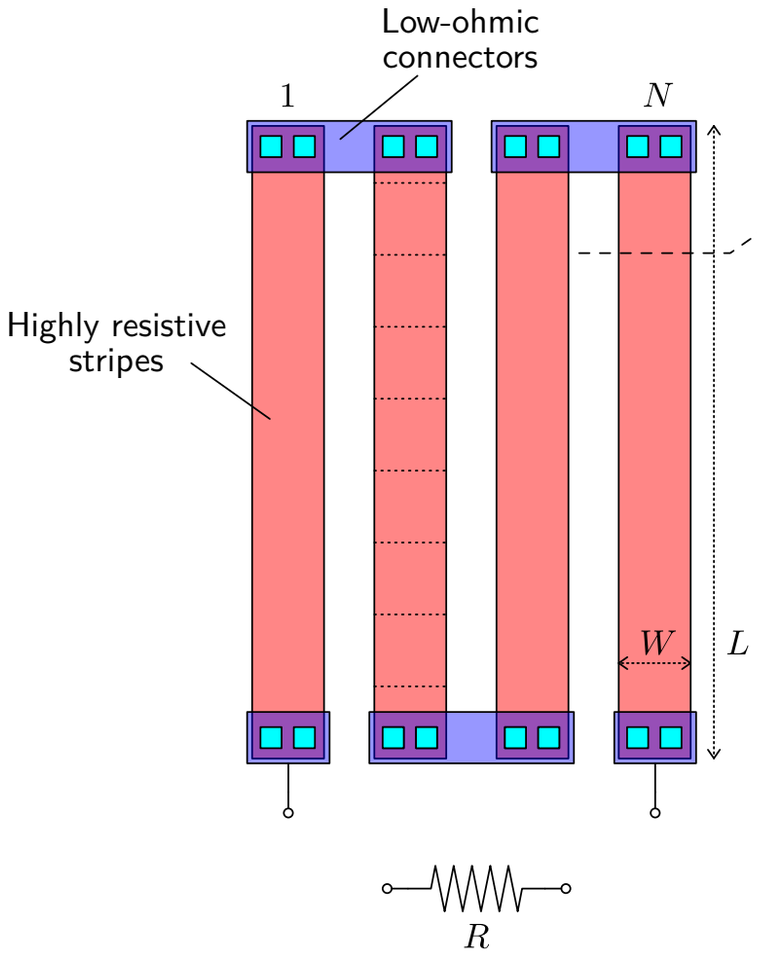
PolySi-insulator-PolySi

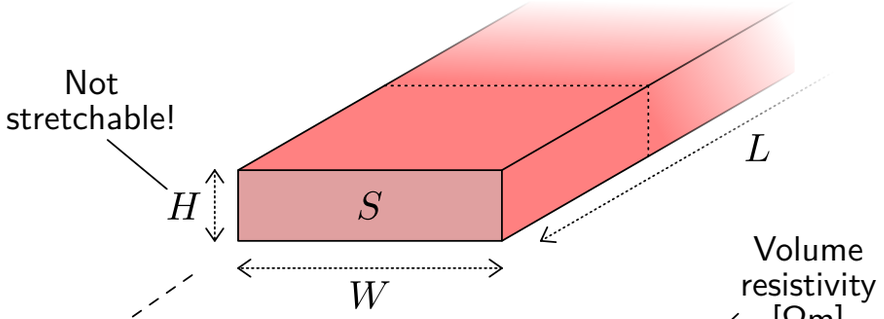
Metal-insulator-Metal

Sandwitch techniques...

Passive Components

- Serpentine **resistors**:





Volume resistivity [Ωm]

$$R = N\frac{L}{S}\rho$$

- **Square** resistance:

$$R_{\square} \doteq \frac{\rho}{H} \quad [\Omega/\square]$$

Process dependent

$$R = N\frac{L}{W}R_{\square}$$

Design aspect ratio

e.g. $\frac{L}{W} = 8.5\square$

- Typ. available **CMOS structures**:

	$R_{\square}$ [Ω/□]	Voltage linearity	Temp. indep.
Well	~1k		
Diffusion	~100		
PolySi	~10		
Metal	~1m		
HiPo	1k~10k		

Highly resistive PolySi

Technological Mismatching

- **Statistical Gaussian** model:

$$\sigma^2(\Delta P) = \underbrace{\frac{A_P^2}{WL}}_{\text{Local}} + \underbrace{B_P^2 D}_{\text{Global}}$$

σ: Standard deviation

A_P: e.g. dopant non-uniformity

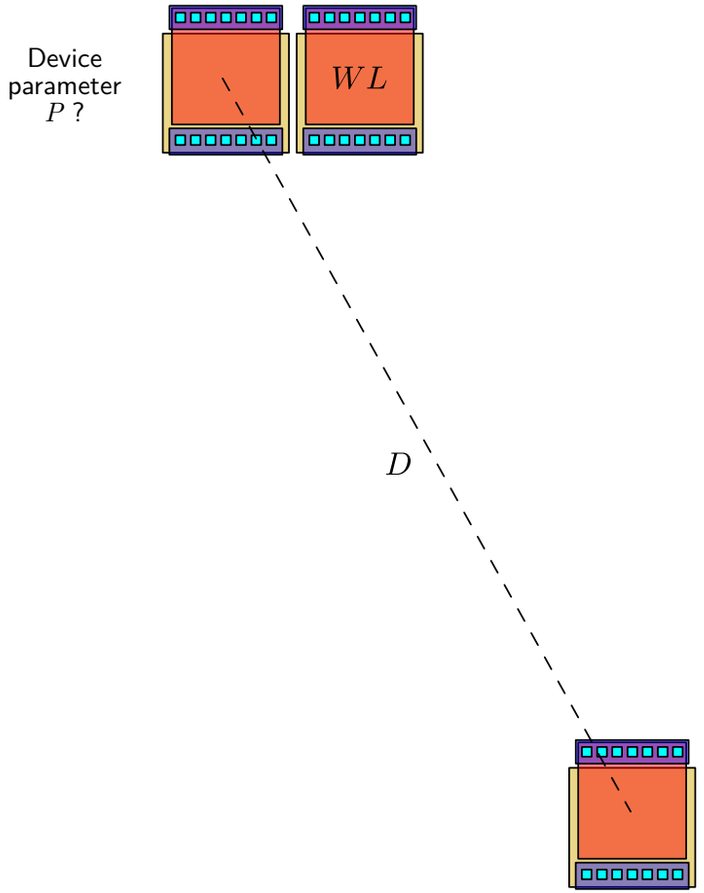
B_P: e.g. thickness gradient

General **Pelgrom Law**

$$\sigma(\Delta P) \simeq \frac{A_P}{\sqrt{WL}}$$

A_P: CMOS process dependent

↗ M.J.M.Pelgrom et al.
Matching Properties of MOS Transistors
IEEE Journal Solid-State Circuits, 24(5):1433-9, Oct 1989
doi.org/10.1109/JSSC.1989.572629



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Standard deviation; e.g. dopant non-uniformity; e.g. thickness gradient

CMOS process dependent

$$\sigma(\Delta P) \simeq \frac{A_P}{\sqrt{WL}}$$

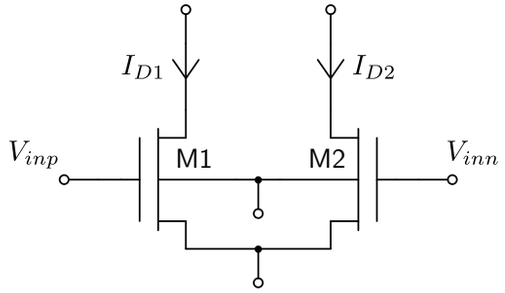
- e.g. MOS **differential pair**:

$$V_{off} \doteq V_{inp} - V_{inn}|_{I_{D1} \equiv I_{D2}}$$

small-signal uncorrelated phenomena

$$\sigma^2(V_{off}) = \sigma^2(\Delta V_{TH}) + \frac{\sigma^2(\Delta\beta)}{g_{mg}^2}$$

$$\sigma(V_{off}) \simeq \sigma(\Delta V_{TH}) \simeq \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$$



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Standard deviation; e.g. dopant non-uniformity; e.g. thickness gradient

$$\sigma(\Delta P) \simeq \frac{A_P}{\sqrt{WL}}$$

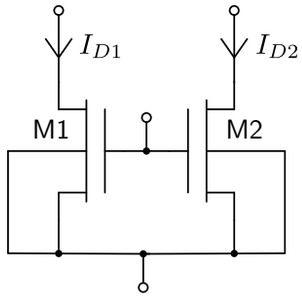
CMOS process dependent

- e.g. MOS **current mirror**:

$$\sigma^2(\Delta I_D) = \sigma^2(\Delta\beta) + g_{mg}^2 \sigma^2(\Delta V_{TH})$$

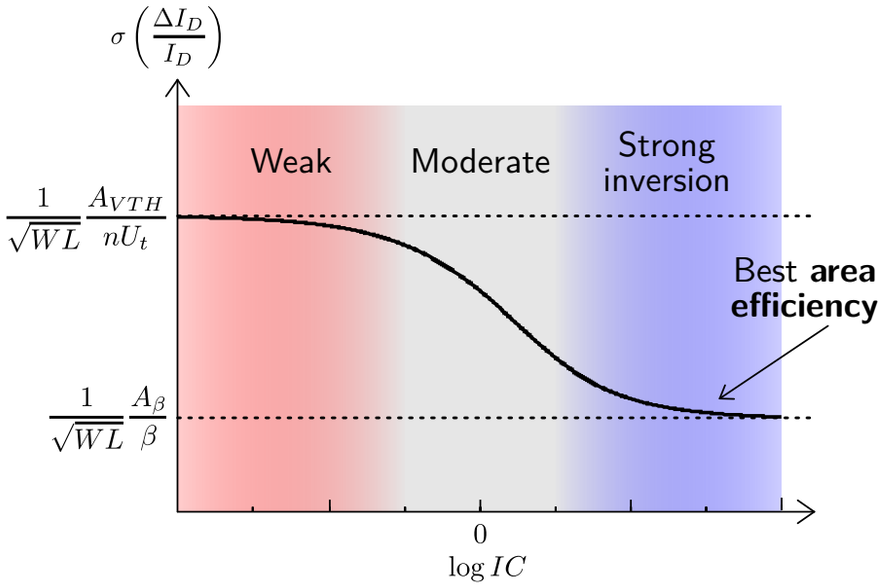
small-signal uncorrelated phenomena

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \frac{1}{WL}\left[\left(\frac{A_\beta}{\beta}\right)^2 + \left(\frac{g_{mg}}{I_D}\right)^2 A_{VTH}^2\right]$$



$$\Delta I_D \doteq I_{D2} - I_{D1}$$

$$I_D \doteq \frac{I_{D1} + I_{D2}}{2}$$

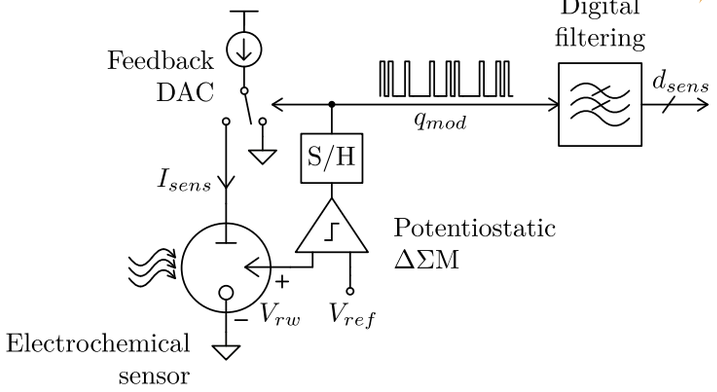


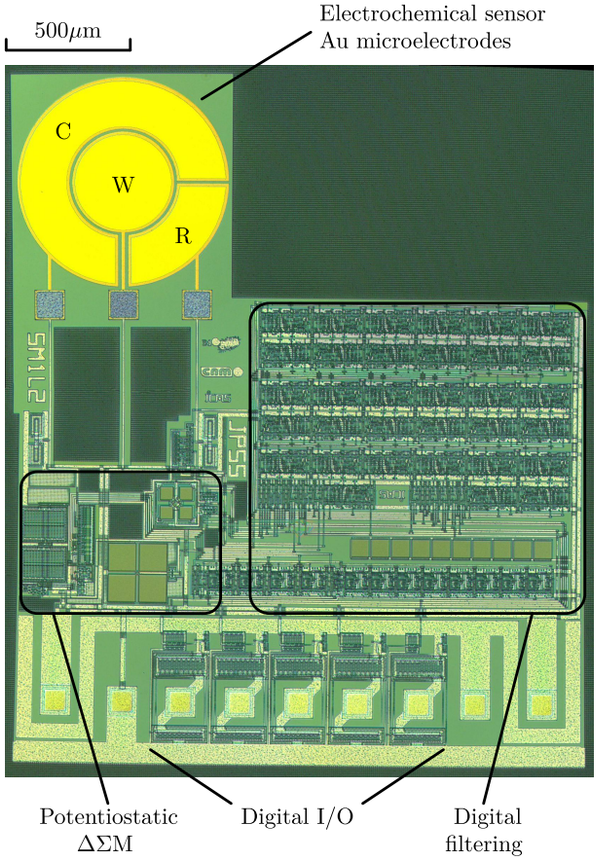
- Typically, $\boldsymbol{V_{TH}}$ mismatch is dominant...

Mixed IC Design

- Must deal with several **hierarchy** and **abstraction** levels

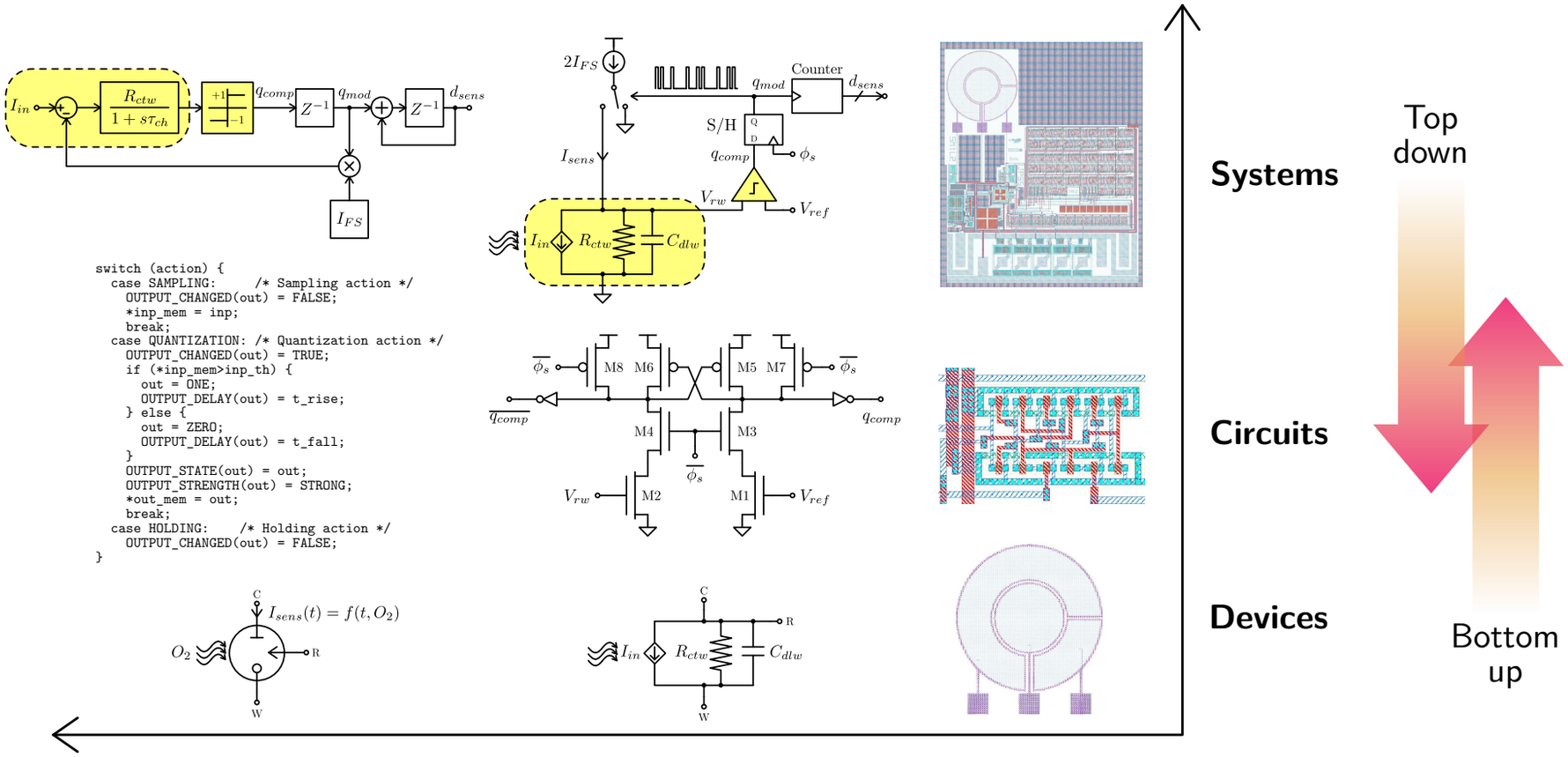
e.g. electrochemical smart sensor





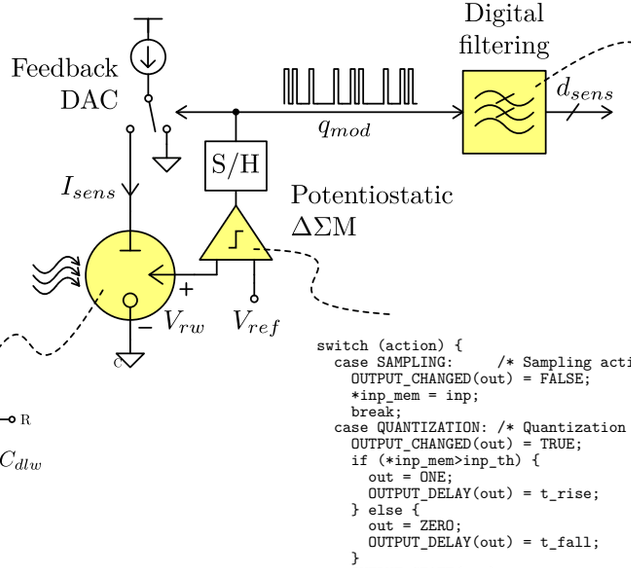
Mixed IC Design

- Must deal with several **hierarchy** and **abstraction** levels

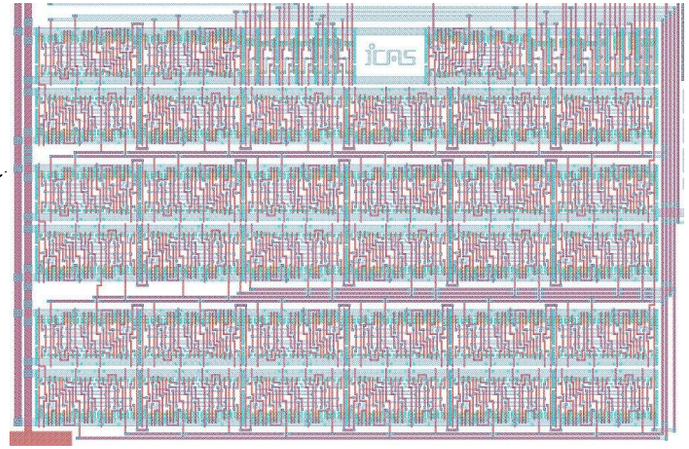


Mixed IC Design

- Must deal with several **hierarchy** and **abstraction** levels
- **Combining** abstraction levels during design



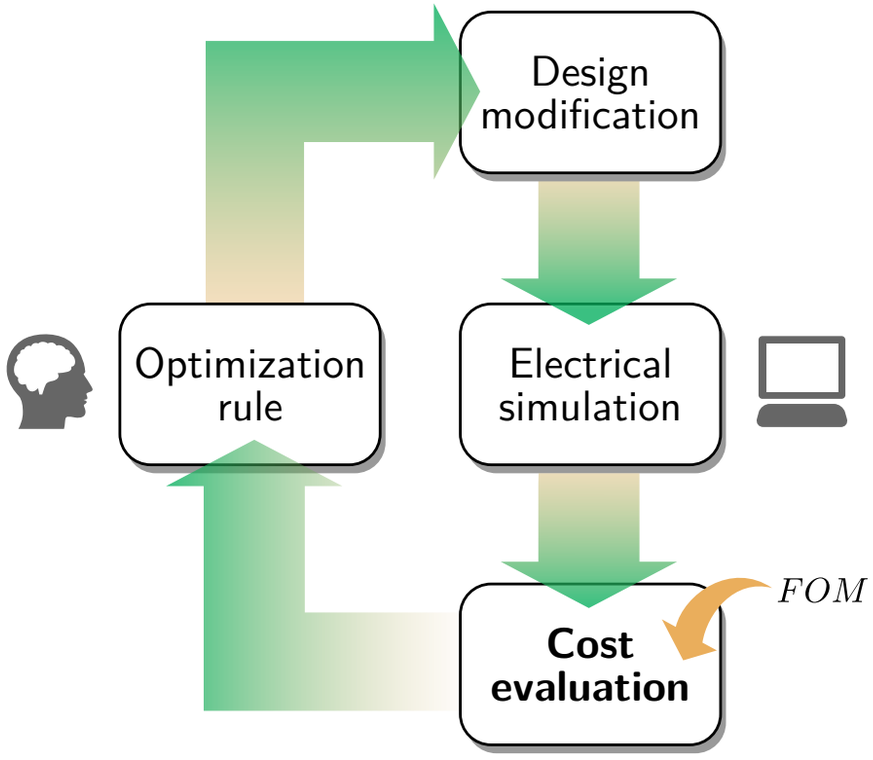

```
switch (action) {
  case SAMPLING:     /* Sampling action */
    OUTPUT_CHANGED(out) = FALSE;
    *inp_mem = inp;
    break;
  case QUANTIZATION: /* Quantization action */
    OUTPUT_CHANGED(out) = TRUE;
    if (*inp_mem>inp_th) {
      out = ONE;
      OUTPUT_DELAY(out) = t_rise;
    } else {
      out = ZERO;
      OUTPUT_DELAY(out) = t_fall;
    }
    OUTPUT_STATE(out) = out;
    OUTPUT_STRENGTH(out) = STRONG;
    *out_mem = out;
    break;
  case HOLDING:    /* Holding action */
    OUTPUT_CHANGED(out) = FALSE;
}
```



- ▲ Simulation **speed up**
- ▲ Study of circuit **non-ideal** effects
- ▼ **Multi-level** and **multi-domain** simulation needed (single engine or glue approach)

IC Optimization

- **Quantitative** design comparison



- **Power** consumption (lifetime, range...)
- Silicon **area** (costs, packaging...)

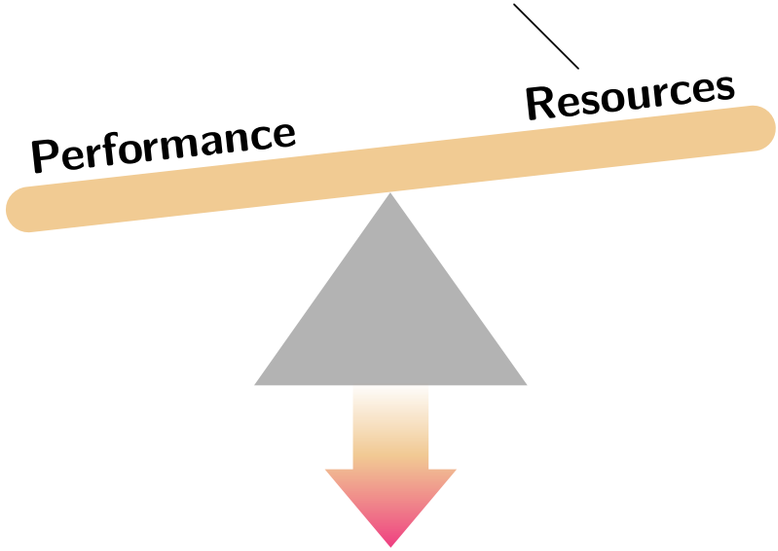
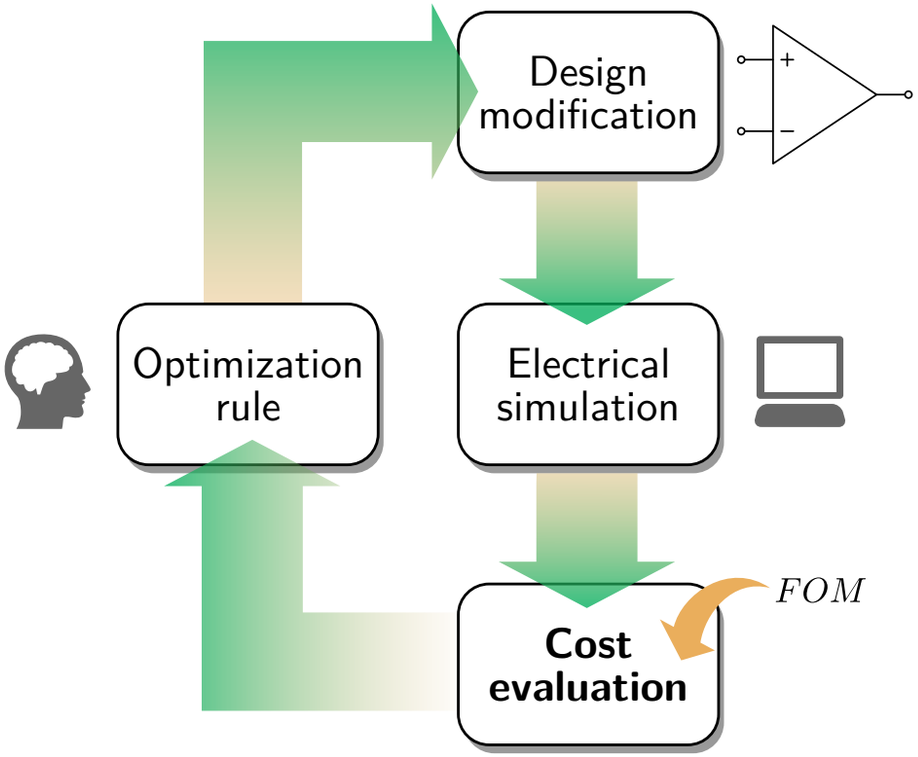


Figure of Merit (**FoM**)

IC Optimization

- **Quantitative** design comparison



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- Silicon **area** (costs, packaging...)

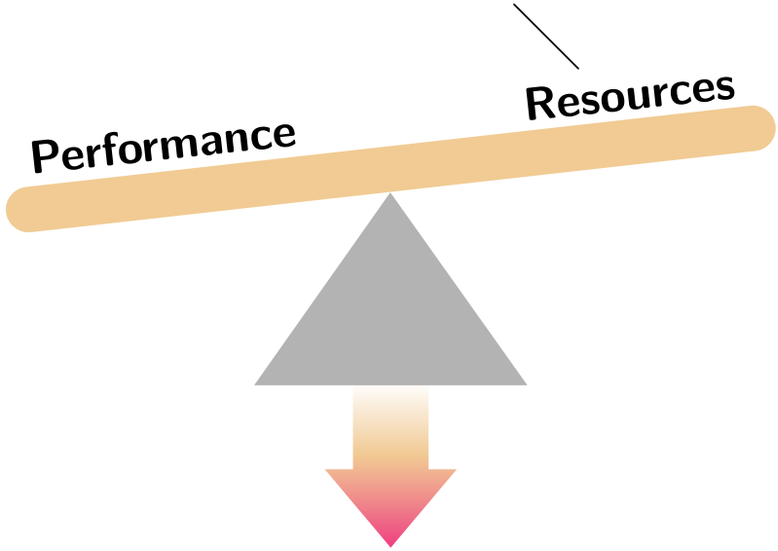


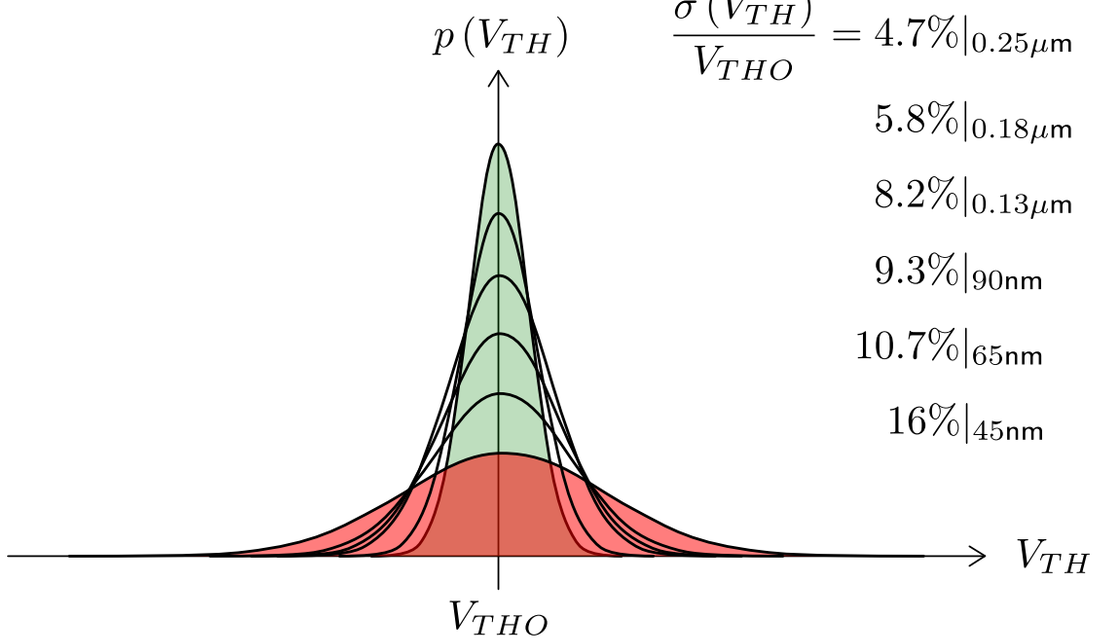
Figure of Merit (**FoM**)

- Circuit **specific**...

$$FOM_{OpAmp} \equiv \begin{cases} \frac{C_{load} SR}{P_D} & \text{e.g. line buffer} \\ \frac{1}{P_D v_{neq}^2 A_{Si}} & \text{e.g. pre-amplifier} \\ \frac{C_{load} GBW}{P_D} & \text{e.g. RF amplifier} \end{cases}$$

Impact of Technology Scaling

- Increase of **process variability** demands robust design techniques



Impact of Technology Scaling

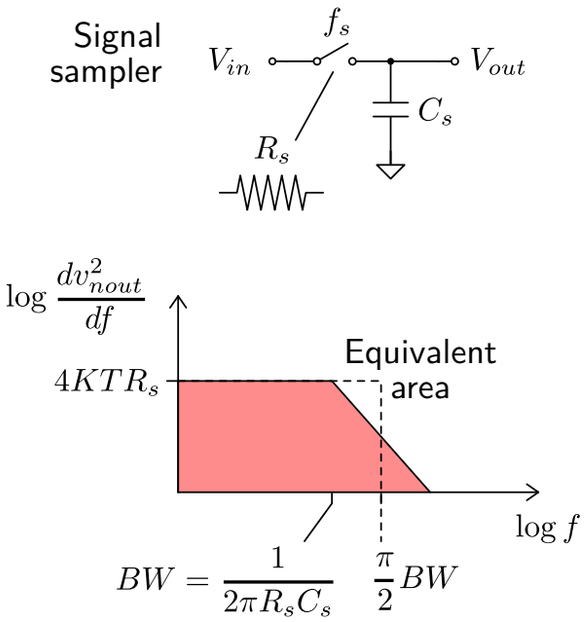
- Increase of **process variability** demands robust design techniques
- **Supply-voltage** downscaling can reduce signal dynamic range or require larger area

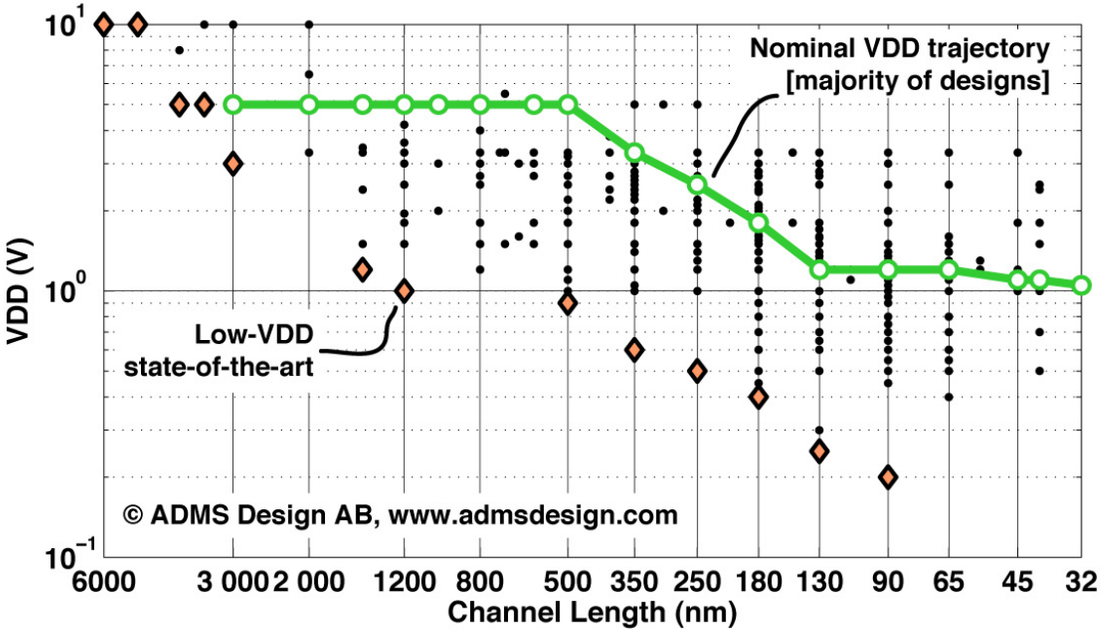
Thermal noise:

$$v_{nout}^2 \equiv \frac{KT}{C_s}$$

Dynamic range:

$$DR \doteq \left(\frac{V_{FS}}{v_{nout}}\right)^2 \propto V_{DD}^2 C_s$$





Impact of Technology Scaling

- Increase of **process variability** demands robust design techniques
- **Supply-voltage** downscaling can reduce signal dynamic range or require larger area
- **Matching** parameters do rule area savings vs circuit precision

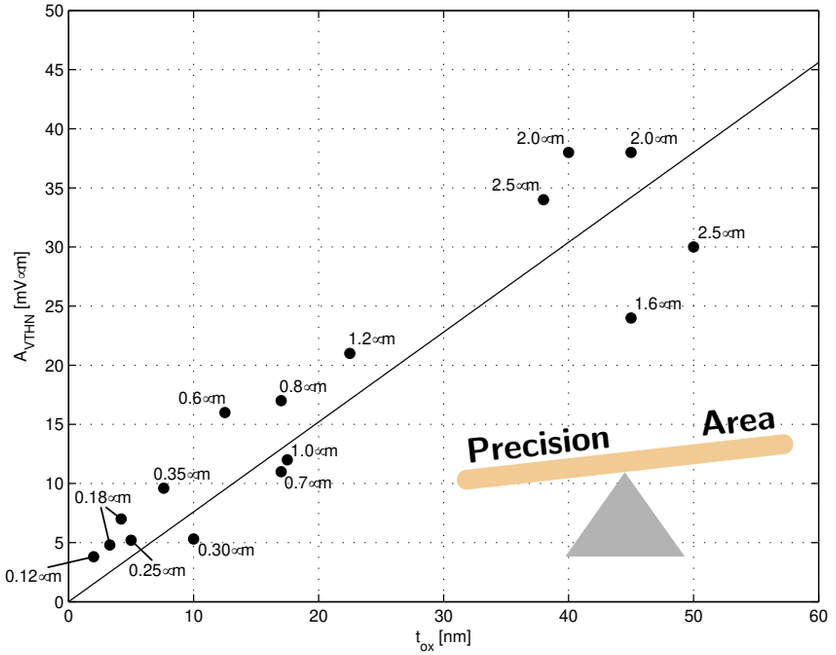
$$\sigma\left(\Delta V_{TH}\right) \simeq \frac{A_{VTH}}{\sqrt{MWL}}$$

$$A_{VTH} = \sqrt{2}\frac{q\sqrt{N_A X_D}}{C_{ox}}$$

Depletion layer

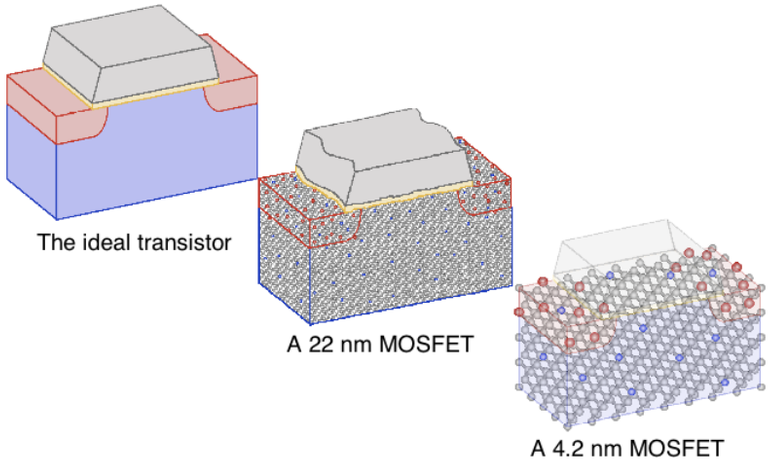
$1/t_{ox}$

Rule of thumb: $A_{VTH} \sim 1\text{mV}\mu\text{m} \times t_{ox}[\text{nm}]$



Impact of Technology Scaling

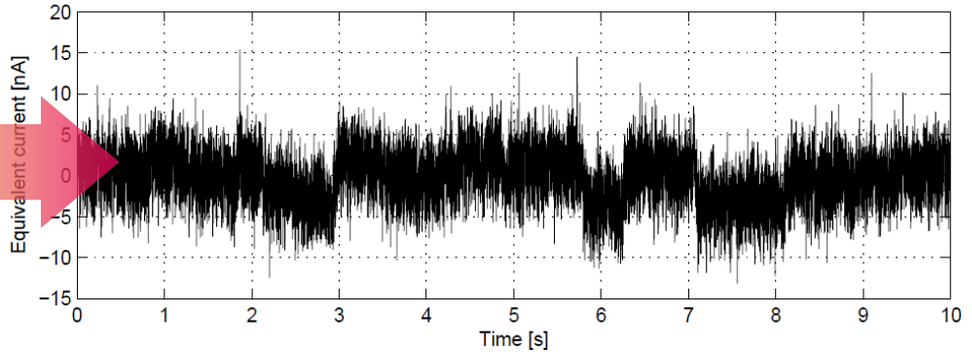
- Increase of **process variability** demands robust design techniques
- **Supply-voltage** downscaling can reduce signal dynamic range or require larger area
- **Matching** parameters do rule area savings vs circuit precision
- **Noise** statistics (time/freq) may be modified at atomic scale



$$\frac{dv_{nfk}^2}{df} = \frac{K_{fk}}{MWL}\frac{1}{f}$$

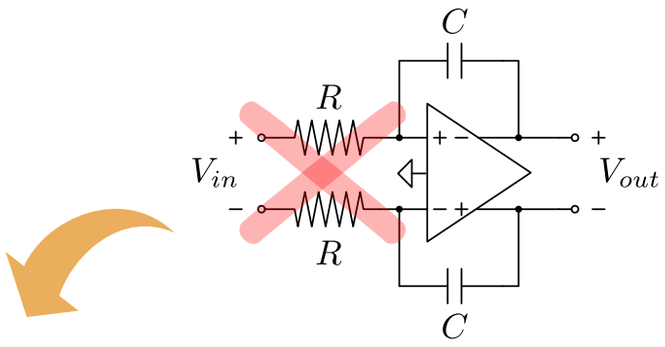
Classic flicker "macro" noise PSD

Actual random telegraph noise (**RTN**) measured in 0.18um

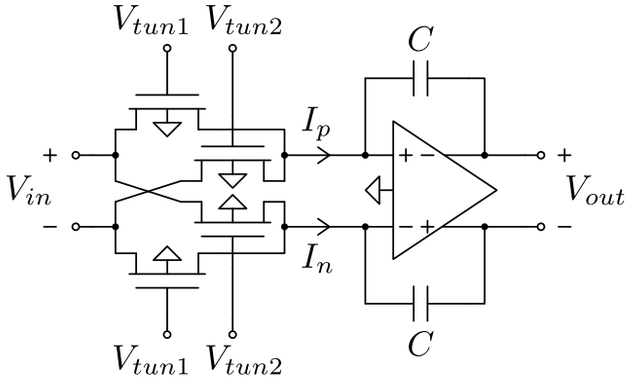


Modern Trends

- **All-MOS** techniques for circuit implementation



e.g. MOS resistive circuit (**MRC**):



- ▲ **Compact** area
- ▲ **Tunable** resistance
- ▼ Technology **sensitivity**
- ▼ Distortion due to worse **mismatching**

supposing matched devices operating in strong inversion and non-saturation:

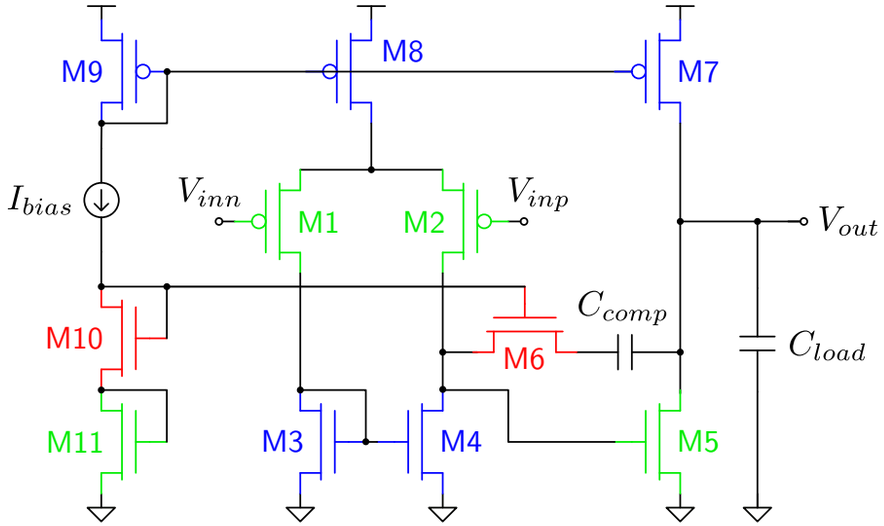
$$I_p = \beta\left[V_{tun1} - V_{TO} - \frac{n}{2}\left(\frac{V_{in}}{2}\right)\right]\left(\frac{V_{in}}{2}\right) + \beta\left[V_{tun2} - V_{TO} - \frac{n}{2}\left(-\frac{V_{in}}{2}\right)\right]\left(-\frac{V_{in}}{2}\right)$$

$$\left.\begin{aligned} I_p &= \beta\left(V_{tun1} - V_{tun2} - n\frac{V_{in}}{2}\right)\frac{V_{in}}{2} \\ I_n &= \beta\left(V_{tun2} - V_{tun1} - n\frac{V_{in}}{2}\right)\frac{V_{in}}{2} \end{aligned}\right\} \quad I_{in} = I_p - I_n = \beta\left(V_{tun1} - V_{tun2}\right)V_{in}$$

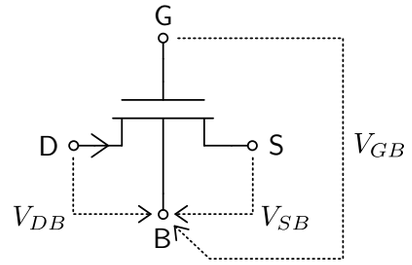
$$R \equiv \frac{1}{\beta\left(V_{tun1} - V_{tun2}\right)}$$

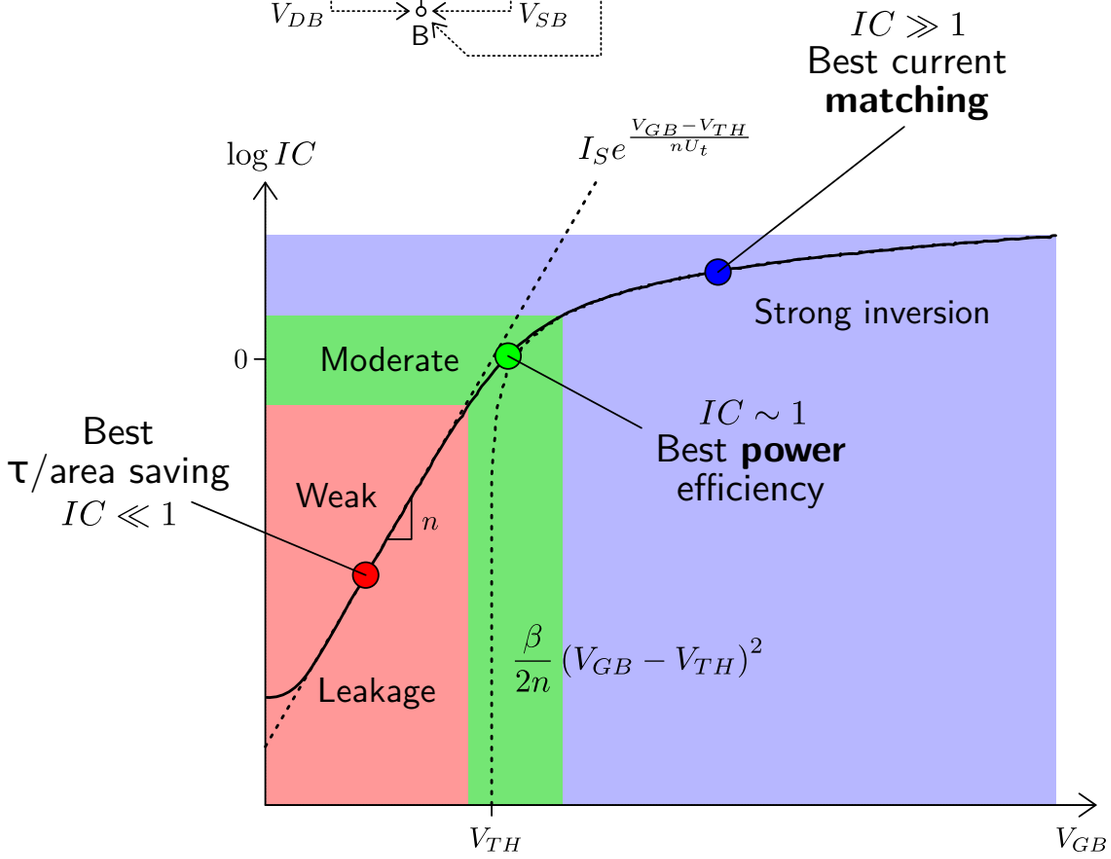
Modern Trends

- **All-MOS** techniques for circuit implementation
- **IC**-based **low-power** circuits
  - Low-**current**
  - Low-**voltage**



$$IC_X = \frac{I_{DX}}{I_{SX}} \propto \frac{I_{bias}}{(W/L)_X}$$



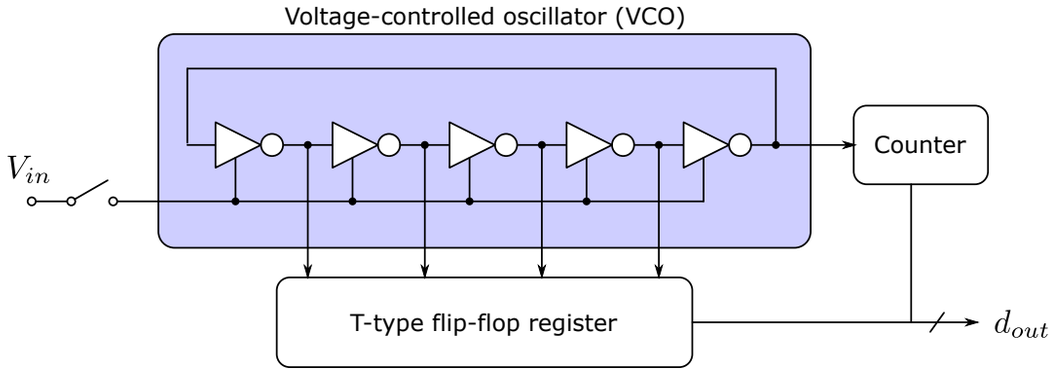


- Simple bias design by **current** and **sizing** selection
- Independent from **technology** if $I_{bias} \propto I_S = 2n\beta U_t^2$

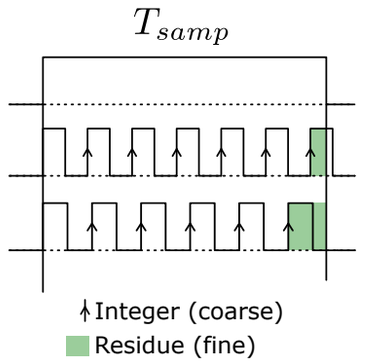
Modern Trends

- **All-MOS** techniques for circuit implementation
- **IC**-based **low-power** circuits
  - Low-**current**
  - Low-**voltage**
- **Time/frequency** domain processing

e.g. **all-digital** flash ADC:



- ▲ Benefit of **high-speed** CMOS technologies
- ▼ **Non-linearity**
- ▼ Technology **sensitivity**



Modern Trends

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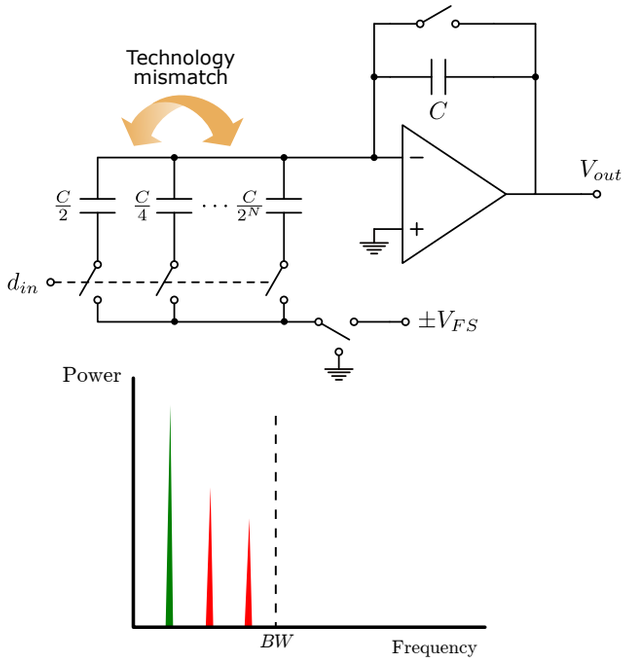
- **IC**-based **low-power** circuits
  - Low-**current**
  - Low-**voltage**
- **Time/frequency** domain processing
- **Digitally assisted** analog minimalist

e.g. dynamic element matching (**DEM**) in SC flash DAC:



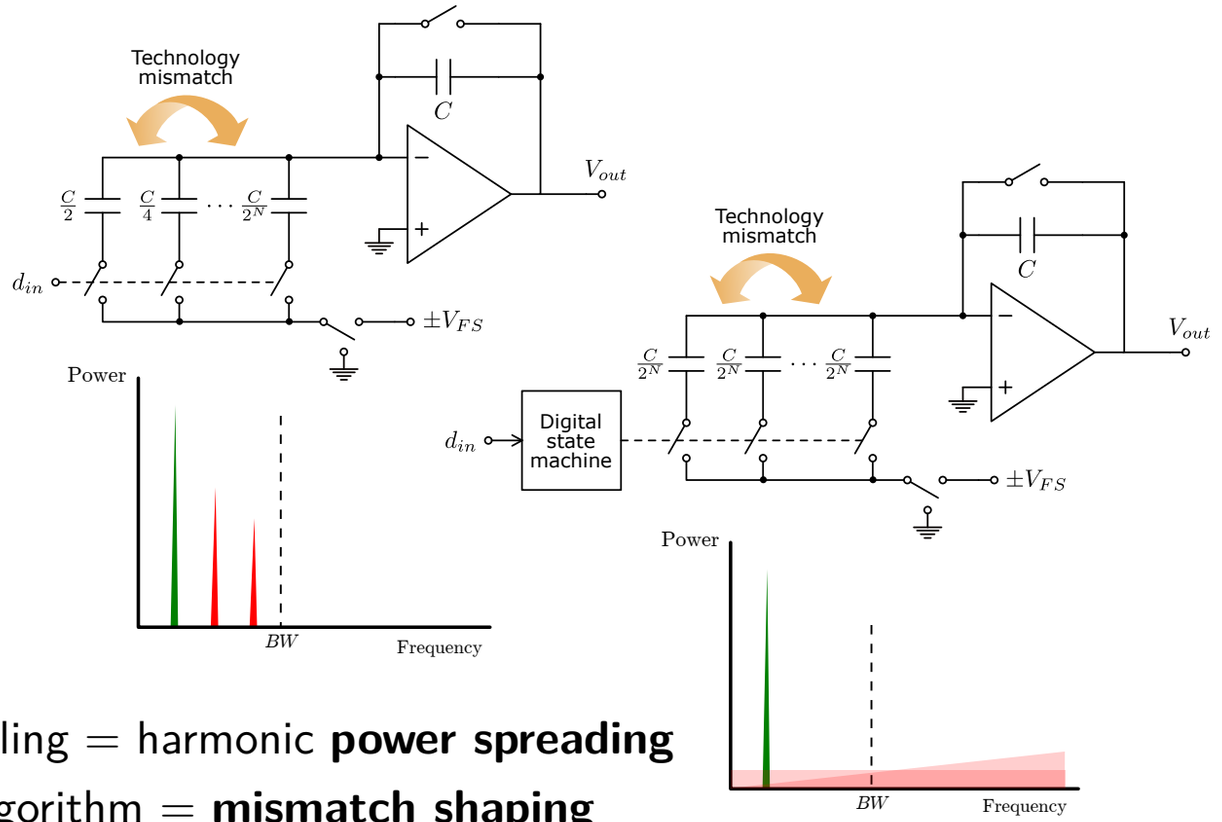
- Capacitor mismatching = binary weight non-linearity = **harmonic distortion**
- Increase of **circuit area** according to **Pelgrom's Law**

$$\sigma\left(\frac{\Delta C}{C}\right) \propto \frac{1}{\sqrt{WL}}$$

Modern Trends

- **All-MOS** techniques for circuit implementation
- **IC**-based **low-power** circuits
  - Low-**current**
  - Low-**voltage**
- **Time/frequency** domain processing
- **Digitally assisted** analog minimalist

e.g. dynamic element matching (**DEM**) in SC flash DAC:

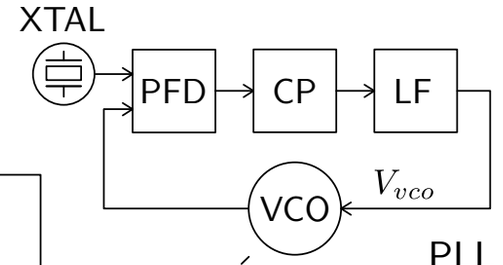


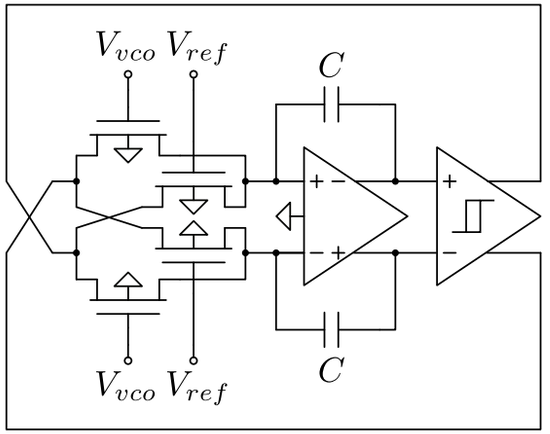
- ▲ Thermometric scrambling = harmonic **power spreading**
- ▲ Frequency selective algorithm = **mismatch shaping**
- ▲ **Dynamic range** improvement (or **silicon area** saving)

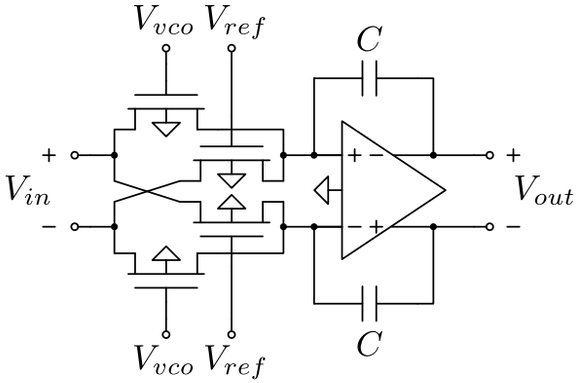
Modern Trends

- **All-MOS** techniques for circuit implementation
- **IC**-based **low-power** circuits
  - Low-**current**
  - Low-**voltage**
- **Time/frequency** domain processing
- **Digitally assisted** analog minimalist
- **Technology independent** tuning strategies

e.g. **master-slave** tuning strategy:







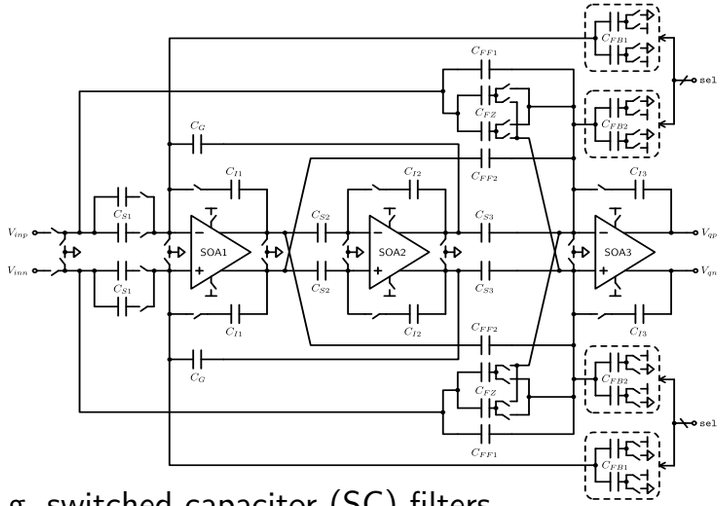
$$\tau \equiv \frac{C}{\beta\,(V_{vco} - V_{ref})}$$

▲ **PVT** (process, supply voltage, temperature) compensation

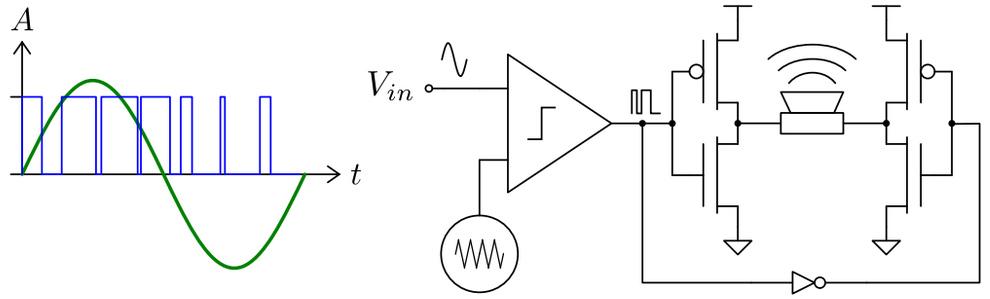
▼ **Area** and **power** overheads

Signal Domains

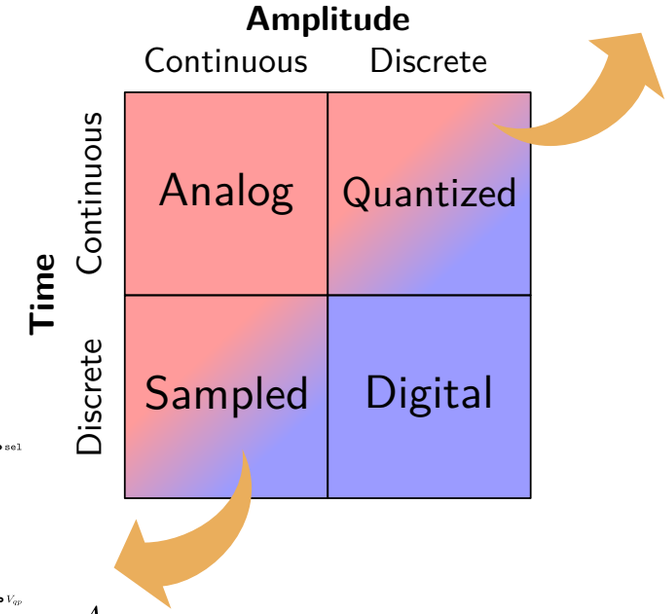
- **Analog** is related with external world, like:
  - Sensor read-out
  - Wireless RF signal
- **Digital** is common inside electronic systems, like:
  - Computation
  - Stored memory

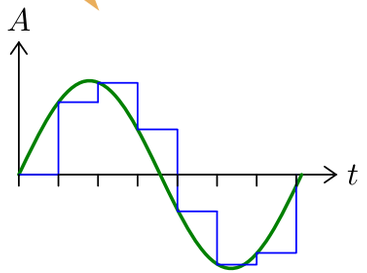


e.g. switched-capacitor (SC) filters



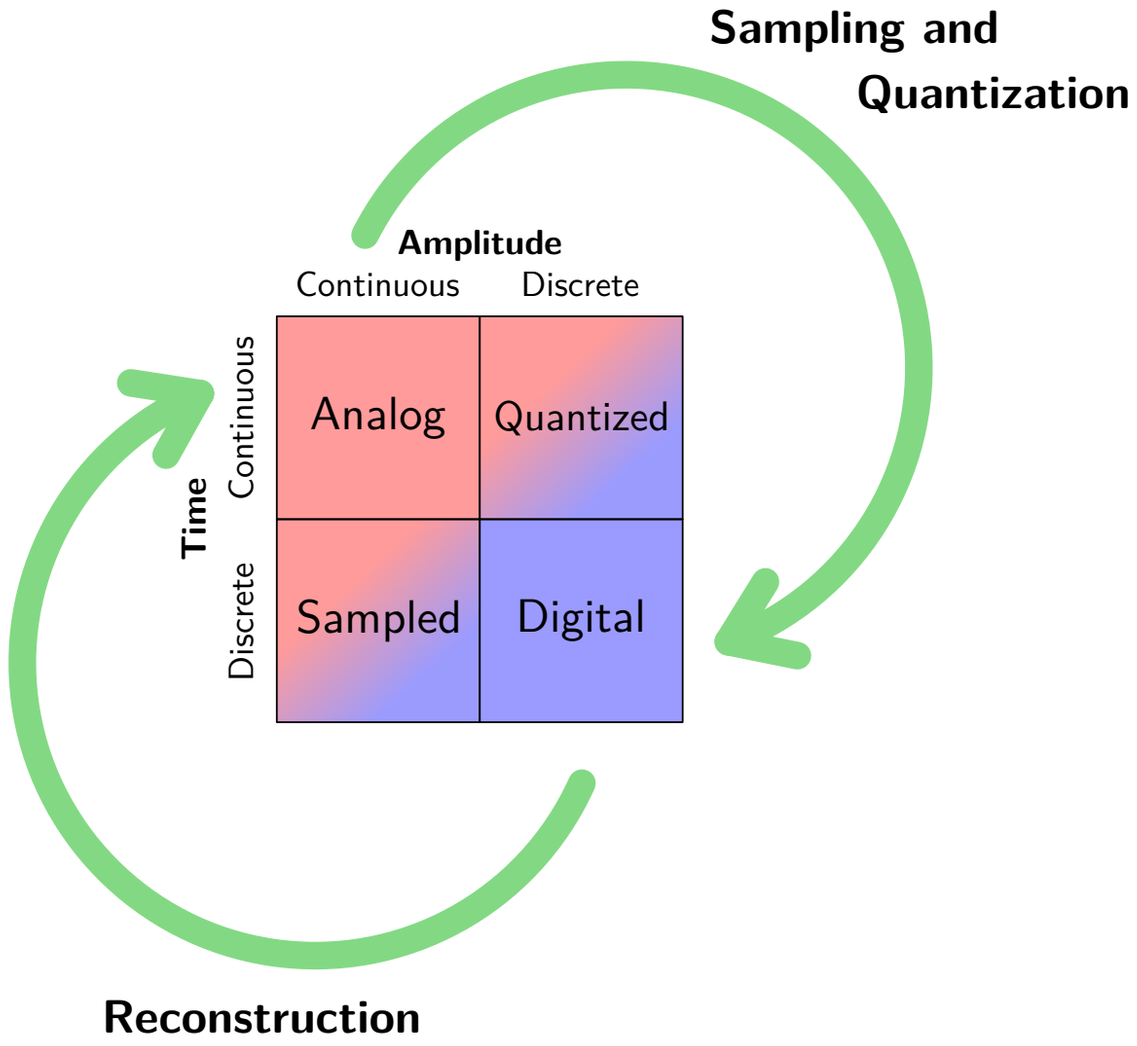
e.g. pulse-width modulation (PWM) in Class-D audio amplifiers





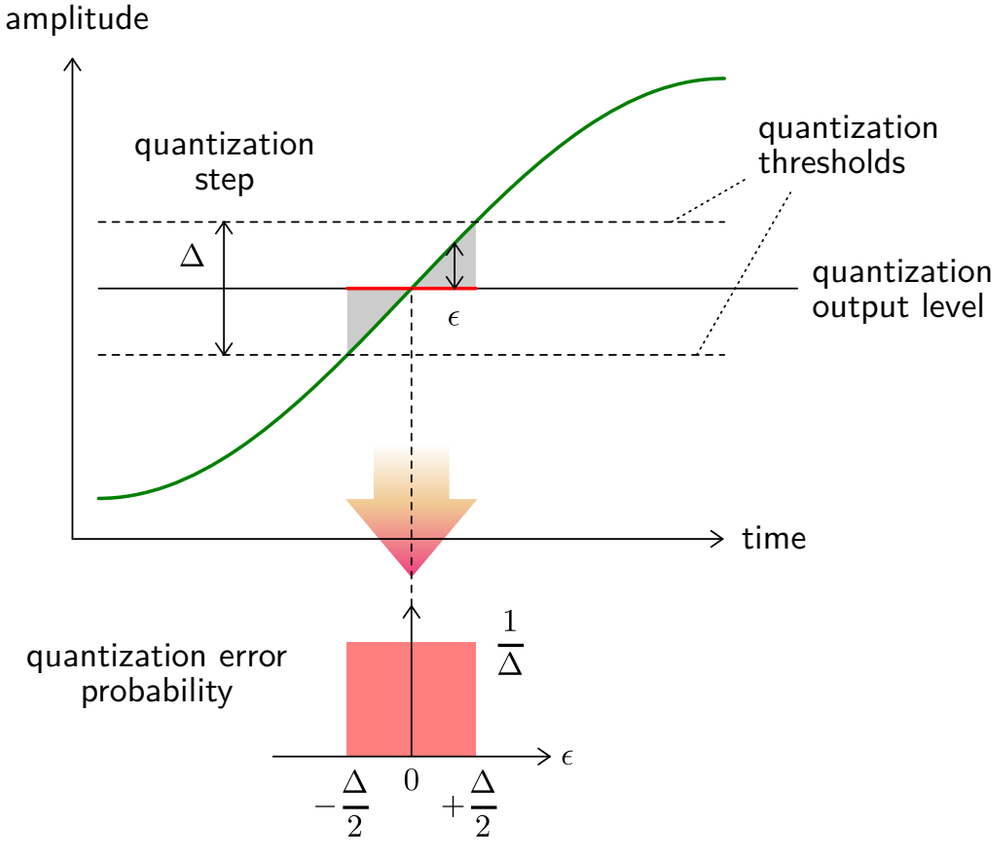
Signal Domains

- **Analog** is related with external world, like:
  - Sensor read-out
  - Wireless RF signal
- **Digital** is common inside electronic systems, like:
  - Computation
  - Stored memory
- **Intermediate** domains present in A/D and D/A interfaces
- Always finite **dynamic range** and **bandwidth**!



Quantization

- Intrinsic error called **quantization noise**
- **Uniform** distribution probability
- Signal **uncorrelated**



estimated power:

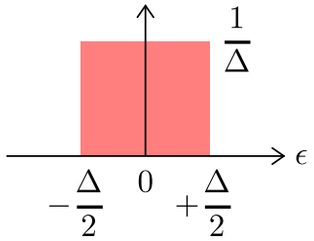
$$QN = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} \epsilon^2 d\epsilon = \frac{1}{\Delta}\frac{\epsilon^3}{3}\Big|_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} = \frac{\Delta^2}{12} \quad \text{[rms]}$$

independent from sampling frequency

Quantization

- Intrinsic error called **quantization noise**
- **Uniform** distribution probability
- Signal **uncorrelated**
- ***N*-bit** quantization (2^N-1 decision levels)
- **Harmonic** signal full-scale occupancy

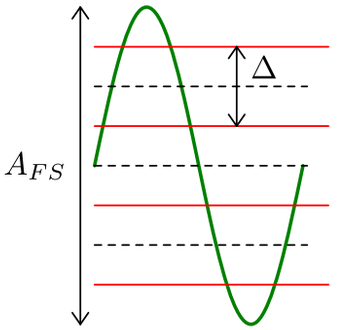
quantization error probability



estimated power:

$$QN = \frac{\Delta^2}{12} \quad \text{[rms]}$$

$$A_{FS} = 2^N \Delta \quad \text{[peak-to-peak]}$$

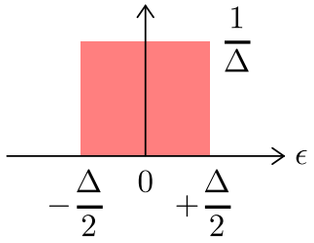


$(2^N - 1)$ thresholds

Quantization

- Intrinsic error called **quantization noise**
- **Uniform** distribution probability
- Signal **uncorrelated**
- ***N*-bit** quantization (2^N-1 decision levels)
- **Harmonic** signal full-scale occupancy
- Signal-to-quantization-noise **ratio**

quantization error probability



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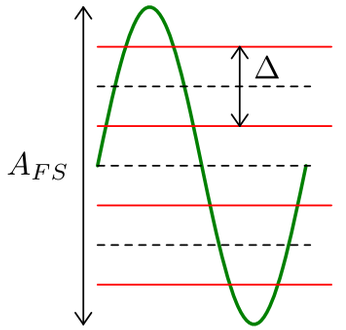

$(2^N - 1)$ thresholds

harmonic analysis:

$$S_{max} = \left(\frac{A_{FS}}{2\sqrt{2}}\right)^2 \quad \text{[rms]}$$

$$SQNR_{max} \doteq \frac{S_{max}}{QN} = \left(2^N \sqrt{1.5}\right)^2$$

$$SQNR_{max} = 6.02N + 1.76 \quad \text{[dB]}$$

± 1bit $\equiv \pm 6$dB

Quantization

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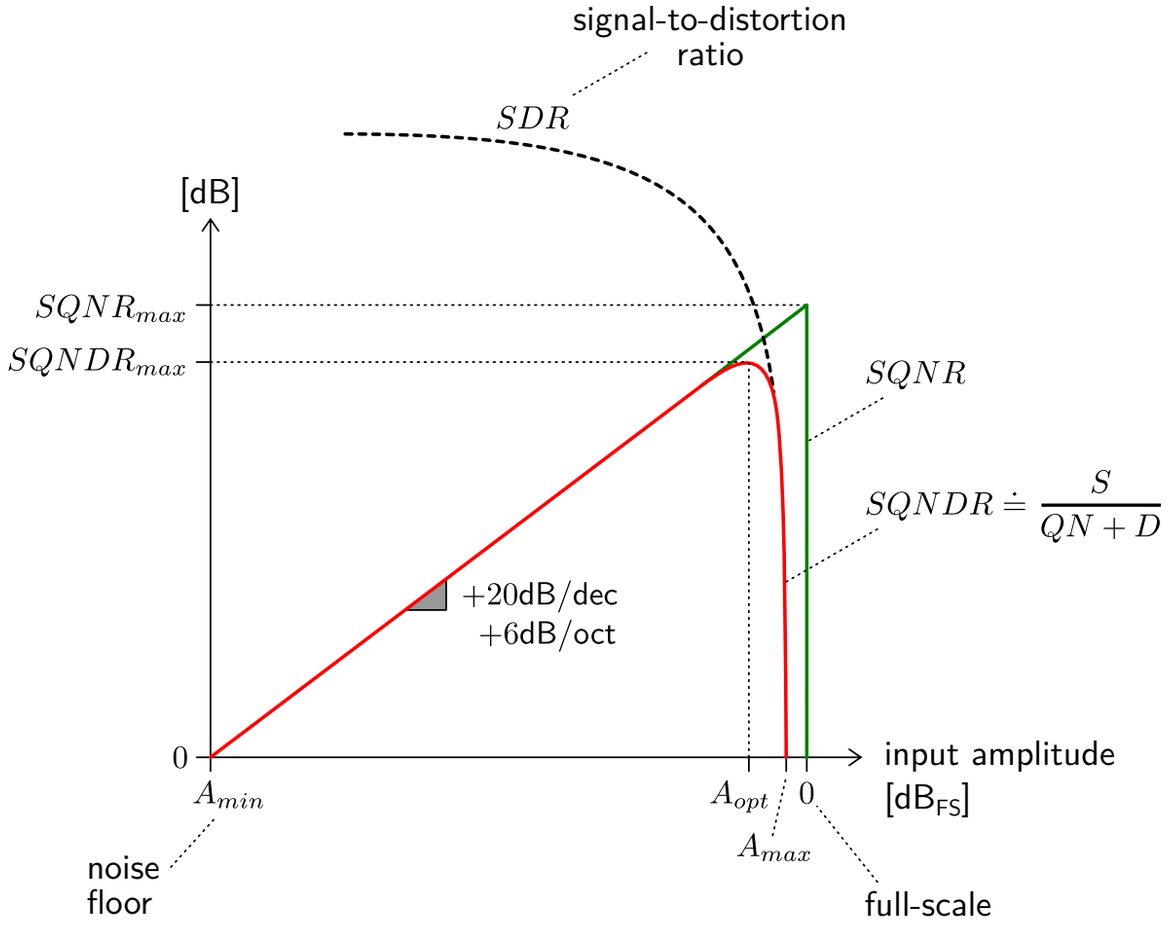
- **Harmonic** signal full-scale occupancy
- Signal-to-quantization-noise **ratio**
- **Dynamic range** considerations



$$DR \doteq 20 \log \frac{A_{max}}{A_{min}} \text{ [dB]} \quad \leq \quad SQNR_{max}$$

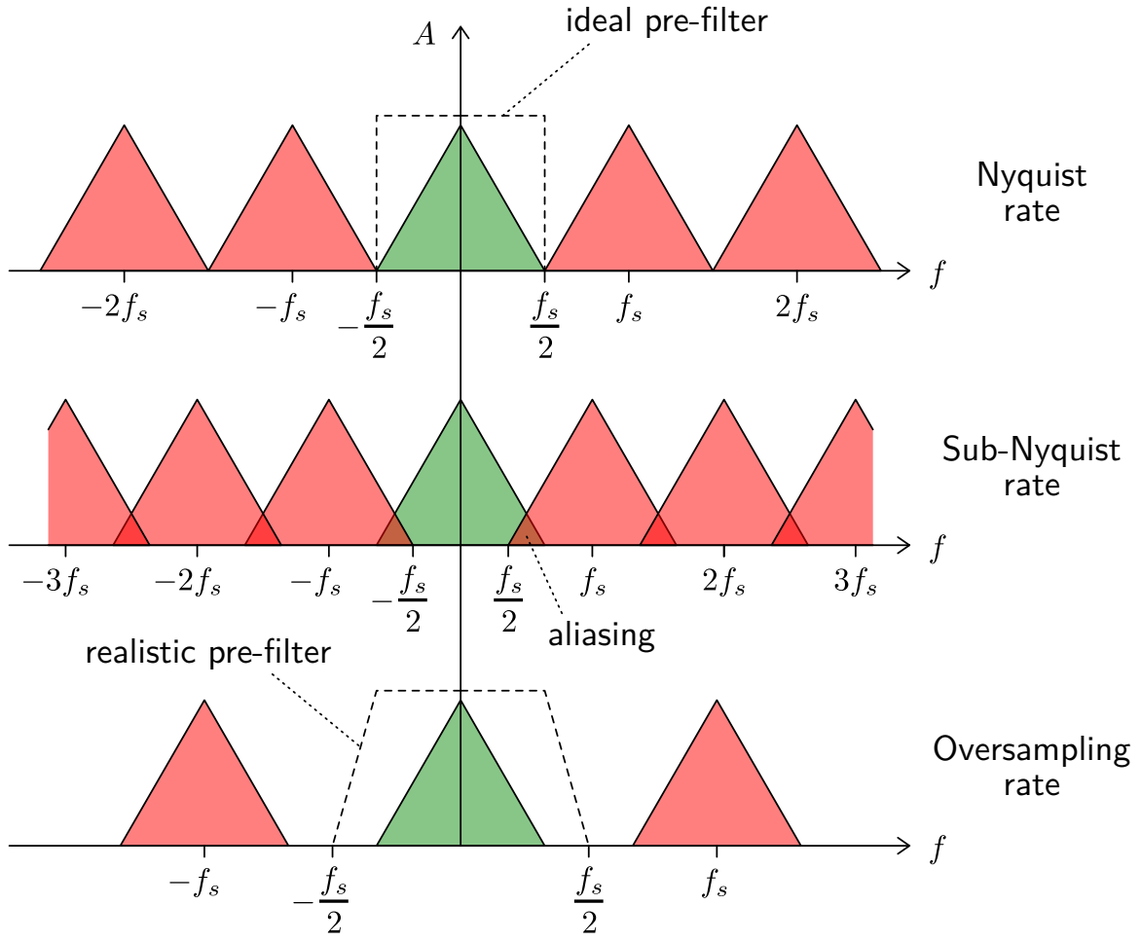
Only when **no distortion** is considered: $DR \equiv SQNR_{max}$

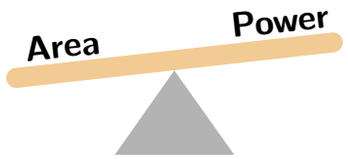
Sampling

- **Nyquist** rate

$$f_{nyq} = 2BW$$

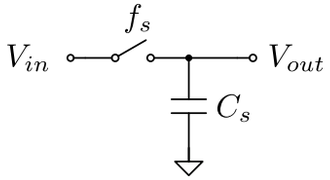
- Sub-Nyquist rate generates **aliasing**
  - Signal distortion
  - **Noise folding**
- Oversampling relaxes **pre-filter** sharpness and stop-band attenuation
- ▲ More **compact circuits**
- ▼ Higher **clock frequencies**

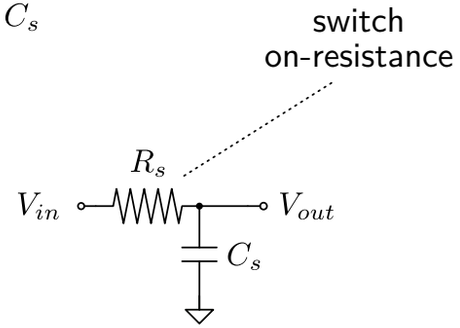




Sampling

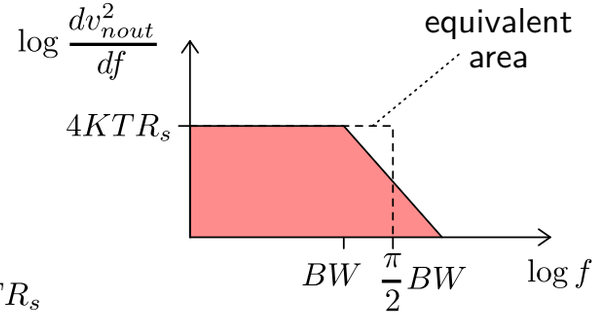
- Switched capacitor **sampler** model
- **Thermal noise** equivalent circuit





$$\frac{dv_{nin}^2}{df} = 4KTR_s$$

$$BW = \frac{1}{2\pi R_s C_s}$$



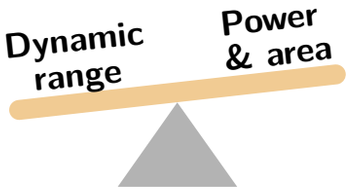
$$v_{nout}^2 = \frac{\pi}{2}\frac{1}{2\pi R_s C_s}4KTR_s$$

$$v_{nout}^2 \equiv \frac{KT}{C_s}$$

$$DR \propto \frac{1}{v_{nout}^2} \propto C_s$$

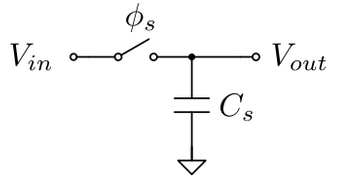
+3dB/oct
+0.5bit/oct

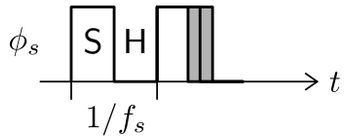
- Capacitance only driven design (**KT/C**)
- Large **passive** devices
- Low **impedance** loads



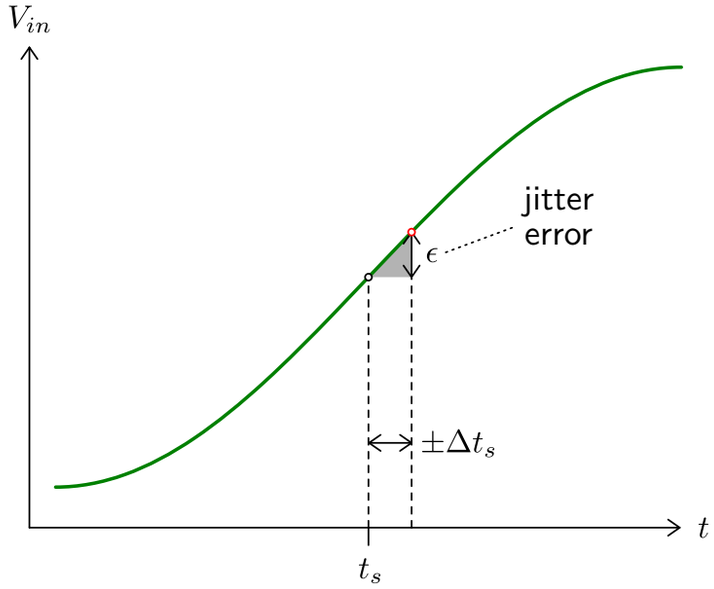
Sampling

- Switched capacitor **sampler** model
- **Clock jitter** causes amplitude errors
- **Harmonic** analysis

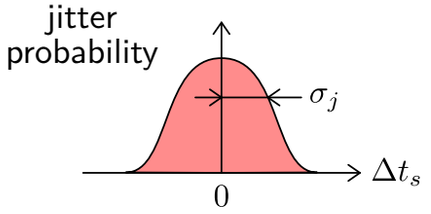




$$\epsilon \simeq \frac{dV_{in}}{dt}\Delta t_s$$



$$V_{in} = \frac{A_{FS}}{2}\sin(2\pi BWt) \qquad \epsilon = A_{FS}\pi BW\cos(2\pi BWt)\Delta t_s$$



estimated power:

$$JN = (\sigma_j A_{FS}\pi BW)^2\left[2BW\int_0^{\frac{1}{2BW}}\cos^2(2\pi BWt)dt\right] = \frac{1}{2}(\sigma_j A_{FS}\pi BW)^2$$

$$\int_0^{\pi}\cos^2(x)dx = \frac{\pi}{2}$$

Sampling

- Switched capacitor **sampler** model
- **Clock jitter** causes amplitude errors
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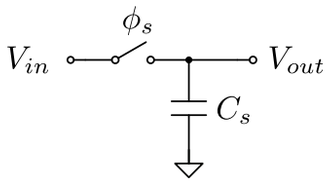


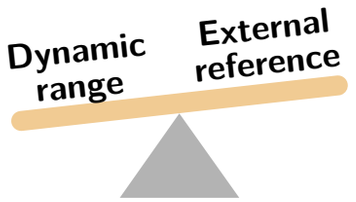
$$JN = \frac{1}{2}(\sigma_j A_{FS} \pi BW)^2$$

- ▲ Negligible for **low frequency**
- ▼ **High accuracy** clock generator

if jitter effect is **dominant**:

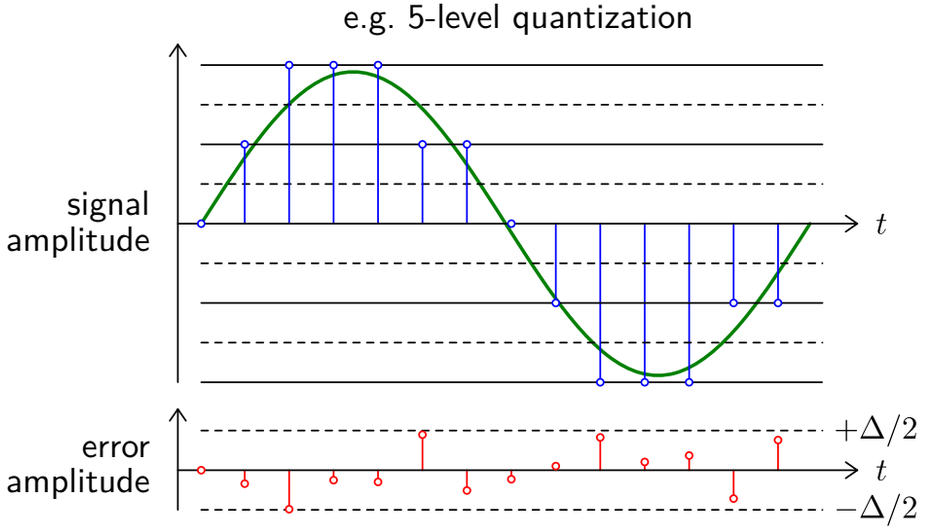
$$SJNR_{max} = 2\left(\frac{A_{FS}/2\sqrt{2}}{\sigma_j A_{FS} \pi BW}\right)^2 = \frac{1}{(2\sigma_j \pi BW)^2}$$

-6dB/oct
-1bit/oct



Sampling and Quantization

- Constant (**white**) error spectrum profile



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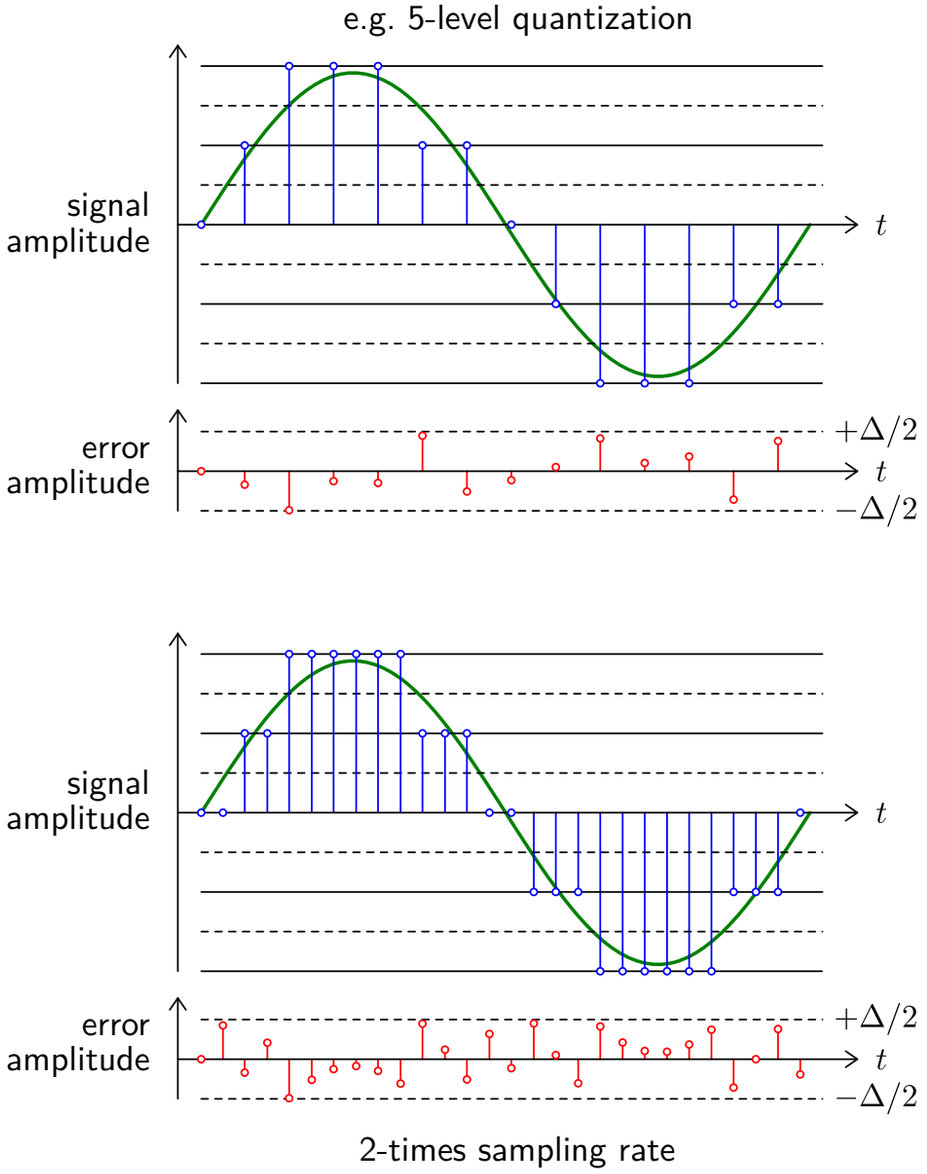
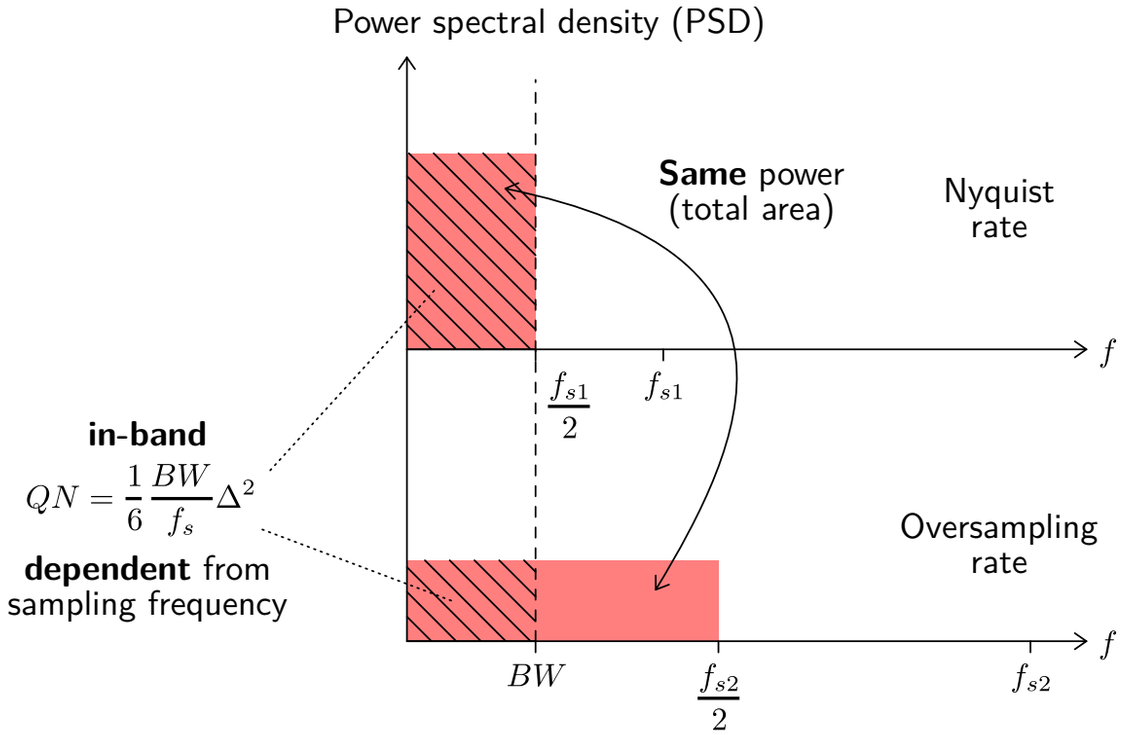


Sampling and Quantization

- Constant (**white**) error spectrum profile

$$QN(f) = \frac{\Delta^2/12}{f_s/2} = \frac{1}{6}\frac{\Delta^2}{f_s} \quad \text{[W/Hz]}$$

- **Spread** across spectrum (fs/2)



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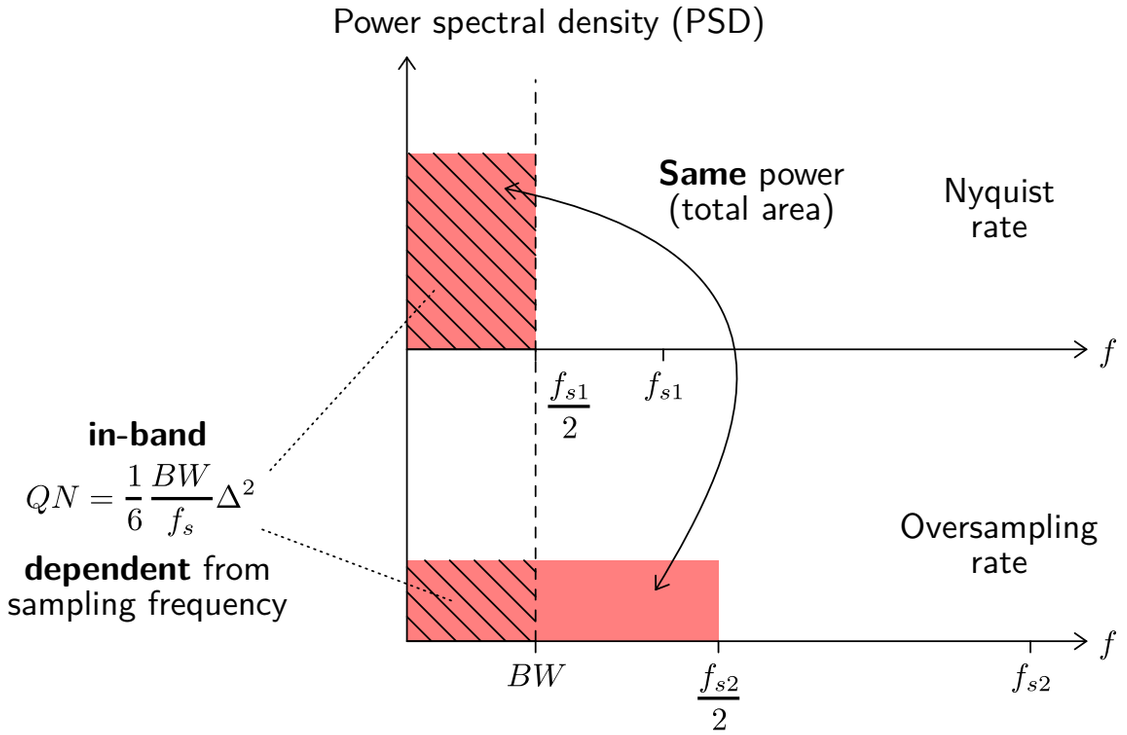
- **Spread** across spectrum (fs/2)
- **Oversampling** ratio

$$OSR \doteq \frac{f_s}{f_{nyq}} \equiv \frac{f_s}{2BW}$$



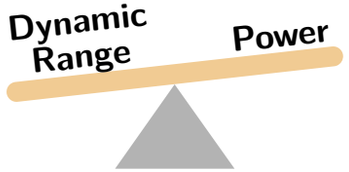
$$QN = \frac{\Delta^2}{12}\frac{1}{OSR} \qquad SQNR_{max} = \left(2^N\sqrt{1.5}\right)^2 OSR$$

▲ Lower **in-band noise**

▼ Higher **clock frequencies**

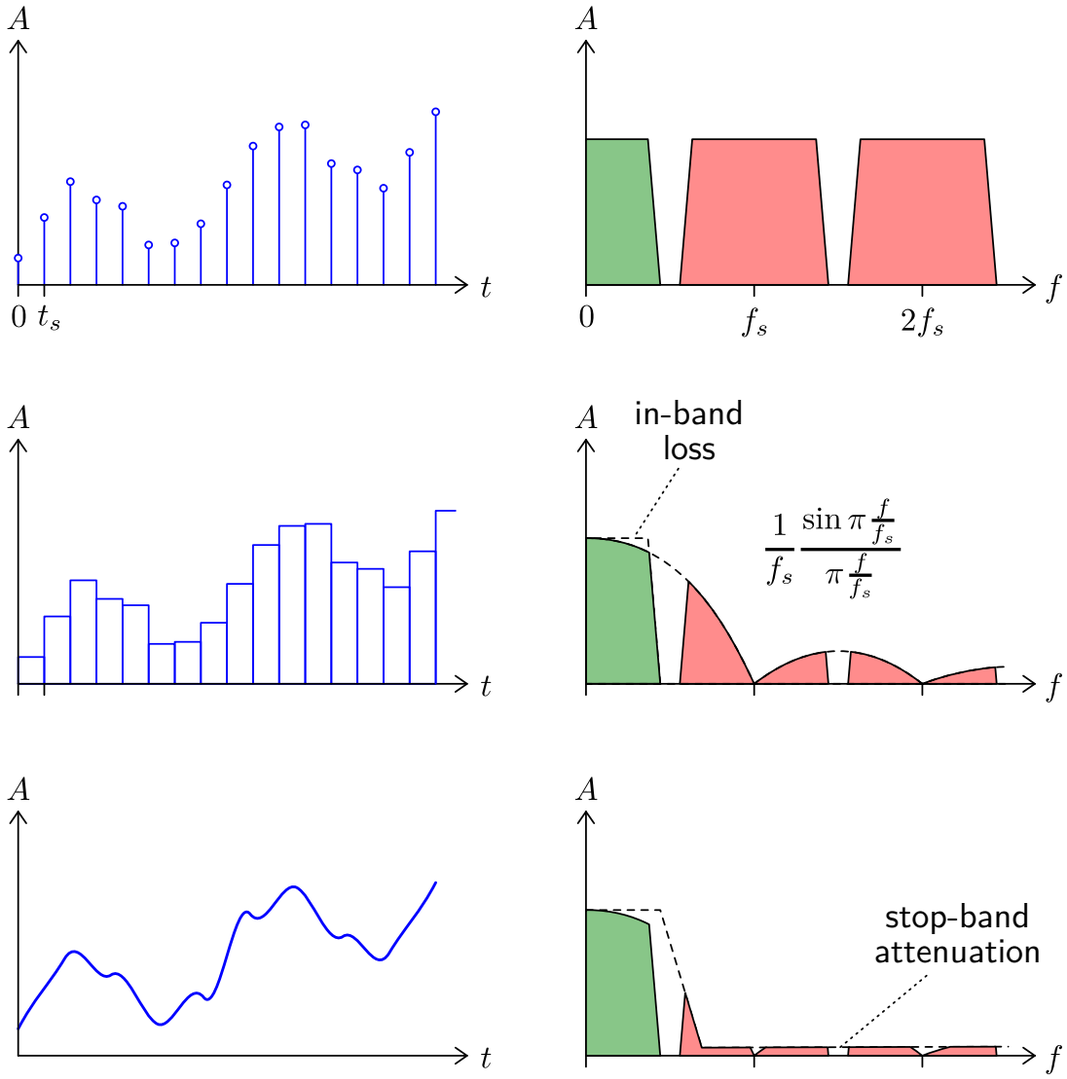
$$SQNR_{max} = 6.02N + 1.76 + 10\log OSR \quad \text{[dB]}$$

+3dB/oct
+0.5bit/oct



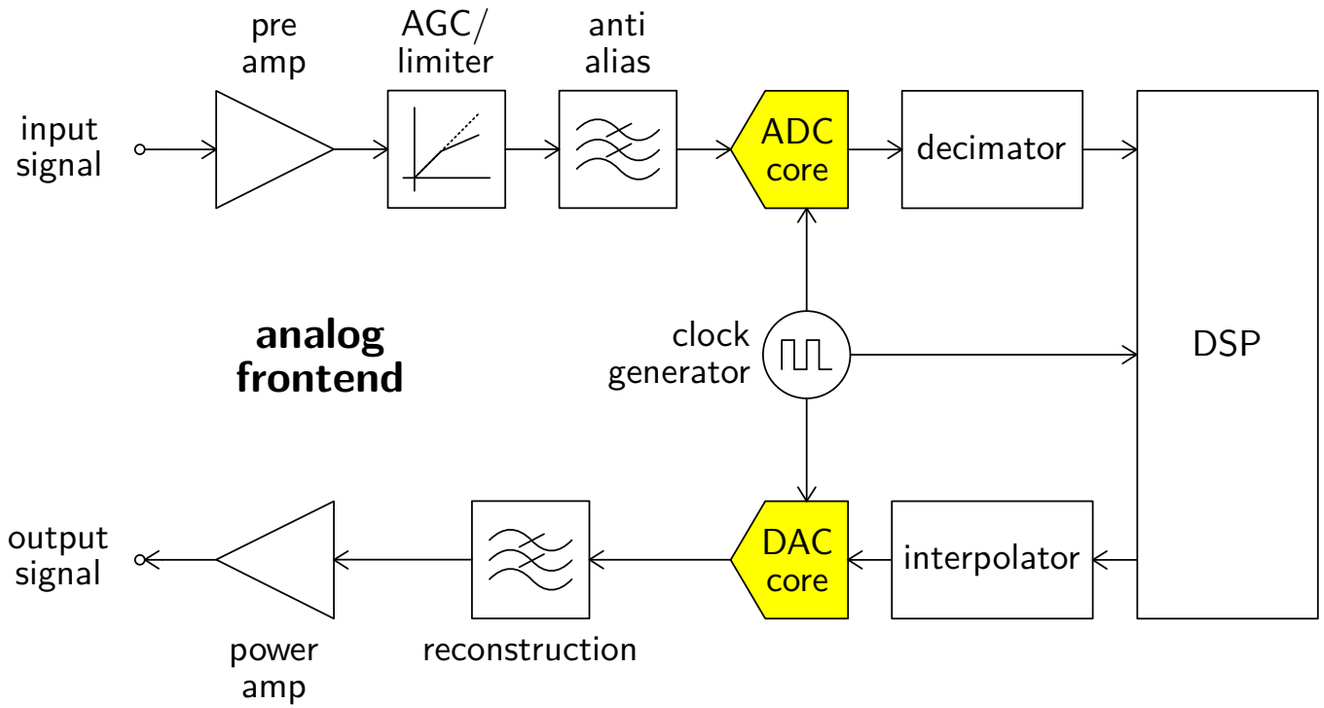
Reconstruction

- ▶ Signal **interpolation** from discrete to continuous time
- ▶ Zero-order **hold** (S/H like)
- ▶ Continuous-time **low-pass** filtering for alias rejection
- ▼ Distortion due to upper band **amplitude loss**
- ▼ High-frequency **residual** contents
- ▲ Attenuation by **oversampling**



A/D and D/A Converters

- Typical **pre** and **post** signal processing stages around ADC and DAC...



...out of the scope of this course!

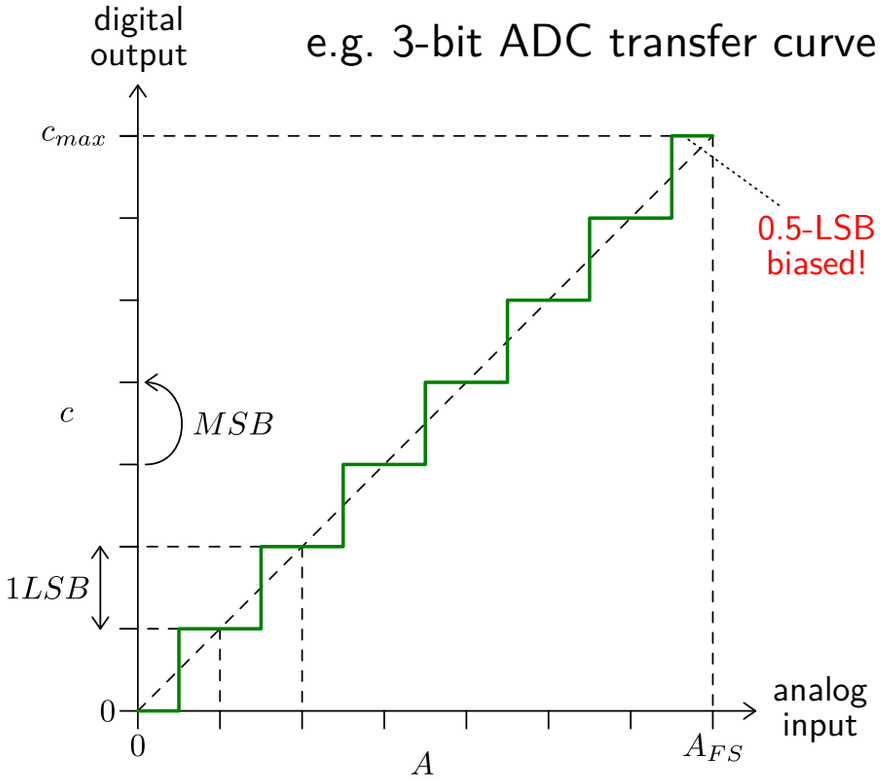
Static FoMs

- Least significant bit (**LSB**):

$$1LSB \doteq \frac{A_{FS}}{2^N - 1}$$

except for full-scale boundaries!

- **Absolute accuracy** is ± 0.5LSB
- DC transfer curve



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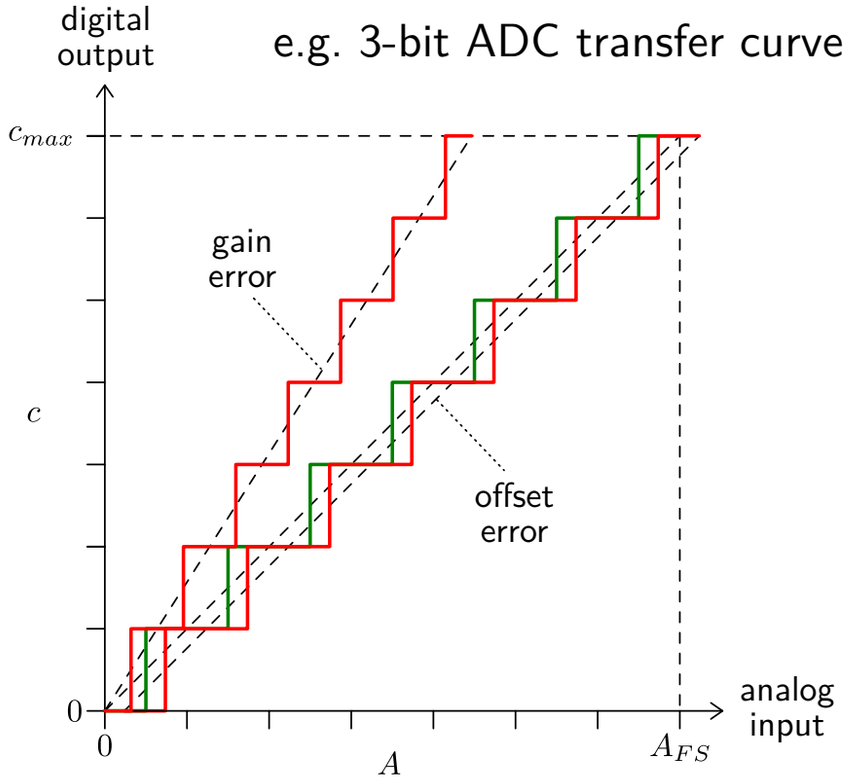
- **Gain** and **offset** errors



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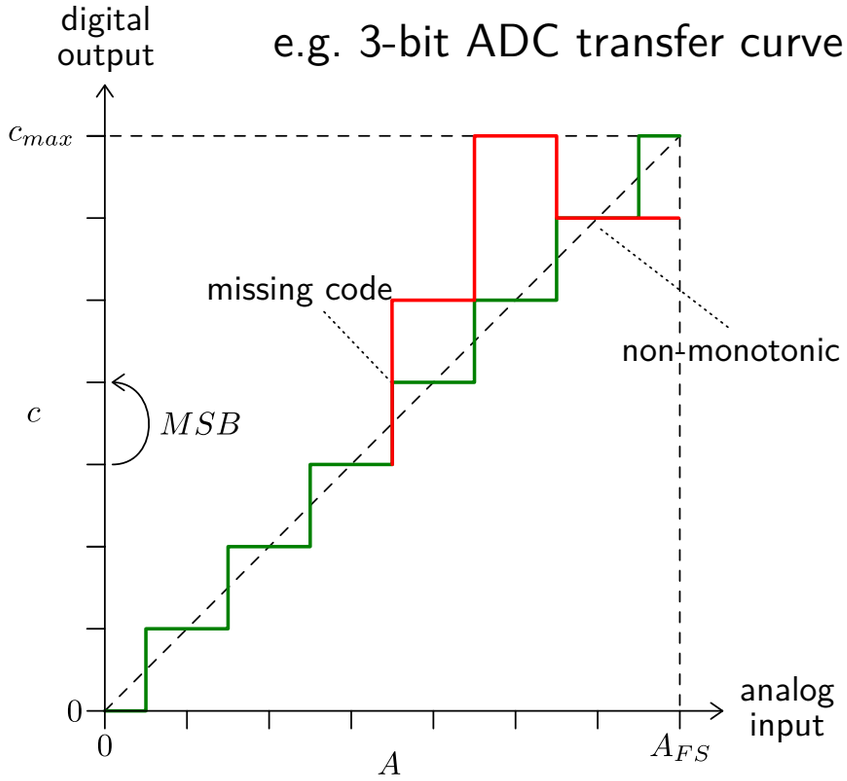
- **Non-monotonicity** and **missing codes**



Static FoMs

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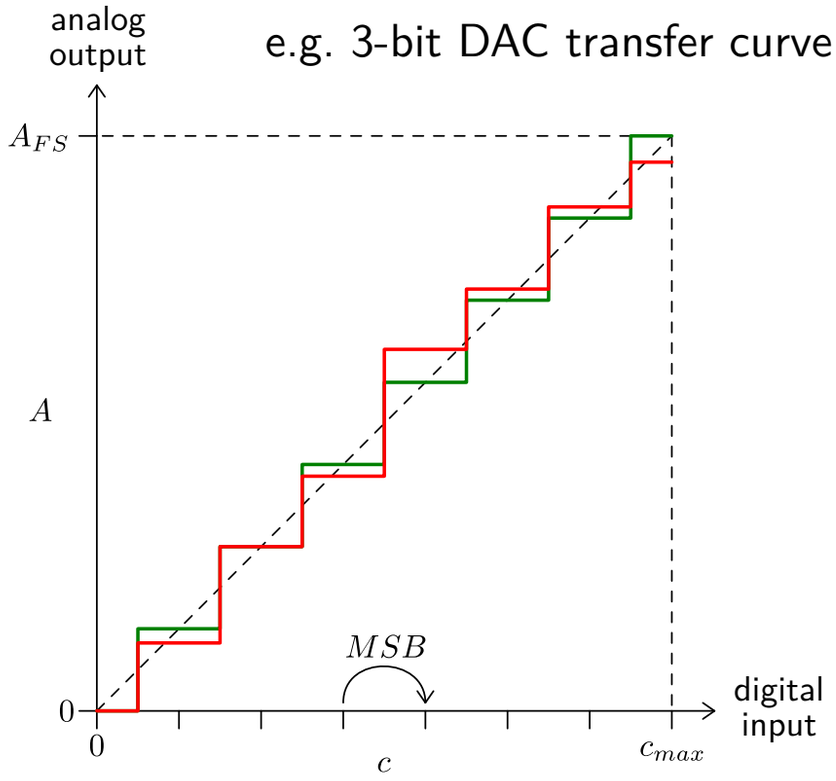
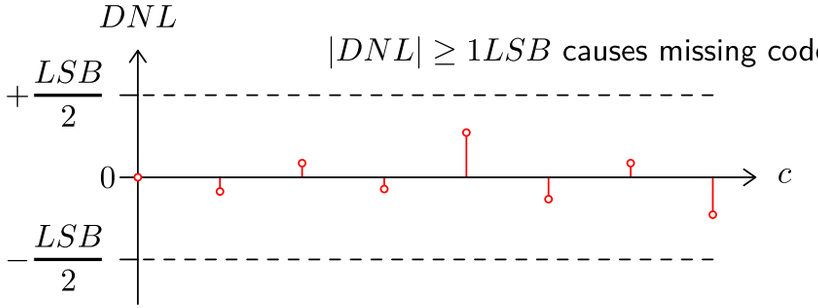
- **Absolute accuracy** is ± 0.5LSB
- DC transfer curve
- **Gain** and **offset** errors
- **Non-monotonicity** and **missing codes**
- Differential non-linearity (**DNL**)

$$DNL(c) \doteq A(c) - A(c-1) - 1LSB$$





Static FoMs

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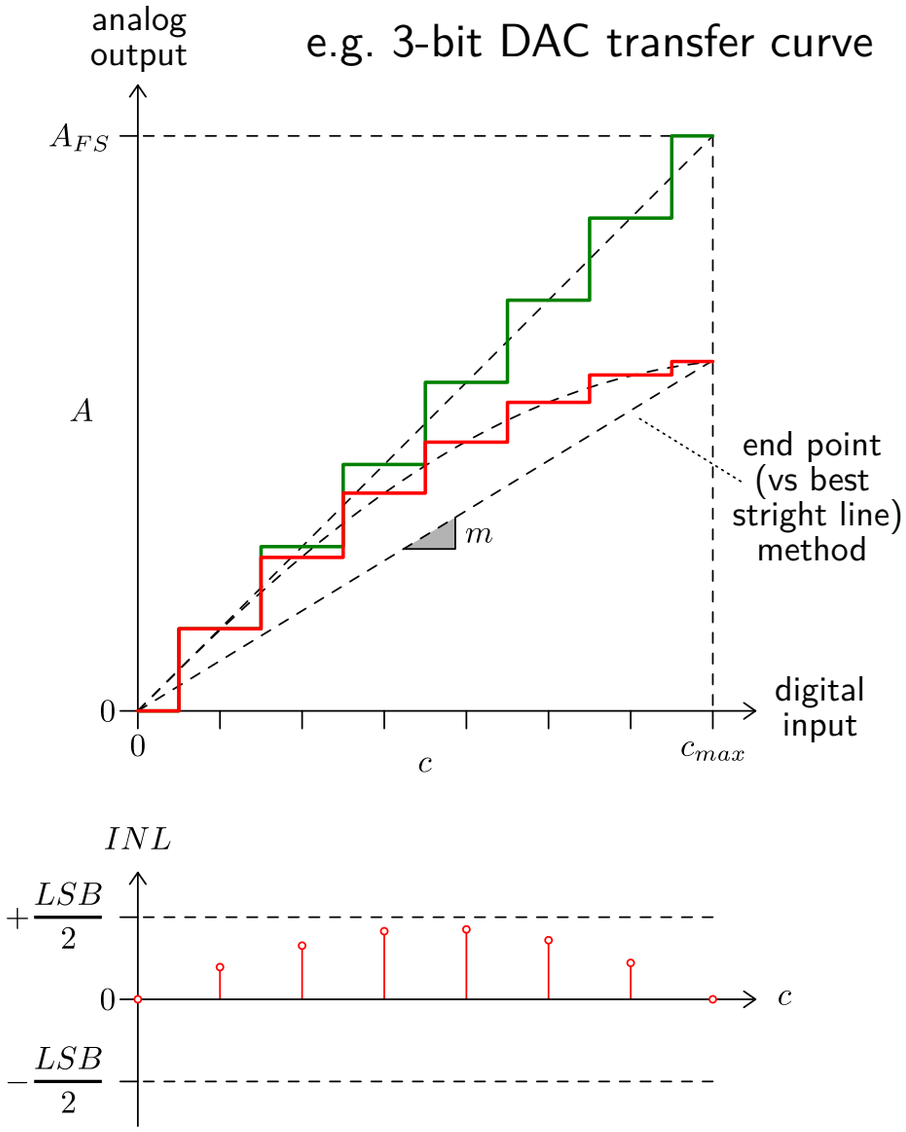
- **Non-monotonicity** and **missing codes**
- Differential non-linearity (**DNL**)

$$DNL(c) \doteq A(c) - A(c-1) - 1LSB$$

- Integral non-linearity (**INL**)

$$INL(c) \doteq A(c) - A(0) - m \cdot c$$

$$m \doteq \frac{A(c_{max}) - A(0)}{c_{max}}$$



Dynamic FoMs

- Based on single or multiple **harmonic** stimulus
- **Sampling rate**:

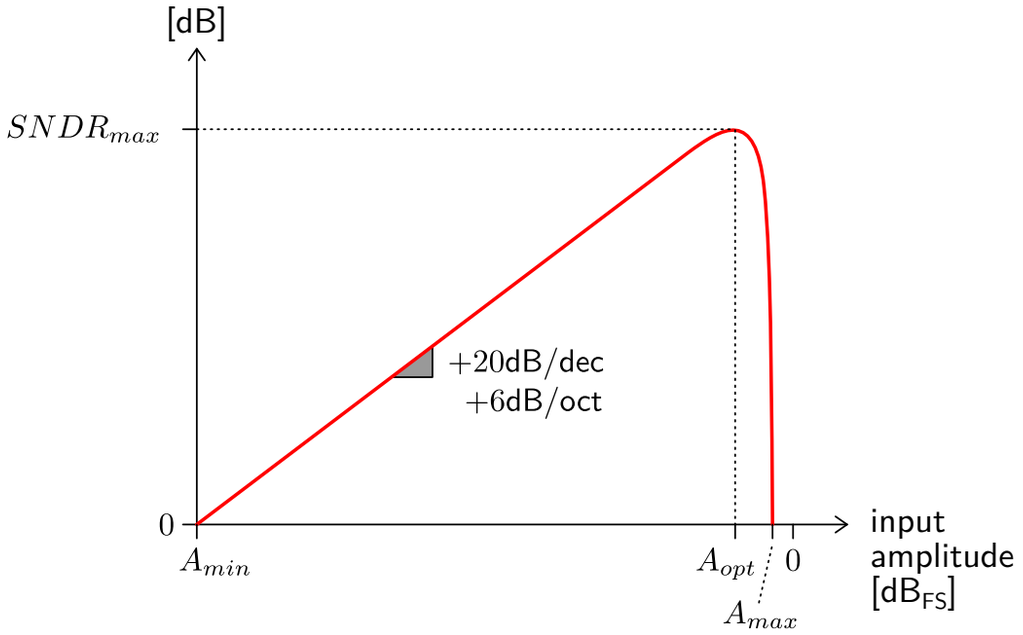
$$f_s \geq f_{nyq} = 2BW$$

- Oversampling ratio (**OSR**):

$$OSR = \frac{f_s}{f_{nyq}}$$

- Signal to noise and distortion ratio (**SNDR** or **SINAD**)
- Effective number of bits (**ENOB**):

$$ENOB = \frac{SNDR_{max}[\text{dB}] - 1.76}{6.02}$$



- Dynamic range (**DR**):

$$DR \doteq 20 \log \frac{A_{max}}{A_{min}} \quad [\text{dB}] \quad \geq \quad SNDR_{max}$$

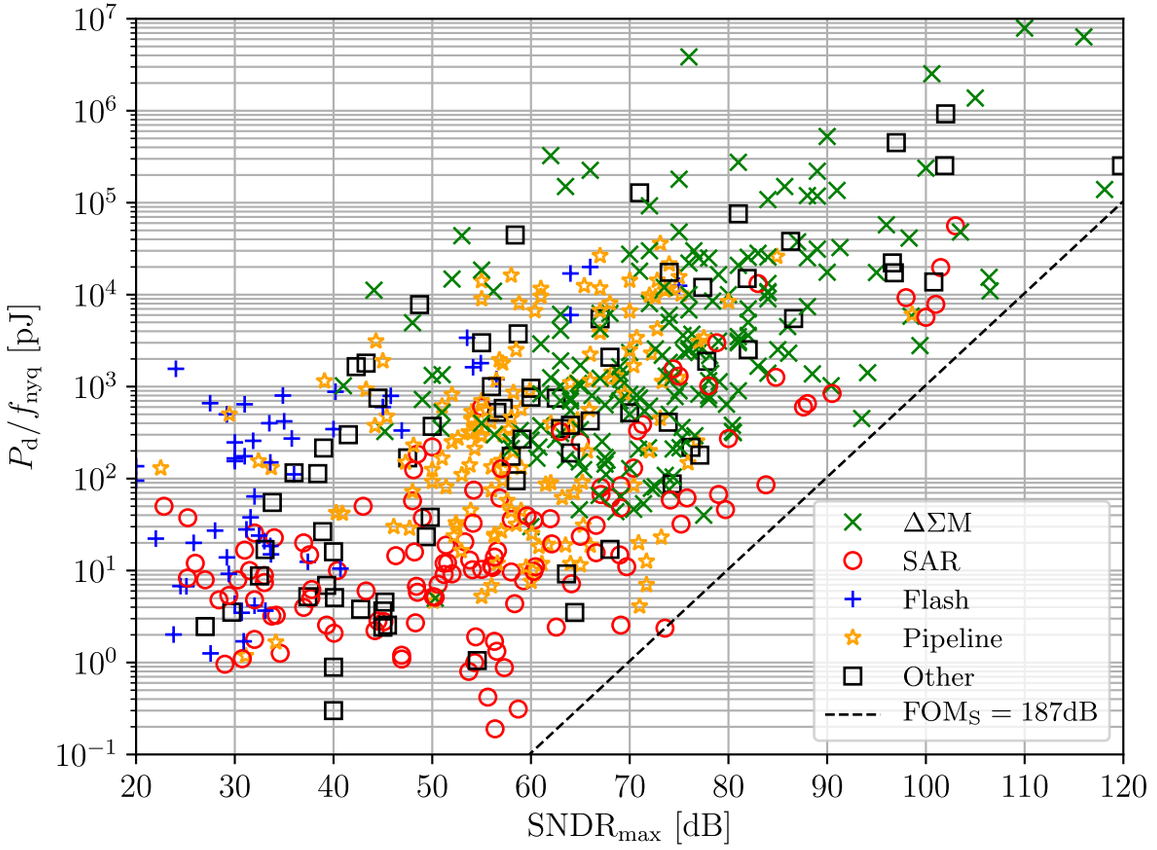
Combined FoMs

- **Quantitative** expression
- **Performance** and **resources** mixed
- Objective rule for design **comparison** purposes
- Examples for **ADC**:
  - R.H. Walden (1999)

$$FOM_W \doteq \frac{P_D}{f_{nyq} \cdot 2^{ENOB}} \quad [\text{J/conv-step}]$$

  - R. Schreier (2005)

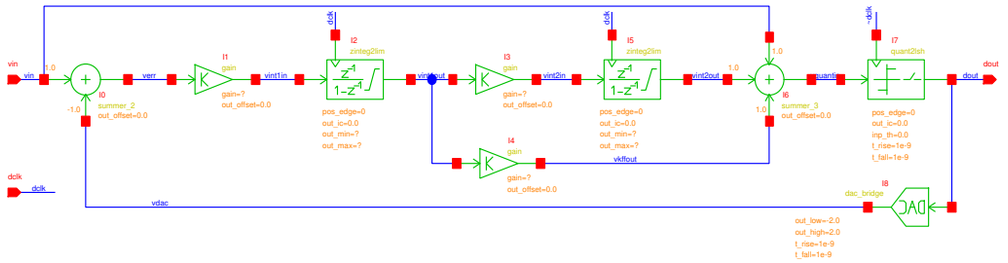
$$FOM_S \doteq SNDR_{max} + 10 \log \frac{f_{nyq}}{2P_D} \quad [\text{dB}]$$

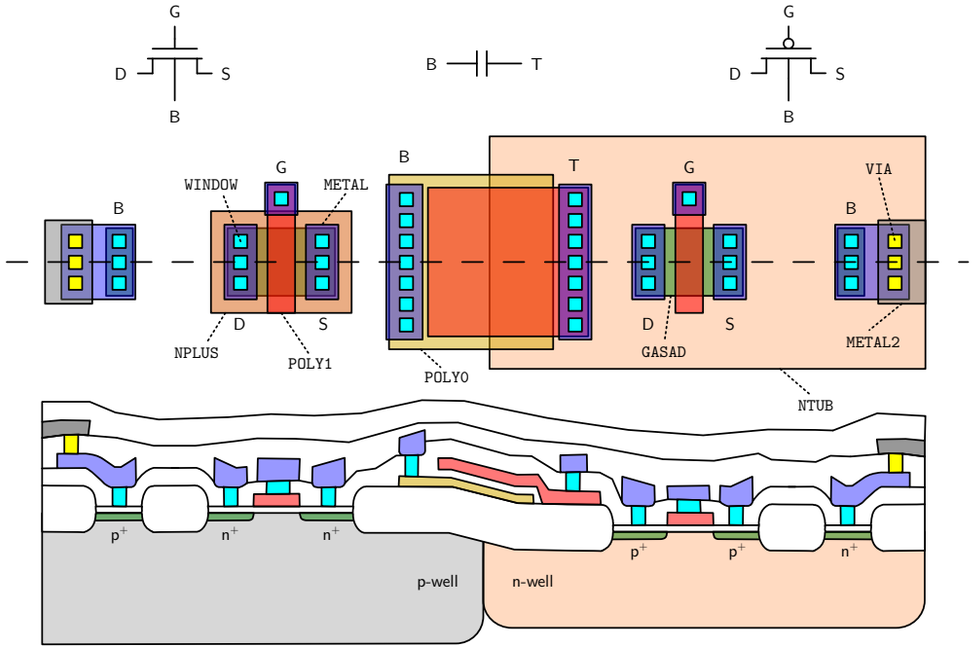


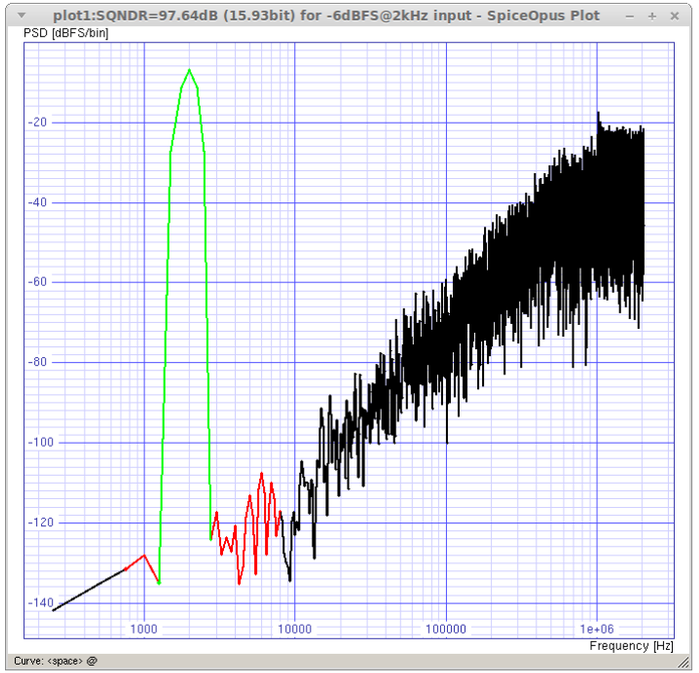
↗ B. Murmann
ADC Performance Survey 1997-2022
github.com/bmurmann/ADC-survey

My ΔΣM in CNM25

- Second-order single-bit A/D **ΔΣ modulator** design case
- **Simple** 2.5µm 2P2M CMOS technology (CNM25)

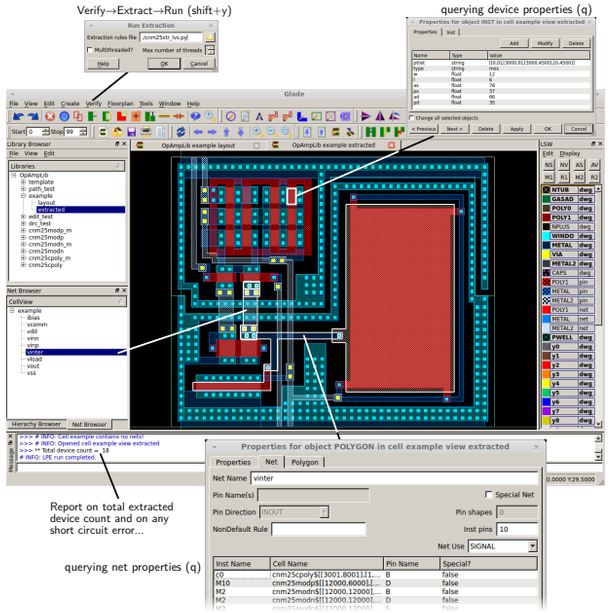


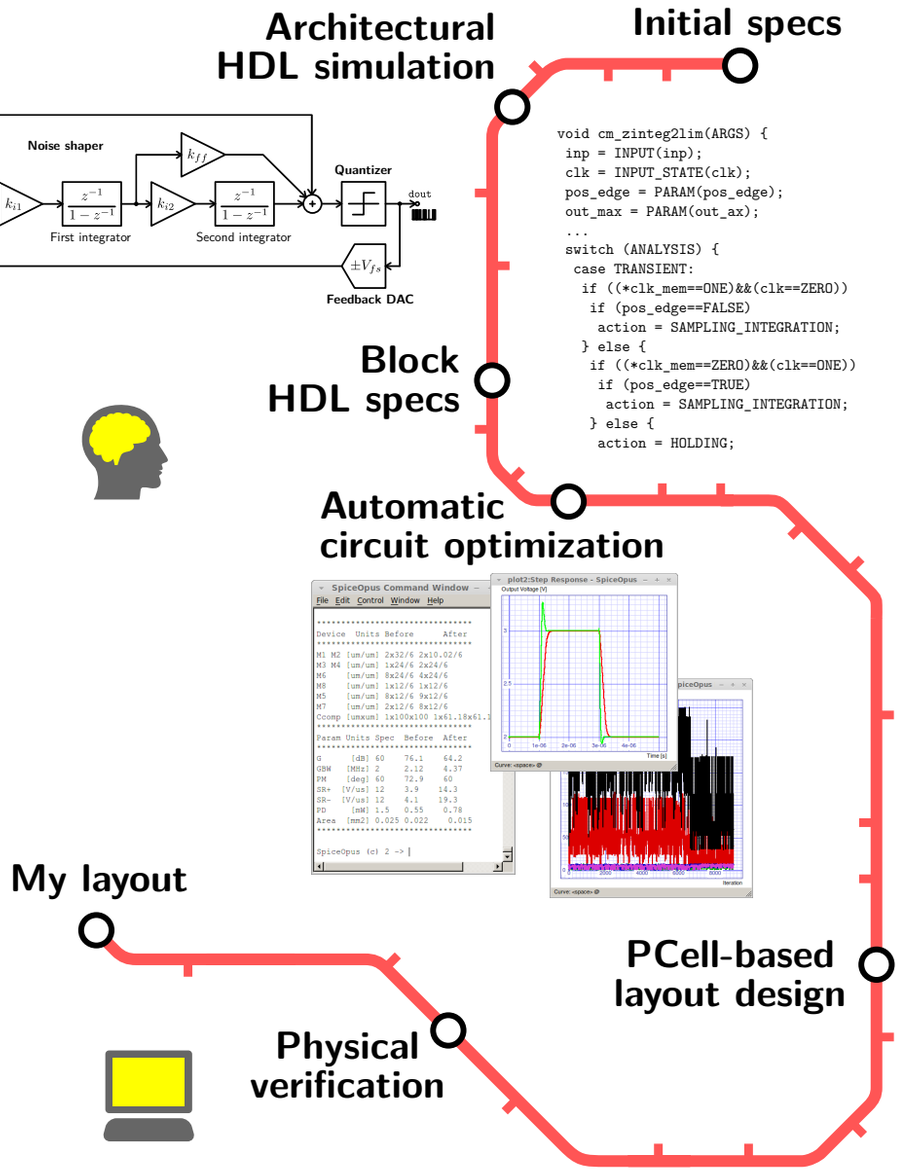




My ΔΣM in CNM25

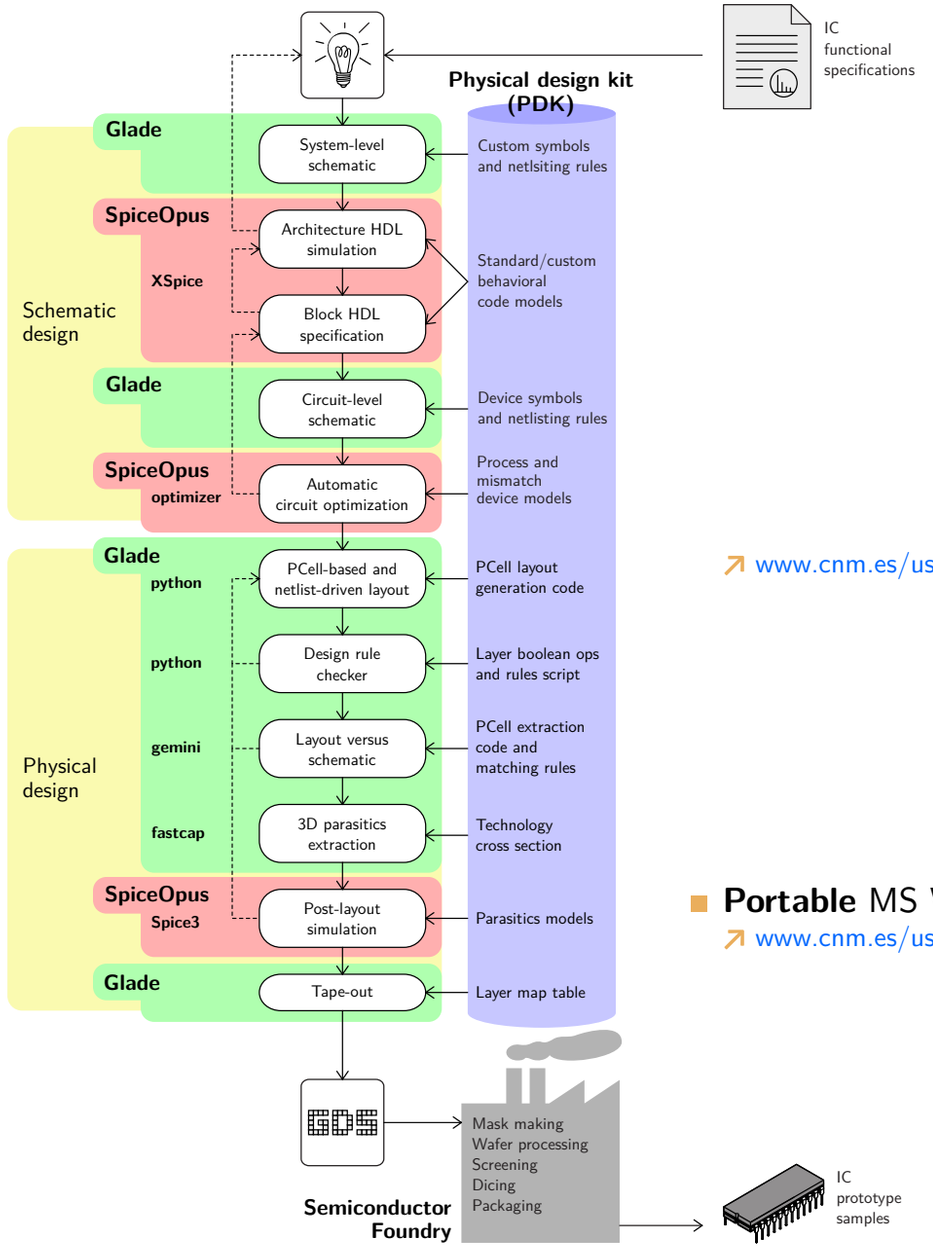
- Second-order single-bit A/D **ΔΣ modulator** design case
- **Simple** 2.5µm 2P2M CMOS technology (CNM25)
- From **system HDL** simulation...
  ...to **full-custom layout**





My ΔΣM in CNM25

- Second-order single-bit A/D **ΔΣ modulator** design case
- **Simple** 2.5µm 2P2M CMOS technology (CNM25)
- From **system HDL** simulation... ...to **full-custom layout**
- **Freeware** and **multi-OS** (MS Windows, Linux) EDA tools:
  - **Glade** (schematic/layout edition and physical verification with Python user language)
    ↗ peardrop.co.uk
  - **SpiceOpus** (SPICE/XSpice mixed-signal simulation and circuit optimization with NUTMEG user language)
    ↗ fides.fe.uni-lj.si/spice
- Work at **home** and tutorial at **lab**!



↗ www.cnm.es/users/pserra/apdk/

- **Portable** MS Windows version:
  ↗ www.cnm.es/users/pserra/uab/ihsd/lab.html