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Analog Integrated Circuit Optimization Using Spice

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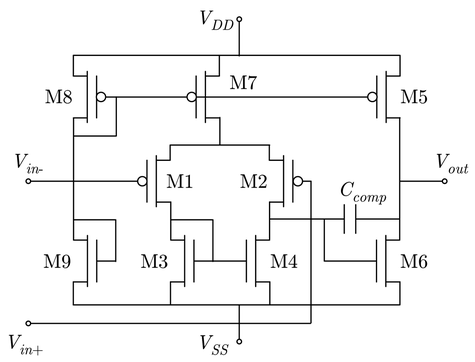
1 Introduction

This paper proposes a training strategy based on Spice simulation to teach analog integrated circuit optimization. The choice of the Spice-language standard ensures the applicability of the acquired knowledge in most of the analog design fields for SoCs (e.g. signal processing, RF communications, power control). In this sense, the Spice Opus CAD tool [1] have been selected here, which is a free Berkeley Spice3 compliant simulator with optimization and XSpice [2] mixed-mode capabilities, so it can be also reused for other related syllabus like full-custom design [3] or mixed modelling [4].

2 Test Circuits

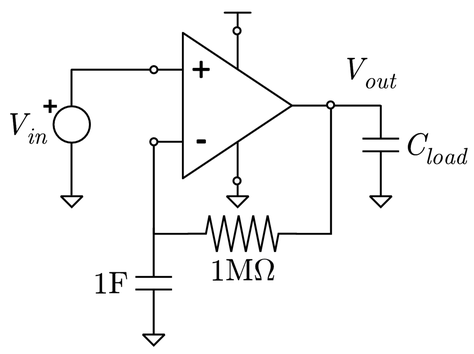
The practice example presented is built around the classic dual-stage Miller operational amplifier of Figure 1(left). In this case, the main specifications are: differential voltage gain at DC (`gdc`), gain-bandwidth product (`gbw`), phase margin (`pm`), slew-rate +/− (`srpos/srneg`), Si circuit area (`area`) and power consumption (`pd`). The first step for the student is to model this cell under test in terms of a Spice subcircuit, like in Figure 1(right). As any CMOS circuit, the basic design variables are the device dimensions (i.e. `w` and `l`) and bias, which in fact are related to the specifications `area` and `pd`, respectively.

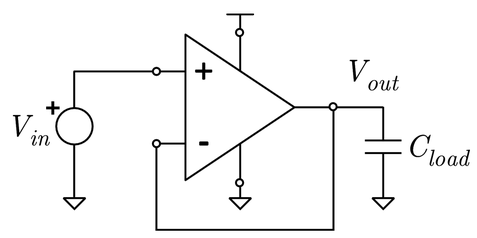



```
.subckt opamp vinn vinp vout vdd vss
m1 vload vinn vcomm vdd modp w=18u l=6u
m2 vinter vinp vcomm vdd modp w=18u l=6u
m3 vload vload vss vss modn w=12u l=12u
m4 vinter vload vss vss modn w=12u l=12u
m5 vout vbias vdd vdd modp w=96u l=6u
m6 vout vinter vss vss modn w=48u l=6u
m7 vcomm vbias vdd vdd modp w=24u l=6u
m8 vbias vbias vdd vdd modp w=12u l=6u
m9 vbias vbias vss vss modn w=3u l=24u
ccomp vout vinter cpoly w=100u l=100u
.ends
```

Fig. 1. Operational amplifier under test (left) and equivalent Spice sub-circuit (right).

In order to cover all the required specifications, the student has to manage with several test circuits around the cell. A good solution in this case is the double test set-up shown in Figure 2.






```
qopenloop.sp3
.include cnm25typ.mod2
.include opamp.sp3
cload vout 0 10p
vin vin 0 dc=2.5v ac=1
xopamp vfb vin vout vdd vss opamp
vss vss 0 dc=0v
vdd vdd 0 dc=5v
cdc vfb 0 1
rdc vfb vout 1000k
.end
```

```
follower.sp3
.include cnm25typ.mod2
.include opamp.sp3
cload vout 0 10p
vin vin 0 pulse(2 3 1u 1n 1n 2u)
xopamp vout vin vout vdd vss opamp
vss vss 0 dc=0v
vdd vdd 0 dc=5v
.end
```

Fig. 2. Quasi open-loop (left) and follower (right) test circuits.

3 Automatic Characterization

The next step towards the cell optimization is the automatic extraction of its performance. The challenge for the student in this stage is both, to perform several analysis in different test circuits and to program the automatic measurements to be applied to the simulation results, like:

```
.control
source qopenloop.sp3
source follower.sp3
setcirc qopenloop.sp3
op
let pd=-i(vdd)*v(vdd)*1e3
let area=(@m1:xopamp[w]+6u)*(@m1:xopamp[l]+11u)+(@m2:xopamp[w]+6u)*(@m2...
ac dec 50 10 10e6
let gmag=20*log10(mag(v(vout)))
let gph=phase(v(vout))
let gdc=gmag[0]
let gbw=abs(frequency[sum(gmag ge 0)])/1e6
let pm=180+gph[sum(gmag ge 0)]
setcirc follower.sp3
tran 1n 5u
let vrise=v(vout)*(time lt 3u)+3*(time ge 3u)
let trisebot=min(time*(vrise ge 2.1)+(vrise lt 2.1))
let trisetop=min(time*(vrise ge 2.9)+(vrise lt 2.9))
let srpos=0.8/(trisetop-trisebot)*1e-6
let vfall=v(vout)*(time ge 3u)+3*(time lt 3u)
let tfalltop=min(time*(vfall lt 2.9)+(vfall ge 2.9))
let tfallbot=min(time*(vfall lt 2.1)+(vfall ge 2.1))
let srneg=0.8/(tfallbot-tfalltop)*1e-6
.endc
```

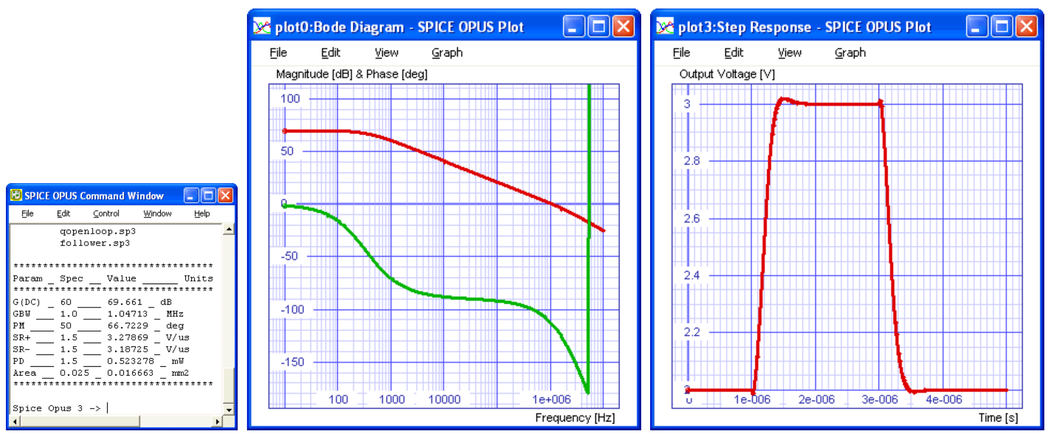


Fig. 3. Simulation results (center and right), and datasheet (left) after automatic extraction of Figure 1.

4 Optimization Process

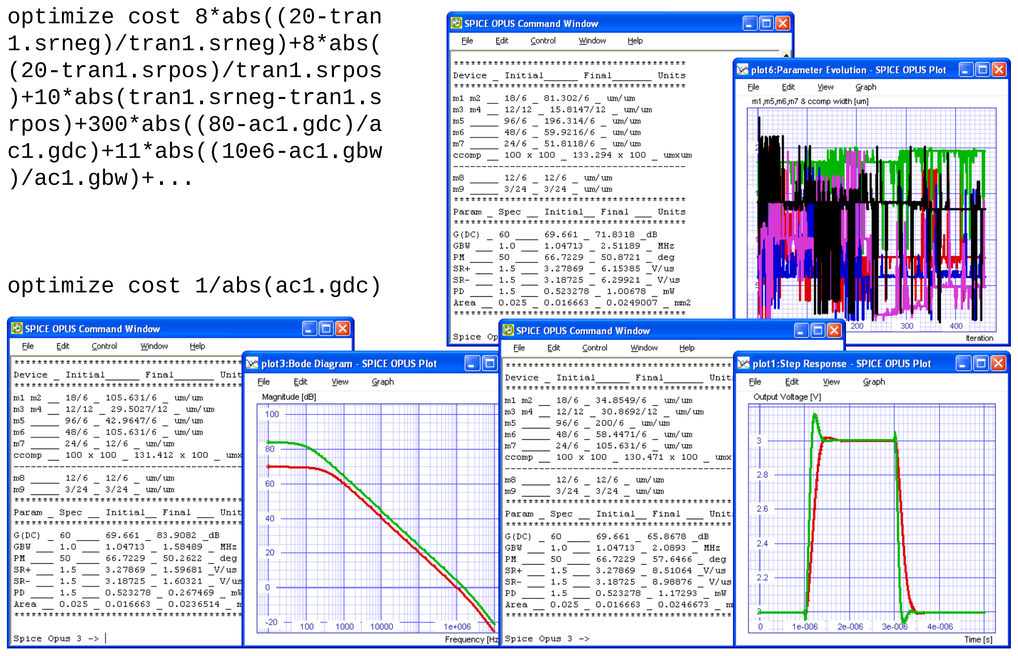
Its definition involves the declaration of the design variables, the required analysis, the implicit constraints, and the cost function. In this sense, the student should minimize the number of design variables by, for example, exploiting circuit symmetries. Also, proper ranges and initial values should be derived from the analytical design equations:

```
optimize parameter 0 element m1:xopamp parameter w low 12u high 200u initial 12u
optimize parameter 1 element m5:xopamp parameter w low 12u high 200u initial 96u
...
optimize analysis 0 setcirc qopenloop.sp3
optimize analysis 1 op
...
optimize implicit 0 op1.pd lt 1.5
optimize implicit 1 op1.area lt 0.025
```

Finally, but most important, the success of any optimization process is not only given by the algorithm itself but also by the cost function, which classifies the solution obtained in each iteration. At this point, students can experiment with a wide variety of expressions:

```
optimize cost 8*abs((20-tran
1.srneg)/tran1.srneg)+8*abs(
(20-tran1.srpos)/tran1.srpos
)+10*abs(tran1.srneg-tran1.s
rpos)+300*abs((80-ac1.gdc)/a
c1.gdc)+11*abs((10e6-ac1.gbw
)/ac1.gbw)+...
```

```
optimize cost 1/abs(ac1.gdc)
```




```
optimize cost 1/abs(tran1.srneg)+1/abs(tran1.srpos)+1000*abs(op1.pd-1.5)
```

Fig. 4. Cost function examples and results for both, global (upper) and specific (lower) optimizations.

5 Conclusions

The main advantages of the proposed training methodology for analog integrated circuit optimization are: full control of all steps by the student, standard language scripting, high flexibility, applicability to a wide range of analog integrated circuits, and free CAD tools.

References

[1] Group for Computer Aided Circuit Design, *Spice Opus 2.03*, University of Ljubljana, Slovenia.

[2] F.L. Cox et al, *XSpice Software User's Manual*, Georgia Tech Research Corp.

[3] F. Serra-Graells and N. Barniol, *Design of Analogue Integrated Circuits: Freeware PC-based CAD for Student Practices*, EWME, pp.289-292, 2000.

[4] F. Serra-Graells and N. Barniol, *Mixed Integrated Circuit Design with CMOS VLSI Technologies for Pre-Graduated Students*, EWME, pp.209-212, 2002.