Mixed Integrated Circuit Design in CMOS VLSI Technologies for Pre-Graduated Students

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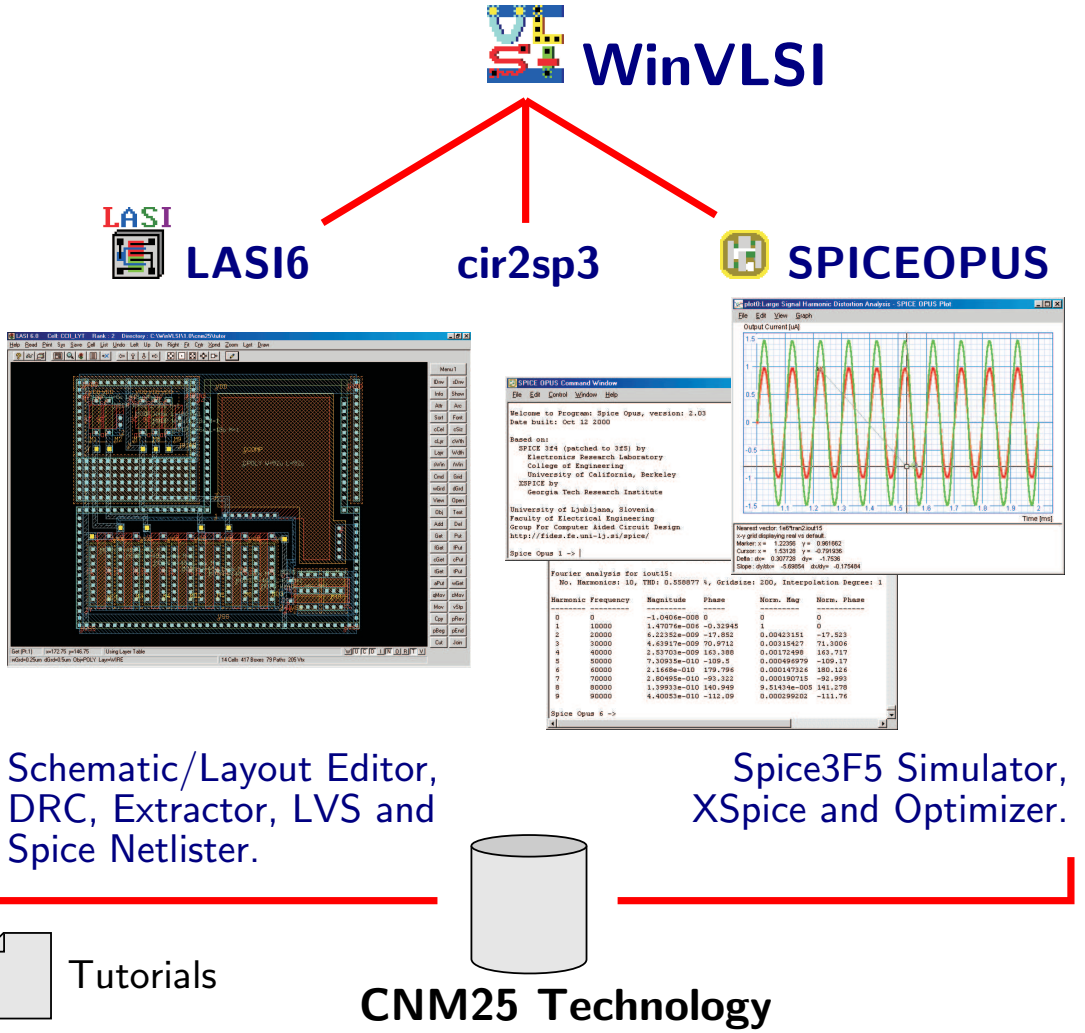
- Introduction to WinVLSI
- Mixed-Simulation Strategy
- Design Examples
  - A First-Order Low-Pass Switched-Capacitor Filter
  - A Third-Order Low-Pass $\Sigma\Delta$ Modulator for ADCs
- Conclusions

- Wanted features:
  - Full-Custom Design
  - Mixed Simulation
  - Circuit Optimization
  - Easy to use
  - Freeware
  - Windows Platforms

- Tested tools:

Electric, www.staticfreesoft.com
Magic, vlsi.cornell.edu/magic
XCircuit, xcircuit.ece.jhu.edu
WinSpice, www.winspice.com
Microwind2, intrage.insa-tlse.fr/~etienne
Kic, www.srware.com
...

- The developed Design Kit:



- Main parts:

LASI 6.2, members.aol.com/lasicad

SPICEOPUS 2.03, fides.fe.uni-lj.si/spice

cir2sp3, custom parser for netlist interface

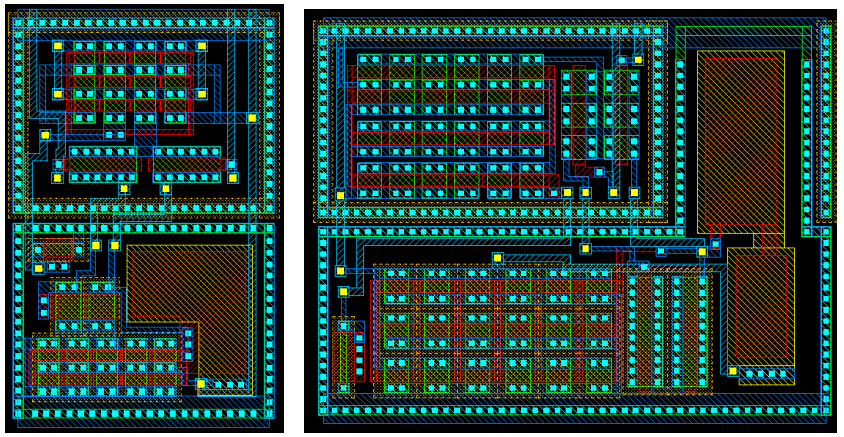
- Target technology:

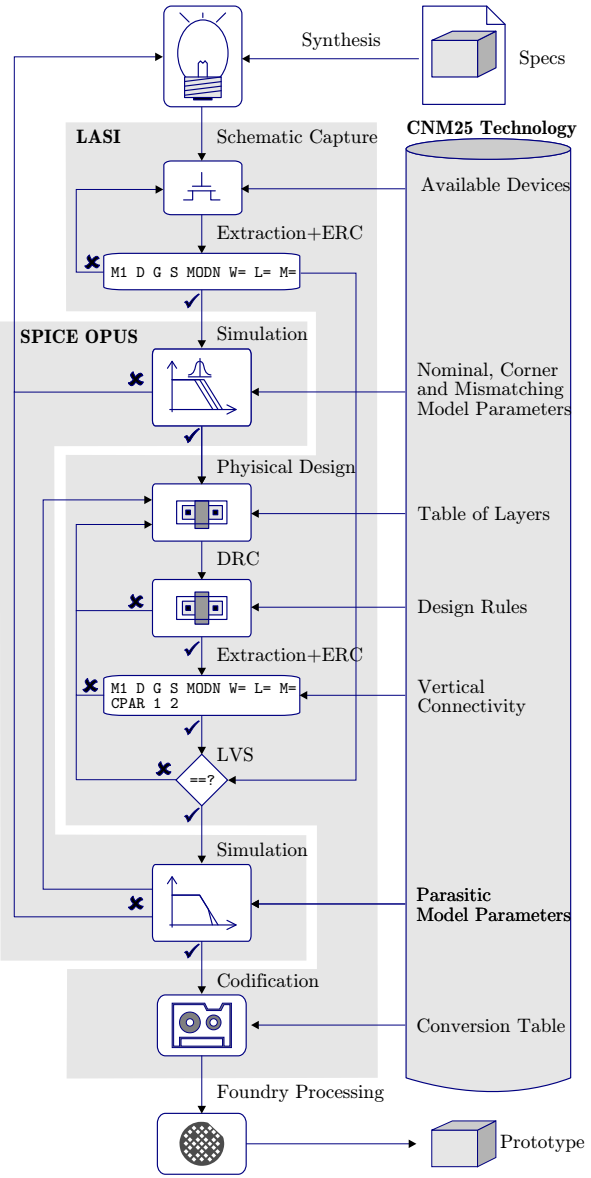
2.5μm 2P 2M CMOS (CNM25), www.cnm.es

- Homepage of WinVLSI 1.31:

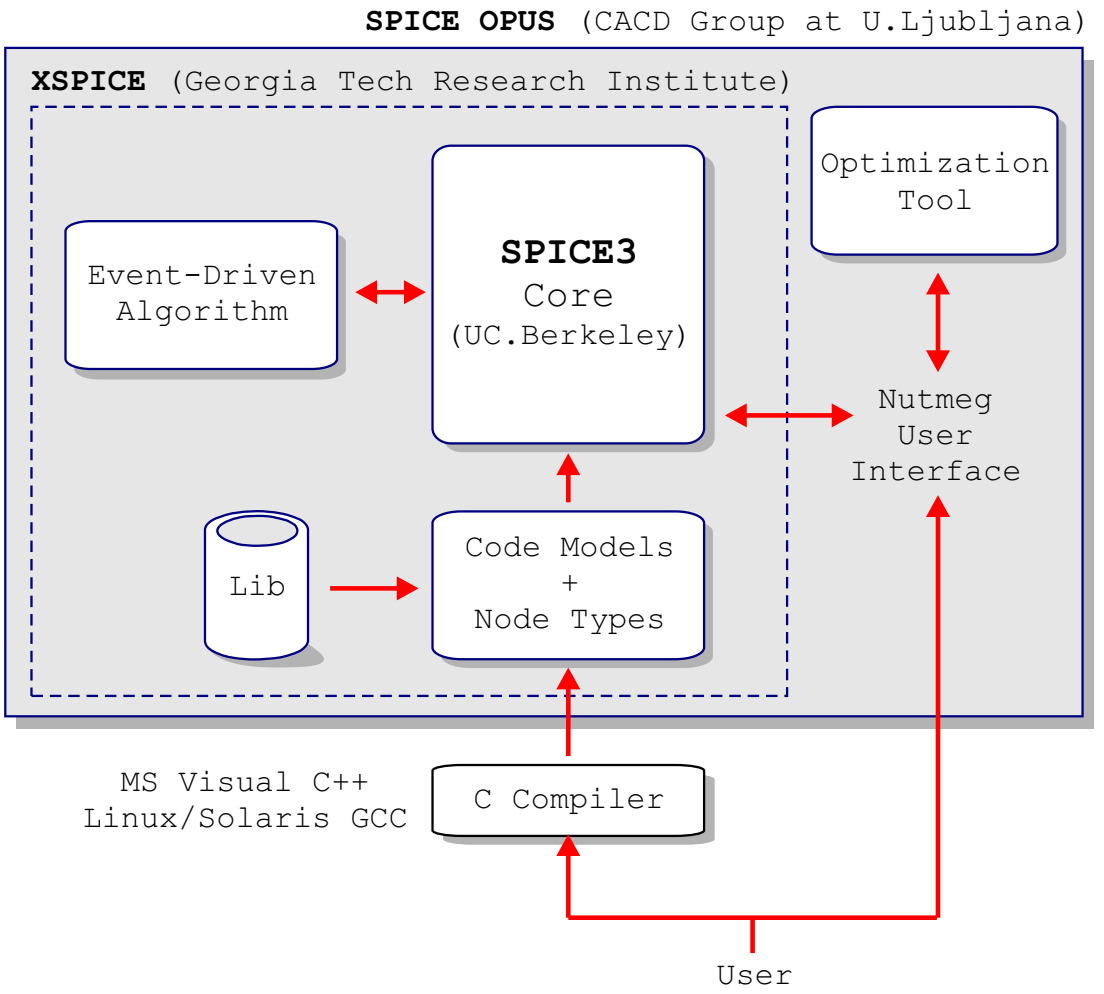
www.cnm.es/~pserra/winvlsi

- Students designs (e.g. Miller OpAmp):

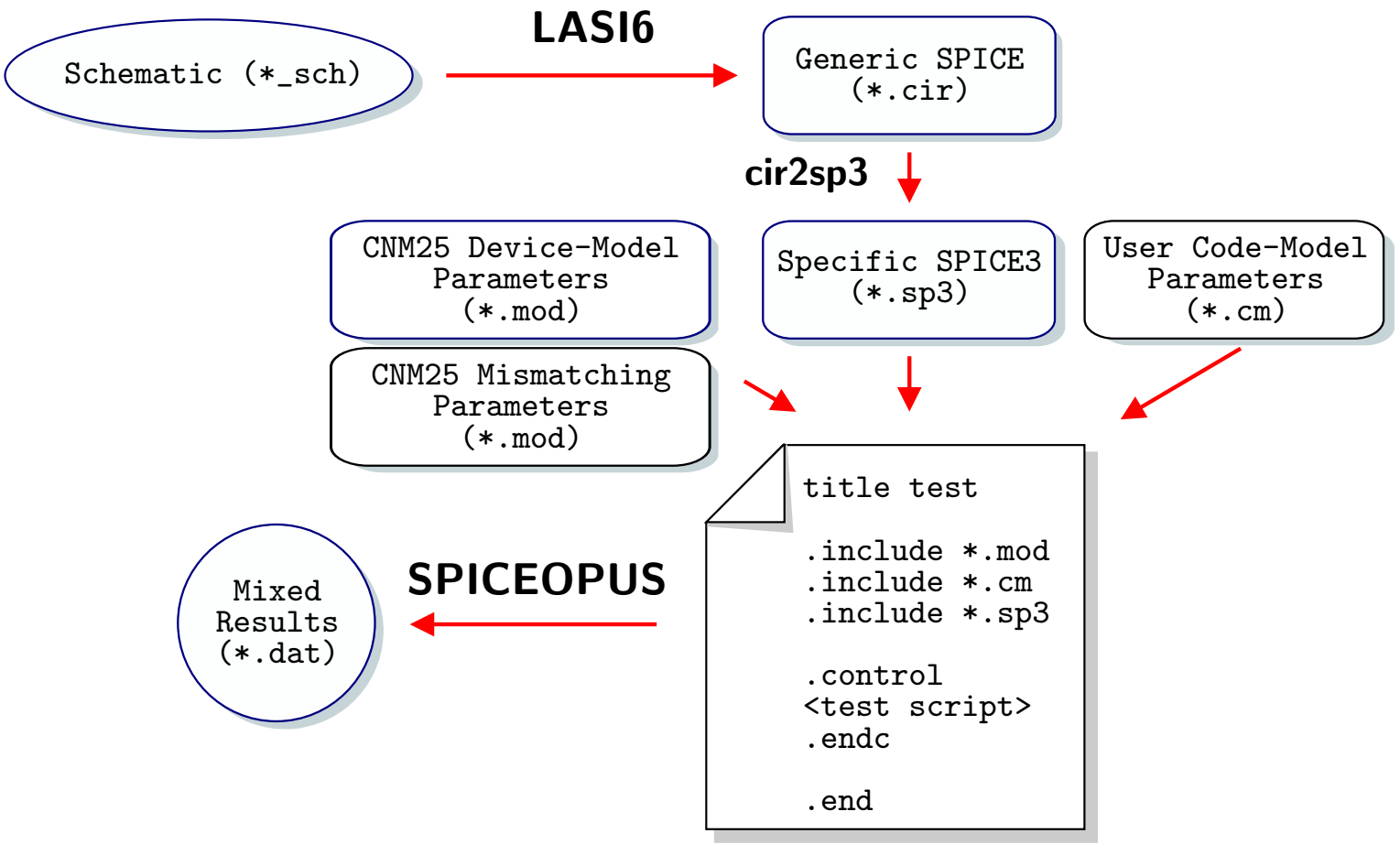




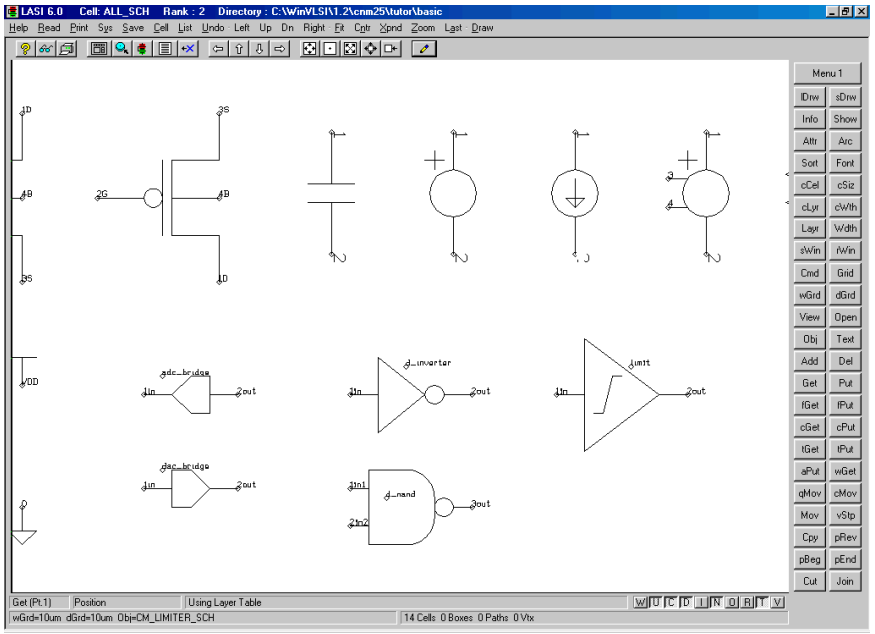
- Analog/Digital and Multi-Level engine:



- Netlist interface:



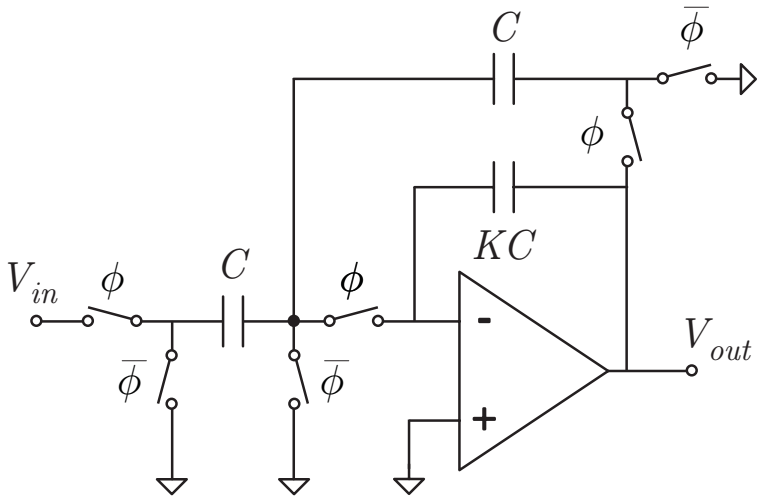
- Pre-defined symbols, code-models and node-types examples:



Node type	Description
analog	Built-in, used for analog circuits
d	3-state 4-strength digital data
int	integer valued data
real	real valued data

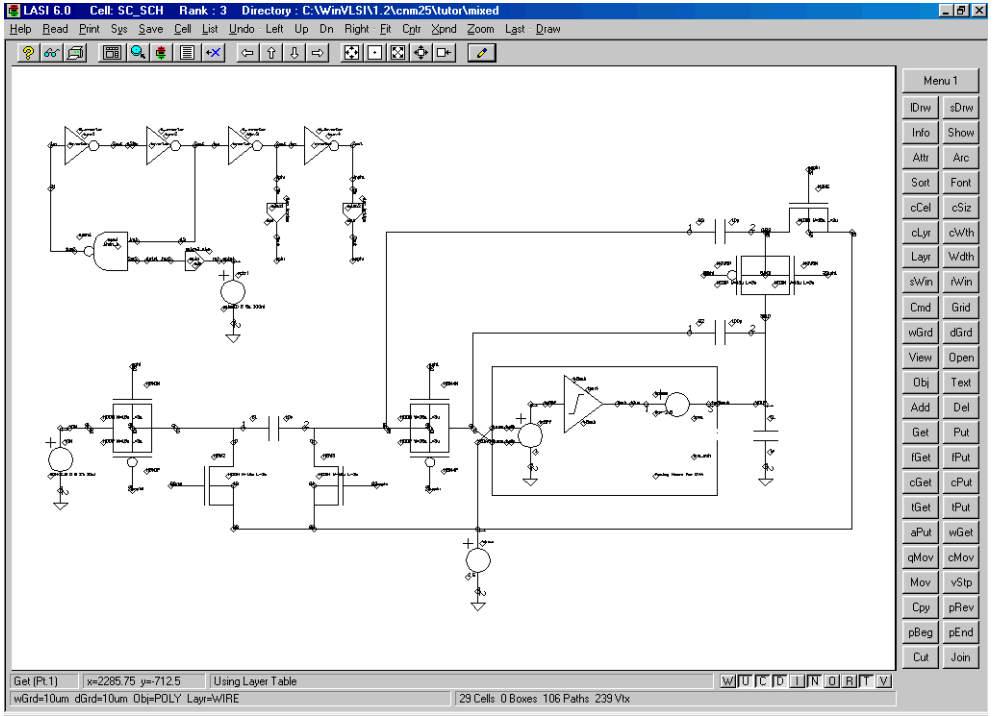
Code Model	Description
d_dt	differentiator block
gain	a simple gain block
hyst	hysteresis block
limit	limit block
mult	multiplier block
oneshot	one-shot
s_xfer	s-domain transfer function block
d_and	digital n-input and gate
d_buffer	digital one-bit-wide buffer
d_dff	digital d-type flip flop
d_fdiv	digital frequency divider
d_open_c	digital one-bit-wide open-collector buffer
d_pulldown	digital pulldown resistor
d_ram	digital random-access memory
d_source	digital signal source
d_state	digital state machine
real_delay	a z ** -1 block working on real data
adc_bridge	analog-to-digital converter node bridge
dac_bridge	digital-to-analog converter node bridge
d_to_real	node bridge from digital to real with enable
real_to_v	node bridge from real to analog voltage

- Stray-insensitive topology [Mosc84]:



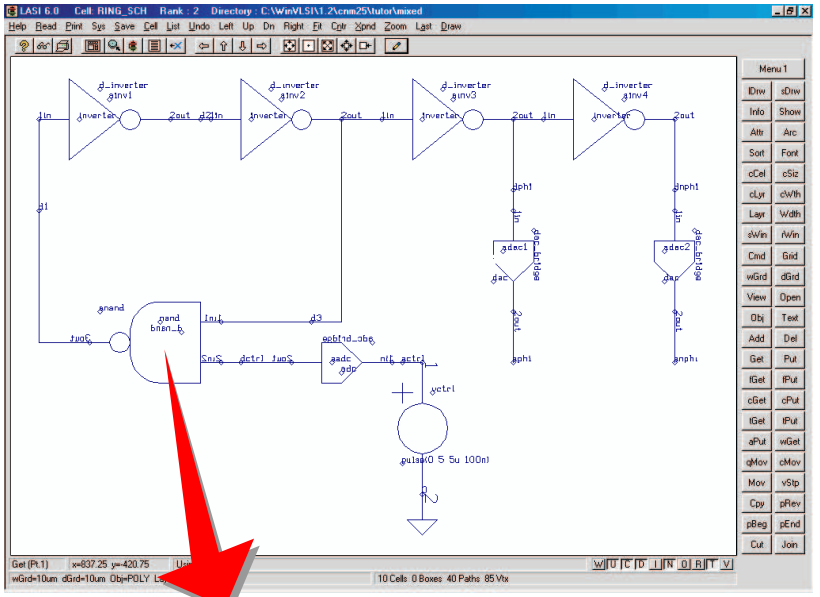
$$f_{-3\text{dB}} \simeq \frac{f_s}{(2K+1)\pi} \qquad f_{-3\text{dB}} \ll f_s$$

- Mixed and multi-level schematic:



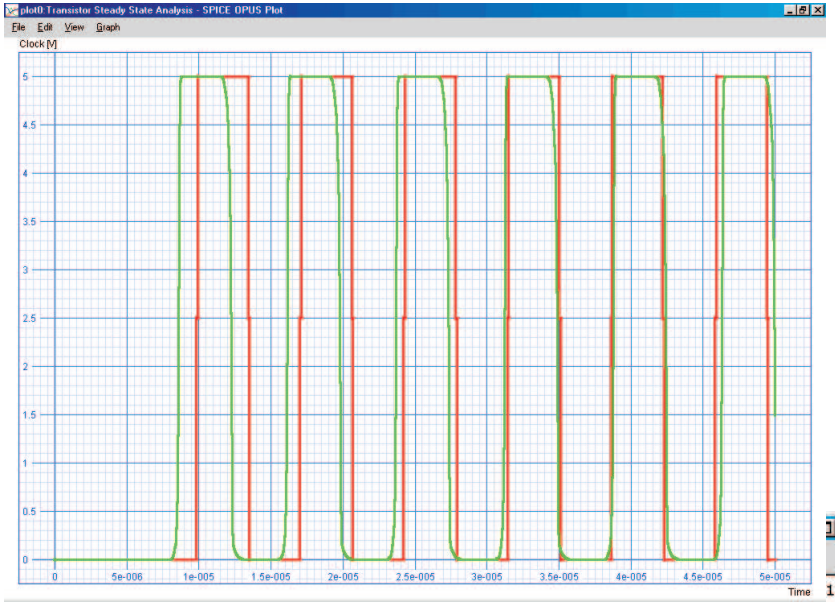

```
.model dac dac_bridge (out_low=0 out_high=5)
.model adc adc_bridge (in_low=0.3 in_high = 3.5)
.model inverter d_inverter (rise_delay=1.2e-6 fall_delay=1.2e-6)
.model nand d_nand (rise_delay=1.2e-6 fall_delay=1.2e-6)
.model vlimit limit (gain=1000 out_lower_limit=-2.5 out_upper_limit=2.5 limit_range=1)
```

- Transistor versus Functional:



```
anand [d3 dctrl] d1 nand2
.model nand2 d_nand (rise_delay = 1.2e-6
+                    fall_delay = 1.2e-6)
```

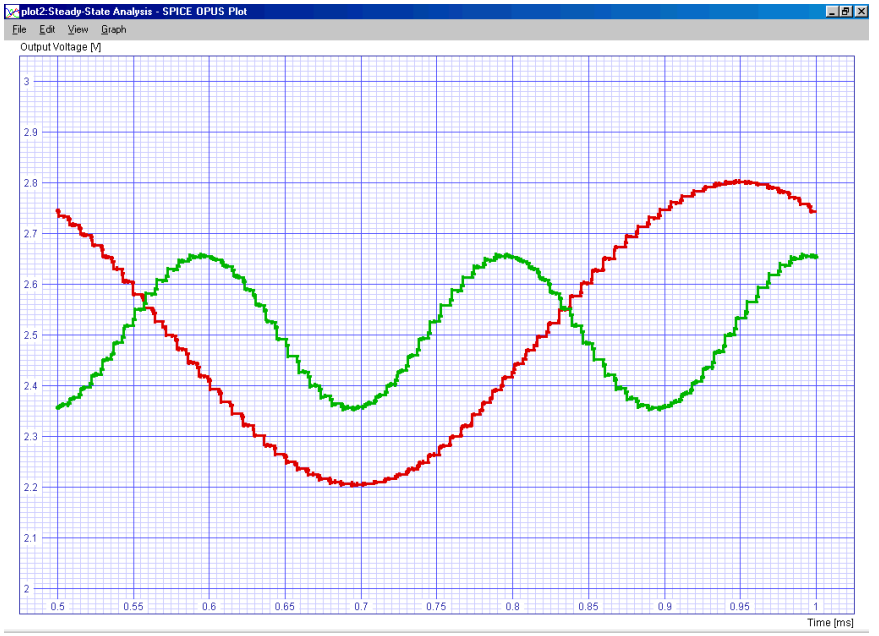
```
xnand a3 actrl a1 nand2
.subckt nand2 a b y
vdd 99 0 5
mna 1 a 0 0 modn w=6e-6 l=6e-6
mnb y b 1 0 modn w=6e-6 l=6e-6
mpa y a 99 99 modp w=6e-6 l=6e-6
mpb y b 99 99 modp w=6e-6 l=6e-6
.ends nand2
```




```
Warning: vctrl: no DC value, transient time 0 value used
++++++++++ SIMULATION TIME FOR BEHAVIORAL MODEL ++++++++++
elapsed time since last call: 0.110 seconds.

Total elapsed time: 4.780 seconds.

Current dynamic memory usage = 5300224,
Dynamic memory limit = 2139779072.
Dynamic memory reserved information not available.
Set memory_status variable.

Circuit: *** Transistor-level model for the ring oscillator

Warning: vctrl: no DC value, transient time 0 value used
++++++++++ SIMULATION TIME FOR TRANSISTOR MODEL ++++++++++
elapsed time since last call: 0.990 seconds.

Total elapsed time: 5.770 seconds.

Current dynamic memory usage = 5853184,
Dynamic memory limit = 2139779072.
Dynamic memory reserved information not available.
Set memory_status variable.

Spice Opus 2 ->
```

- Complete mixed-mode and multi-level simulation (e.g. f_s=125KHz and K=10):

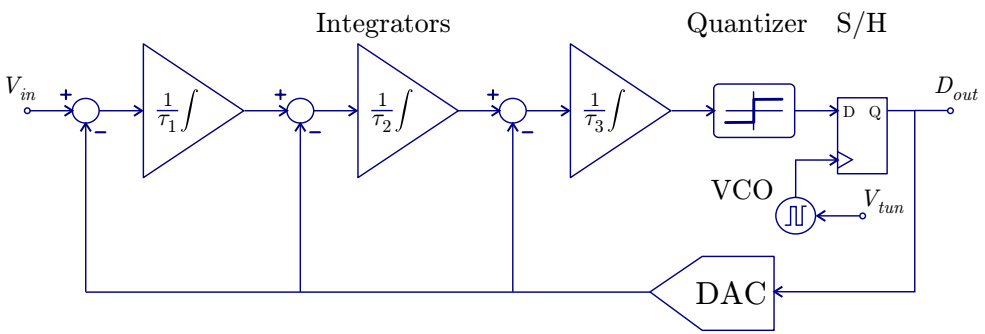
```
* Steady-State Analysis

.include cnm25typ.mod2
.include cm.mod
.include sc_sch.sp3
.options gmin=1e-12

.control
foreach fin 2k 5k
    let @vin[sin]=(2.5;0.5;$fin;10u)
    tran 0.08u 1m 500u
    end
plot tran1.v(vout) tran2.v(vout) vs time*1e3
.endc

.end
```



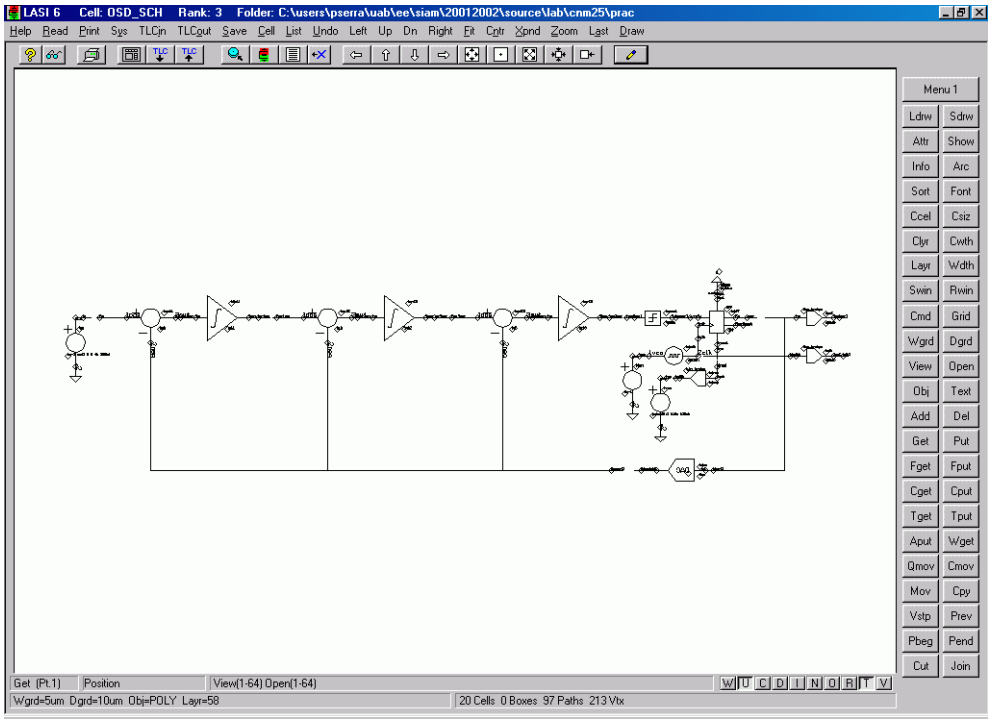
$$\left|\frac{H(f_1)}{H(f_2)}\right|^2 = \frac{(f_2/f_{-3\text{dB}})^2+1}{(f_1/f_{-3\text{dB}})^2+1} \simeq \left(\frac{0.6\text{V}_{pp}}{0.3\text{V}_{pp}}\right)^2$$

$$f_{-3\text{dB}} \simeq 1.7\text{KHz} \leftrightarrow 1.9\text{KHz (theory)}$$

- Single-loop topology [Teme94]:



- Mixed and multi-level schematic:



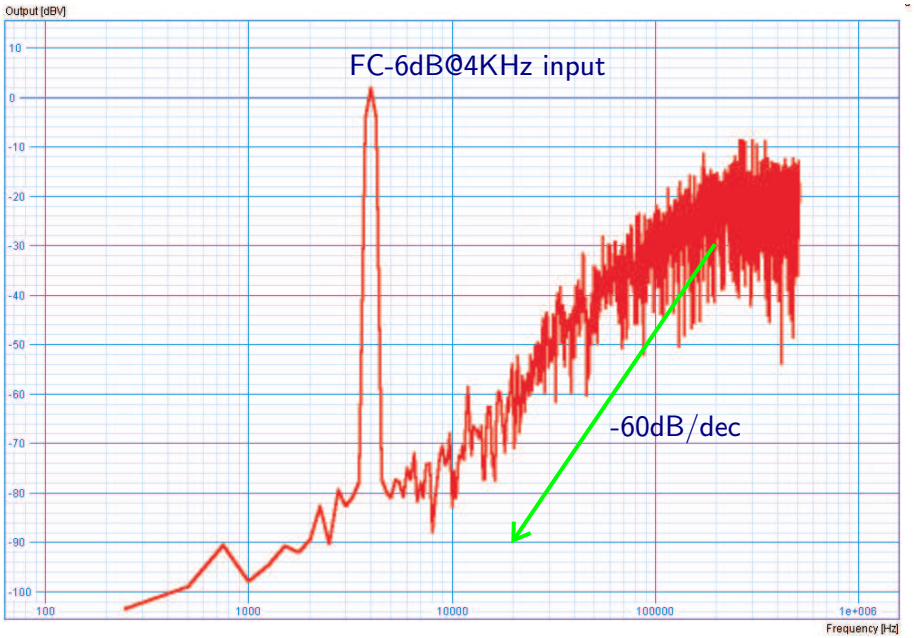
Optimal parameters [Marq98]:

$$\frac{1}{\tau_1} = 0.2 f_s \qquad \frac{1}{\tau_{2,3}} = 0.5 f_s$$

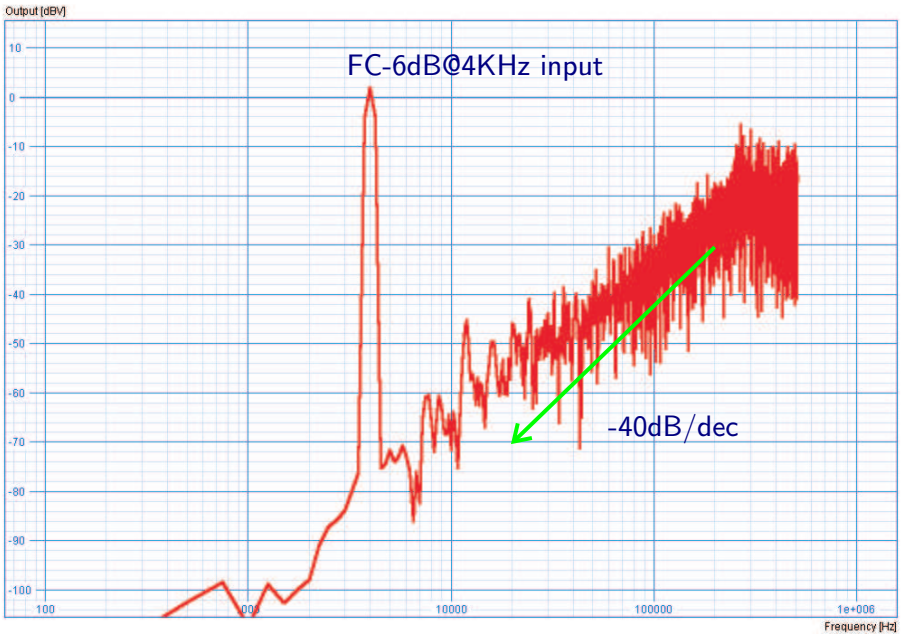
$$f_s \doteq 1024\text{KHz}$$

```
.model int1 int (in_offset=0 gain=205k out_lower_limit=0 out_upper_limit=5 limit_range=100m out_ic=0)
.model quant adc_bridge (in_low=2.49975 in_high=2.50025 rise_delay=10n fall_delay=10n)
.model clkgen d_osc (cntl_array=[0 1] freq_array=[0 1.024e6] duty_cycle=0.5 init_phase=0 rise_delay=10n fall_delay=10n)
```

- Playing with the modulator order...

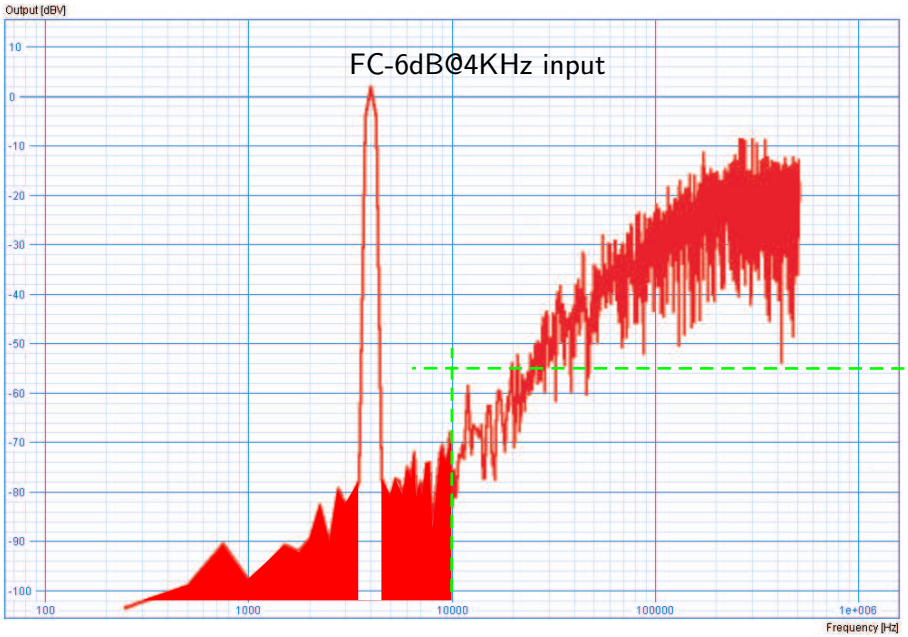


order=3

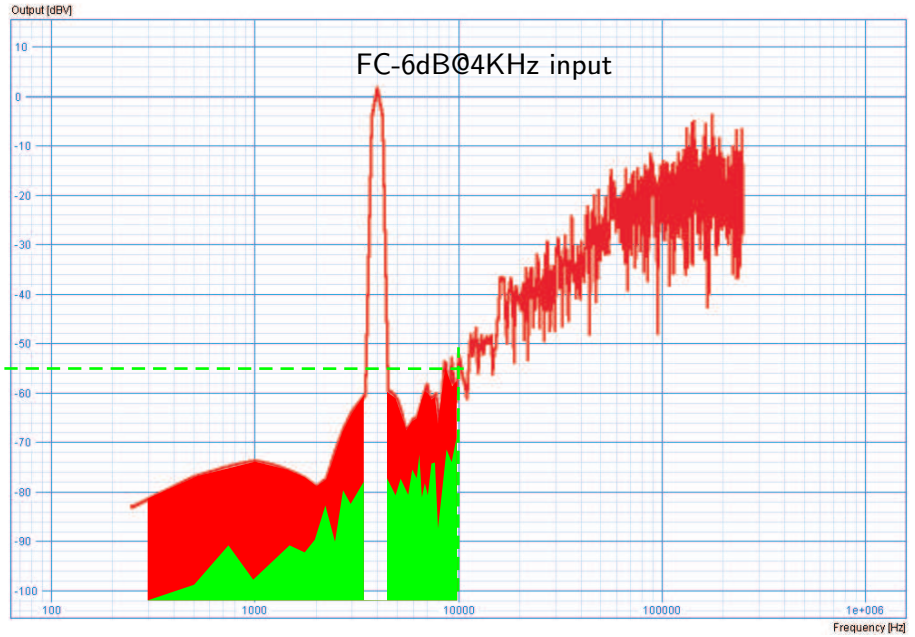


order=2

- . . . and the oversampling ratio:

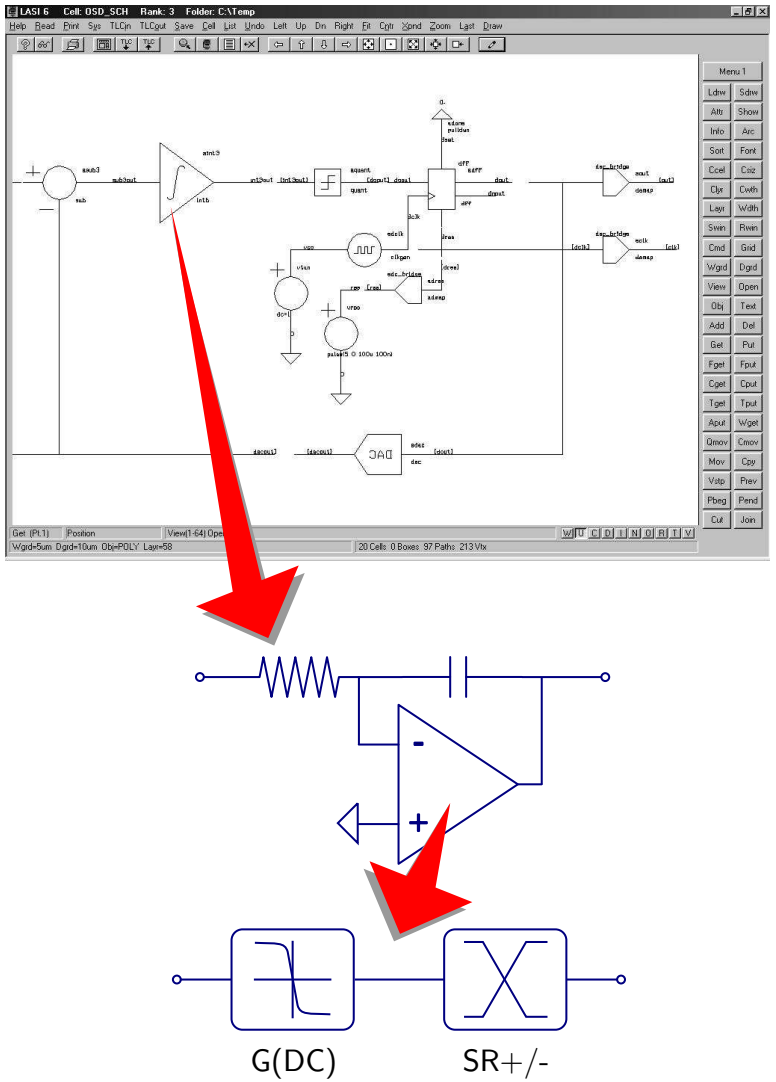


OSR=64

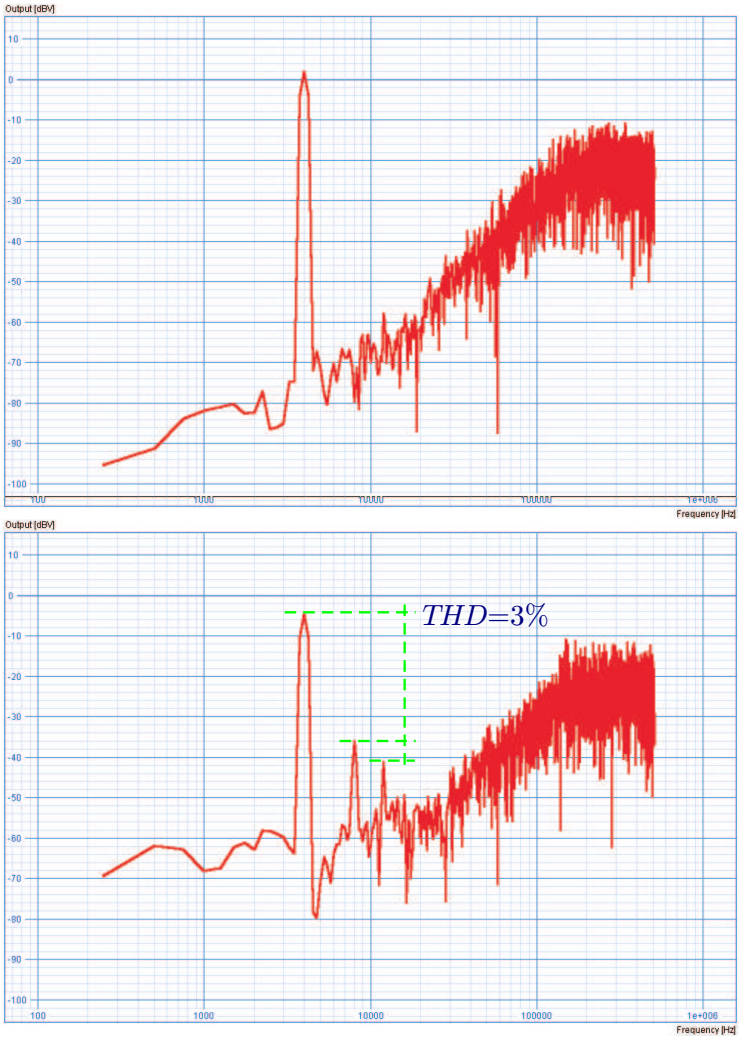


OSR=32

- Quantifying second-order effects:



$G(DC)$=60dB and $SR\pm$=10V/μs



$G(DC)$=20dB and $SR\pm$=10V/μs

- A **free** environment for **VLSI** teaching in **Windows** platforms
- Configurable for **most technologies**
- **Mixed** analog and digital **native** simulation
- Functional/block/transistor-**level** schematics
- Practical **examples** and **tutorials** available
- Also covering **full-custom** design and circuit **optimization**