Mixed integrated circuit design with CMOS VLSI technologies for pre-graduated students

Francesc Serra-Graells[1], Núria Barniol[2]

[1]Institut de Microelectrònica de Barcelona. CNM. Departament d'Informàtica.
Universitat Autònoma de Barcelona. 08193-Bellaterra. Spain.
paco.serra@cnm.es
[2]Departament d'Enginyeria Electrònica. Universitat Autònoma de Barcelona. 08193-Bellaterra. Spain.
nuria.barniol@uab.es

Abstract- The simulation of an oversampling sigma-delta analog-to-digital converter is used in order to introduce in a simple and direct form the need for a mixed analog-digital simulation environment in VLSI microelectronics design. The objective is to provide the students with a freeware PC-based CAD environment with the capabilities of mixed design. Behavioural and transistor-level modelling of analogue and digital circuits and electrical current/voltages signals or nodes defined in the digital domain can be simultaneously used. Trade-offs between simulations at transistor level or at high level are addressed.

1. Introduction

The increasing market demand on integrated system-on-a-chip applications has pushed the necessity of new CAD tools to support the design of heterogeneous and large systems usually involving also mixed circuits. The aim of this work is to supply a simple but flexible tool for the practical teaching of mixed simulation in the VLSI environment.

During the previous semester, electronic engineering students have already been introduced to the basics of integrated analog design [1]. Such practical work is based on the PC free WinVLSI kit [2] and consists on designing a CMOS Miller Operational Amplifier from schematic to layout following a full-custom approach. Prior to that there are two other subjects in which VLSI digital design is already done. In the final year there is one semester related with the design of analog-to-digital converters. Oversampling converters and in particular $\Sigma\Delta$ type are very particular converters in which several concepts have to be assumed by the students and in which there is a need for a mixed simulation environment.

The tool proposed here for mixed analysis is also based on the WinVLSI kit and more particularly on the XSPICE standard [3], an extension of the SPICE language to include both high-level analog and digital models and the required new signal types. Basically, instead of the classic glue strategy involving two simulators working in parallel for each the analog and the digital parts, XSPICE allows new Code Models and Node Type using a kind of System-C description. After recompiling the complete SPICE simulator with such new code, the new primitives allow true native analog and

digital simulation. Obviously, speed improvement is still reached using two internal engines, an event driven algorithm and the classic solver for the digital and analog domains, respectively.

2. Design Example: An Oversampling SD ADC

The particular topology chosen is a third order 1-bit converter (*Figure 1*). The working principle of the circuit is based on the high gain of the transfer function of the circuit (integrators) and the negative feedback of the digital-to-analog converter. Due to the oversampling and the modulation it can be demonstrated that the quantization noise of the converter will be reduced by the digital circuitry at the output of the system (not shown on the figure). In fact the oversampling expands the noise power spectral density, thus reducing it in the signal bandwidth, and the ΣΔ transfer function acts as a high pass filter for the noise (noise shaping function), translating the noise to higher frequencies.

After some exercises using Simulink (MATLAB) for understanding the advantages of oversampling and the behavior of the ΣΔ converter, the students are asked to use the WinVLSI simulator to learn the specific procedure for the simultaneous simulation of analog and digital systems. The objective of the practical work is to demonstrate to the students the importance of the high level modelization for all the components of a system to reduce the simulation time and also show the different requirements for simulation of analog (in which accuracy is desired) and digital (reduce simulation time). Finally oversampling converters will show problems arising from the different time constants of the high switching and the low frequency of the input signal.

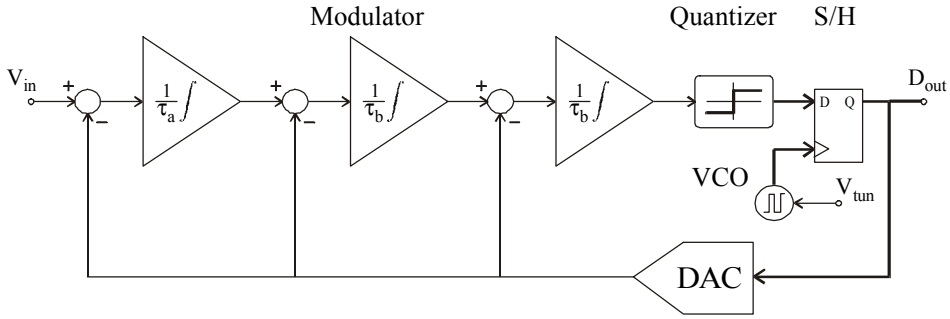


Figure 1. Electrical schematic of a third order one-bit sigma-delta converter. Note that the signals on the right side (latch, clock and digital/analogue converter) are in the digital domain (thick lines) while the rest of the circuit (integrators and quantizer) corresponds to classical v/i analog signals (thin lines).

The student work is related with the determination of the oversampling ratio, the evaluation of the time constants for each of the integrators to have the adequate signal bandwidth and after some simulation to determine the static behavior of the converter. The non-linear model shown partly in *Figure 2* (only one integrator, the quantizer or comparator, the latch and the digital-to-analogue converter from the full third order

sigma-delta converter in *Figure 1* is shown) is used to perform these simulations. After that the students are asked to design the comparator as full custom (low level synthesis) and again simulate the converter.

The macro models shown in *Figure 2* describe all the analog and digital circuits as behavioral level elements using Xspice code models called new a-type SPICE macro elements. Only in the case of the comparator, it is written the macro model and the subcircuit using the transistor-level description. Also note the existence of bridge elements for unidirectional conversion from one domain (analog or digital) to the other domain (digital or analog).

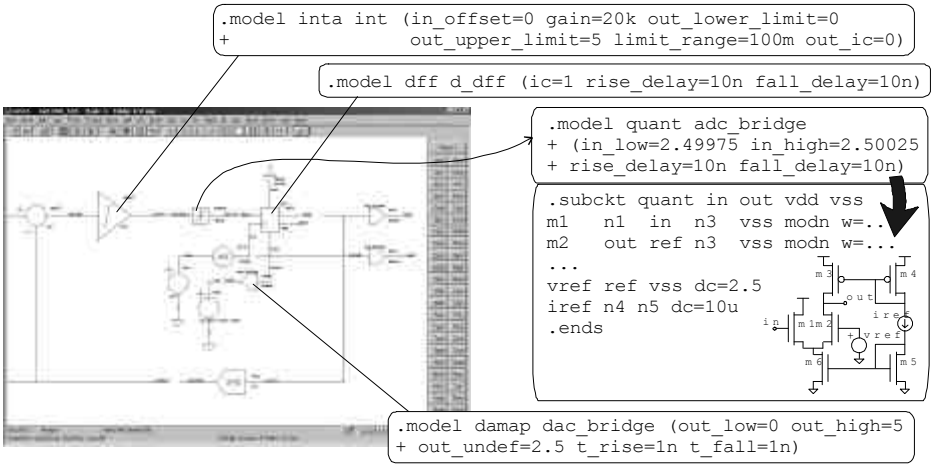


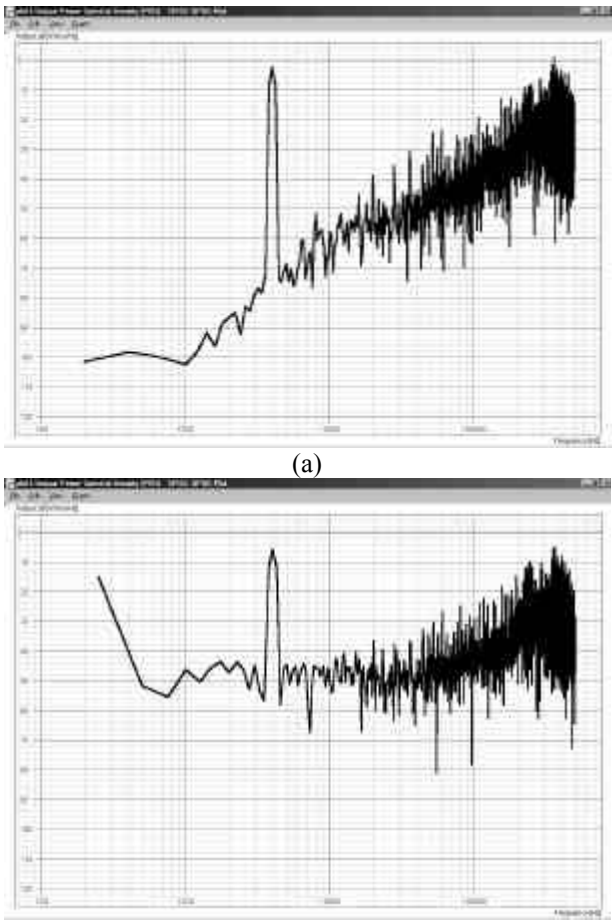
Figure 2. Mixed signal simulation example: On the left there is a screenshot of partly of the schematic to simulate. On the right there are the functional definitions of each component (integrator, latch and comparator). Note that the comparator is described in two ways (i) the high level or macro model and (ii) the description for a transistor-level simulation (a simple comparator is depicted in the inset). Also the definition of the bridges between the digital and the analogue simulation modes are described.

3. Simulation Results

In *Figure 3* there are two power spectral densities obtained by one of the students using an steady-state harmonic analysis from a transient simulation. The input signal is a 4 kHz@1V, sampled at 1,024 MHz, with a time vector of 8ms. Under these conditions spectral plots of 8192 samples are obtained.

From *Figure 3(a)* it is clear that the typical quantization noise modulation at high frequencies of the ΣΔ converters is obtained. In the case of a simulation under a transistor-level models (*Figure 3(b)*) there are two remarkable points: (i) simulation time is much more longer (at least twice = more than 20 minutes in a 1GHz Pentium III machine) and (ii) convergence problems due to the new complex and non-linear equations introduced by the MOSFETs appear. Noise-like spectrum comes from the

distortion itself (due to a non ideal comparator with a poor settling time and DC gain), but also from the simulation convergence problems at transistor level.



(a)

(b)

Figure 3. Power spectral density of the sigma-delta modulator with a 4 kHz, 1V sinusoidal input and with an oversampling frequency of 1,024 MHz. (a) Simulation results with the high level model and (b) simulation results with a transistor-level defined comparator.

References

1 F.Serra-Graells, N.Barniol. *Design of analog integrated circuits: freeware PC-based CAD for student practices*. Microelectronics Education. Proc. 3rd European Workshop on Microelectronics education. Kluwer, 2000. Pp289-292.

2 F.Serra-Graells, *WinVLSI 1.31: A Free Windows CAD Framework for Mixed Full-Custom VLSI Design, CNM25 Kit Edition Manual*, http://www.cnm.es/~pserra/winvlsi, 2002

3 F.L.Cox et al., *XSPICE Software User's Manual*, Georgia Institute of Technology, 1992