7. Integrated Data Converters

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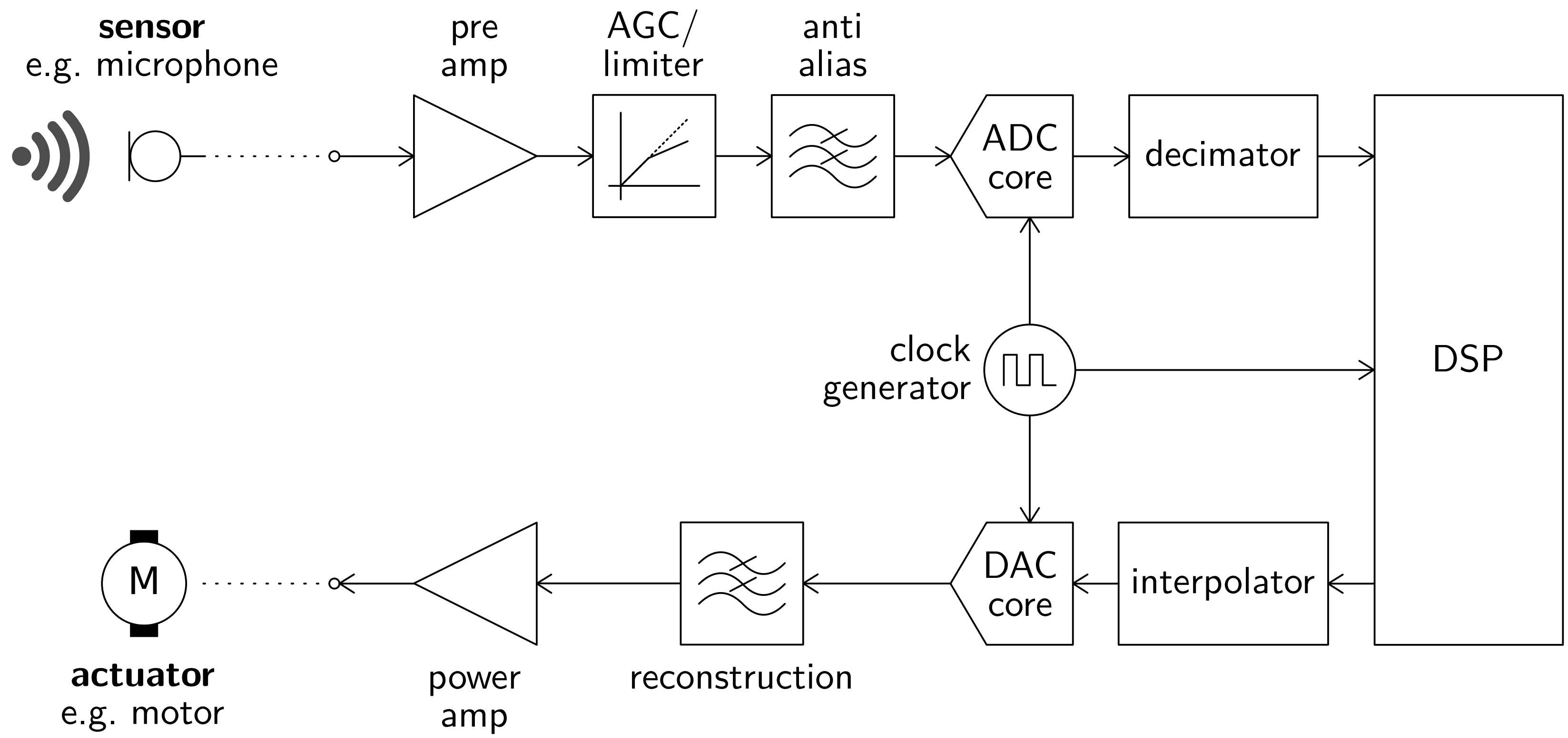
ADC vs DAC

- General **mixed-mode** frontend for **smart transductors**:



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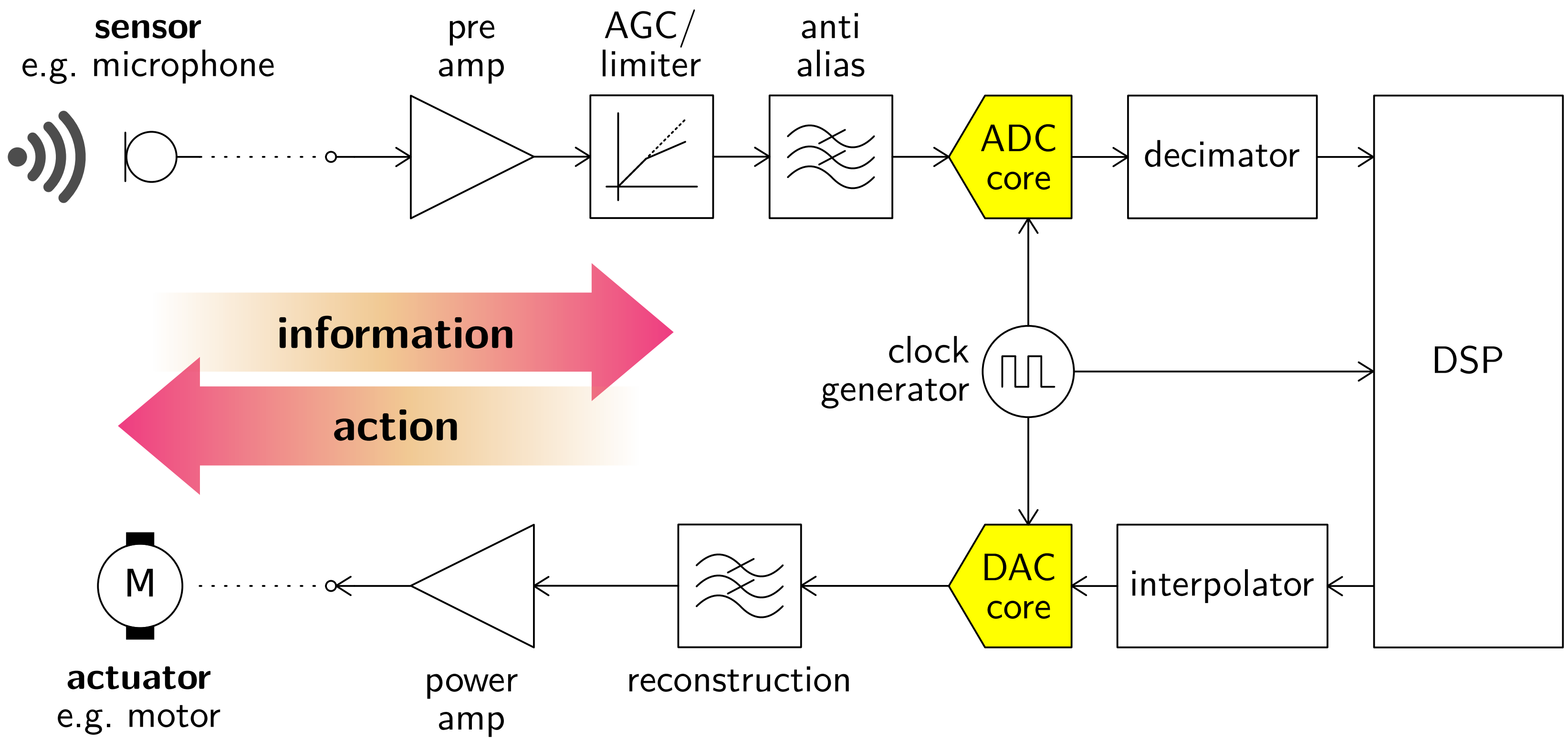
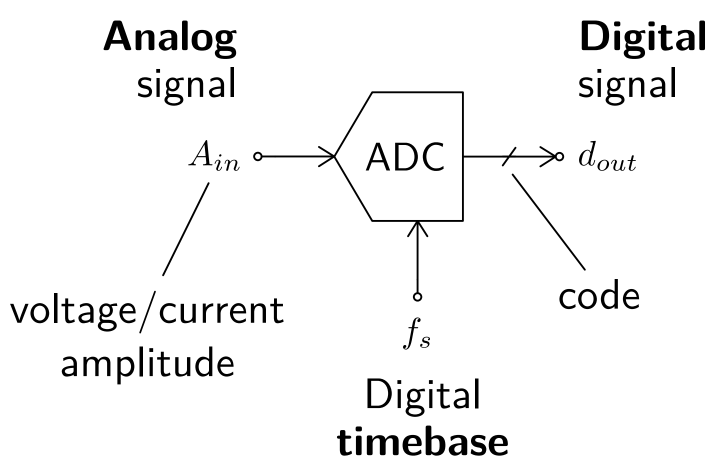
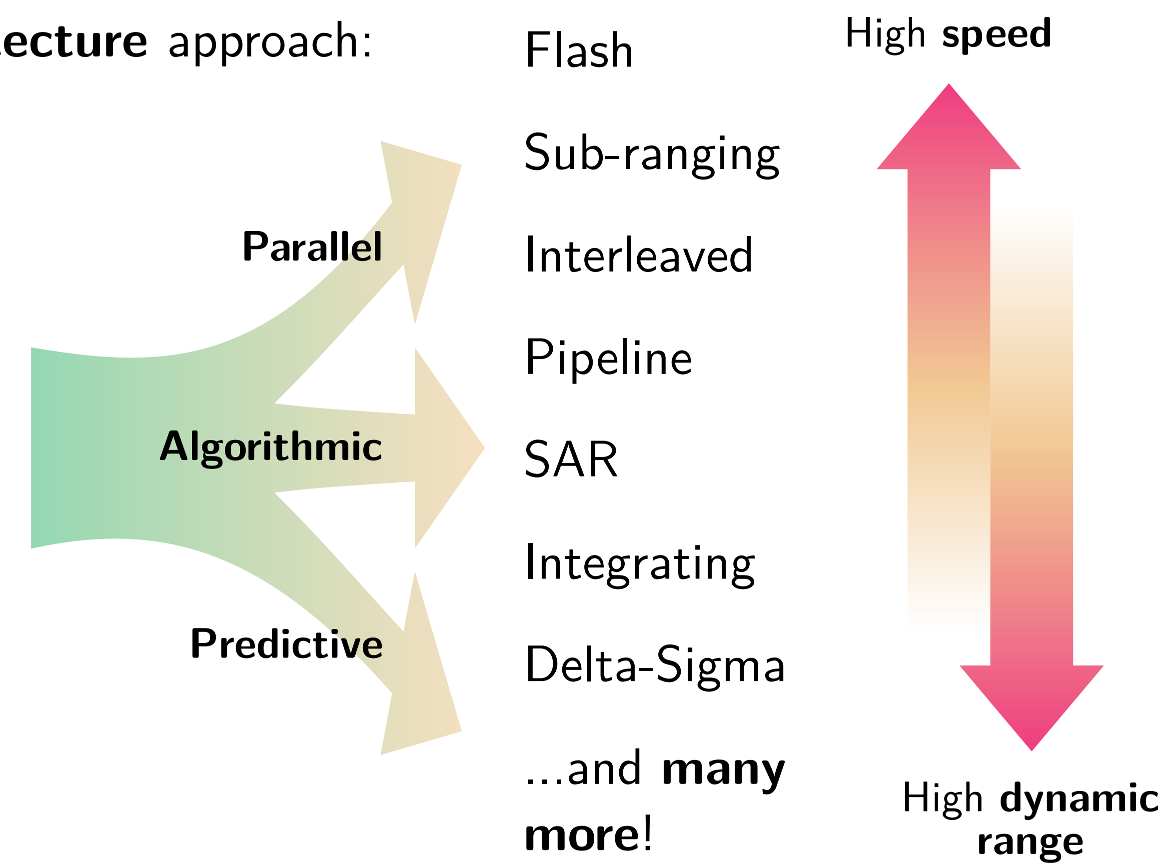


...typically **ADC** is more performance demanding!

ADC Families

- Classification based on **architecture** approach:





- Distinctive **characteristics**:
  - Feedforward vs feedback control
  - Single vs multiple stages
  - Amplitude vs time domains

- Typically **mixed** solutions...

ADC Evolution

$$FOM_S \doteq SNDR_{max} + 10\log\frac{f_{nyq}}{2P_D} \qquad FOM_W \doteq \frac{P_D}{f_{nyq}\cdot 2^{ENOB}}$$

$FOM_S \simeq 85\text{dB}$ $\qquad FOM_W \simeq 5\mu\text{J/conv-step}$

EPSCO DATRAC, B.M. Gordon, 1953
11-bit 50KSps 500W SAR ADC
0.5m x 0.4m x 0.65m, 70Kg
Vacuum tube technology

W. Kester, *Analog-Digital Conversion*
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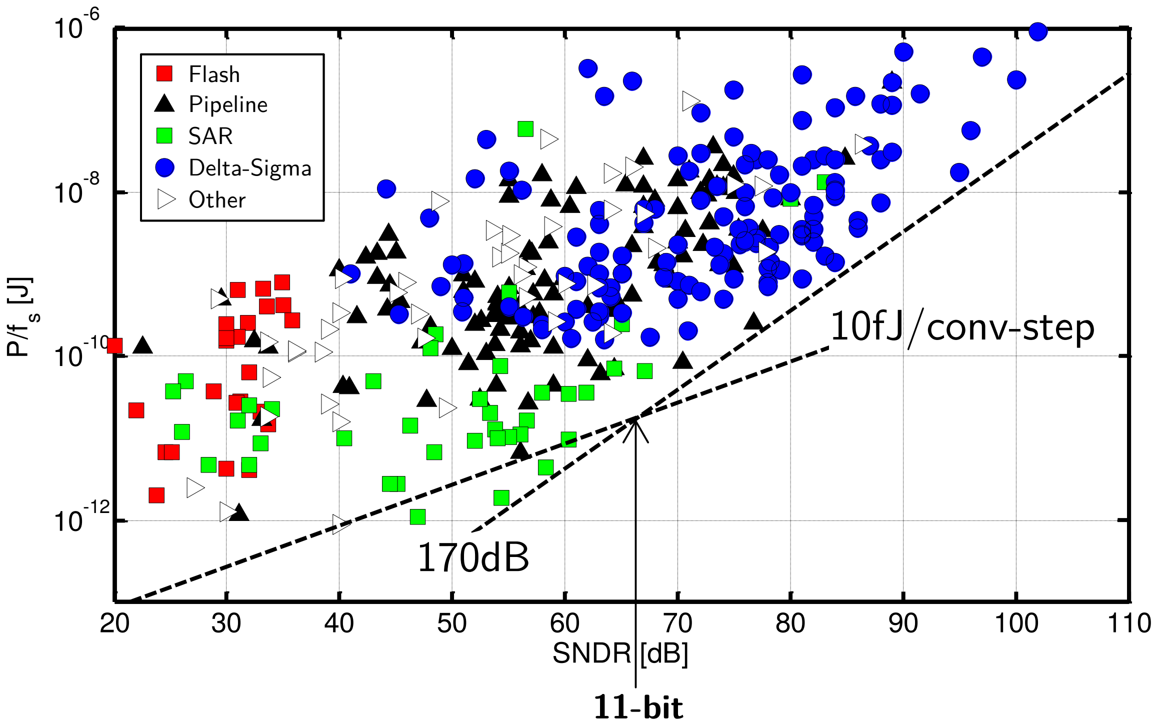
+60years

State-of-art ADC

Solid-state technologies

B. Murmann, *ADC Performance Survey*

http://www.stanford.edu/~murmann/adcsurvey.html



ADC Evolution

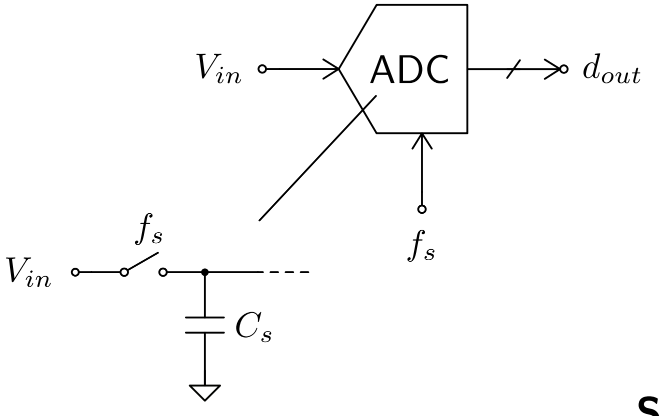
- **Performance** enhancement:
  - Architecture strategy
  - Circuit design
  - Integration technology
- Still room for further **improvement?**

$$SNR_{max} = \frac{(V_{FS}/2\sqrt{2})^2}{KT/C_s}\frac{f_s}{f_{nyq}}$$

$$P_{min} = \underbrace{C_s V_{FS} f_s}_{I_{DD}} V_{DD}$$

$$P_{min}|_{V_{FS}\equiv V_{DD}} \simeq C_s f_s V_{FS}^2$$

$$E_{min} \doteq \frac{P_{min}}{f_{nyq}} \equiv 8KT\, SNR_{max}$$



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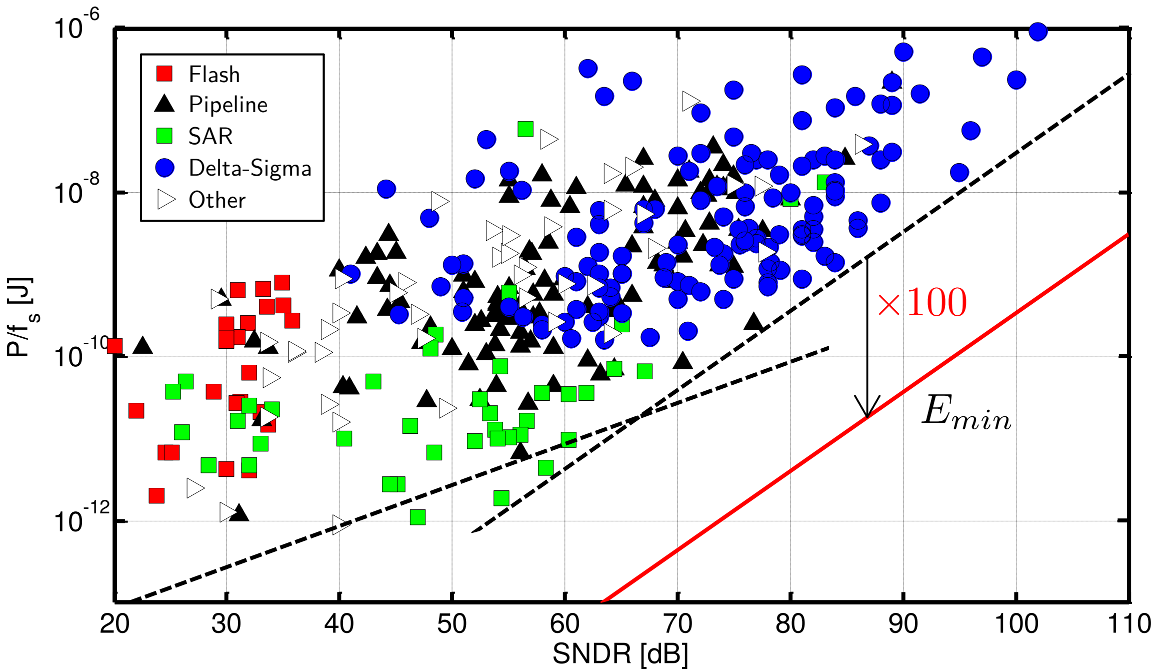
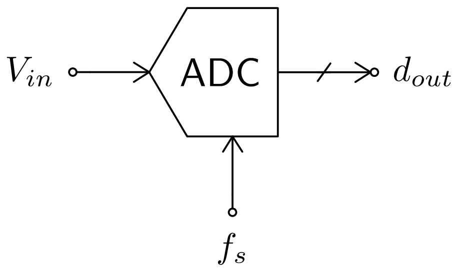
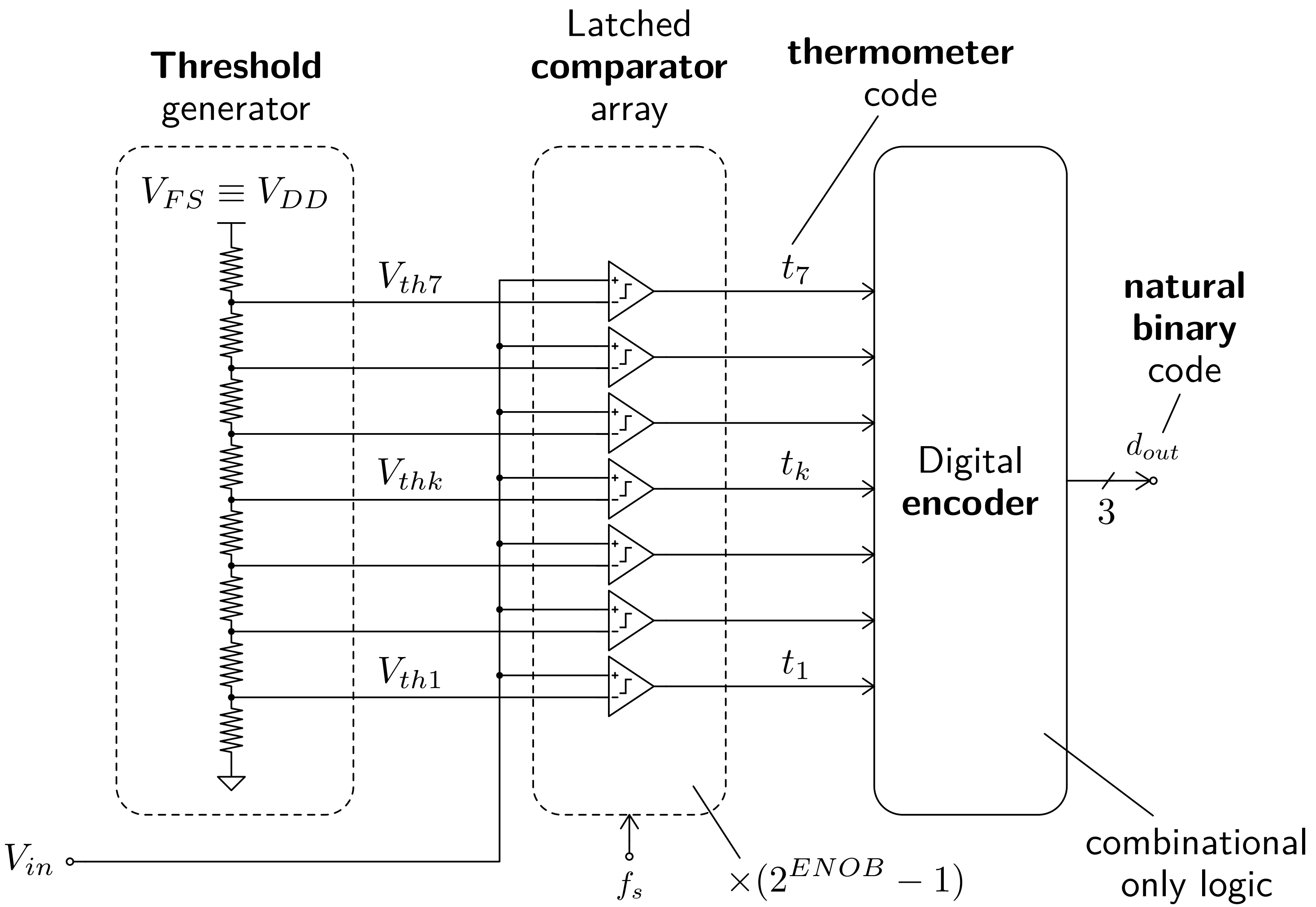


Basic Flash Architecture



- Building **blocks**:

e.g. **single-ended** 3-bit flash ADC



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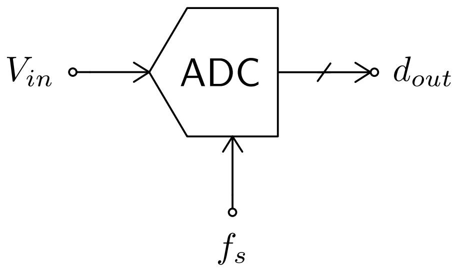

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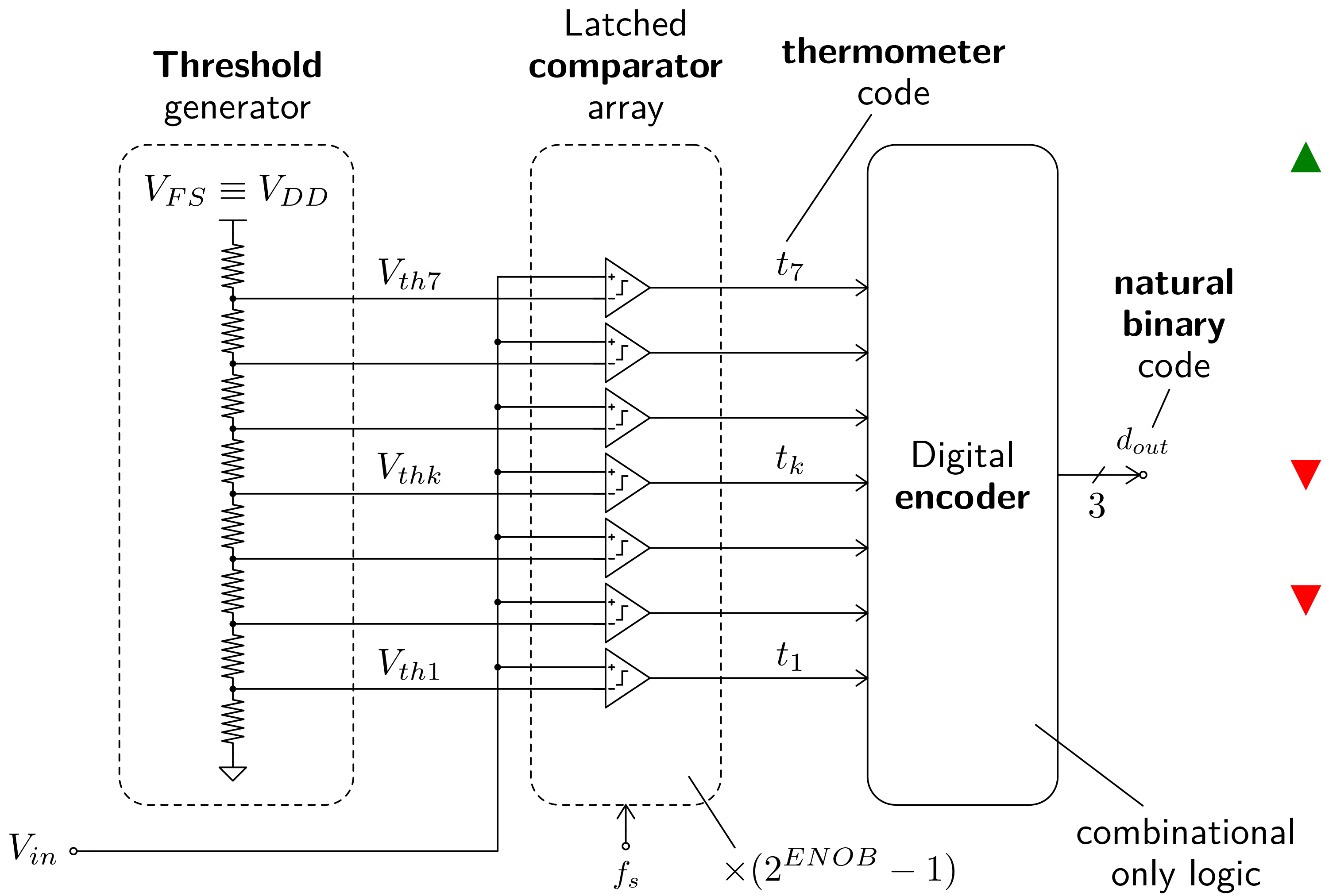
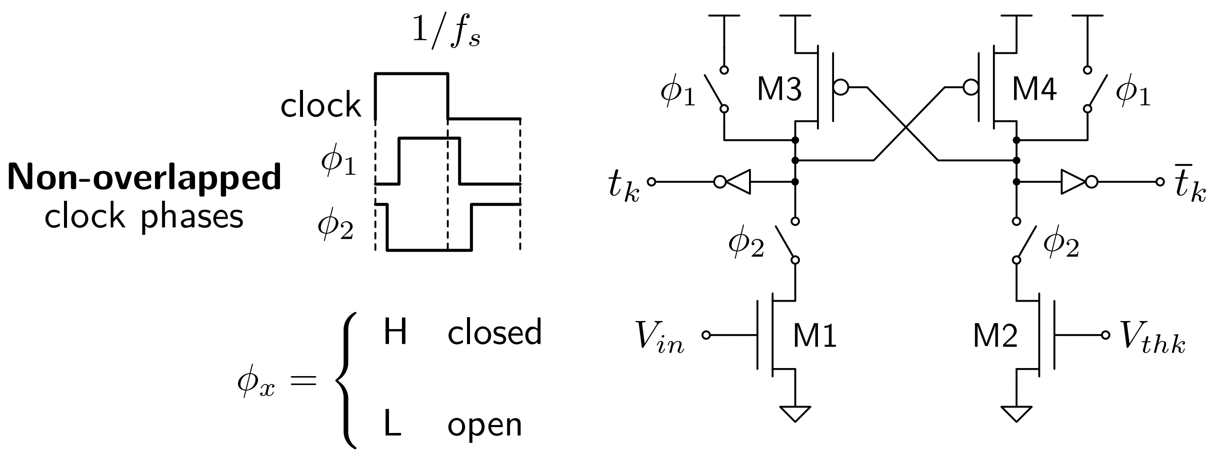


- ▲ 1 clock cycle conversion **time**
- ▼ Area and power **scaling** by 2^{ENOB}
- ▼ Distortion due to technology **mismatching**

Latched Comparator Design

- Compact **CMOS** circuit:



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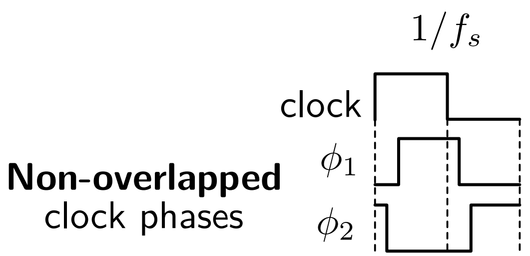
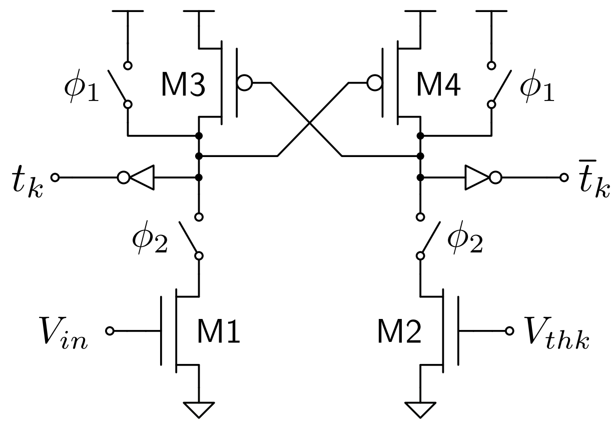
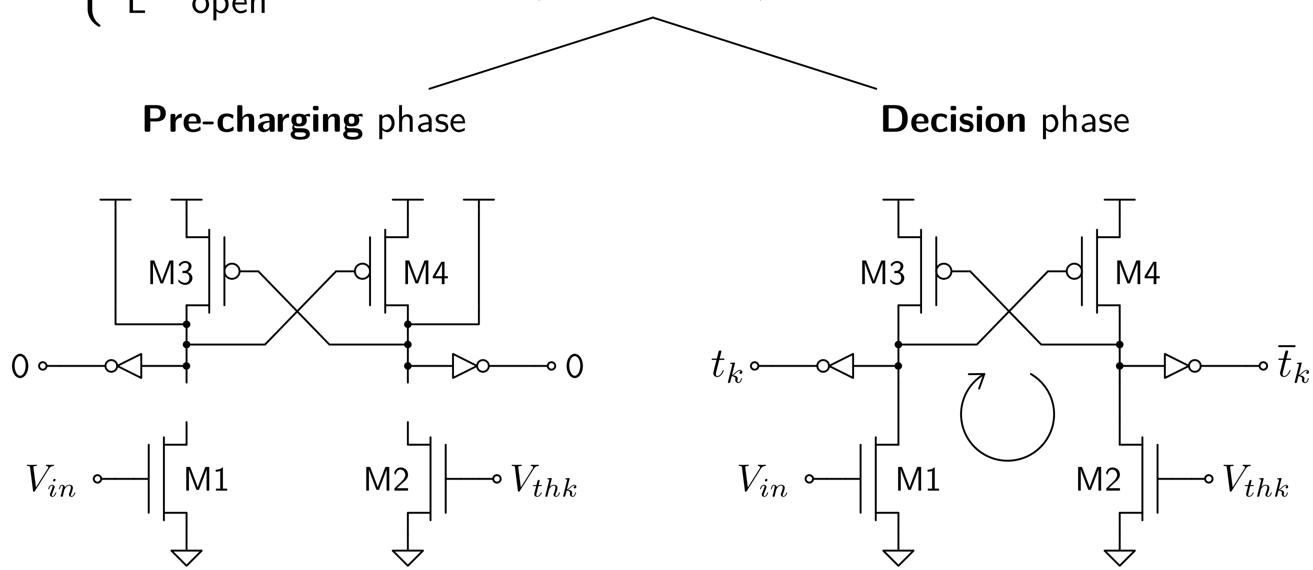


$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$



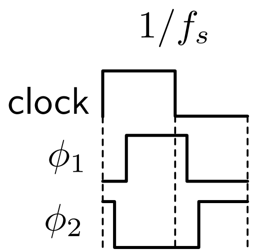
- ▲ **High-speed** operation
- ▼ Each comparator crosses at **different** threshold V_{thk}
- ▼ Threshold voltage **offset**?



- **Positive feedback** to speed-up comparison
- **Symmetrical** loading

Comparator Optimization

- By attaching an array of **level shifters**:



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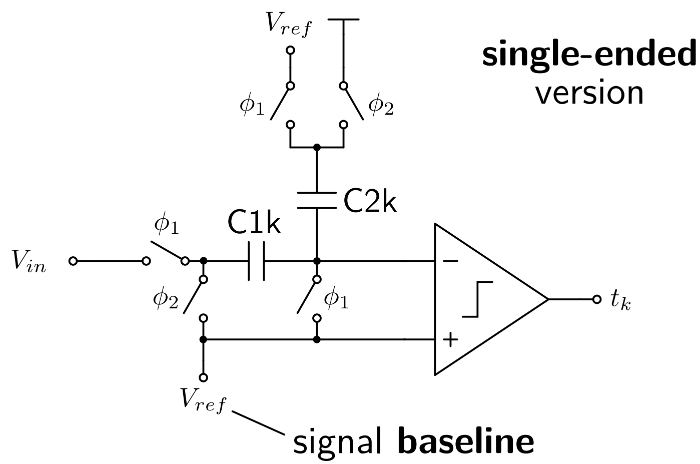

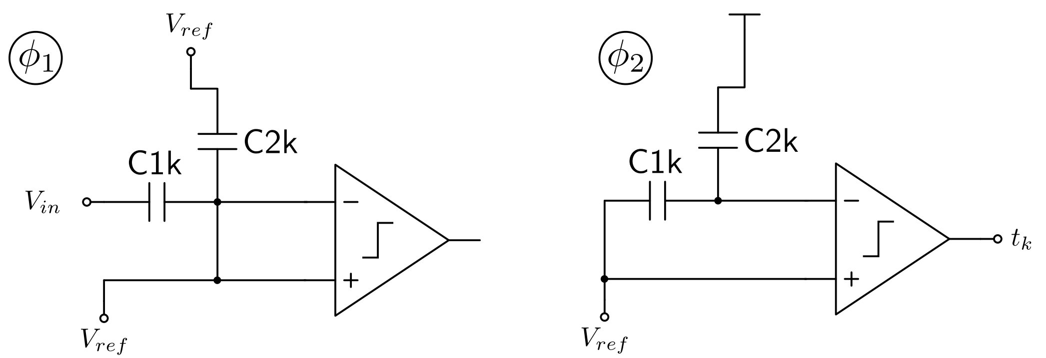

$$t_k = sign\left[V_{ref} - \left(V_{ref} + \frac{C_{1k}}{C_{1k}+C_{2k}}(V_{ref} - V_{in}) + \frac{C_{2k}}{C_{1k}+C_{2k}}(V_{DD} - V_{ref})\right)\right]$$

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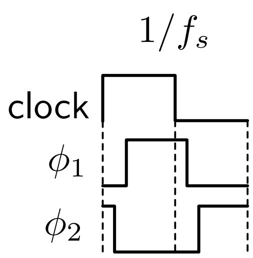

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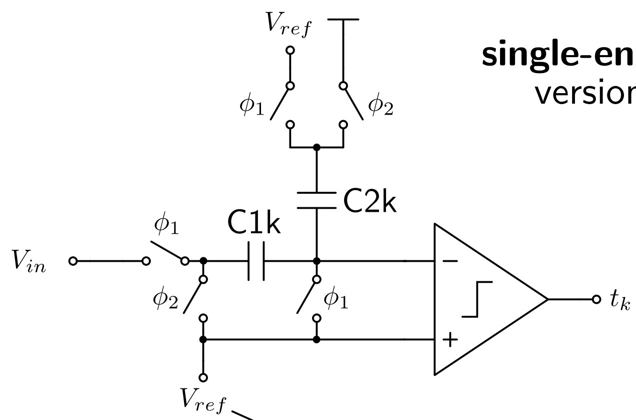
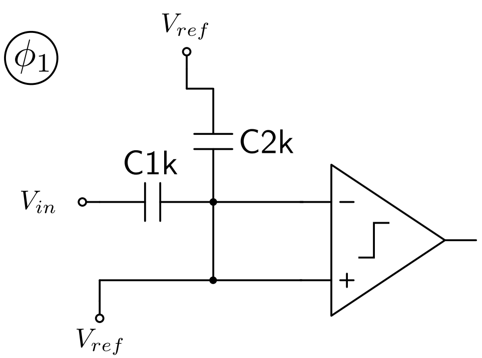
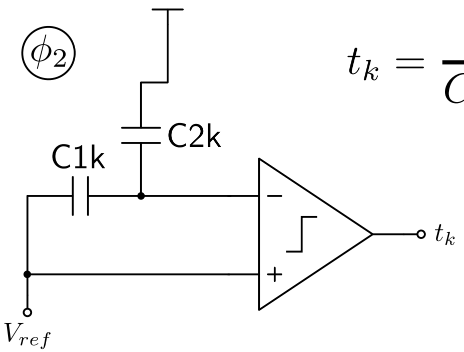


single-ended version

signal **baseline**

- ▲ All comparators latch at the **same** level (V_{ref})
- ▲ **Single** comparator design
- ▲ Low quiescent **power** (resistor-less thresholds)
- ▼ Capacitor **area** overhead
- ▼ Input **capacitance** increased
- ▼ **Slower** operation





$$t_k = \frac{C_{1k}}{C_{1k}+C_{2k}} sign\left[(V_{in}-V_{ref}) - \frac{C_{2k}}{C_{1k}}(V_{DD}-V_{ref})\right]$$

effective signal

effective k-threshold

$$t_k = sign\left[V_{ref} - \left(V_{ref} + \frac{C_{1k}}{C_{1k}+C_{2k}}(V_{ref}-V_{in}) + \frac{C_{2k}}{C_{1k}+C_{2k}}(V_{DD}-V_{ref})\right)\right]$$

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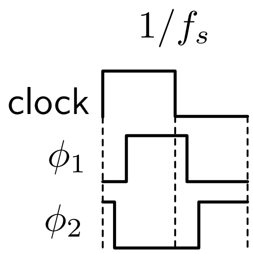

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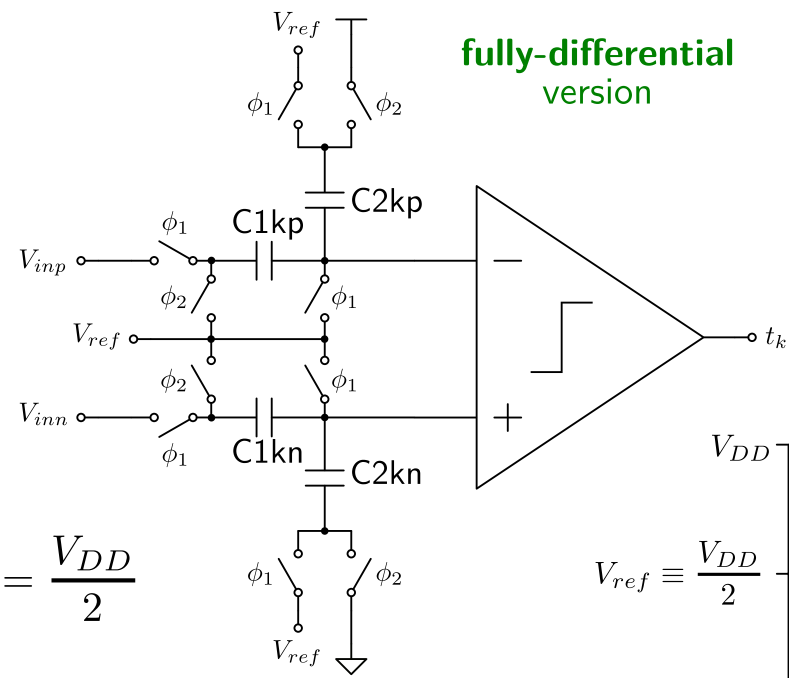
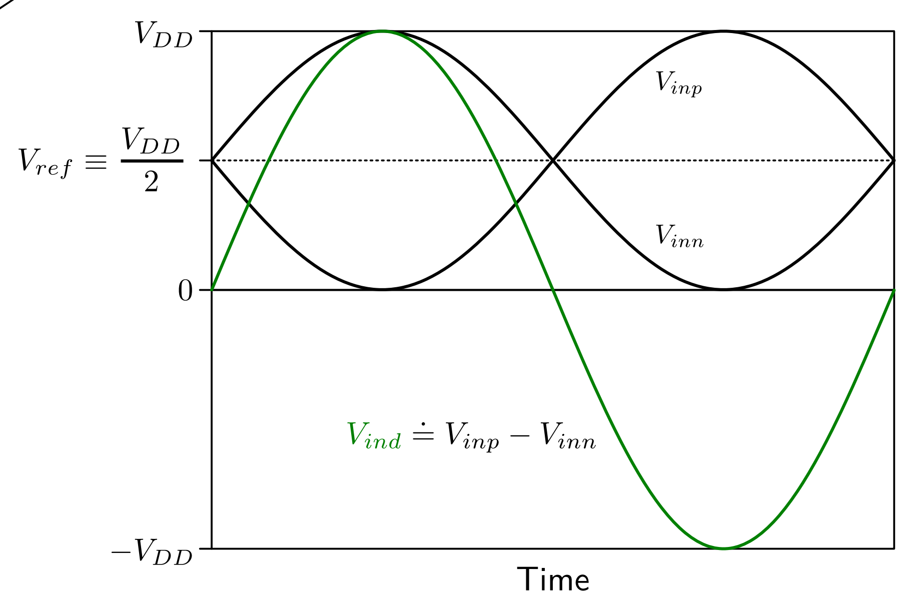


$$V_{ref} = \frac{V_{DD}}{2}$$

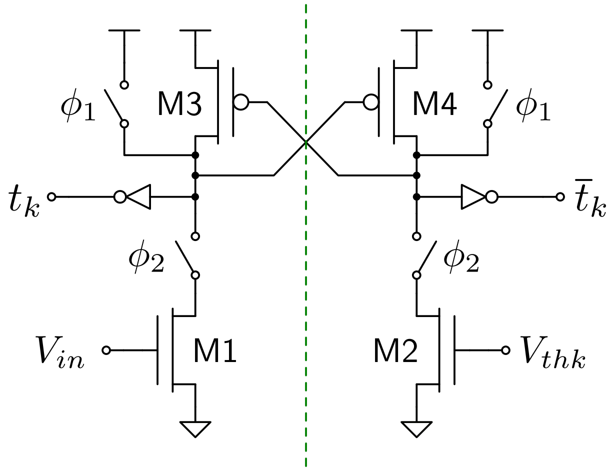
- ▲ Interference **rejection**
- ▲ **Full-scale** extension (+6dB)
- ▲ **SNR** enhancement (+3dB)
- ▲ **Distortion** cancellation (even harmonics)



- ▼ **Area** and **power** overheads (x2)
- ▼ Higher **symmetry** requirements

Comparators Offset

- MOSFET V_{TH} **mismatching** effects:



$$\sigma^2(\Delta V_{off}) = \sigma^2(\Delta V_{TH1,2}) + \left(\frac{g_{mg3,4}}{g_{mg1,2}}\right)^2 \sigma^2(\Delta V_{TH3,4})$$

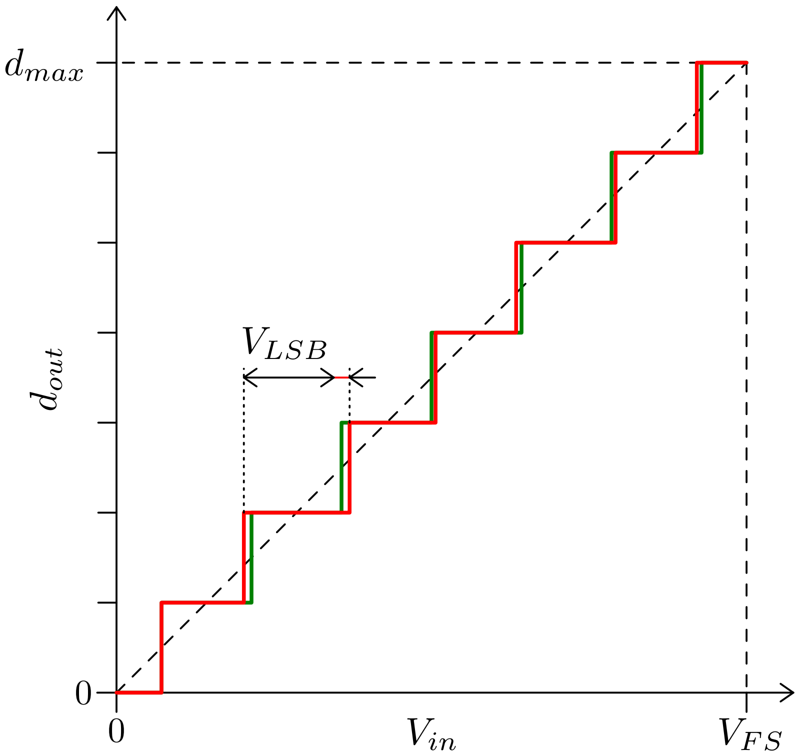
$$\sigma(\Delta V_{off}) \simeq \sigma(\Delta V_{TH1,2}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$$

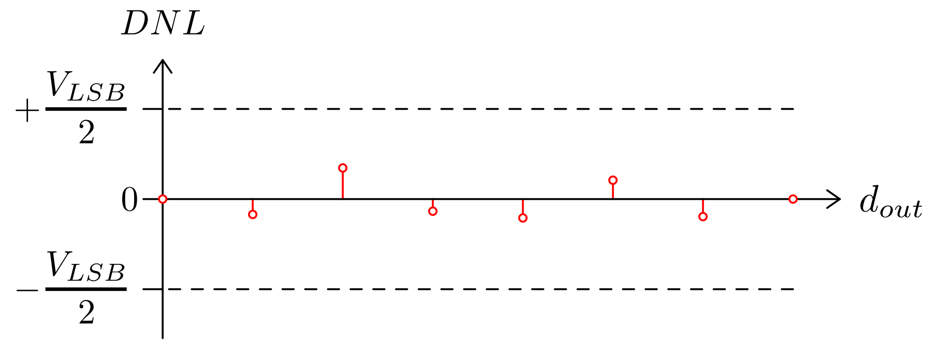
CMOS **technology**

$\left(\frac{W}{L}\right)_{1,2} \gg \left(\frac{W}{L}\right)_{3,4}$

Pelgrom's Law

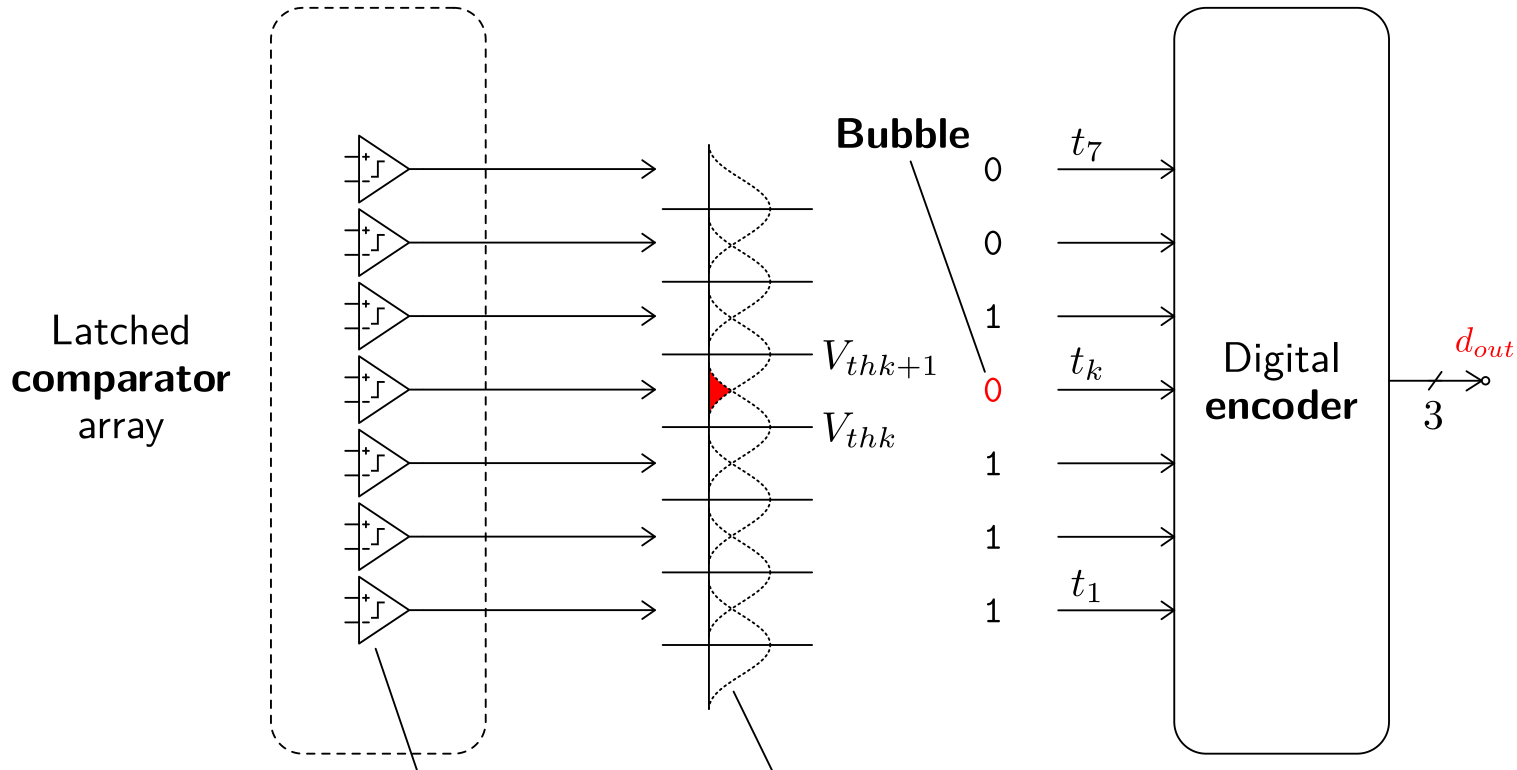
- Distortion due to **DNL**





Comparators Offset

- Thermometer code **bubbles**!

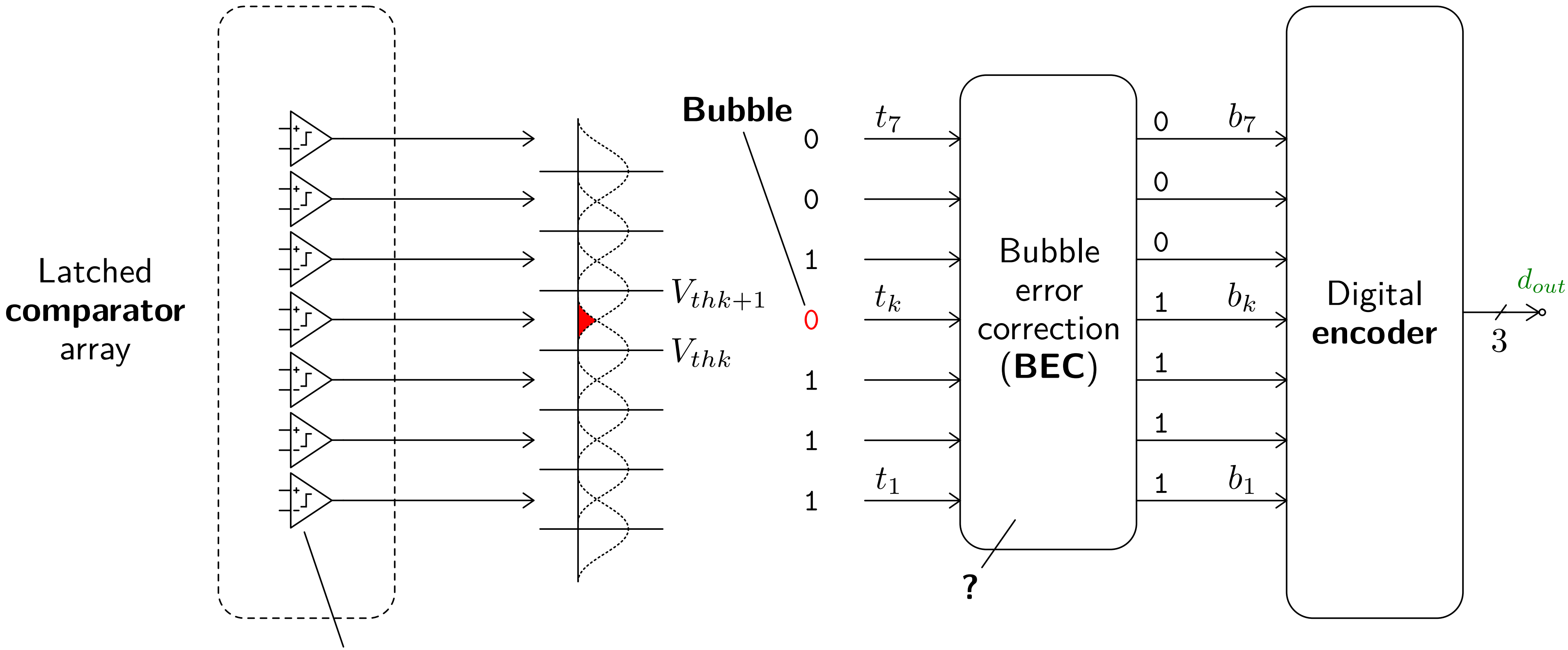


$$\sigma(\Delta V_{off}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$$

- **Error** propagation at encoding...
- Large device **area** (WL) and input **capacitance** penalties

Comparators Offset

- Thermometer code **bubbles**!
- **Digitally assisted** analog design:



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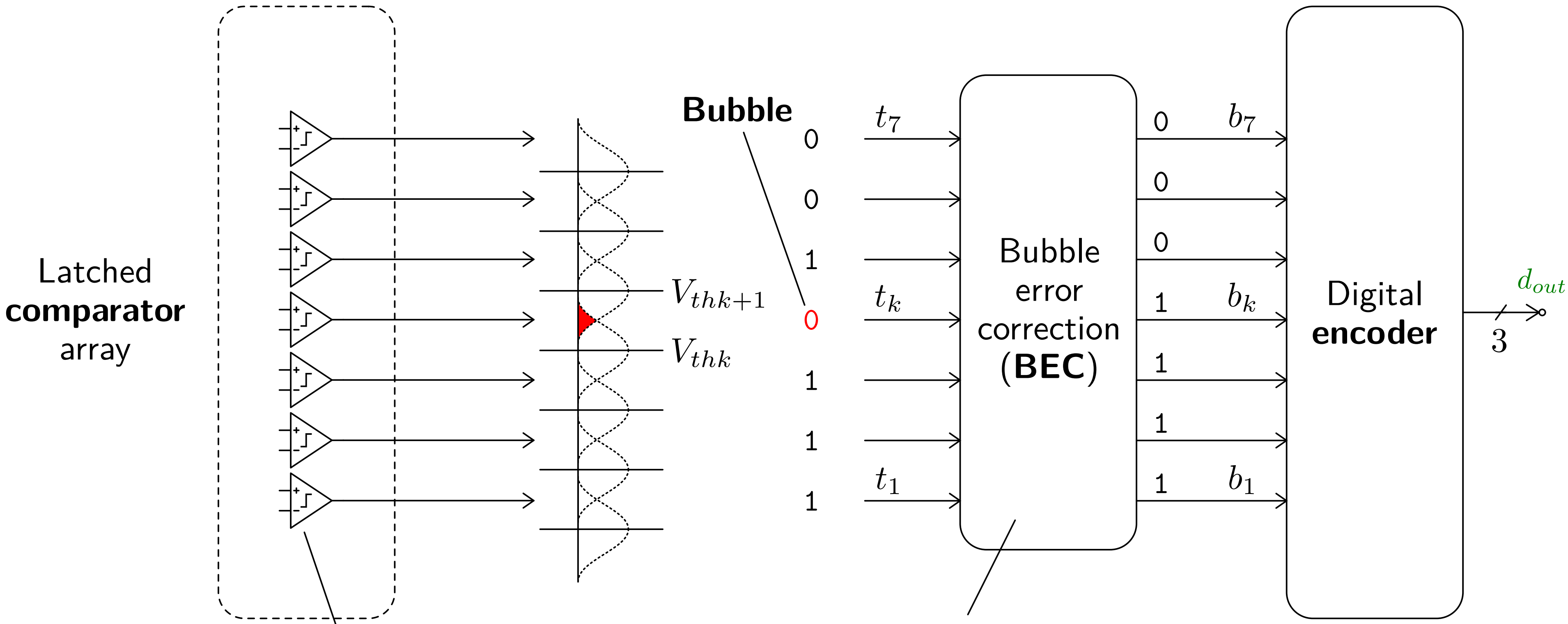


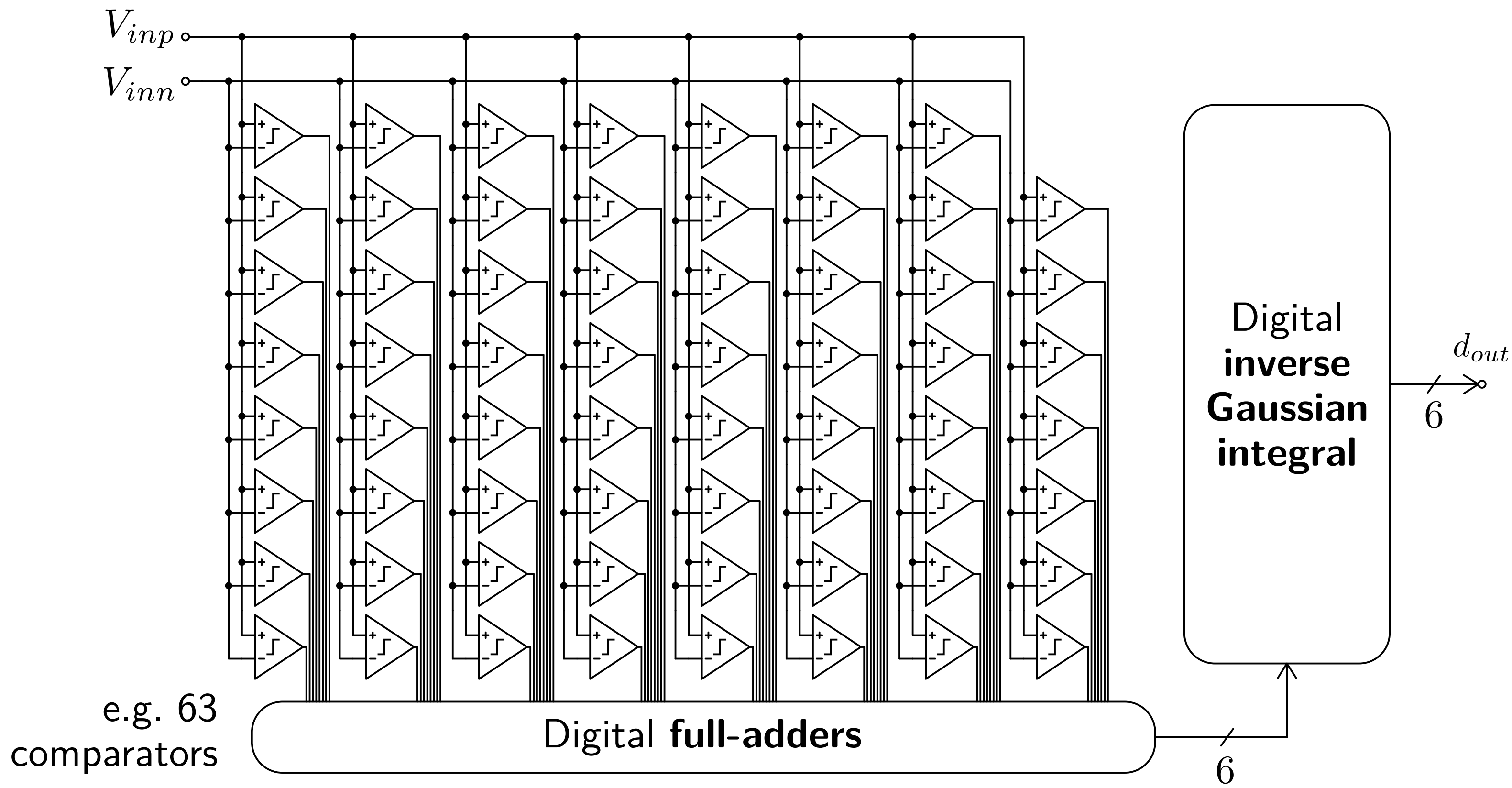
$$\sigma(\Delta V_{off}) = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$$

(WL) large enough to limit bubble **distance** to 1 code:

t_{k-1}	t_k	t_{k+1}	b_k
0	X	X	0
1	X	0	t_k
1	X	1	1

Comparators Offset

- More on digitally assisted analog design: **an stochastic flash ADC**



S. Weaver, B. Hershberg and Un-Ku Moon, *Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells*, IEEE Transactions on Circuits and Systems I, 61(1):84-91, Jan 2014

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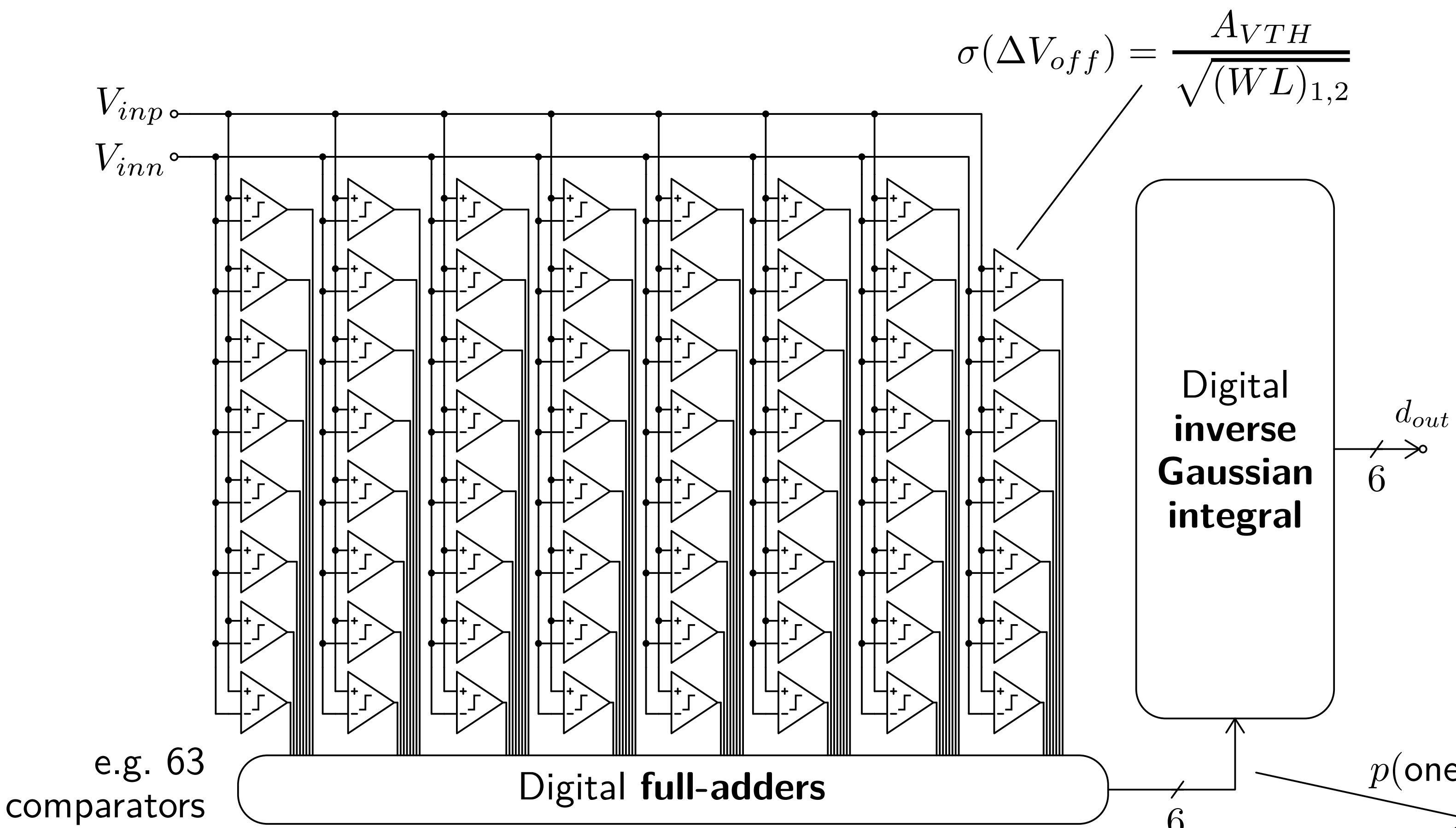
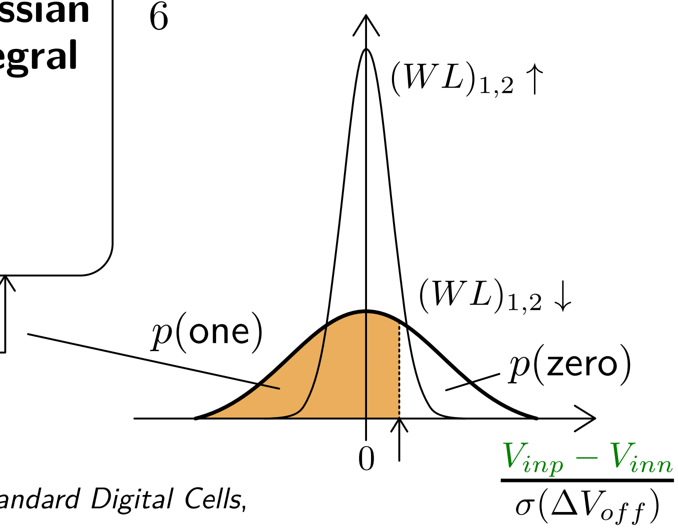


- ▲ Almost **digital**
- ▲ **Compact** area
- ▼ **Non-linearity** compensation required
- ▼ **Power** consumption



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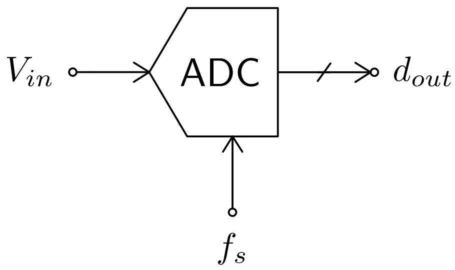
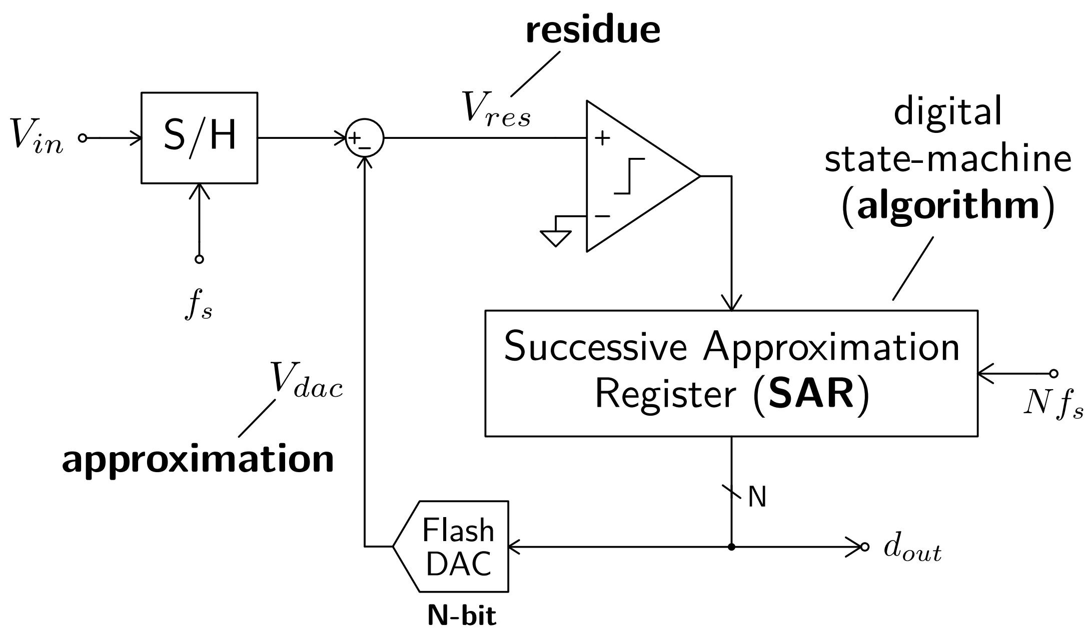
Successive Approximation ADC



- Building **blocks**:



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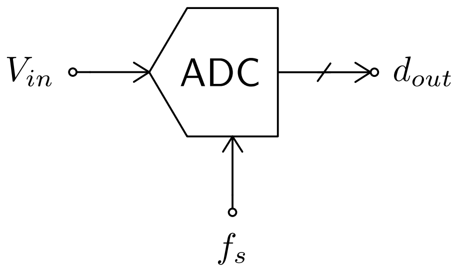

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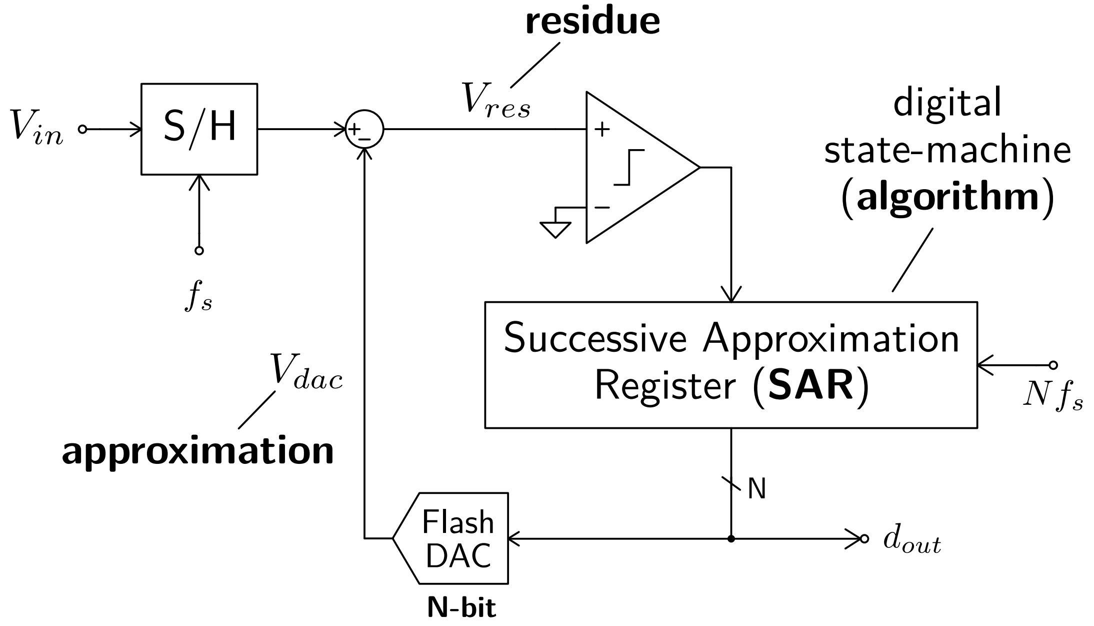
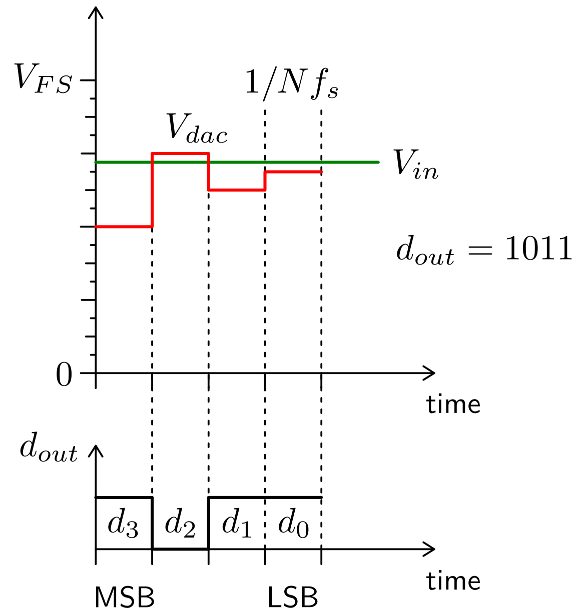


e.g. **4-bit** SAR ADC



▲ Analog **minimalist**

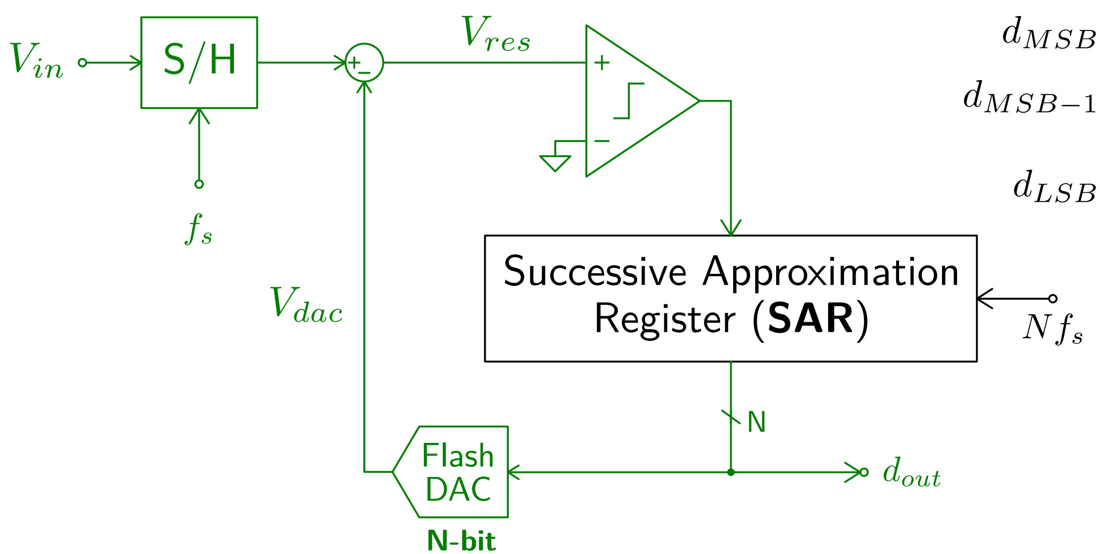
▲ Very **low-power** consumption

▼ **Speed** requirements (xN)

▼ Performance limited by **flash DAC**

Successive Approximation ADC

- **Circuit** implementation:



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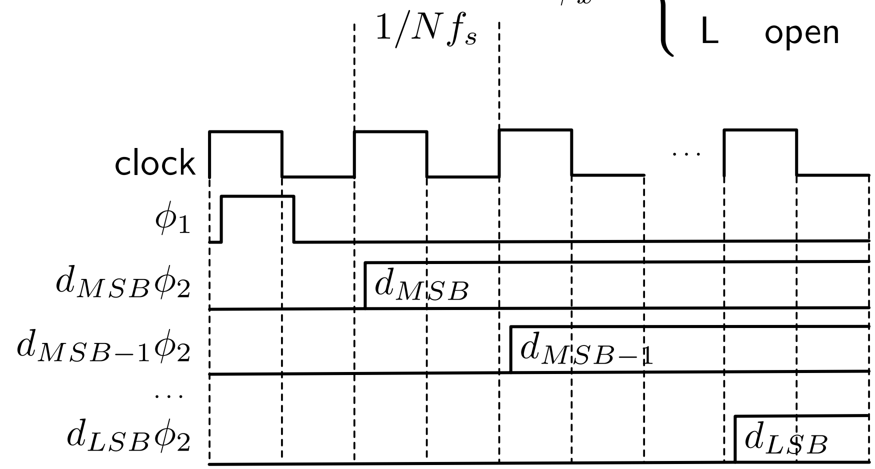
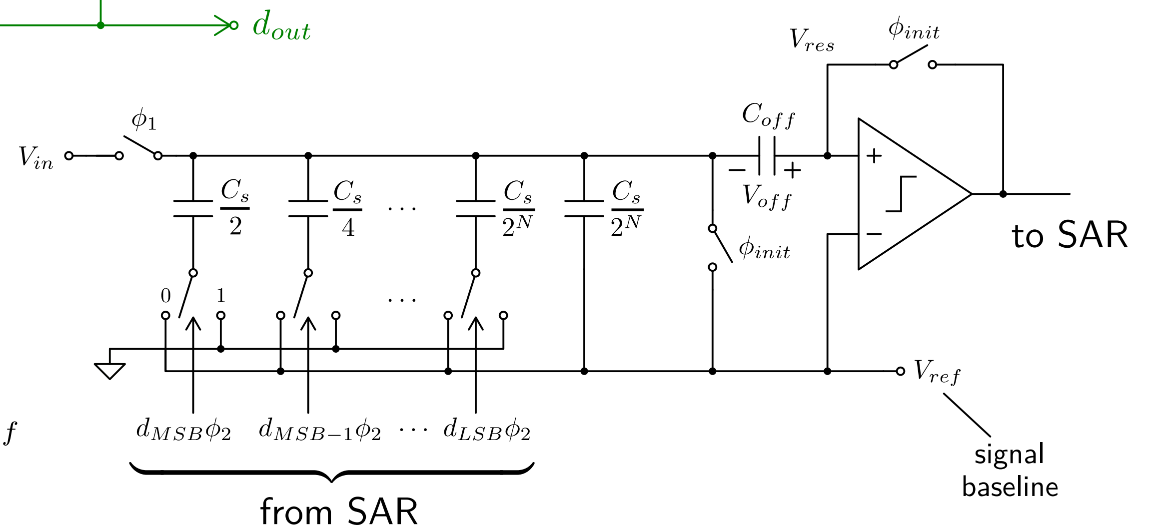


$$V_{FS} \equiv 2V_{ref}$$

single-ended version

$$\frac{C_s}{2^N} + \sum_{i=1}^{N} \frac{C_s}{2^i} \equiv C_s$$

$$V_{res} = V_{in} - V_{off} - \left(\frac{d_{MSB}}{2} + \frac{d_{MSB}}{4} + \cdots + \frac{d_{LSB}}{2^N} \right) V_{ref}$$



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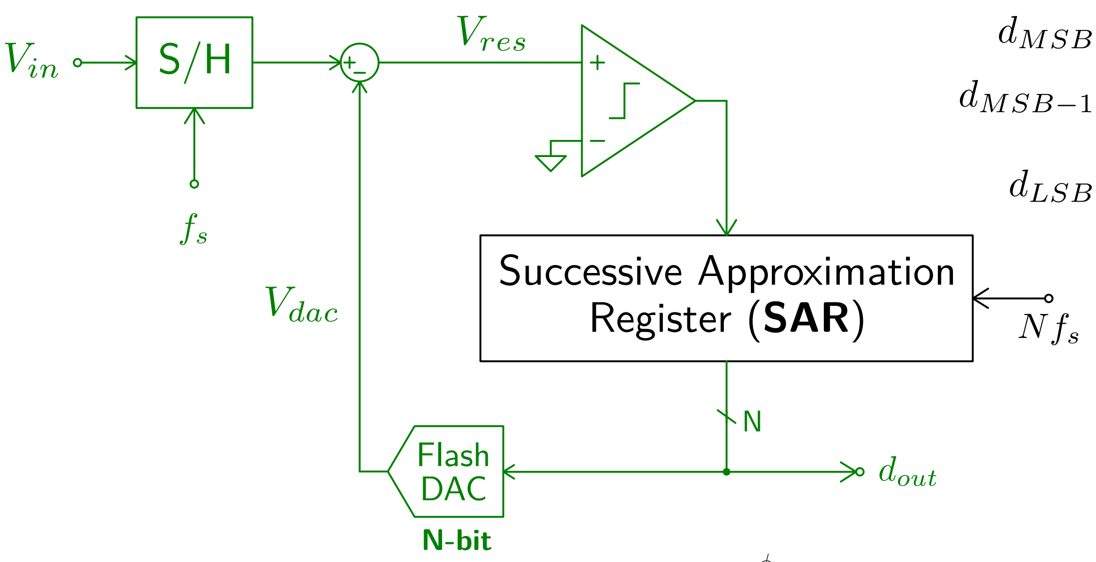

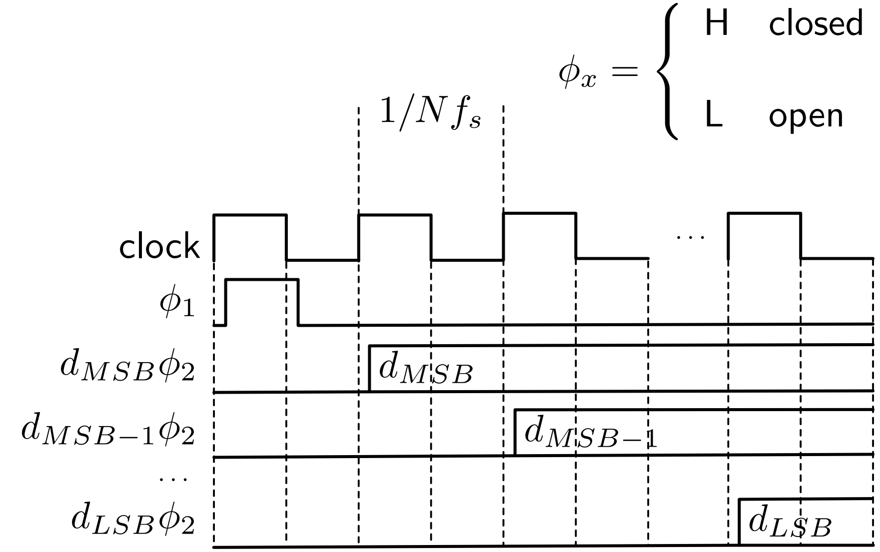

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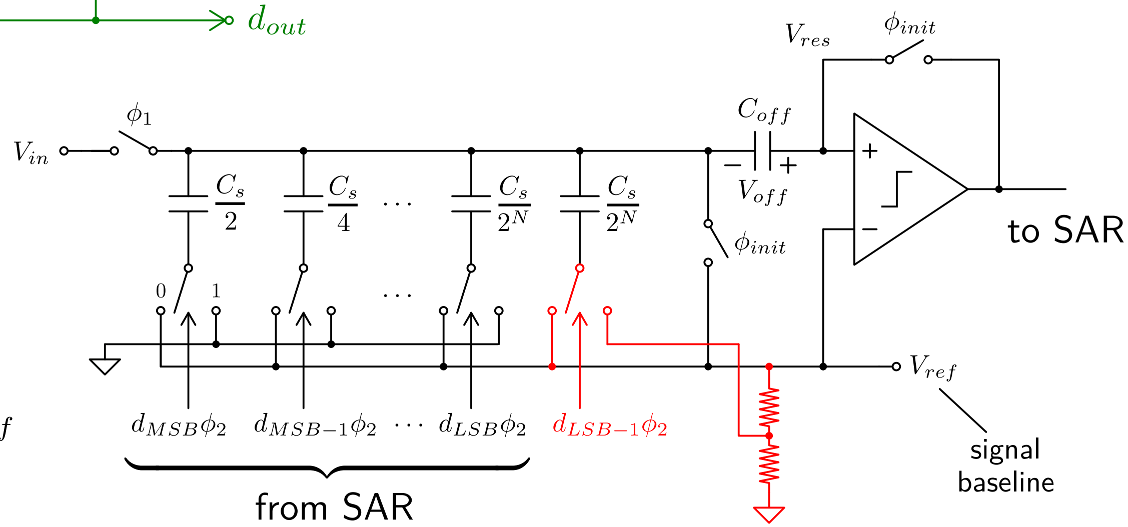

Single-Slope ADC

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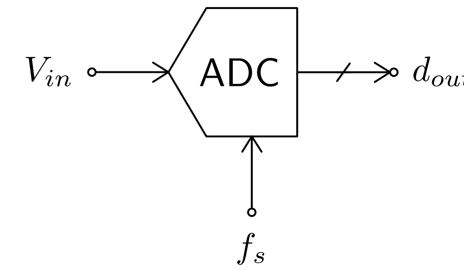

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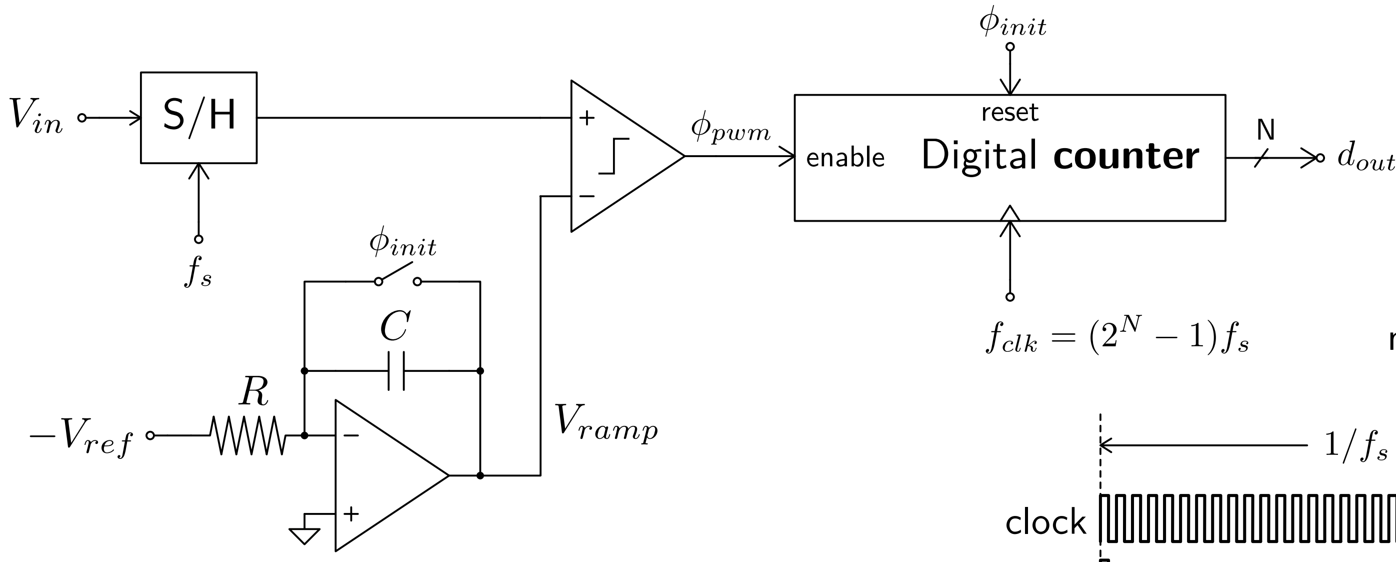
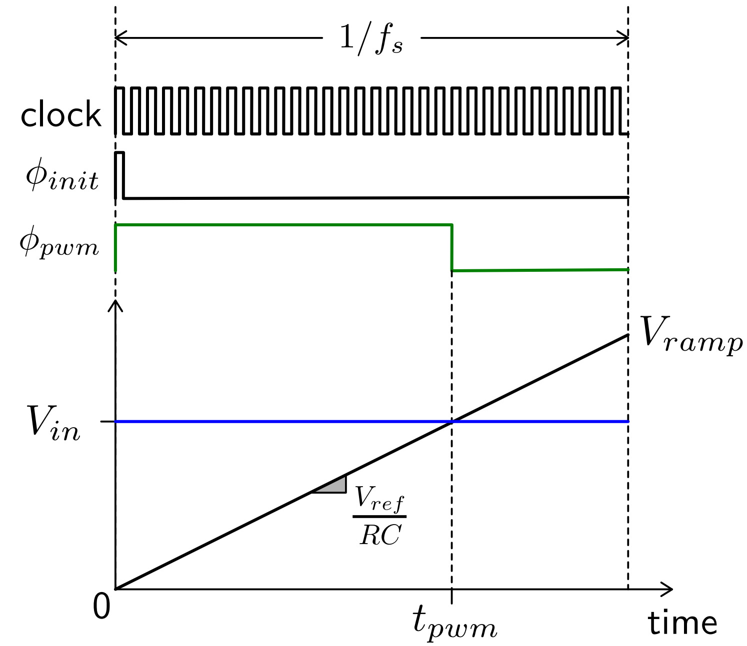


pulse-width modulation (**PWM**)

$$t_{pwm} = RC\frac{V_{in}}{V_{ref}}$$

$$d_{out} = t_{pwm} f_{clk} = (2^N - 1) f_s RC \frac{V_{in}}{V_{ref}}$$



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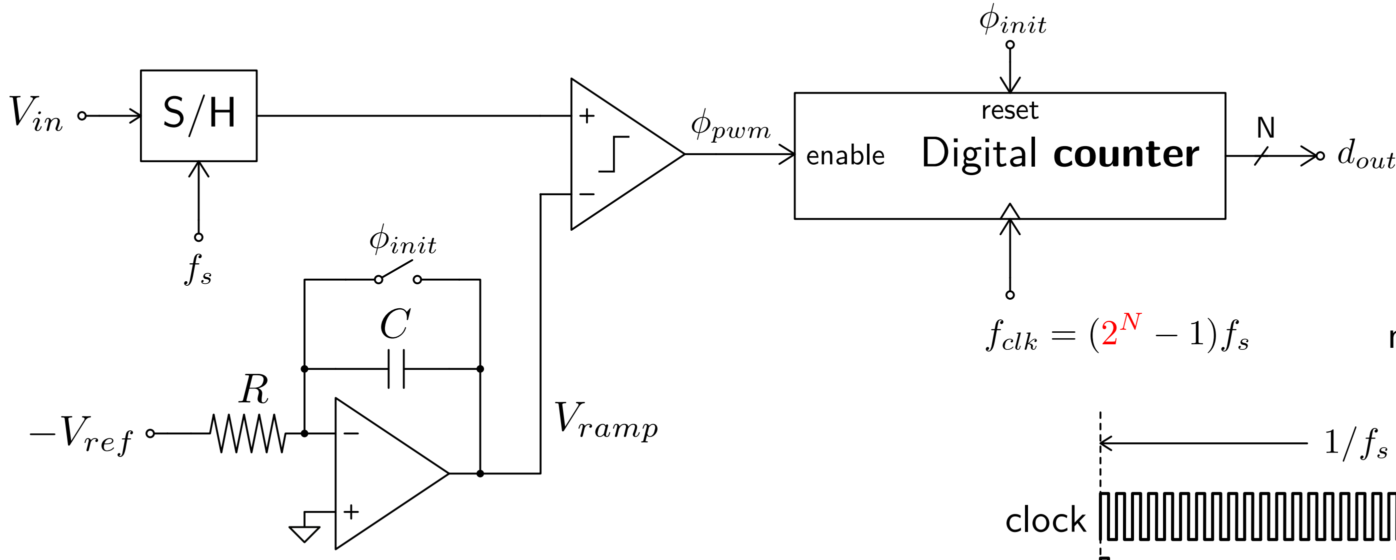
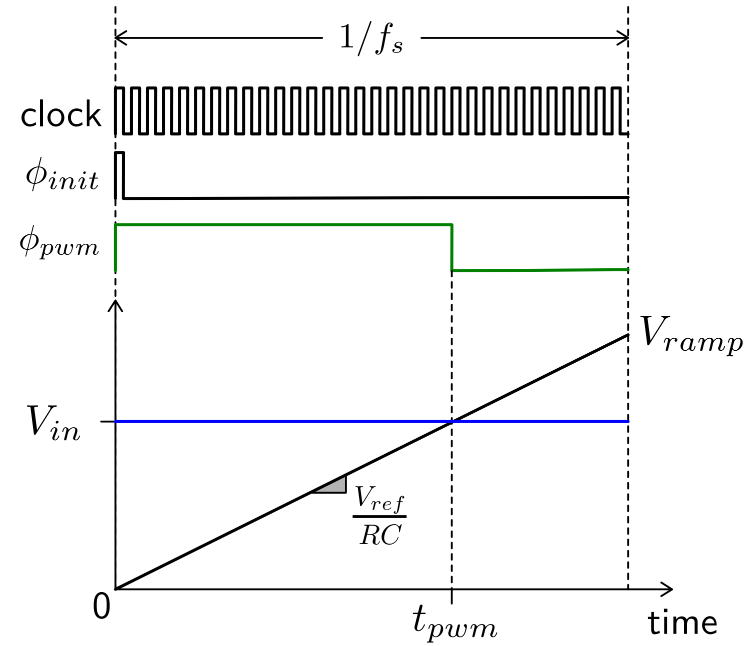


pulse-width modulation (**PWM**)



- ▲ Analog **minimalist**
- ▲ Very **low-power**

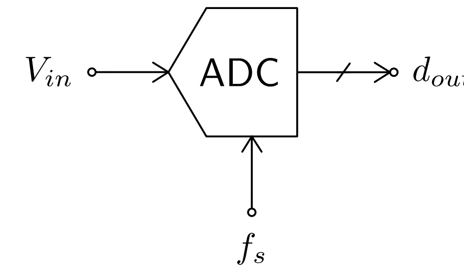
$$t_{pwm} = RC\frac{V_{in}}{V_{ref}}$$

$$d_{out} = t_{pwm} f_{clk} = (2^N - 1) f_s RC \frac{V_{in}}{V_{ref}}$$

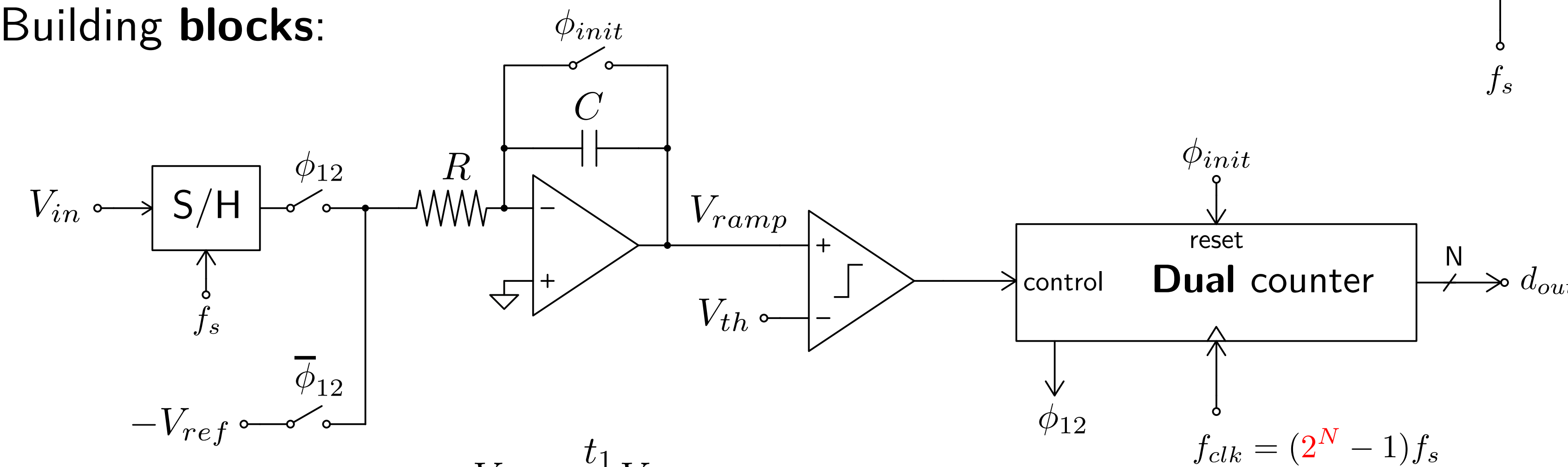
- ▼ **Speed** requirements (x$\mathbf{2^N}$)
- ▼ Technological sensitivity (**RC**)

Dual-Slope ADC

$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

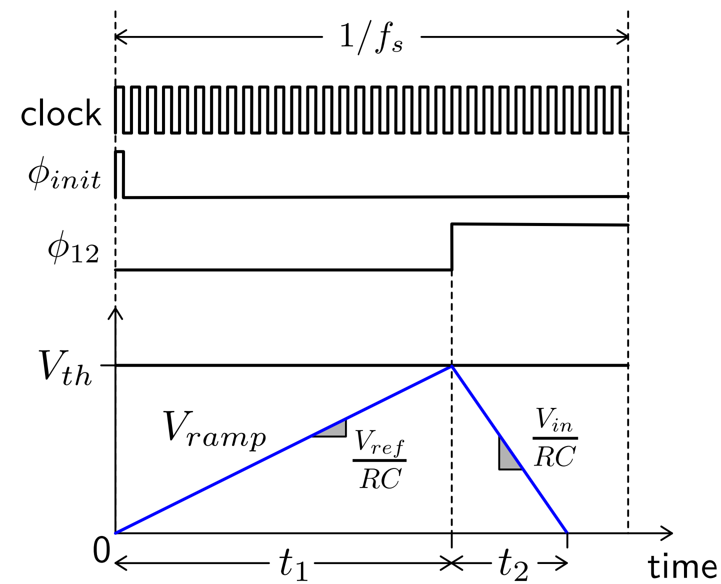


- Building **blocks**:



$$V_{in} \equiv \frac{t_1}{t_2} V_{ref}$$

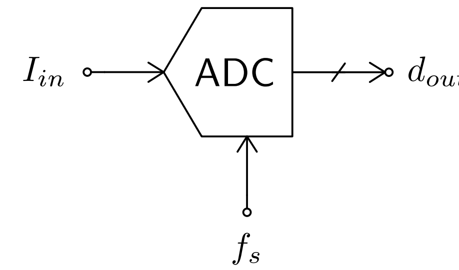
$$d_{out} = \frac{d_1}{d_2} \propto \frac{V_{in}}{V_{ref}}$$



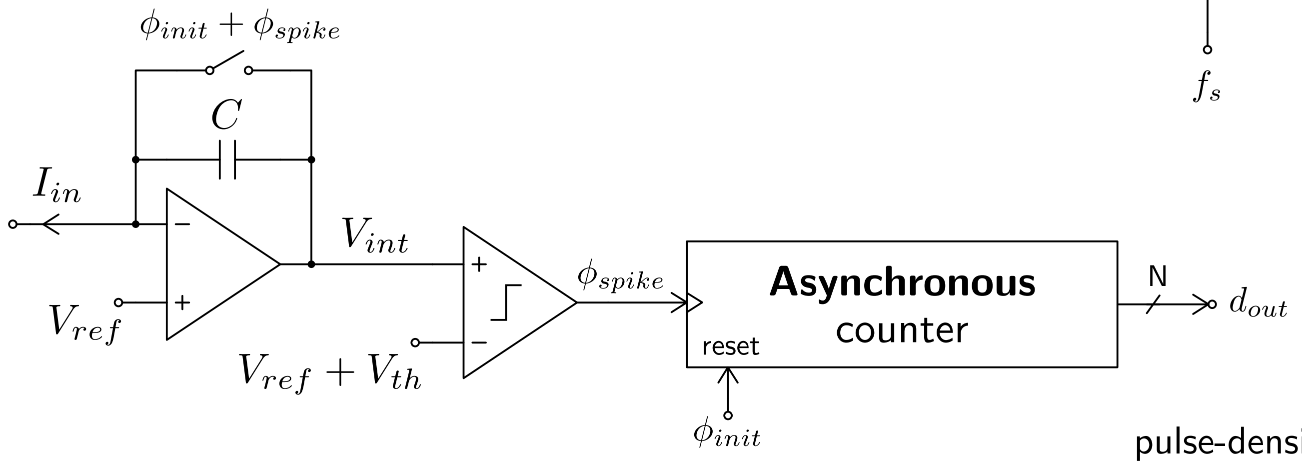
- ▲ Analog **minimalist**
- ▲ Very **low-power**
- ▼ **Speed** requirements (x$\mathbf{2^N}$)
- ▲ Technology independence (**RC**)

Integrate-and-Fire ADC

$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

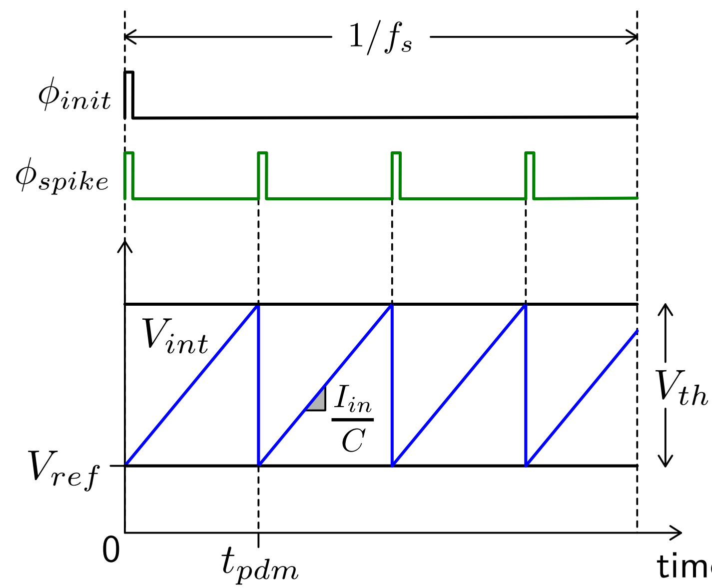


- Building **blocks**:



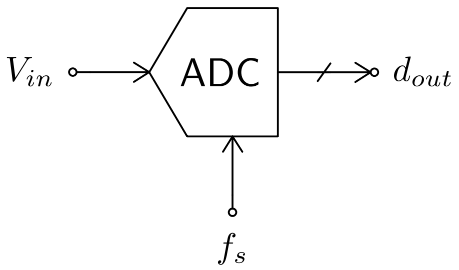
pulse-density modulation (**PDM**)

$$d_{out} = \frac{1/f_s}{t_{pdm}} = \frac{I_{in}}{C V_{th} f_s}$$

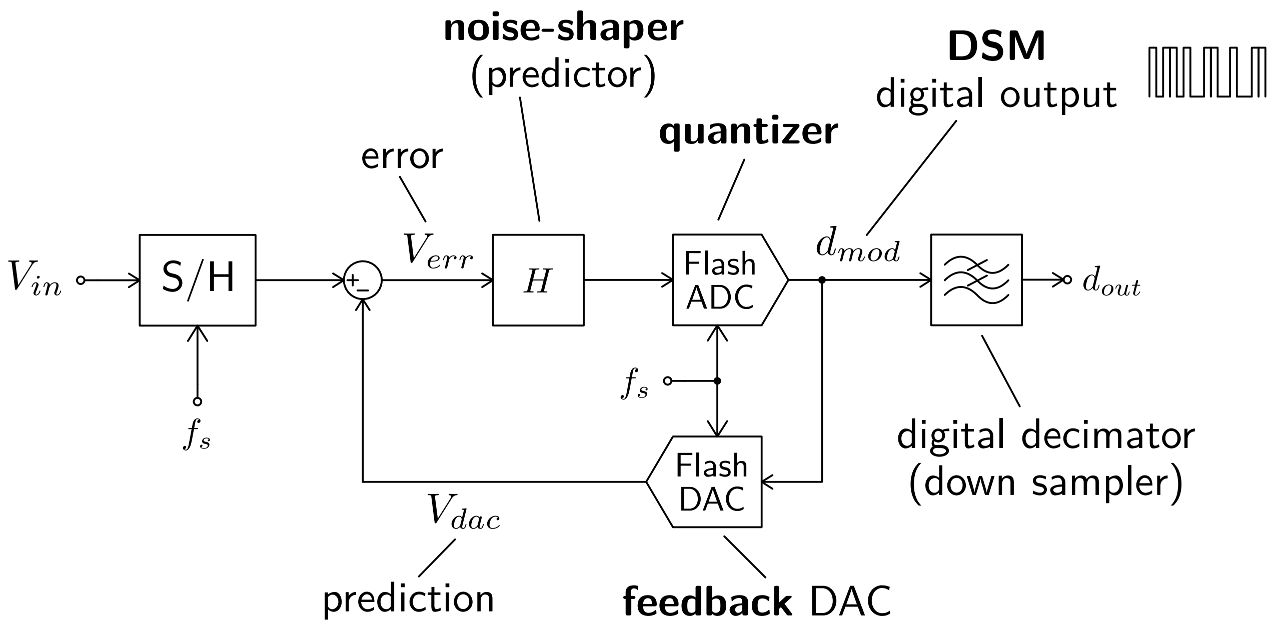


- ▲ **Current-mode** sensors (e.g. imagers)
- ▲ Very **low-power**
- ▶ **Speed** requirements adapted to signal
- ▼ Technology sensitivity (**C**)

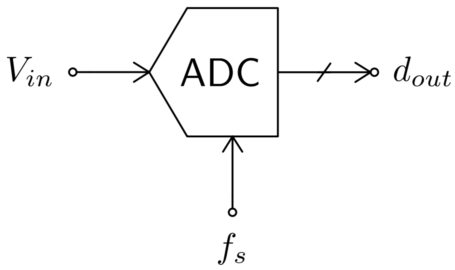
Delta-Sigma Modulator ADC



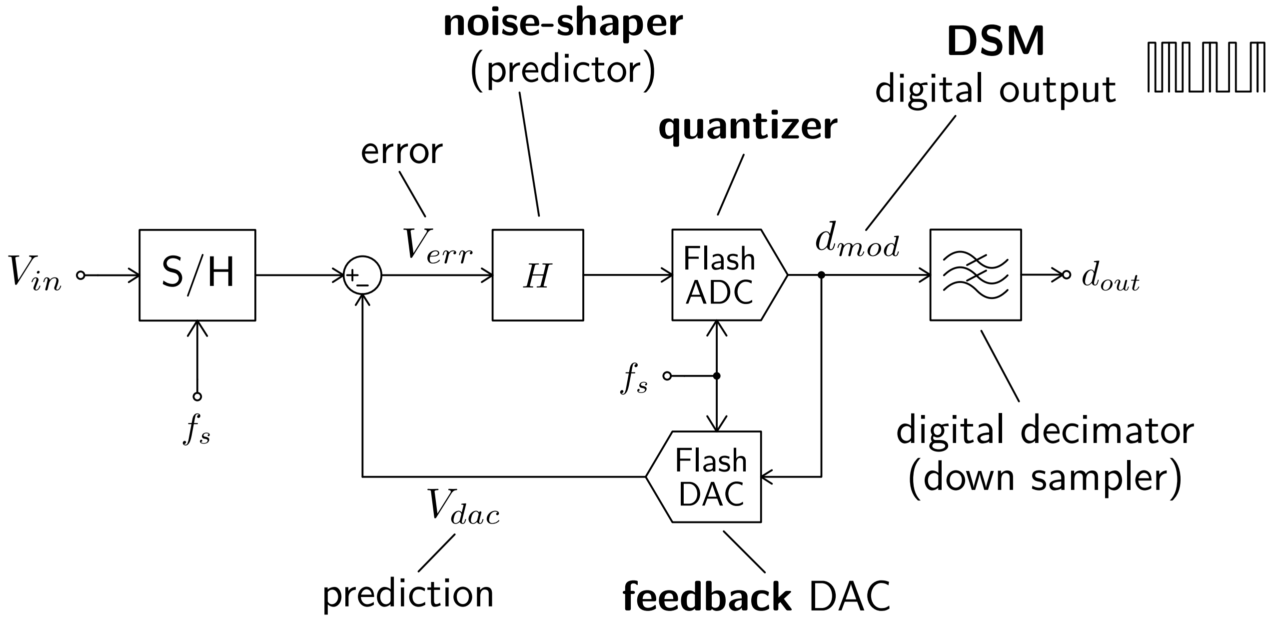
- General **single-loop DSM** architecture:



Delta-Sigma Modulator ADC

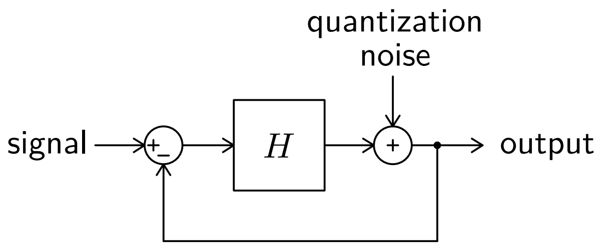


- General **single-loop DSM** architecture:



- Noise-shaper **filter**:
  - In-band **high-gain**
  - Either continuous- H(s) or **discrete-time H(z)**
- Flash ADC and DAC blocks can be **relaxed**!

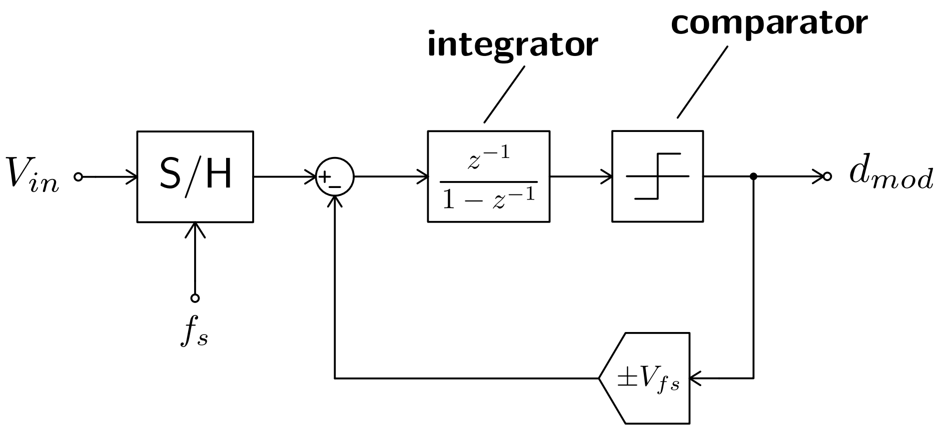
- DSM **signal vs quantization noise** behavior?



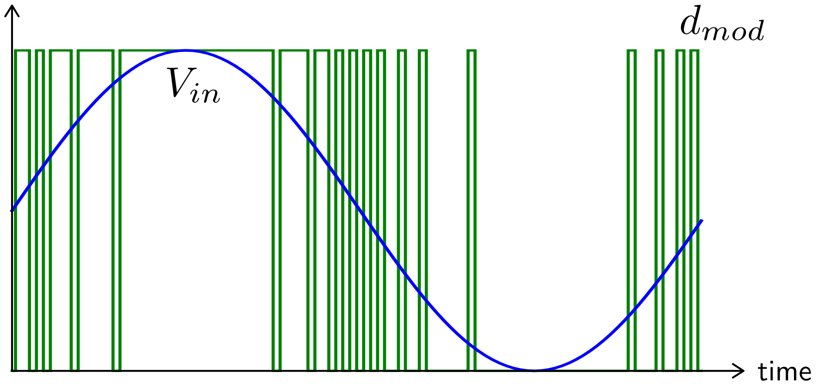
$$\begin{cases} STF = \dfrac{H}{1+H} & \to 1 \\ & H \to \infty \\ NTF = \dfrac{1}{1+H} & \to 0 \end{cases}$$

Delta-Sigma Noise Shaping

- **Simplest** architecture: **first-order** (N=1) **1-bit** (B=1) single-loop DSM

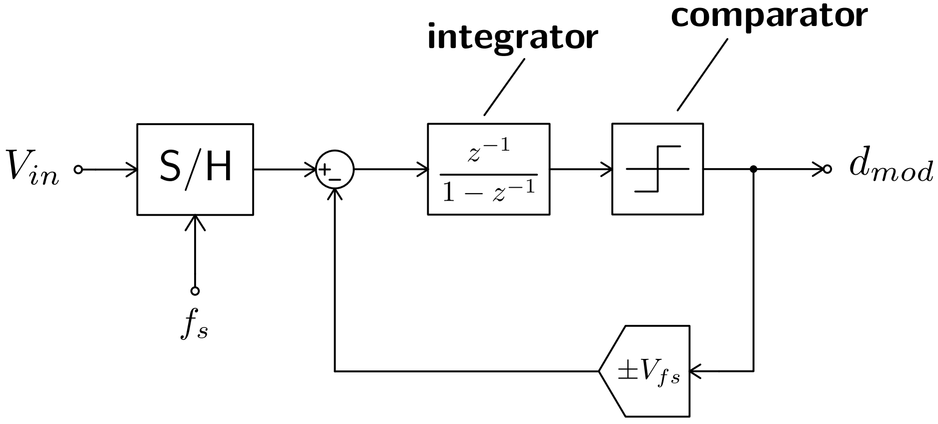


▲ Single-bit feedback DAC is **intrinsically linear**



Delta-Sigma Noise Shaping

- **Simplest** architecture: **first-order** (N=1) **1-bit** (B=1) single-loop DSM



▲ Single-bit feedback DAC is **intrinsically linear**

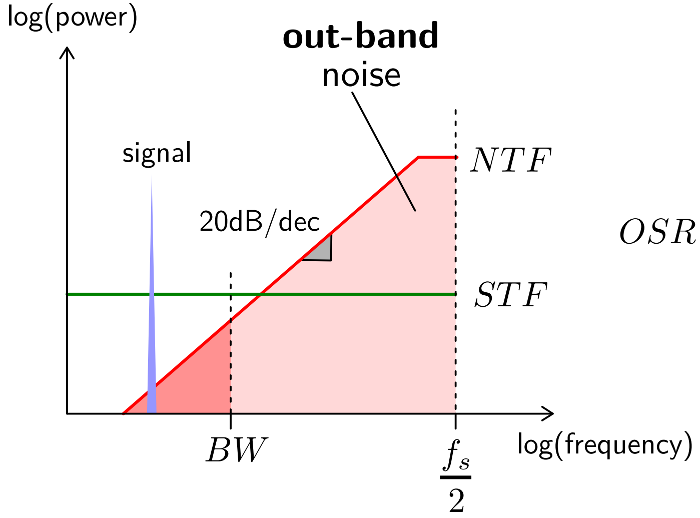
▼ **Oversampling** is needed

$$H(z) = \frac{z^{-1}}{1-z^{-1}}$$

$$\begin{cases} STF = \dfrac{H}{1+H} \equiv z^{-1} & \text{(delay)} \\ NTF = \dfrac{1}{1+H} \equiv 1 - z^{-1} & \text{(differentiator)} \end{cases}$$

all-pass

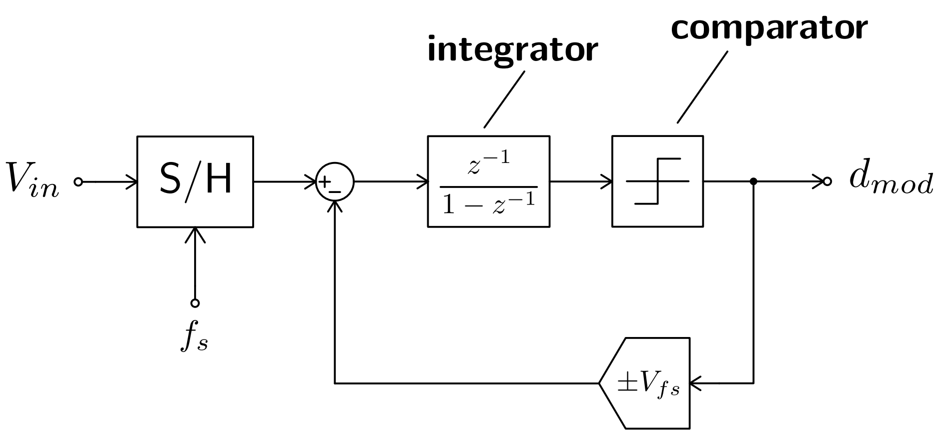
high-pass shaping



$$OSR \doteq \frac{f_s}{2BW} \gg 1$$

Delta-Sigma Noise Shaping

- **Simplest** architecture: **first-order** (N=1) **1-bit** (B=1) single-loop DSM



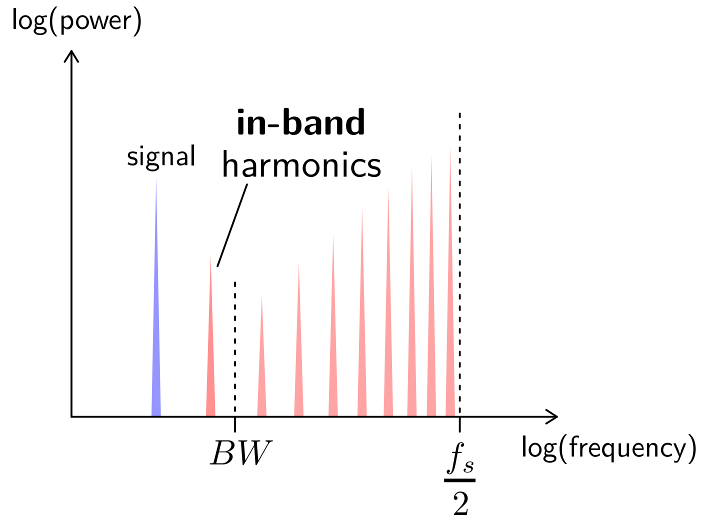
- ▲ Single-bit feedback DAC is **intrinsically linear**
- ▼ **Oversampling** is needed
- ▼ Higher order (**N>1**) shaping to avoid signal to quantization noise correlation (harmonics)

$$H(z) = \frac{z^{-1}}{1-z^{-1}}$$

$$\begin{cases} STF = \dfrac{H}{1+H} \equiv z^{-1} & \text{(delay)} \\ NTF = \dfrac{1}{1+H} \equiv 1 - z^{-1} & \text{(differentiator)} \end{cases}$$

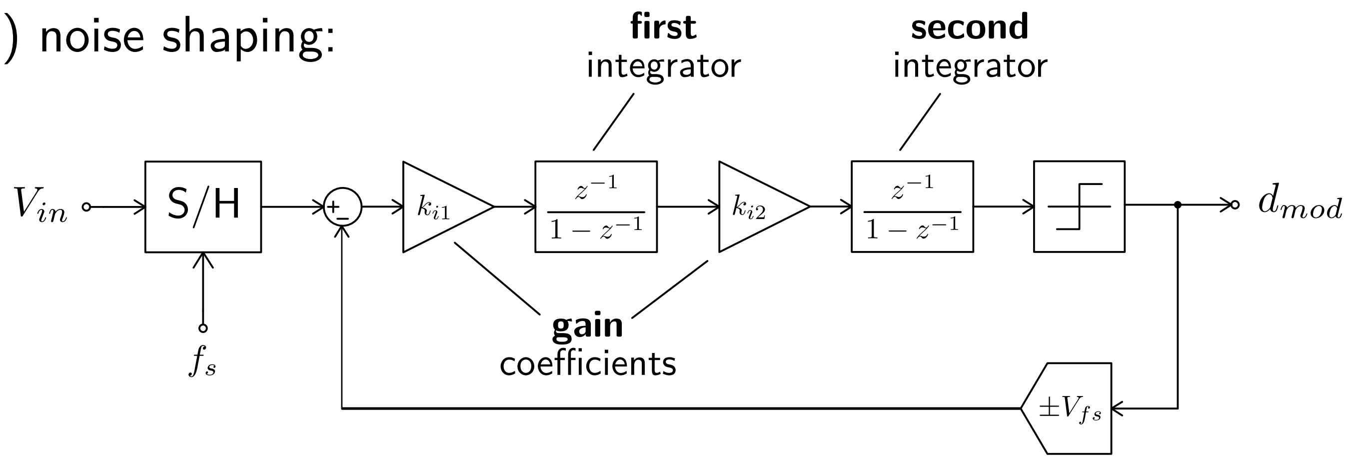
all-pass (z^{-1})

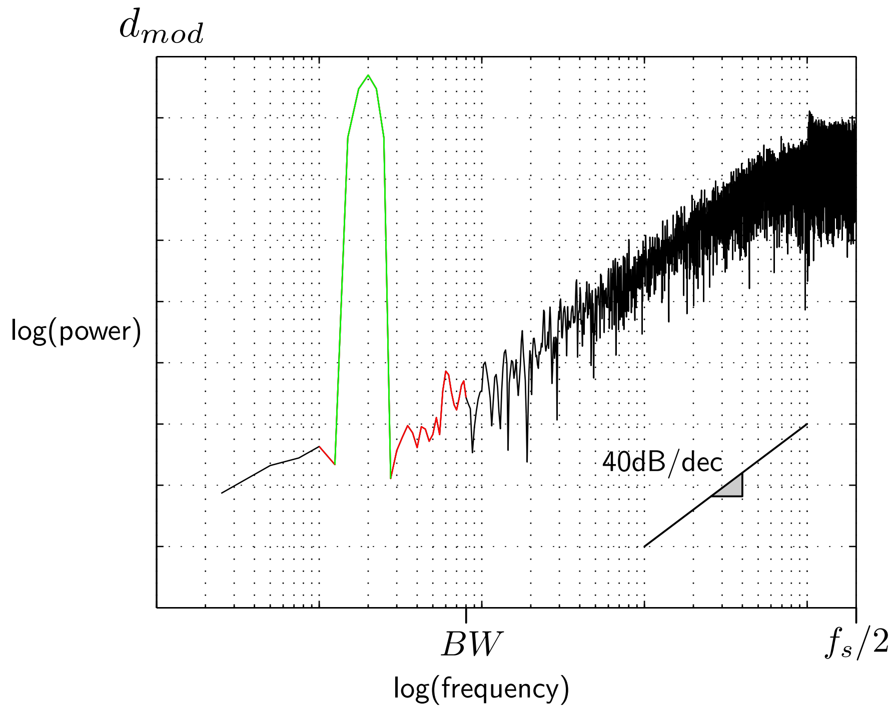
high-pass shaping ($1-z^{-1}$)



Delta-Sigma Noise Shaping

- **Higher-order** (N) noise shaping:

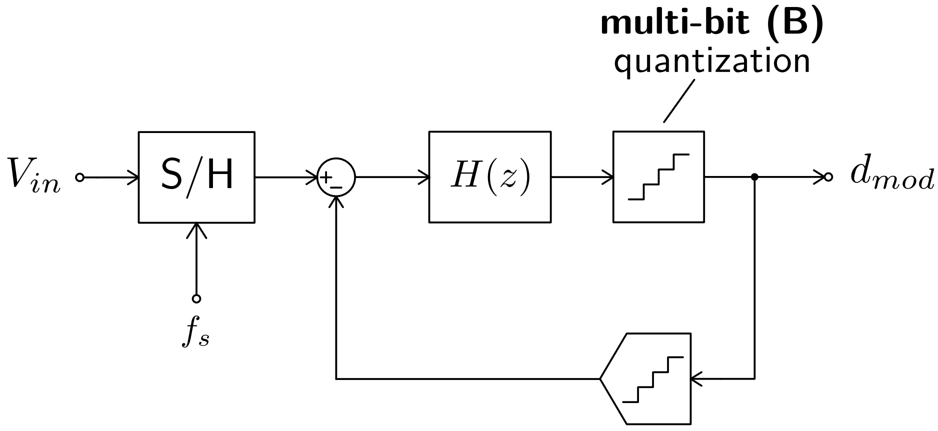




- ▲ **Sharper** noise shaping
- ▲ Signal to quantization noise **uncorrelation** (continuous spectra)
- ▼ Possibility of loop **instability** for N>2
- **Coefficients** optimization!

DSM ADC Design

- **N-order B-bit** single loop architecture:



- **Multi-bit** quantization:
  - Resolution added to overall **DR**
  - **Internal full-scale** reduction
  - Feedback DAC **not intrinsically linear**
- **High-order** filtering:
  - **Sharper** noise shaping
  - **Stability** issues

- **Ideal** dynamic range:

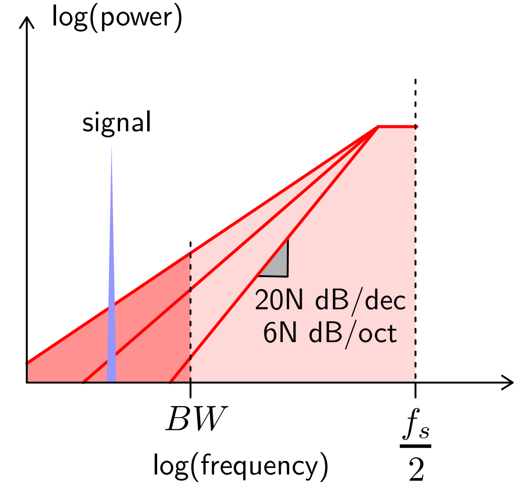
$$DR = \frac{3\pi}{2}\left(2^B-1\right)^2(2N+1)\left(\frac{OSR}{\pi}\right)^{2N+1}$$

shaping order — **oversampling** only

(N+0.5)-bit/oct(OSR)

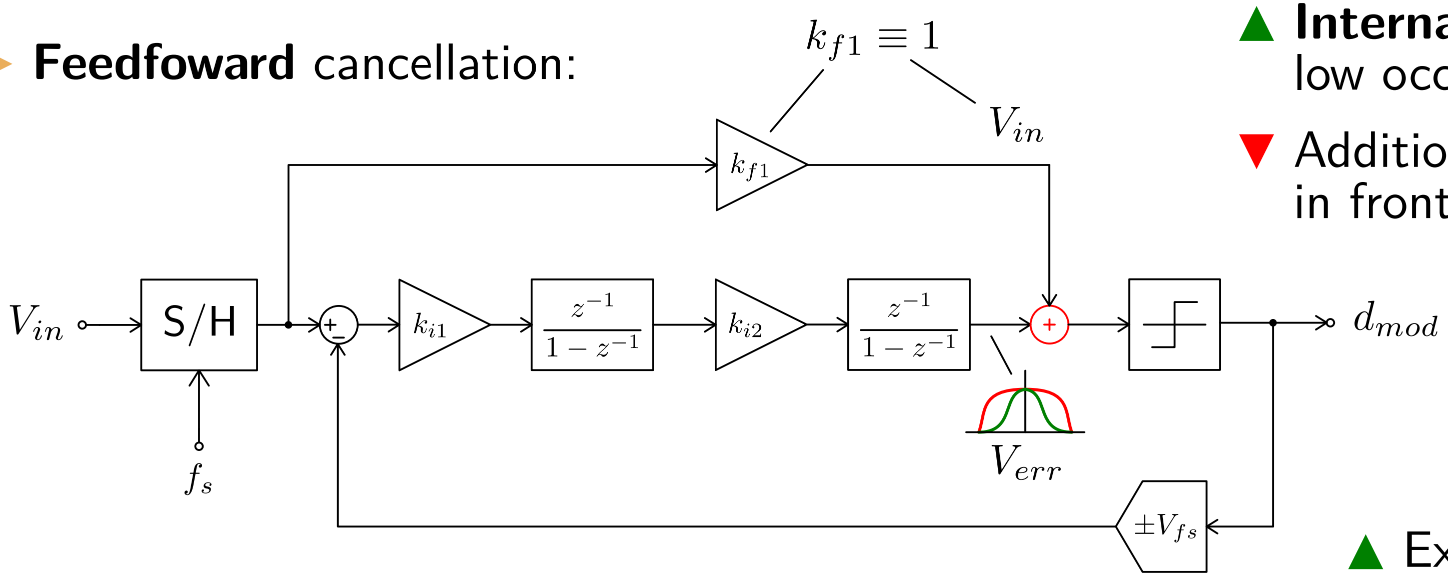
$$DR[\text{dB}] = 6.7 + 20\log\left(2^B-1\right) + 10\log(2N+1) + 20(N+0.5)\log\frac{OSR}{\pi}$$

direct improvement



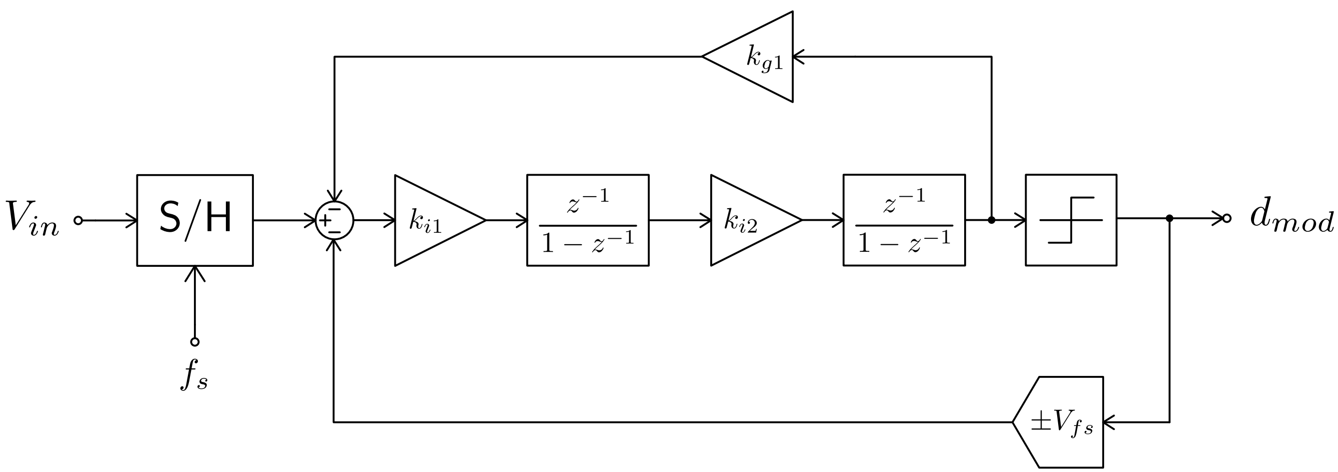
DSM ADC Design

- **Feedfoward** cancellation:

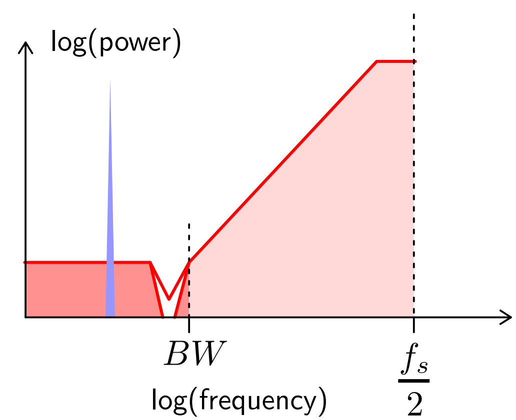


- ▲ **Internal full scale** low occupancy
- ▼ Additional **adder stage** in front of quantizer

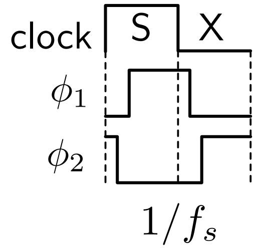
- **Resonator** attenuation:



- ▲ Extra noise shaping at **band edge**
- ▼ Zero sensitivity to coefficient **matching**

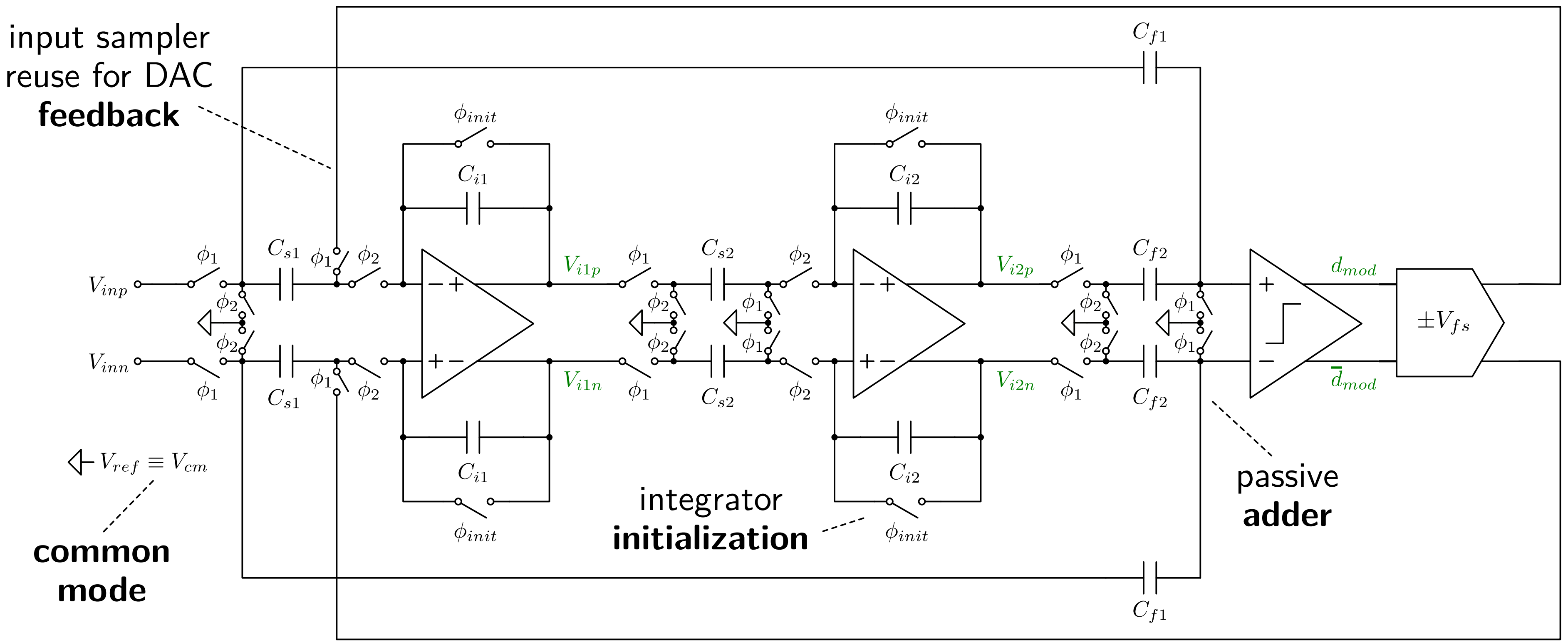


DSM SC Circuits



$$\phi_x = \begin{cases} \text{H} & \text{closed} \\ \text{L} & \text{open} \end{cases}$$

- **Fully-differential** 2nd-order single-bit example:



$$k_{i1} \doteq \frac{C_{s1}}{C_{i1}} \qquad k_{i2} \doteq \frac{C_{s2}}{C_{i2}} \qquad k_{f1} \doteq \frac{C_{f1}}{C_{f2}} \equiv 1$$