5. Low-Power OpAmps

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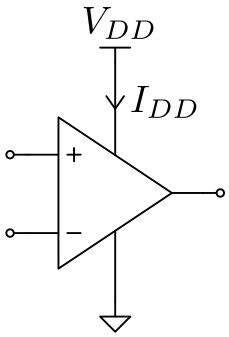
Low-Voltage vs Low-Current

- OpAmp overall **power** consumption:



$$P_{DD} = I_{DD} \times V_{DD}$$

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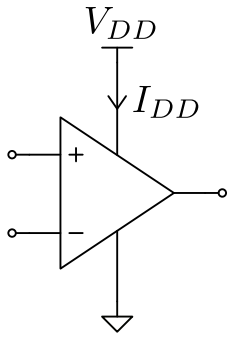

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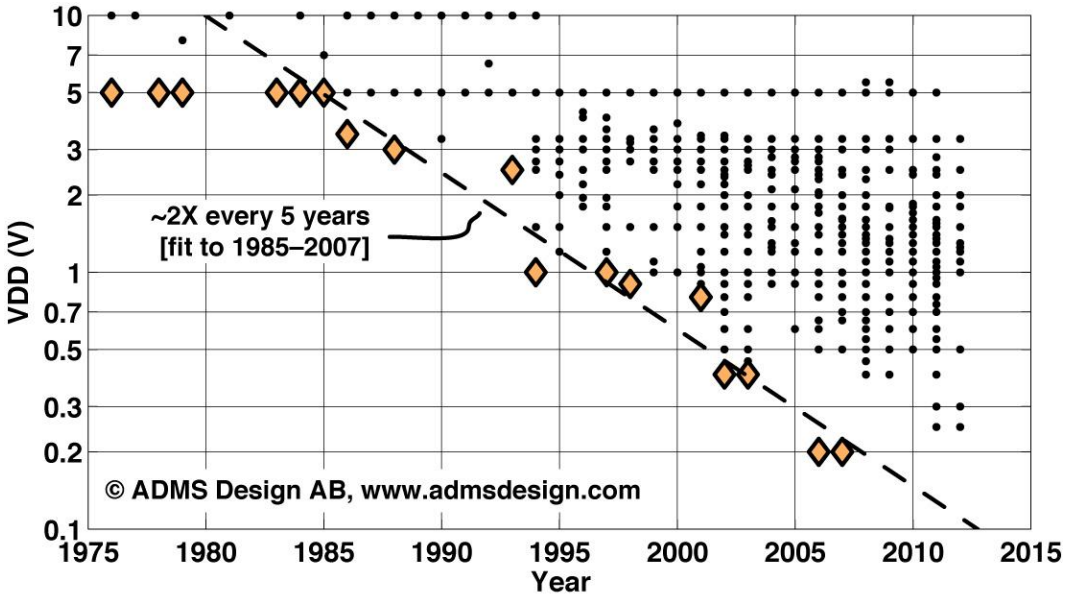

- ▲ Alternative supply **sources** (battery, solar cell, scavenging)
- ▼ **Poor** power scaling
- ▼ Limited by **technology**
- **Low-voltage** circuit techniques:
  - Rail-to-rail
  - Inverter-based
  - Supply multipliers
  - Back gate ...

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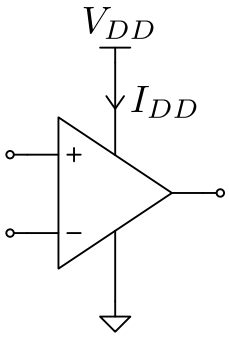

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- ▼ Limited by **noise** and **bandwidth**
- **Low-current** circuit techniques:
  - Subthreshold
  - Class-AB
  - Dynamic biasing
  - Duty cycle ...

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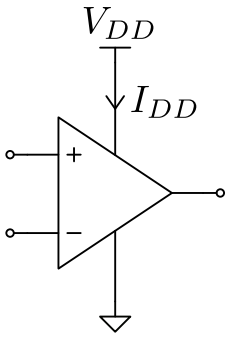

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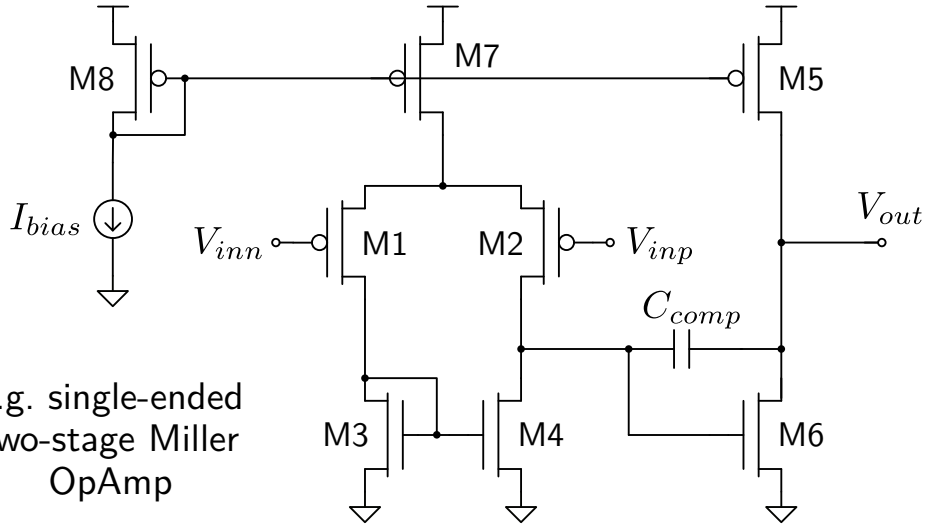
- ▼ **Conflicts** can arise between low-current and low-voltage design techniques!

Optimizing MOSFET Biasing

- Each transistor has its own **purpose** and **requirements**!



e.g. single-ended two-stage Miller OpAmp

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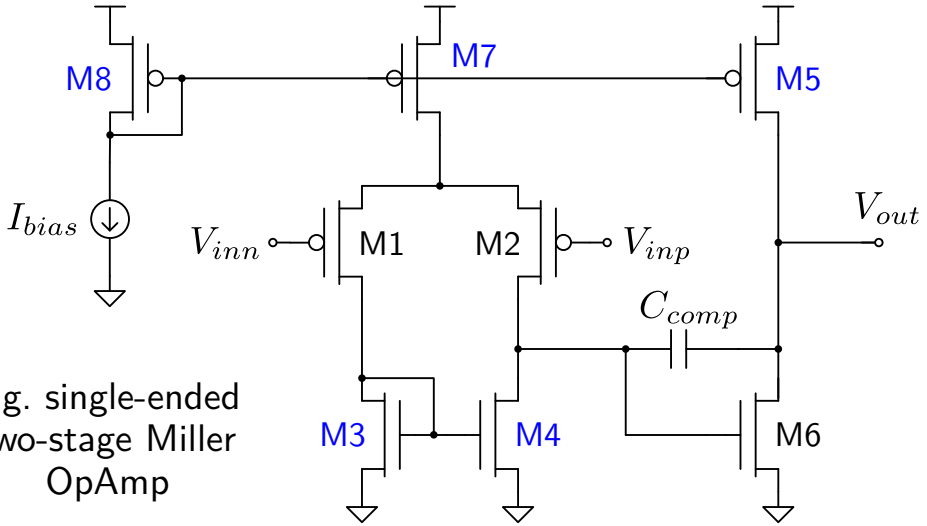

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good current **matching**

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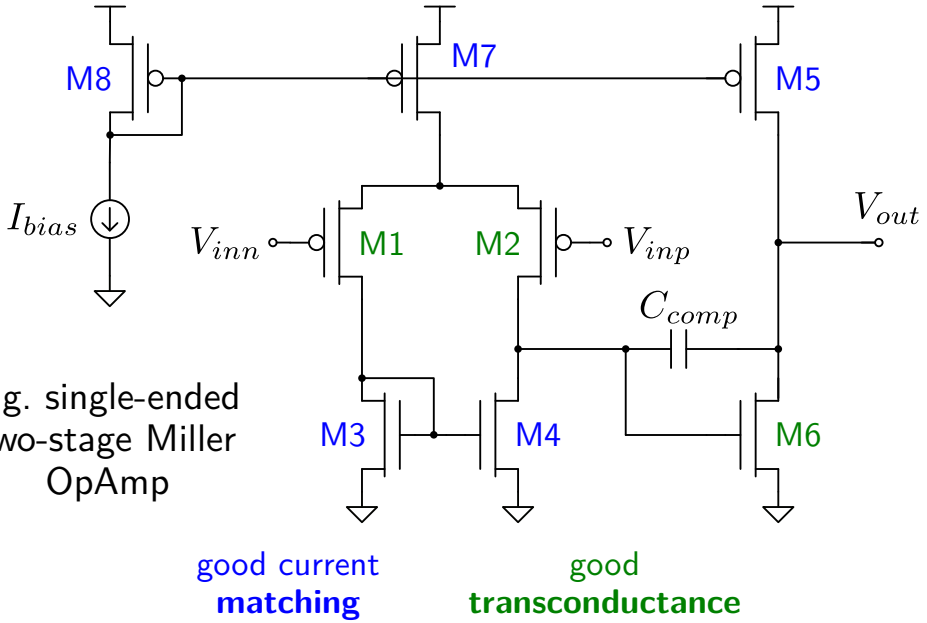

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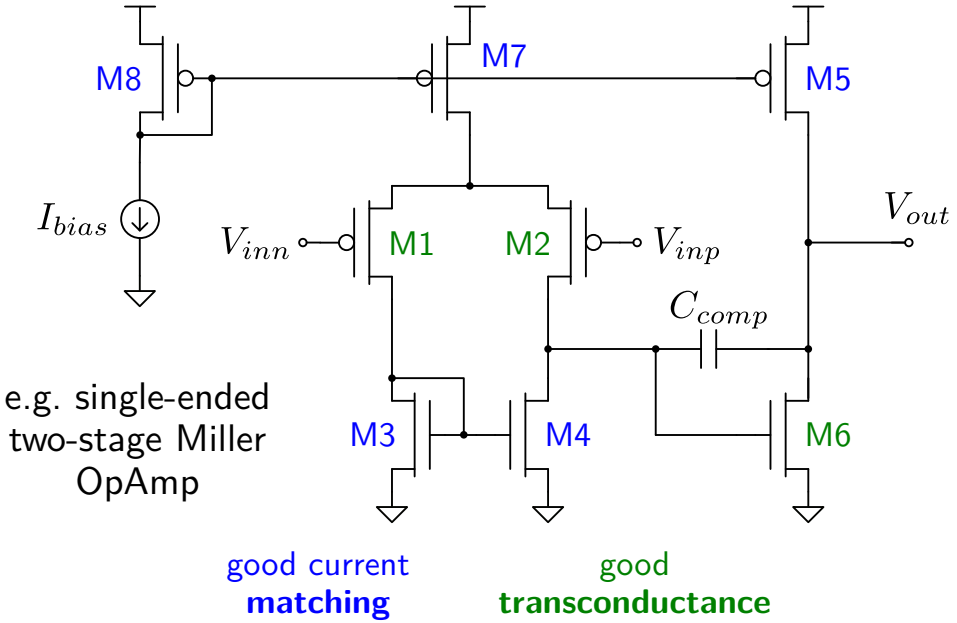

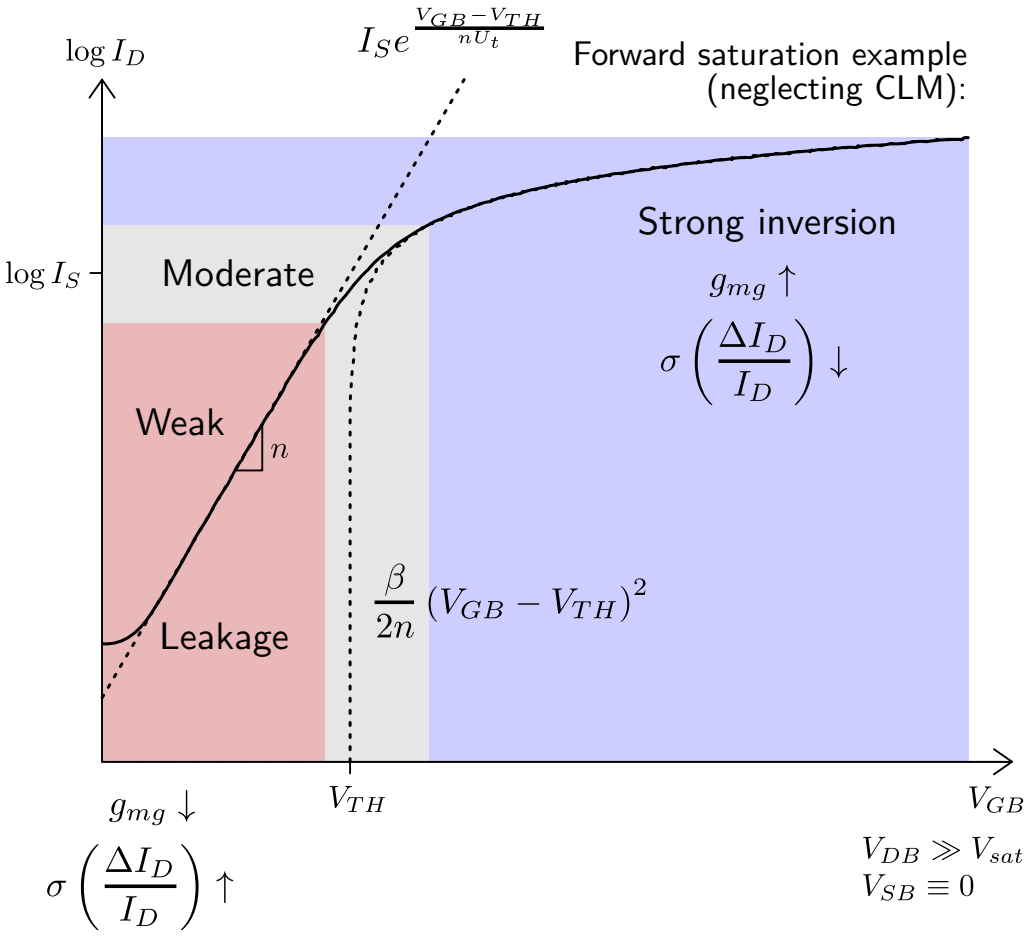

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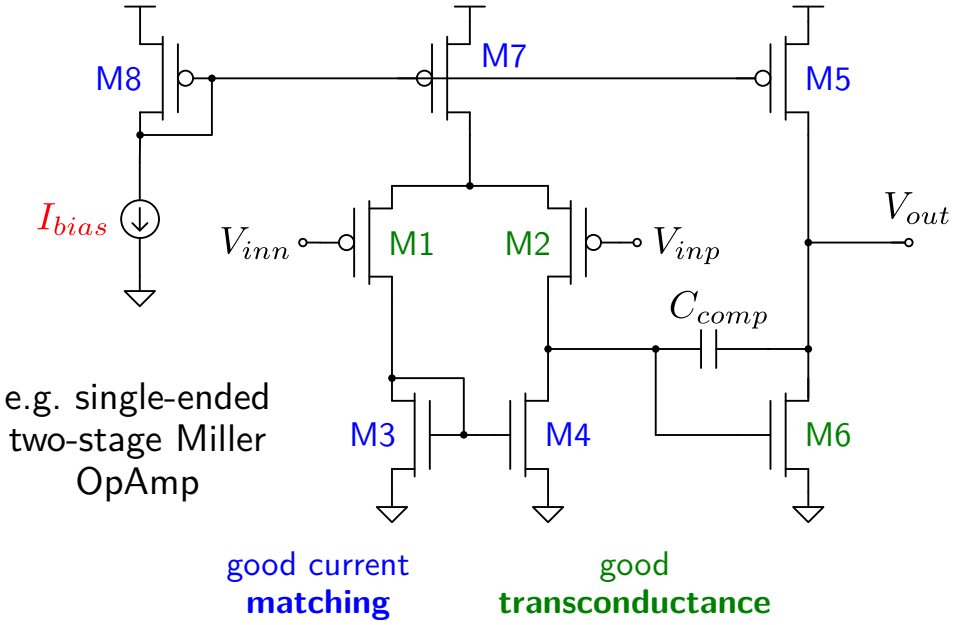
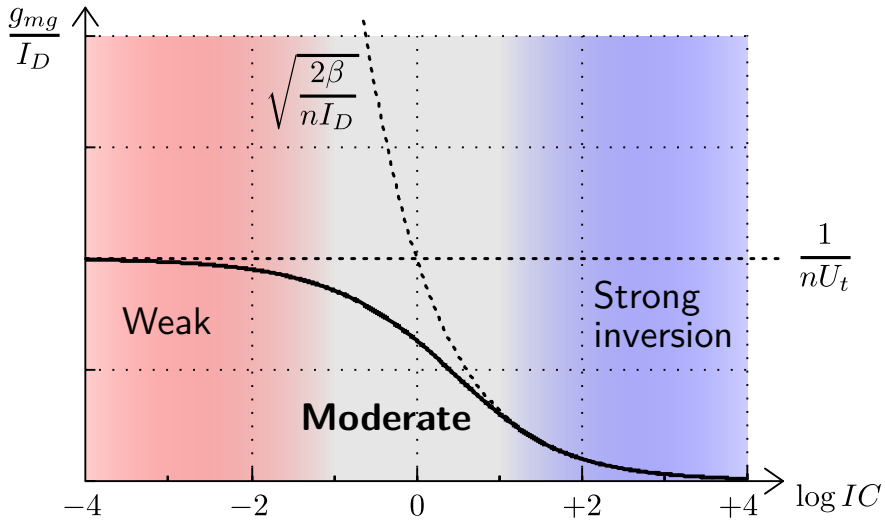


- Individual operating point selection by **sizing** + **biasing**:

$$I_S = 2n\beta U_t^2 \qquad M \times \left(\frac{W}{L}\right)$$

$$IC \doteq \frac{I_D}{I_S}$$

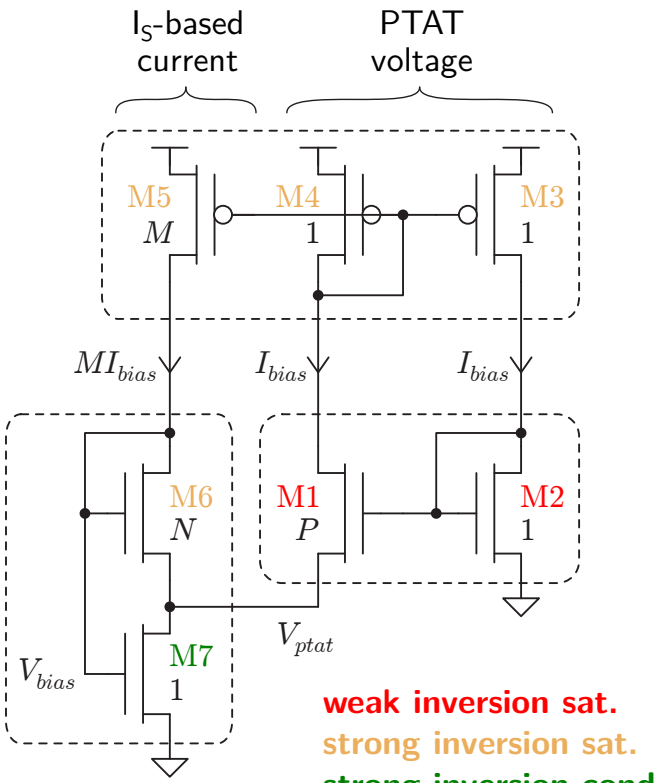
inversion coefficient



- **IC-based** circuit design:
  - IC>>1 e.g. good current matching
  - IC~1 **optimized transconductance/power**
  - IC<<1 e.g. translinear e^x functions

Specific Current Generator

- **I_S-based** current reference:



proportional to absolute temperature (**PTAT**)

$$V_{ptat} = U_t \ln P$$

Neglecting CLM

$$\begin{cases} MI_{bias} = \dfrac{N\beta_7}{2n}(V_{bias} - V_{TH} - nV_{ptat})^2 \\ (M+1)I_{bias} = \beta_7 \left(V_{bias} - V_{TH} - \dfrac{n}{2}V_{ptat}\right) V_{ptat} \end{cases}$$

$$Q = \left[\frac{\ln P}{2(M+1)}\left(\sqrt{\frac{M}{N}} + \sqrt{\frac{M}{N} + M + 1}\right)\right]^2$$

$$I_{bias} \doteq Q I_{S7}$$

- By using I_{bias} for biasing circuits, IC selection is **independent** from technology

http://dx.doi.org/10.1109/JSSC.2002.806258
F. Serra-Graells et al., *Sub-1V CMOS Proportional-To-Absolute-Temperature References*, IEEE Journal of Solid-State Circuits, 38:1(84-8), Jan 2003

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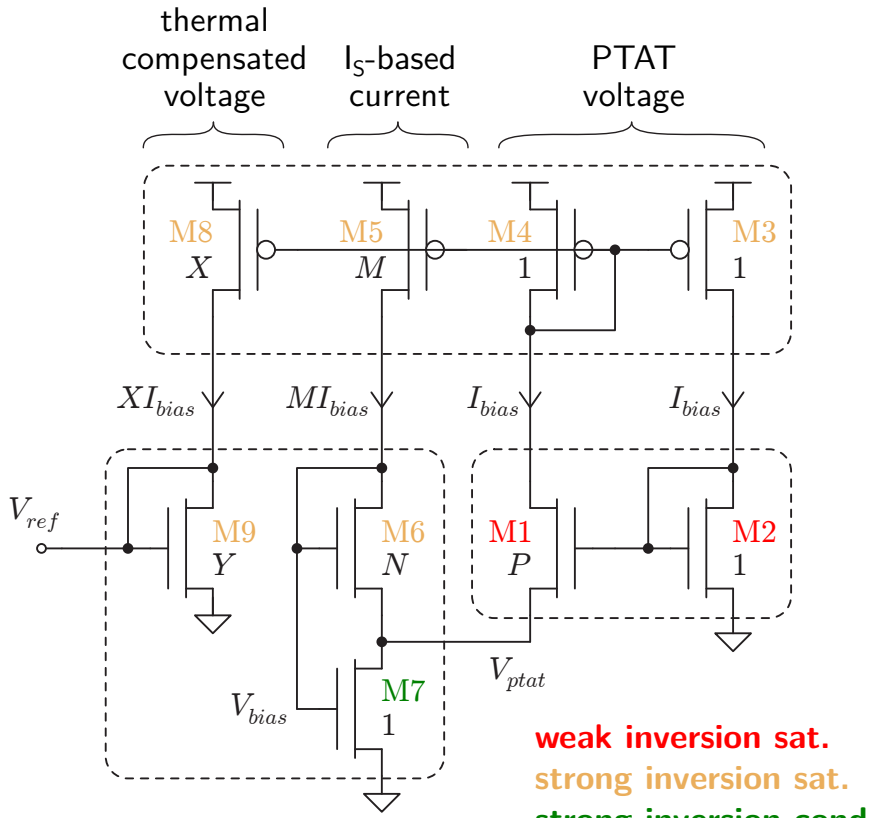

- As a side effect, **temperature compensated** voltage references can be also obtained:

$$V_{ref} = 2n\sqrt{\frac{QX}{Y}}U_t + V_{TH}$$

$$V_{TH}(T) = V_{TH}(T_O) - \alpha\left(\frac{T}{T_O} - 1\right)$$

$$\sqrt{\frac{QX}{Y}} = \frac{1}{2n}\frac{\alpha}{U_t(T_O)}$$

$$V_{ref} \equiv \alpha + V_{TH}(T_O)$$

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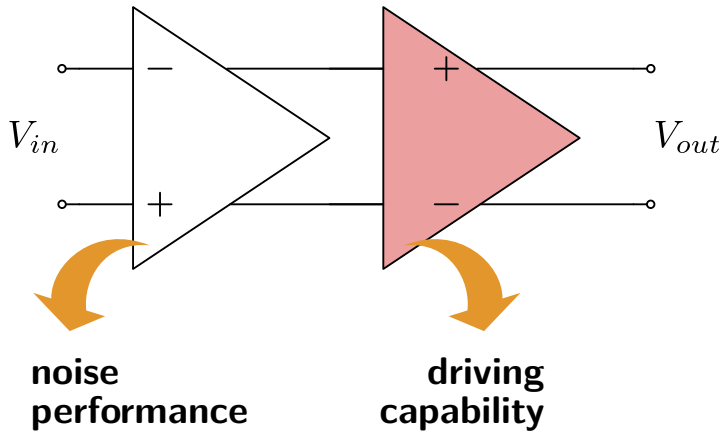
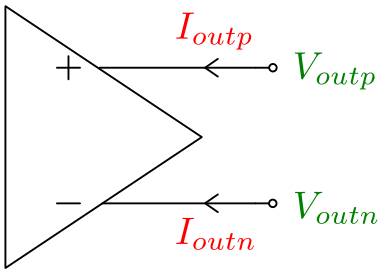
Output Operation Class

- OpAmp **power** investment:



- **Output stage** operation modes:



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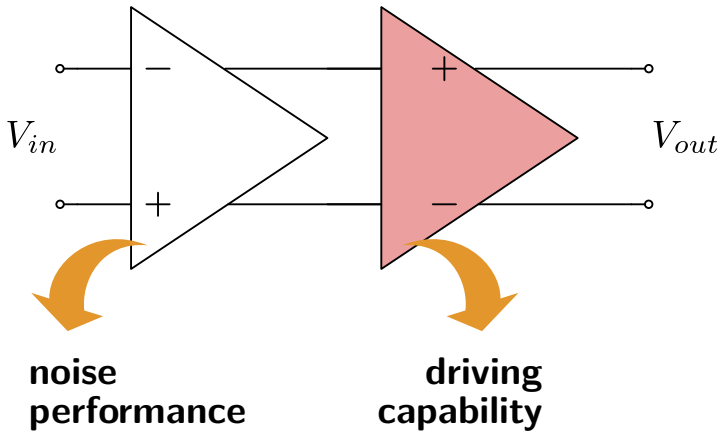

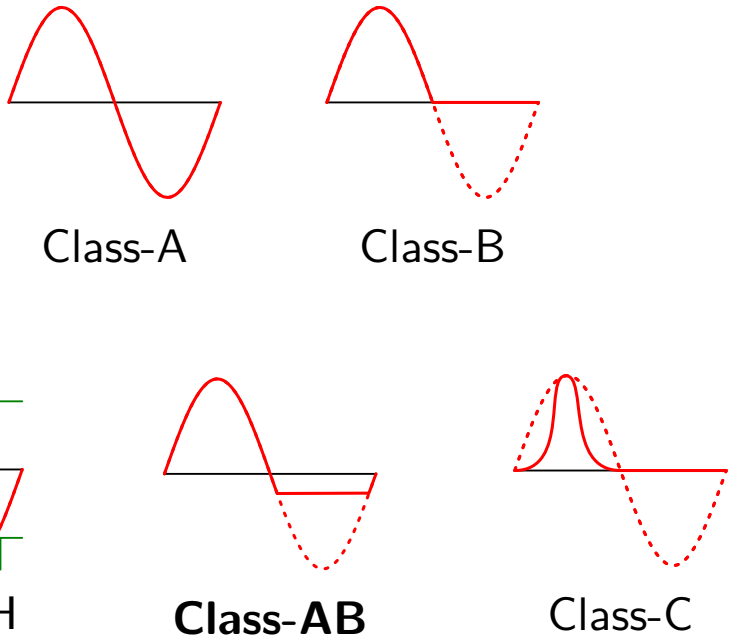

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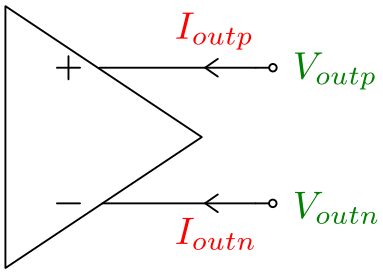
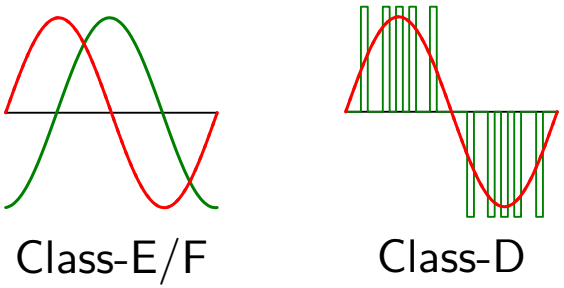
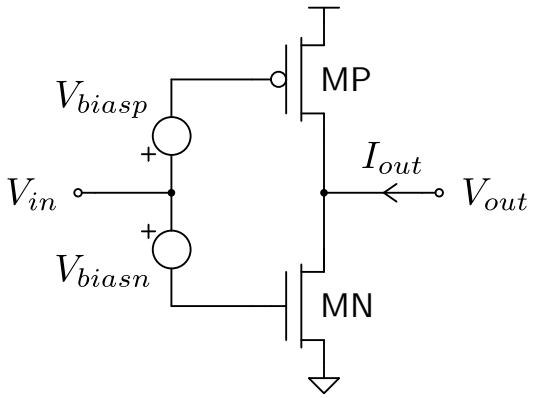




Basic CMOS Topologies

- **Inverter**-like stage:

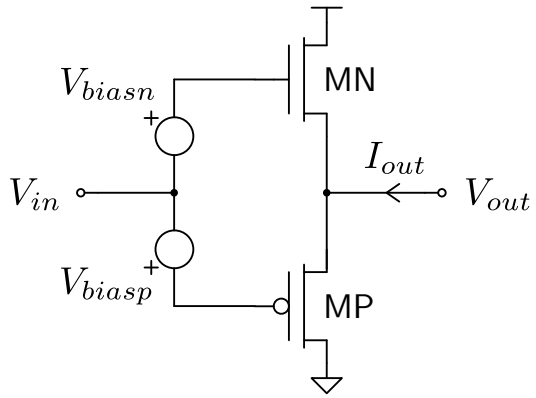


Class-AB **modulation index**

$$m = \frac{|I_{out}|_{max}}{I_{bias}}$$

MN and MP static **bias current**

- **Push-pull** type stage:



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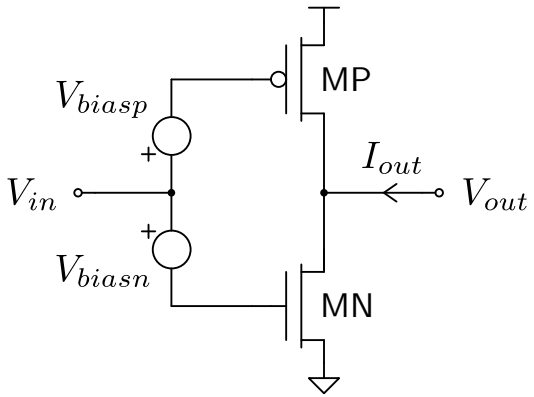

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MN and MP static **bias current**

- High **voltage gain**
- Intrinsic high **output impedance** ($1/g_{md}$)
- Suitable for **capacitive loads only**
- Optimized **full-scale**

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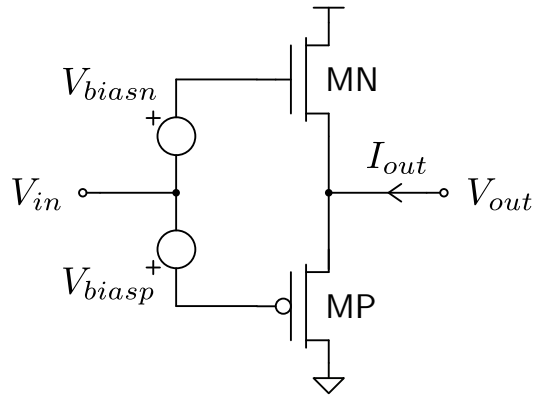
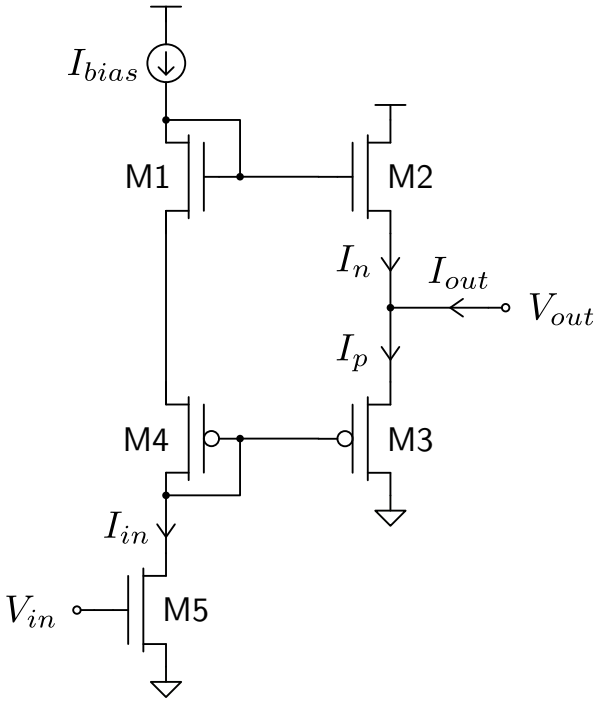


- Unity **voltage gain**
- Intrinsic low **output impedance** ($1/g_{ms}$)
- Suitable for any type of **load impedance**
- Reduced **full-scale**

- **Biasing circuitry** to control $\mathbf{I_{bias}}$ against PVT (CMOS process, supply voltage and temperature) corners and to reach high Class-AB **m**-values?

Class-AB Stage Examples

- **Translinear** loops:



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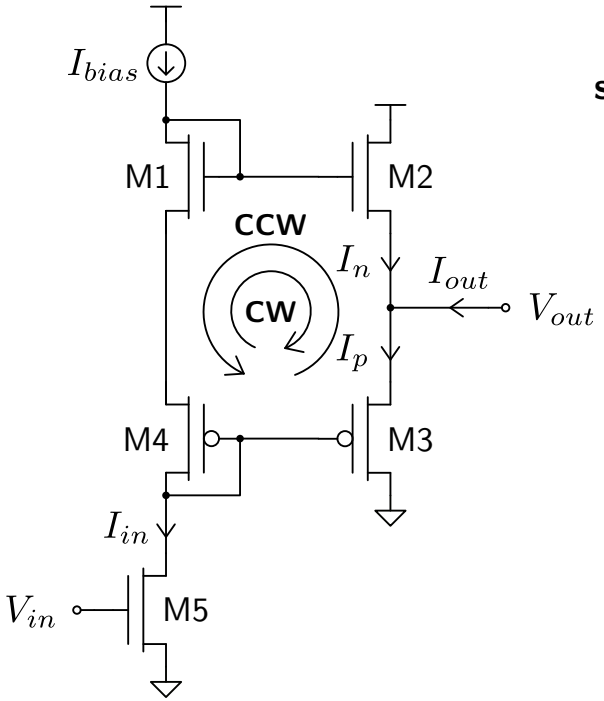

weak inversion sat. $$\frac{I_{bias}}{(W/L)_1}\frac{I_p}{(W/L)_3} = \frac{I_n}{(W/L)_2}\frac{I_{in}}{(W/L)_4}$$

strong inversion sat. $$\sqrt{\frac{I_{bias}}{\beta_1}} + \sqrt{\frac{I_p}{\beta_3}} = \sqrt{\frac{I_n}{\beta_2}} + \sqrt{\frac{I_{in}}{\beta_4}}$$

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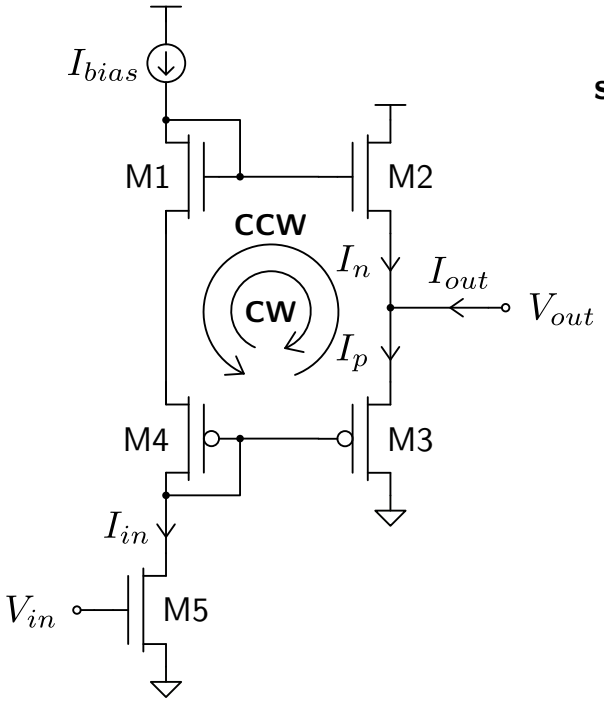
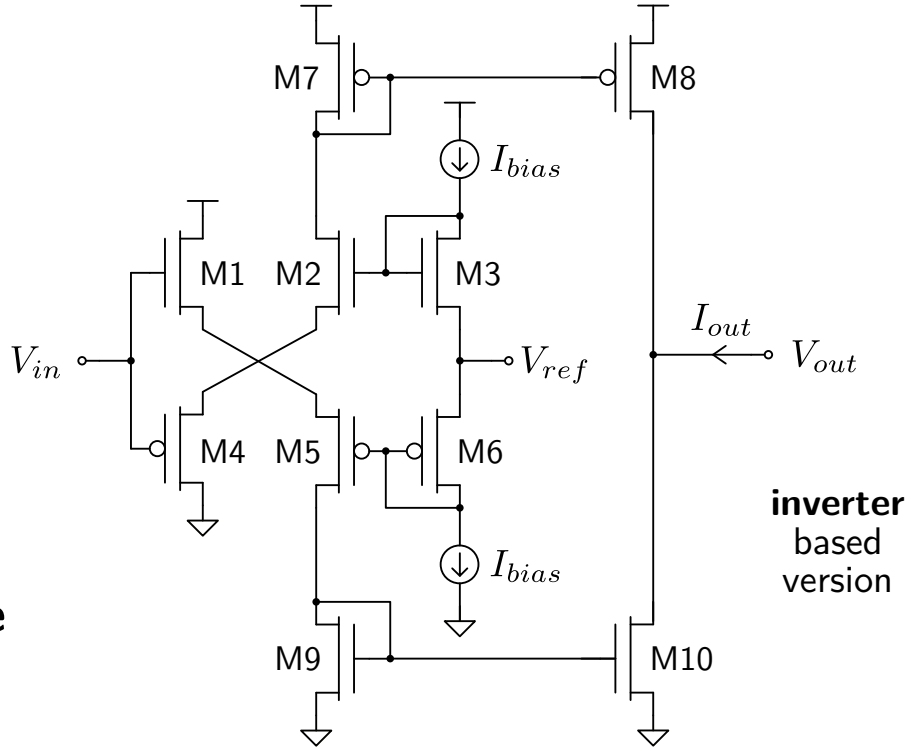


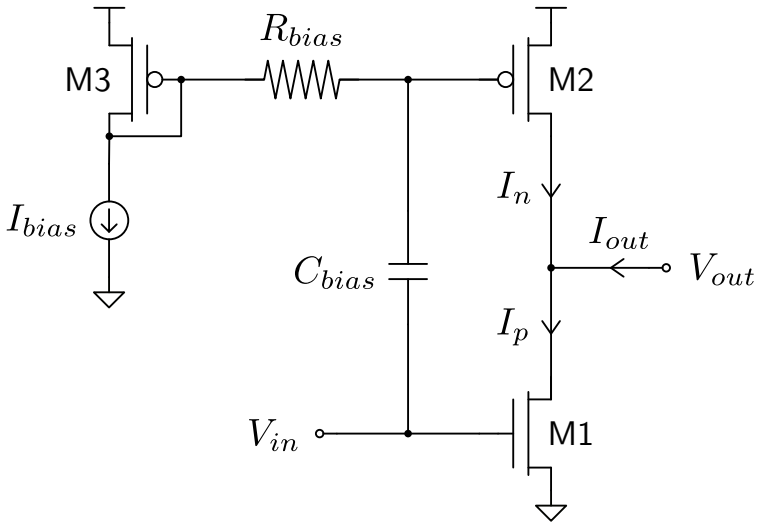
- High **supply voltage** typically required...



inverter based version

Class-AB Stage Examples

- Class-A + **dynamic** biasing:



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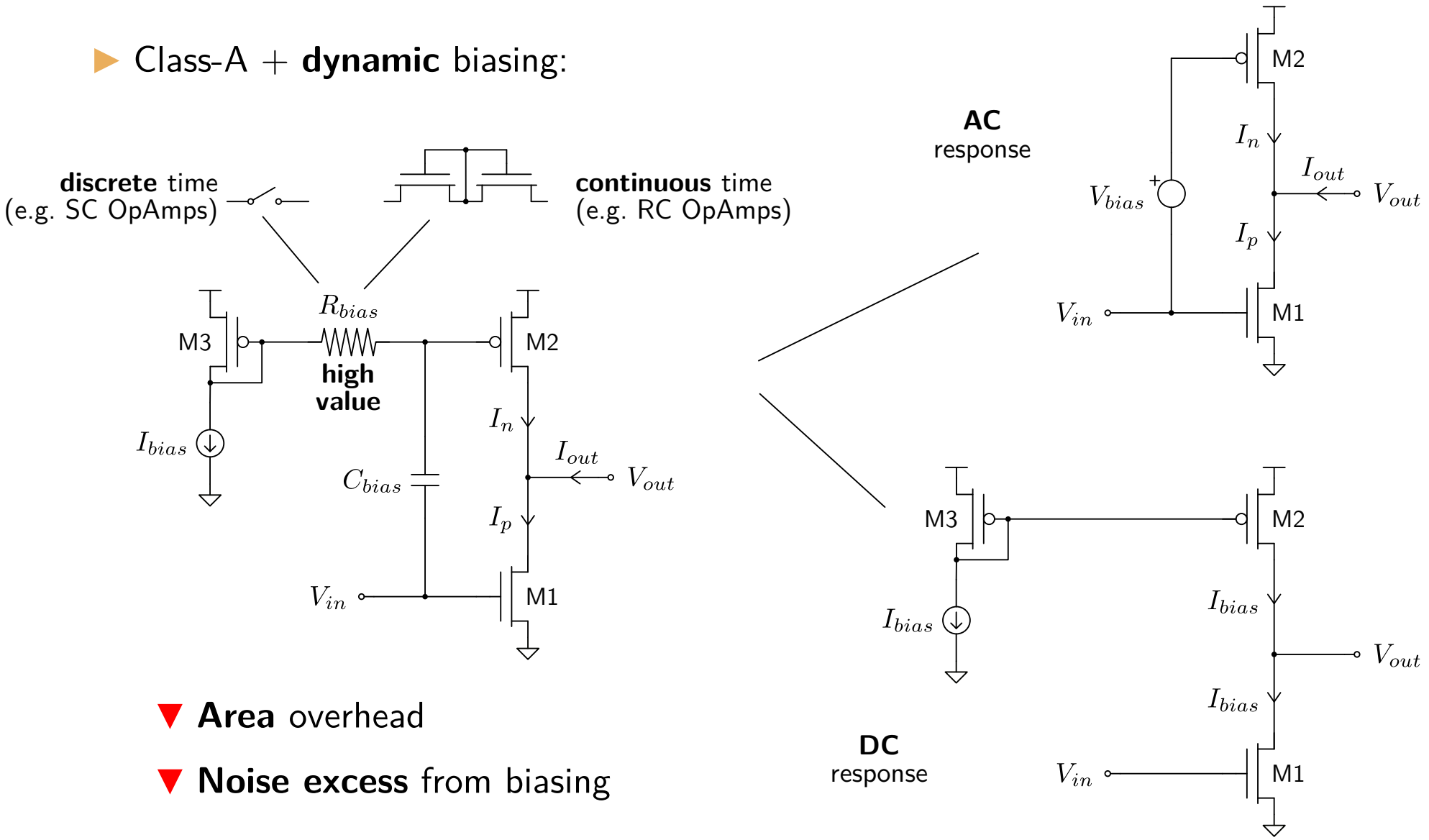
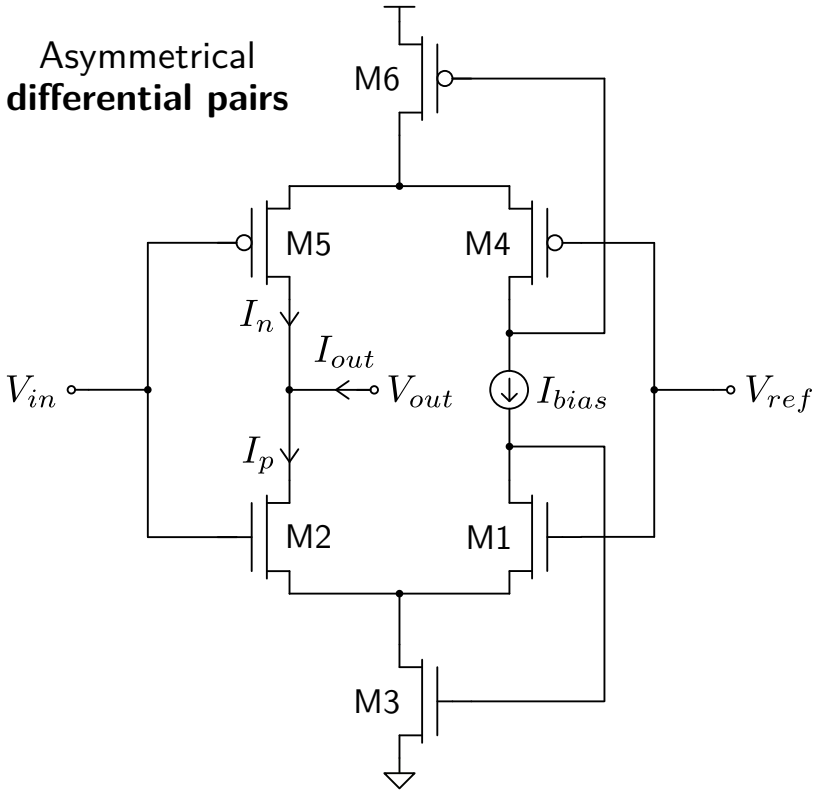
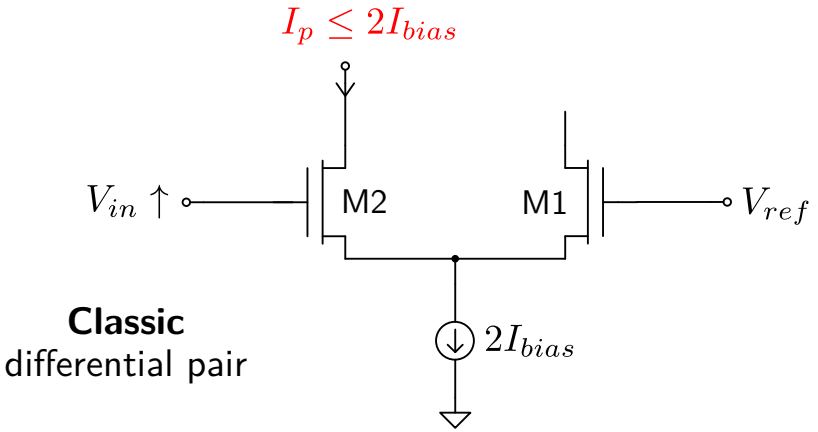


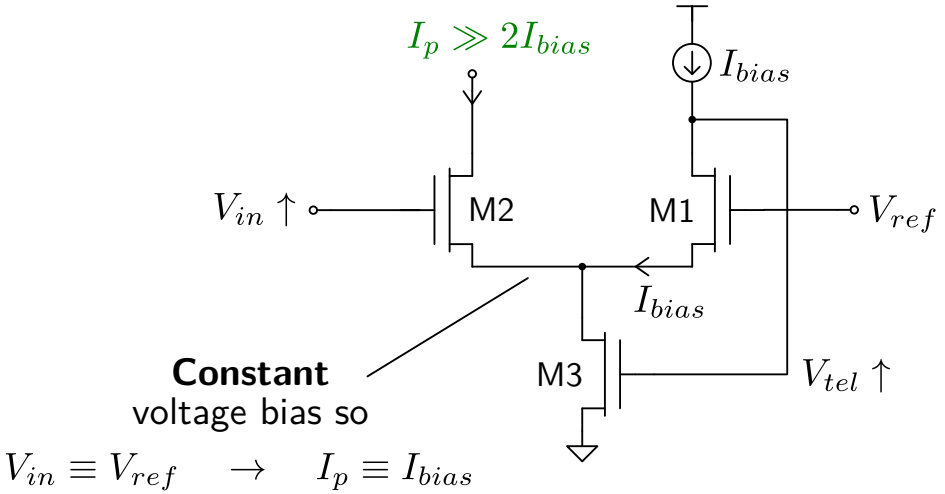
- **Area** overhead
- **Noise excess** from biasing

Class-AB Stage Examples

- **Telescopic** topologies:







$V_{in} \equiv V_{ref} \quad \rightarrow \quad I_p \equiv I_{bias}$

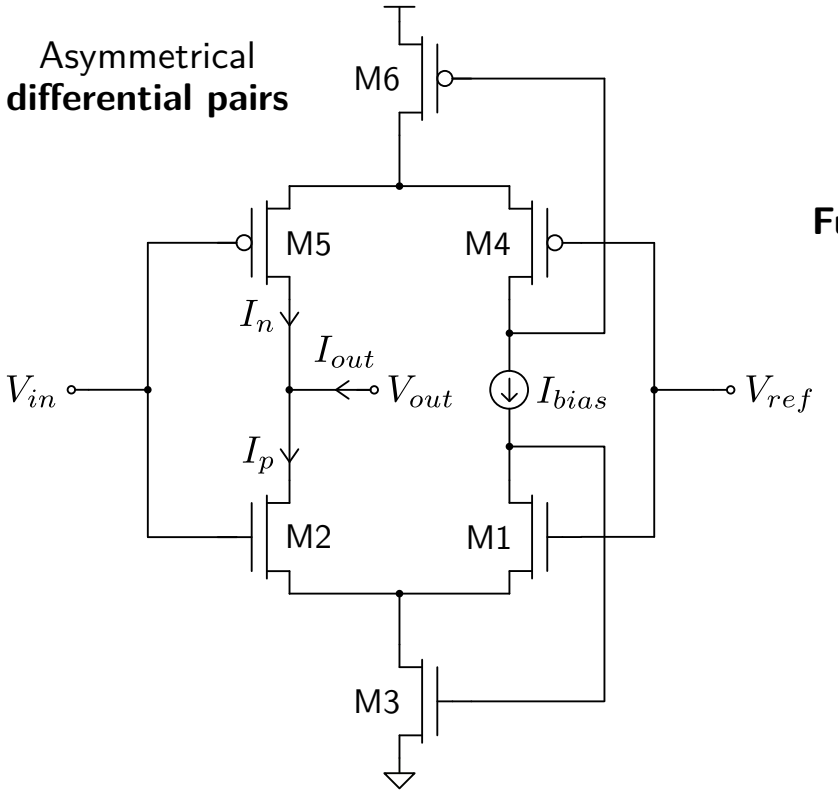
PVT compensated
by **symmetry**...

- Output **range**

Class-AB Stage Examples

- **Telescopic** topologies:

Asymmetrical **differential pairs**



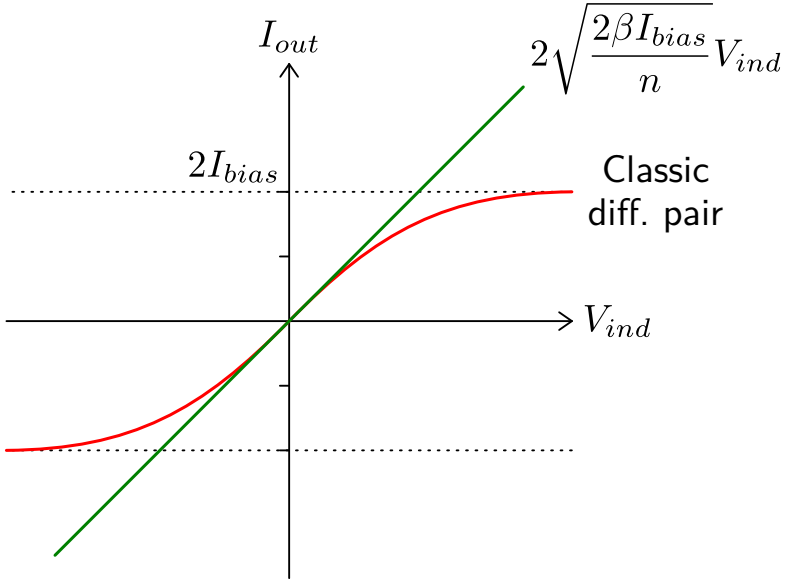
Half-circuit analysis for **strong inversion saturation**

$$\begin{cases} \text{M1:} & I_p = \dfrac{\beta_2}{2n}\left(V_{inp} - V_{TH} - nV_x\right)^2 \\ \text{M2:} & I_{bias} = \dfrac{\beta_1}{2n}\left(V_{inn} - V_{TH} - nV_x\right)^2 \end{cases}$$

$$\sqrt{\frac{2nI_p}{\beta_2}} - \sqrt{\frac{2nI_{bias}}{\beta_1}} = V_{ind}$$

Full-circuit analysis for **M1=M2**

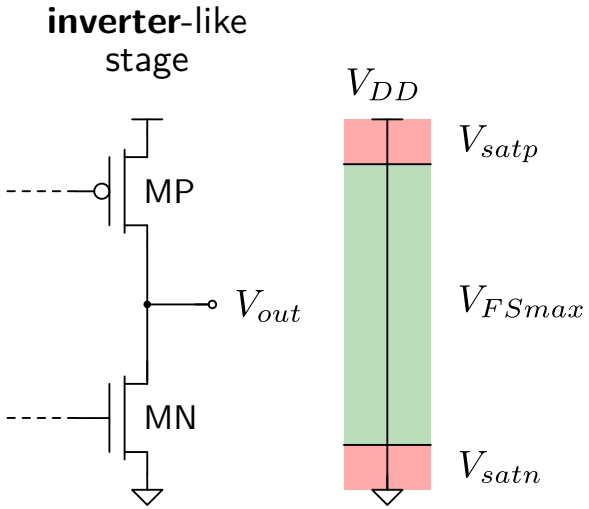
$$\begin{cases} \sqrt{I_p} = \sqrt{I_{bias}} + \sqrt{\dfrac{\beta}{2n}}V_{ind} \\ \sqrt{I_n} = \sqrt{I_{bias}} - \sqrt{\dfrac{\beta}{2n}}V_{ind} \end{cases}$$



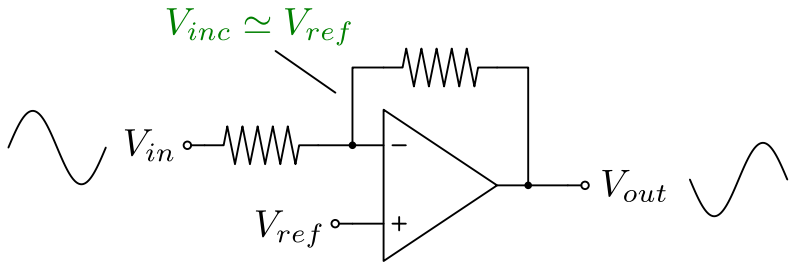
- Output **range**

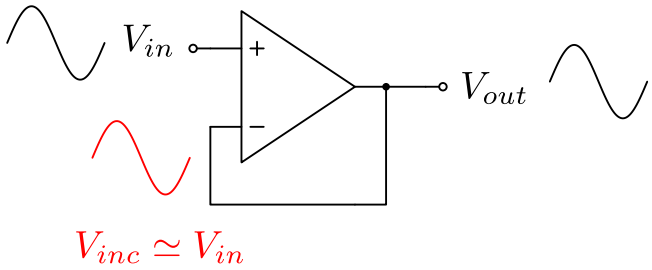
Why Rail-to-Rail?

- Optimization of signal **full-scale** (V_{FS}) and probably dynamic range (DR)
- Compatibility with low **supply voltages** (e.g. battery-powered, energy scavenging)
- Required by **CMFB** in fully differential signal processing
- Already available at OpAmp **output** when no cascode is used:



- Necessary at OpAmp **input**?





Required for certain **feedback** configurations!

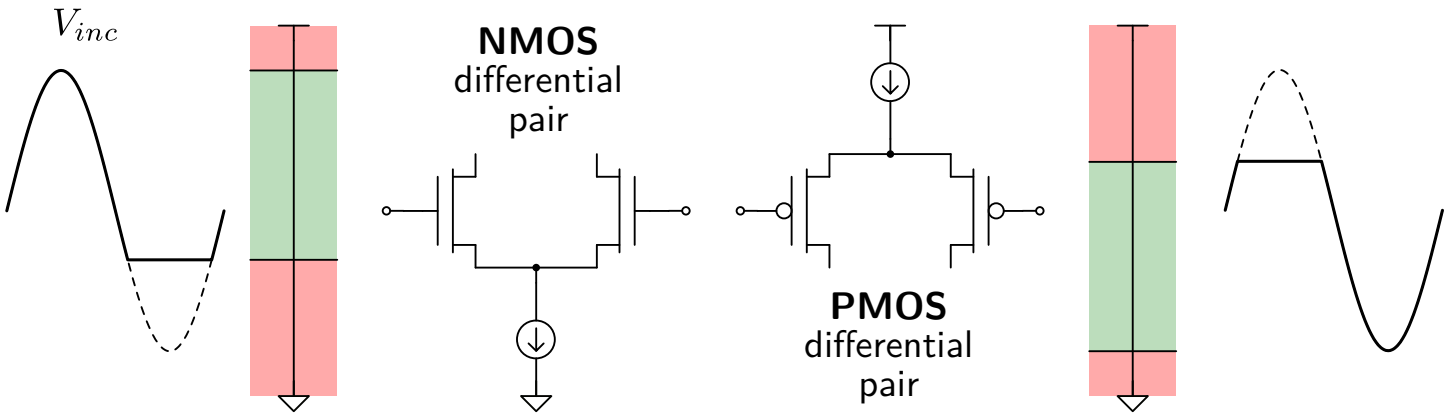
OpAmp Input Transconductance

- Overall **gain** performance:

$$|G(DC)| = g_{in} r_{out}$$

input	output
transconductance	**resistance**
$v \rightarrow i$	$i \rightarrow v$

- **Input** transconductor for rial-to-rail?



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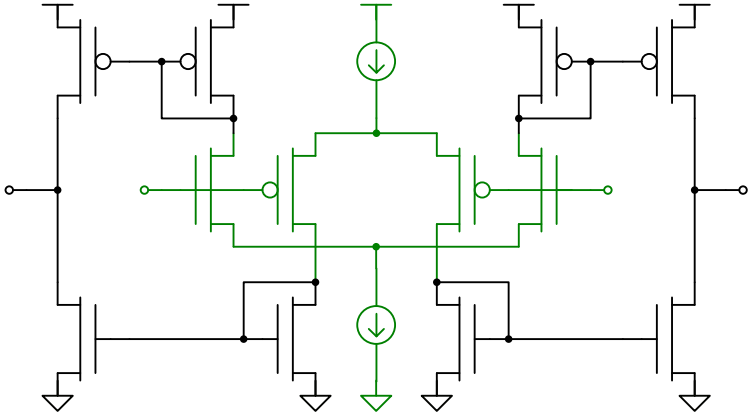
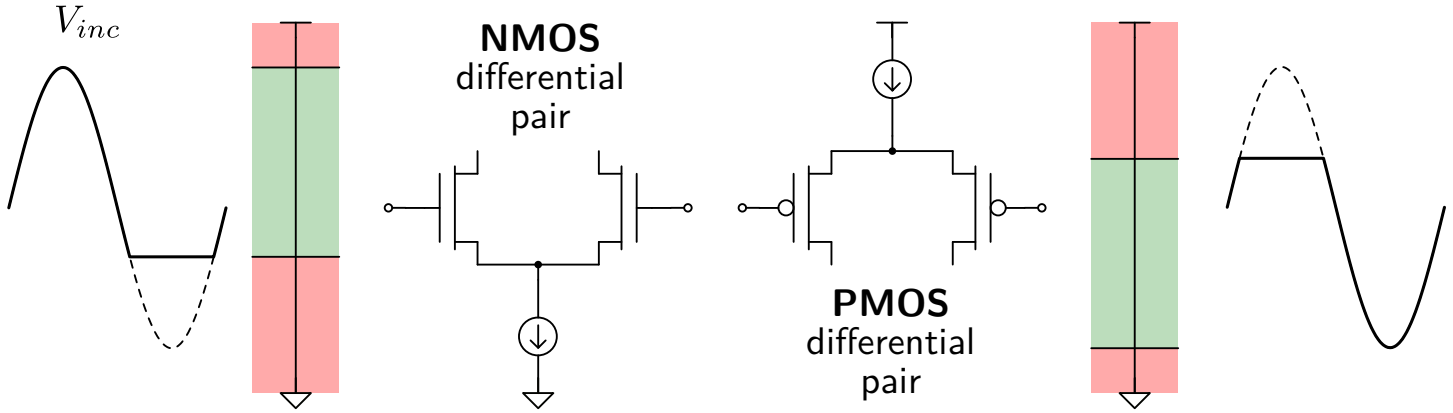
- **Complementary** differential pair





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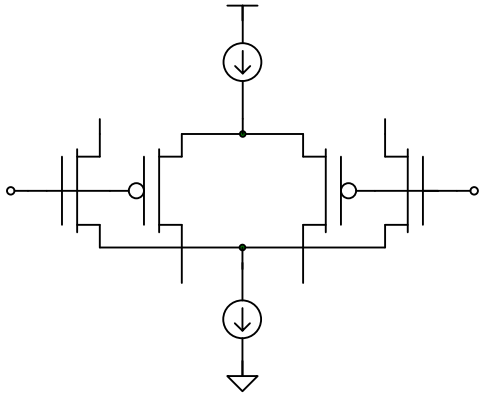
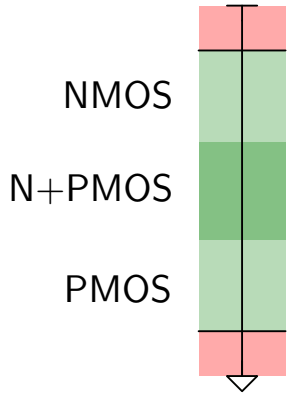
$$|G(DC)| = g_{in} r_{out}$$

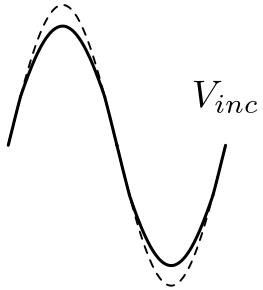
input **transconductance** $v \rightarrow i$

output **resistance** $i \rightarrow v$

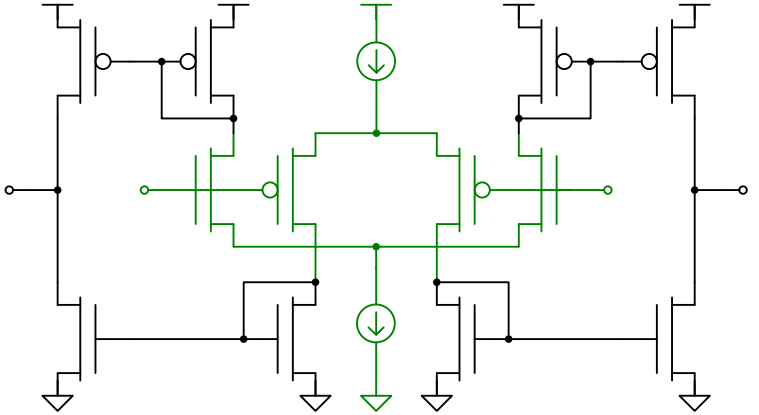
- **Non-constant** transconductance (gain):







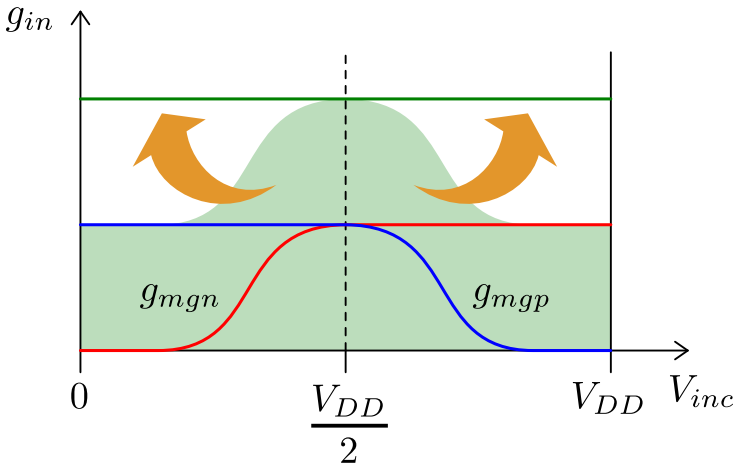
- **Complementary** differential pair

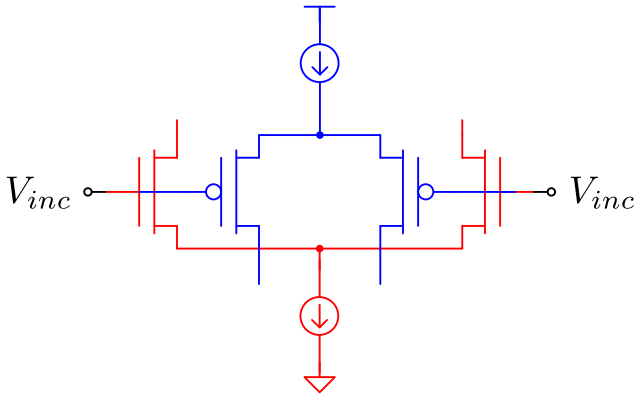


- Specific OpAmp **biasing techniques** are required for rail-to-rail complementary differential pairs

3-Times Current Mirror

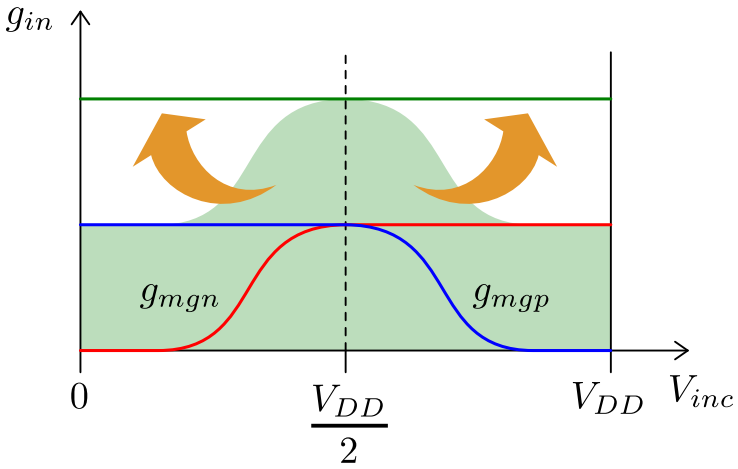
- Complementary differential pair raw input **transconductance**:

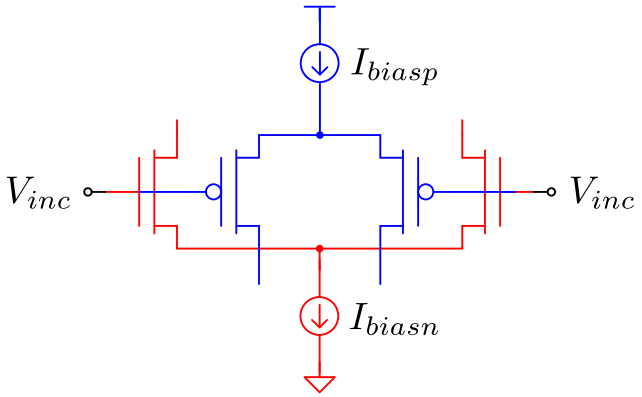




3-Times Current Mirror

- Complementary differential pair raw input **transconductance**:





- Equalization in **strong inversion**:

$$g_{mgn} + g_{mgp} \equiv \text{const}$$

$$\sqrt{2n\beta_n I_{biasn}} + \sqrt{2n\beta_p I_{biasp}} \equiv \text{const}$$

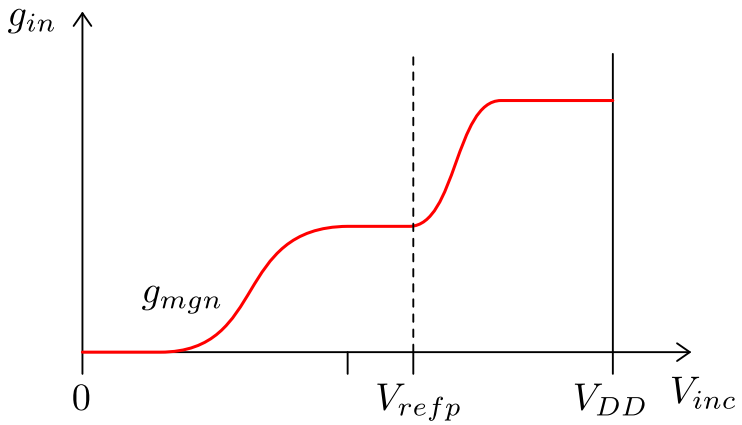
$$\text{e.g. } \frac{(W/L)_p}{(W/L)_n} \equiv \frac{\beta_{un}}{\beta_{up}} \sim 3$$

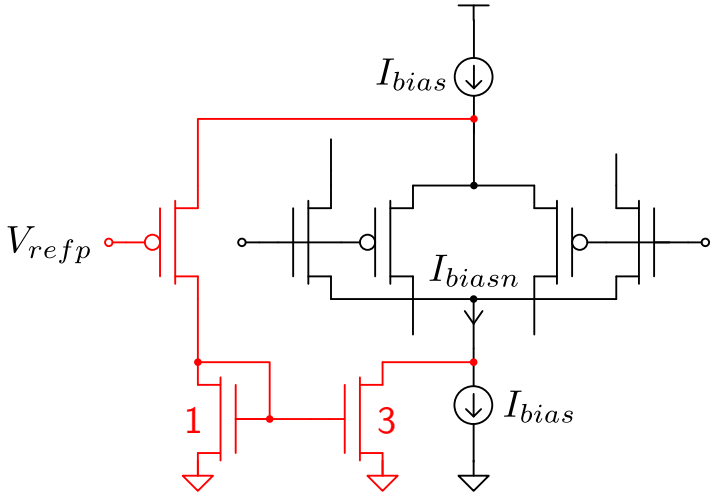
$$\sqrt{I_{biasn}} + \sqrt{I_{biasp}} \equiv \text{const}$$

$$\sqrt{I_{biasn}} + \sqrt{I_{biasp}} = \begin{cases} \sqrt{4I_{bias}} + \sqrt{0} = 2\sqrt{I_{bias}} & \text{NMOS} \\ \sqrt{I_{bias}} + \sqrt{I_{bias}} = 2\sqrt{I_{bias}} & \text{N+PMOS} \\ \sqrt{0} + \sqrt{4I_{bias}} = 2\sqrt{I_{bias}} & \text{PMOS} \end{cases}$$

3-Times Current Mirror

- Equalization in **strong inversion**:

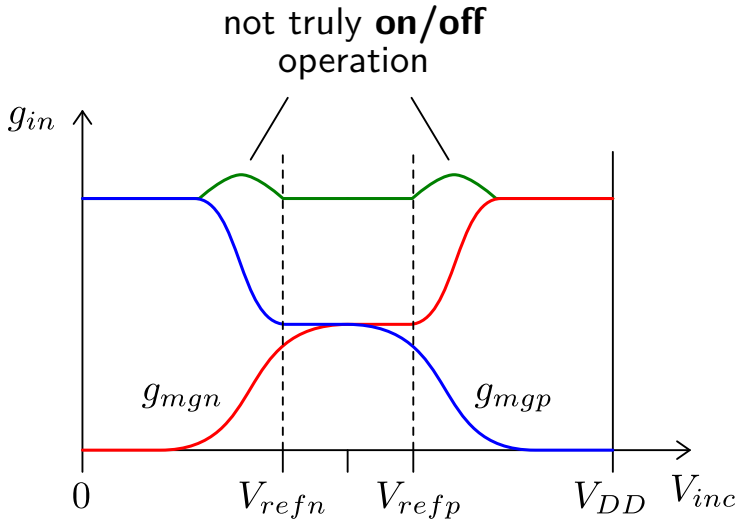


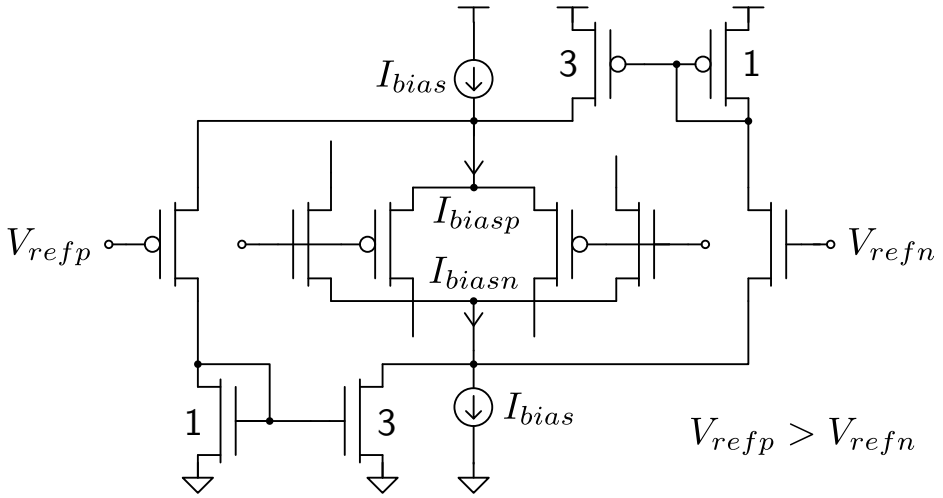


$$\sqrt{I_{biasn}} + \sqrt{I_{biasp}} = \begin{cases} \sqrt{4I_{bias}} + \sqrt{0} = 2\sqrt{I_{bias}} & \text{NMOS} \\ \sqrt{I_{bias}} + \sqrt{I_{bias}} = 2\sqrt{I_{bias}} & \text{N+PMOS} \\ \sqrt{0} + \sqrt{4I_{bias}} = 2\sqrt{I_{bias}} & \text{PMOS} \end{cases}$$

3-Times Current Mirror

- Equalization in **strong inversion**:





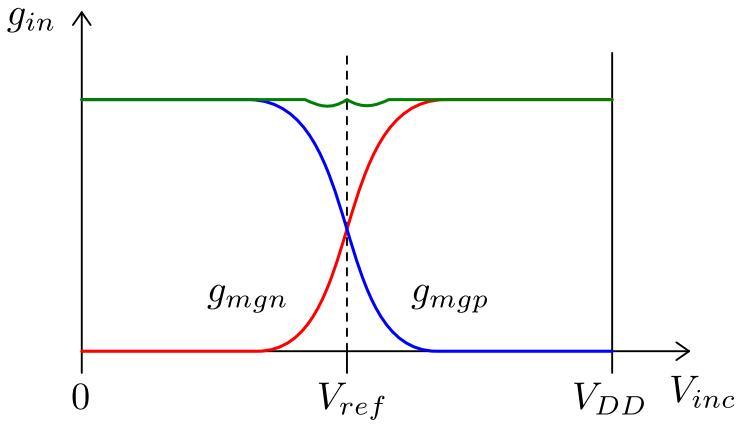
$$\sqrt{I_{biasn}} + \sqrt{I_{biasp}} = \begin{cases} \sqrt{4I_{bias}} + \sqrt{0} = 2\sqrt{I_{bias}} & \text{NMOS} \\ \sqrt{I_{bias}} + \sqrt{I_{bias}} = 2\sqrt{I_{bias}} & \text{N+PMOS} \\ \sqrt{0} + \sqrt{4I_{bias}} = 2\sqrt{I_{bias}} & \text{PMOS} \end{cases}$$

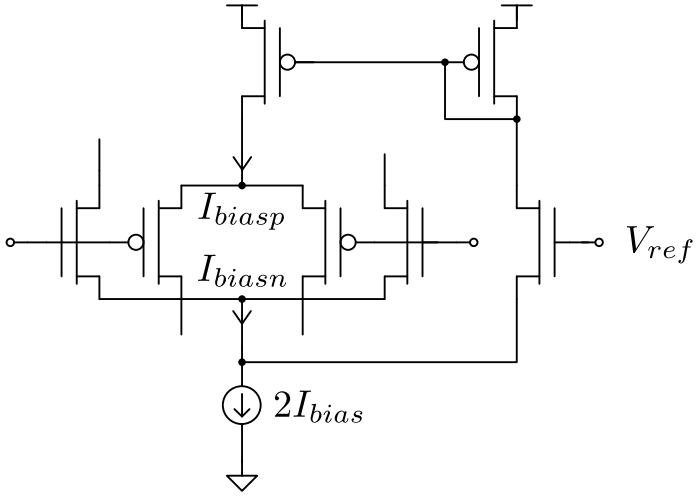
▲ **Compact** bias control

▼ **Non-exact** solution

Current Switch

- Equalization in **weak inversion**:





$$g_{mgn} + g_{mgp} \equiv \text{const}$$

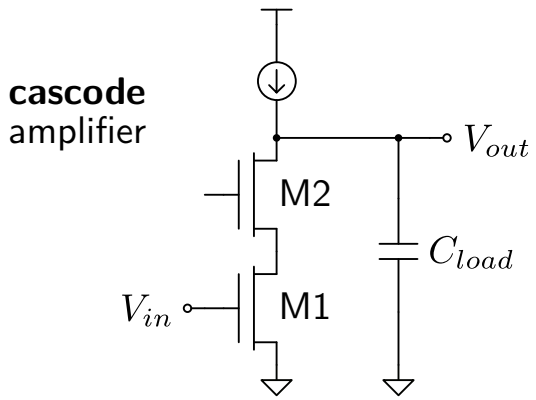
$$\frac{I_{biasn}}{nU_t} + \frac{I_{biasp}}{nU_t} \equiv \text{const}$$

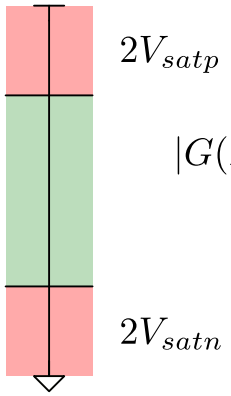
$$I_{biasn} + I_{biasp} \equiv \text{const}$$

- ▲ **Compact** bias control
- ▼ Transconductance equalization **sensitivity** to reference voltage

Cascade vs Cascode

- Low **supply voltage** by avoiding cascoding circuit structures





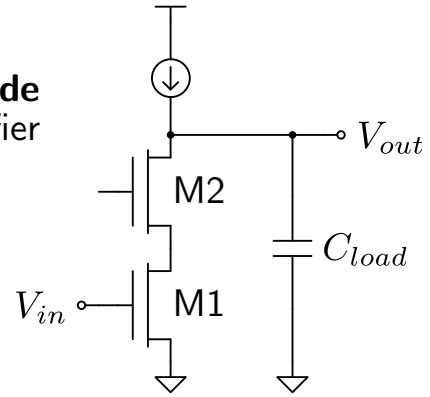
$$|G(DC)| \propto g_{mg1}\left(\frac{1}{g_{md1}}\frac{g_{mg2}}{g_{md2}}\right)$$

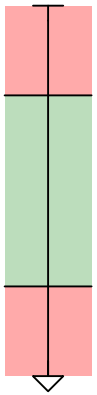
$$GBW = \frac{g_{mg1}}{2\pi C_{load}}$$

Cascade vs Cascode

- Low **supply voltage** by avoiding cascoding circuit structures
- OpAmp **gain** drop may be compensated by **multistage** topologies
- Increase in **power** consumption
- Multipole frequency **compensation** can be tricky!

cascode amplifier

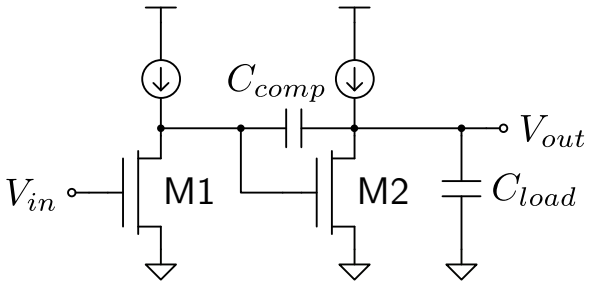


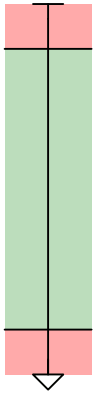


$$|G(DC)| \propto g_{mg1}\left(\frac{1}{g_{md1}}\frac{g_{mg2}}{g_{md2}}\right)$$

$$GBW = \frac{g_{mg1}}{2\pi C_{load}}$$

inverter amplifier



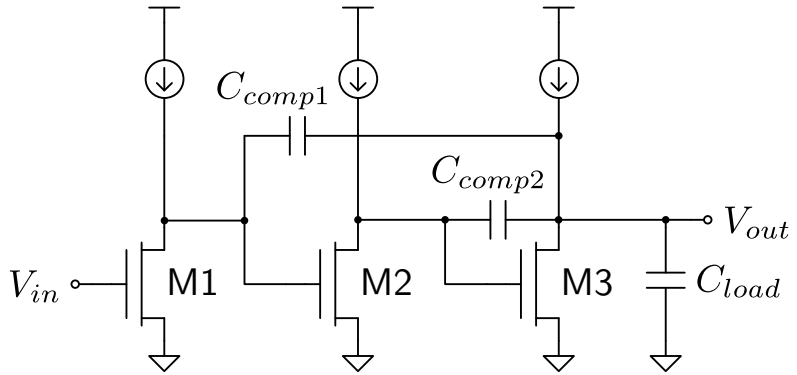


$$|G(DC)| \propto \left(\frac{g_{mg1}}{g_{md1}}\right)\left(\frac{g_{mg2}}{g_{md2}}\right)$$

$$GBW = \frac{g_{mg1}}{2\pi C_{comp}} < \frac{g_{mg2}}{2\pi C_{load}}$$

3-Stage Nested Miller OTA

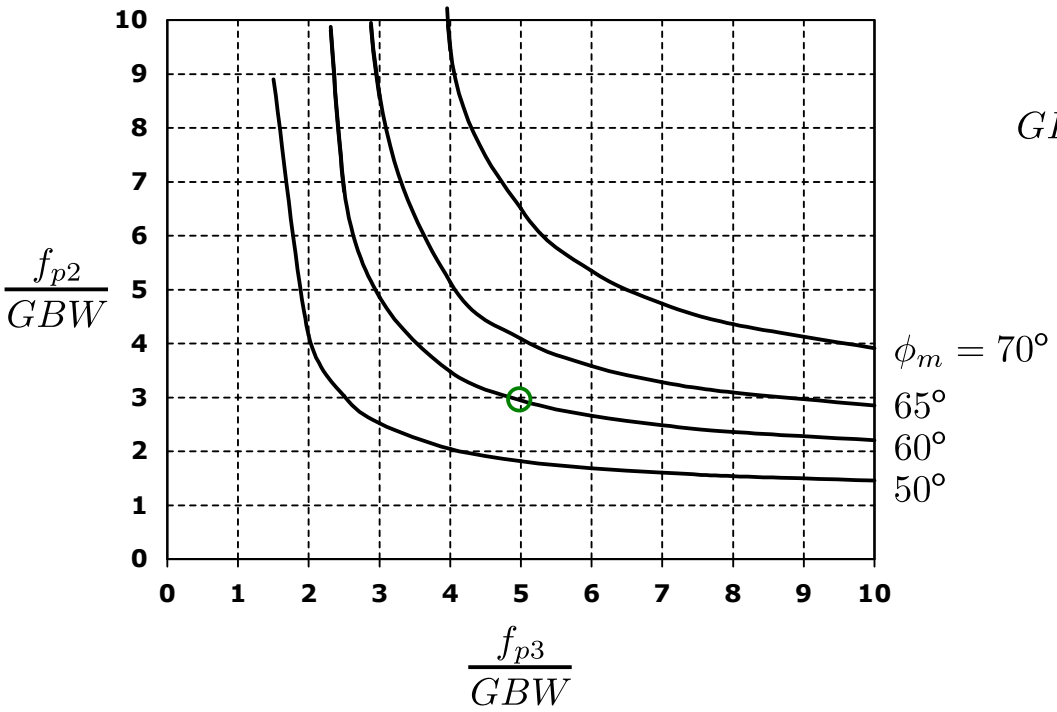
- Inverter as **transconductance** basic building block

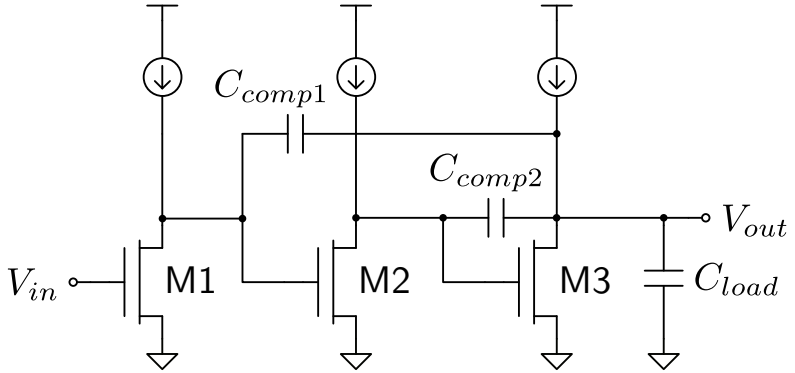


$$GBW = \frac{g_{mg1}}{2\pi C_{comp1}} \qquad f_{p2} = \frac{g_{mg2}}{2\pi C_{comp2}} \qquad f_{p3} = \frac{g_{mg3}}{2\pi C_{load}}$$

3-Stage Nested Miller OTA

- Inverter as **transconductance** basic building block
- **Phase margin** save design





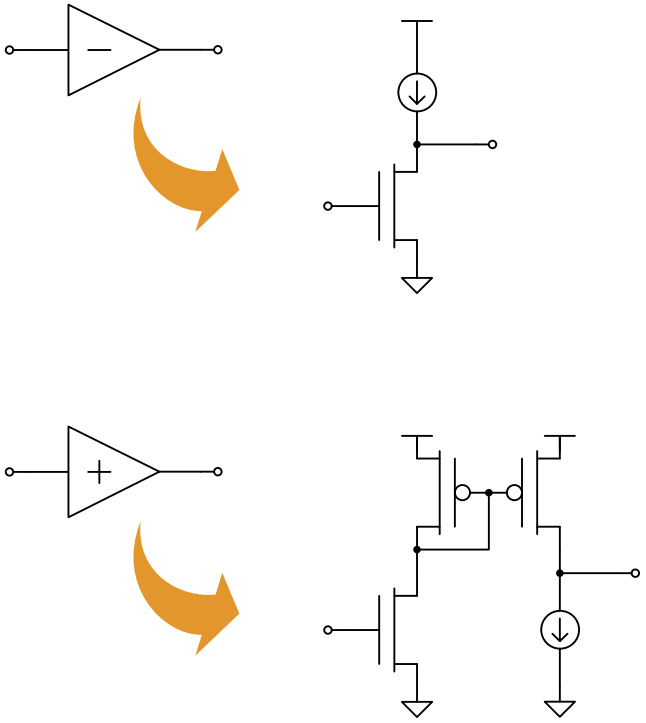
$$GBW = \frac{g_{mg1}}{2\pi C_{comp1}} \qquad f_{p2} = \frac{g_{mg2}}{2\pi C_{comp2}} \qquad f_{p3} = \frac{g_{mg3}}{2\pi C_{load}}$$

$$\phi_m = 90° - \arctan\left(\frac{GBW}{f_{p2}}\right) - \arctan\left(\frac{GBW}{f_{p3}}\right)$$

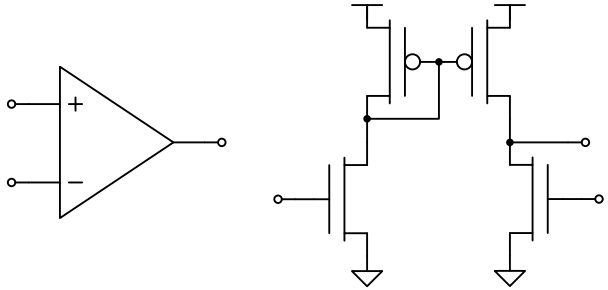
- Increase in **power** consumption
- **Bandwidth** reduction

Nested Gm-C Compensation

- Combination of nested **loops** involving:
  - **Positive**/**negative** transconductors
  - **Miller** compensation capacitors



- **Pseudo**-differential structures:



e.g. **3-stage** OTA