

# Syllabus Guide

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Integrated Circuits and Systems  
IMB-CNM(CSIC)

## 1 Basic Information

## 2 Objectives and Prerequisites

## 3 Theoretical Contents

## 4 Lab Exercises

## 5 Evaluation Methodology

## 6 Recommended Bibliography

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# Basic Info

## ► Who:

- Francesc Serra Graells (**theory + exercises + lab sessions**)  
IMB-CNM(CSIC)  
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tel. 93 5947700

## ► When:

Start!

setembre 2020						
s	Dl	Dt	Dc	Dj	Dv	Ds Dg
0				1	2	3 4
1	7	8	9	10	11	12 13
2	14	15	16	17	18	19 20
3	21	22	23	24	25	26 27
4	28	29	30			

octubre 2020						
s	Dl	Dt	Dc	Dj	Dv	Ds Dg
3				1	2	3 4
4	5	6	7	8	9	10 11
5	12	13	14	15	16	17 18
6	19	20	21	22	23	24 25
7	26	27	28	29	30	31

novembre 2020						
s	Dl	Dt	Dc	Dj	Dv	Ds Dg
8				2	3	4
9	9	10	11	12	13	14 15
10	16	17	18	19	20	21 22
11	23	24	25	26	27	28 29
12	30					

desembre 2020						
s	Dl	Dt	Dc	Dj	Dv	Ds Dg
12				1	2	3 4
13	7	8	9	10	11	12 13
14	14	15	16	17	18	19 20
15	21	22	23	24	25	26 27
16	28	29	30	31		

End!

## ► Where:

- Classroom: Q2/1005
- Laboratory: **TBD**
- <http://cv.uab.cat>
- <http://www.cnm.es/~pserra/uab/damics>

gener 2021						
s	Dl	Dt	Dc	Dj	Dv	Ds Dg
15	4	5	6	7	8	9 10
16	11	12	13	14	15	16 17
17	18	19	20	21	22	23 24
18	25	26	27	28	29	

febrer 2021						
s	Dl	Dt	Dc	Dj	Dv	Ds Dg
19				1	2	3 4 5
20	8	9	10	11	12	13 14
21	15	16	17	18	19	20 21
22	22	23	24	25	26	27 28

- Classroom (Mondays 15:00h-18:00h)
- Laboratory (**TBD**)
- Work presentation (or remedial exam)

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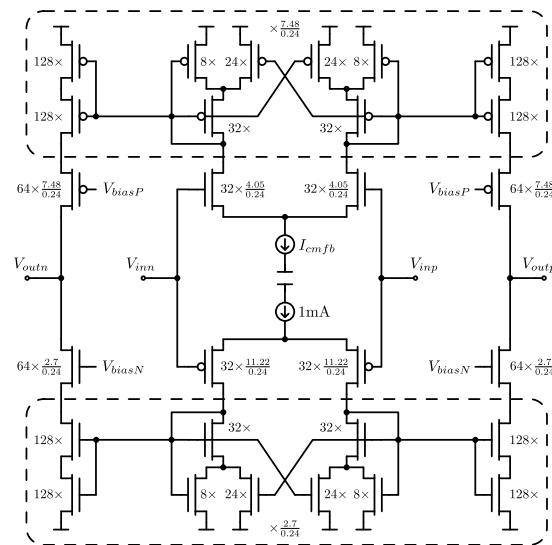
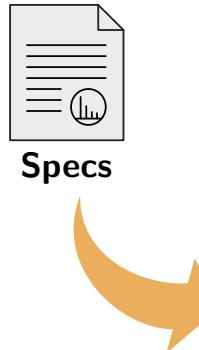
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# Objectives

- ▶ Design techniques for **analog** and mixed integrated circuits in **CMOS** technologies

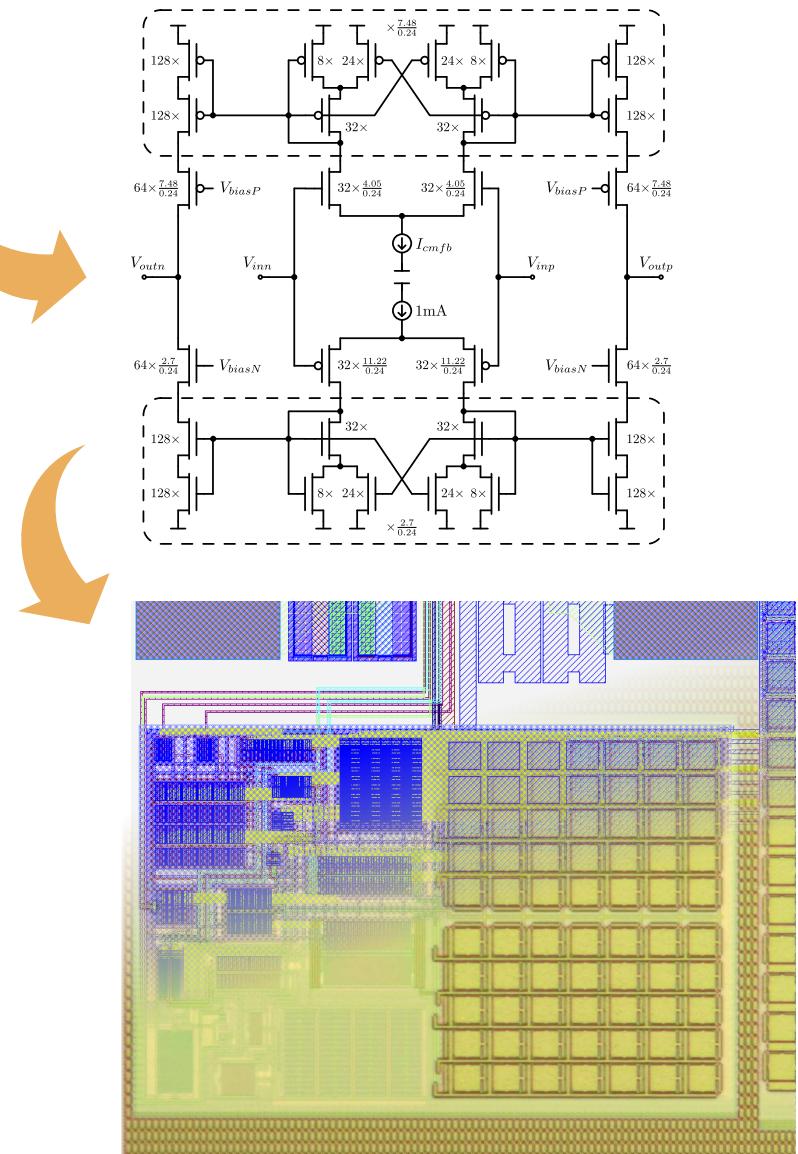


# Objectives

- ▶ Design techniques for **analog** and mixed integrated circuits in **CMOS** technologies
- ▶ Design methodology and EDA tools for **full-custom** ASICs



Specs

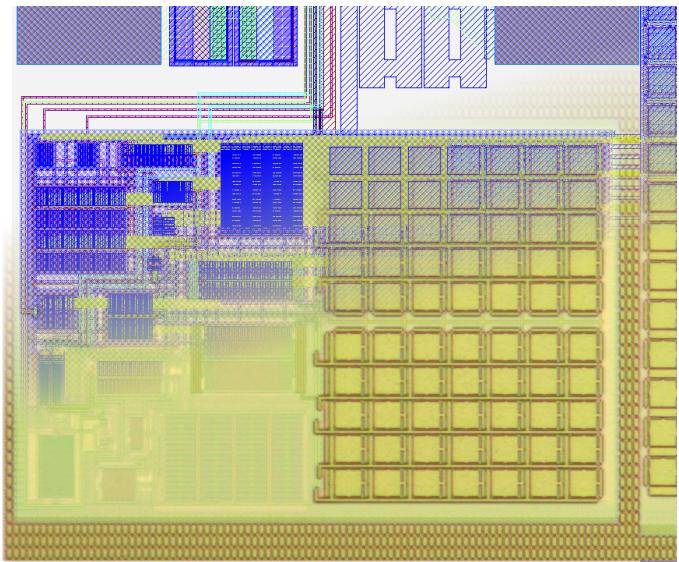
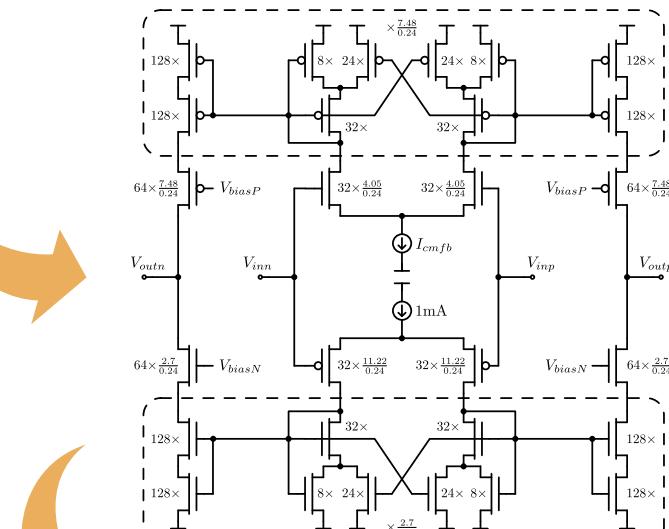


# Objectives

- ▶ Design techniques for **analog** and mixed integrated circuits in **CMOS** technologies
- ▶ Design methodology and EDA tools for **full-custom** ASICs

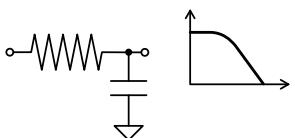


Specs

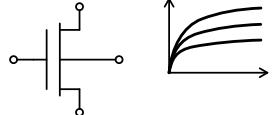


## Prerequisites

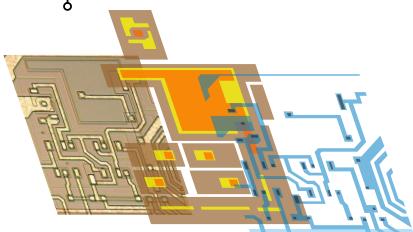
▲ Circuit theory



▲ Electronic devices



▲ Microelectronics technology



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# Theory Contents

## 1 Introduction to the Design of Analog Integrated Circuits

- 1.1 From the Idea to the Chip
- 1.2 Microelectronic vs Electronic Design
- 1.3 CMOS Technologies
- 1.4 Device Modeling
- 1.5 The Operational Amplifier and its FoMs
- 1.6 Lab Proposal: My OpAmp in CNM  
2.5µm CMOS Technology (CNM25)

## 2 Single Stage OpAmps

- 2.1 The Mono-Transistor Amplifier
- 2.2 Differential Topologies
- 2.3 Common Mode Feedback
- 2.4 Folded Amplifiers
- 2.5 Cascode Topologies
- 2.6 Gain Enhancement Techniques

## 3 Multi-Stage OpAmps

- 3.1 Two-Stage Topologies
- 3.2 Miller Effect
- 3.3 Frequency Compensation
- 3.4 Design Space

## 4 Full-Custom Analog Design Methodology

- 4.1 Device Sizing
- 4.2 Process and Mismatching Simulation
- 4.3 The Art of Analog Layout
- 4.4 Physical Verification
- 4.5 Parasitics Extraction
- 4.6 DFM Techniques

# Theory Contents

(Seminar: **Lab Exercises in CNM25**)

## 5 Low-Power OpAmps

- 5.1 Low-Voltage vs Low-Current
- 5.2 Subthreshold Operation
- 5.3 Class-AB Output Stages
- 5.4 Rail-to-Rail Topologies
- 5.5 Inverted-Based Pseudo-Differential Multi-Stage Architectures

## 6 OpAmp Application Examples

- 6.1 Pre-Amplification
- 6.2 MRC-Amplifiers for AGC
- 6.3 Continuous-Time Gm-C Filters
- 6.4 Switched-Capacitor Filters

## 7 Integrated Data Converters

- 7.1 ADC vs DAC
- 7.2 Flash Architectures
- 7.3 SAR Topologies
- 7.4 Integrating Solutions
- 7.5 Delta-Sigma Modulators

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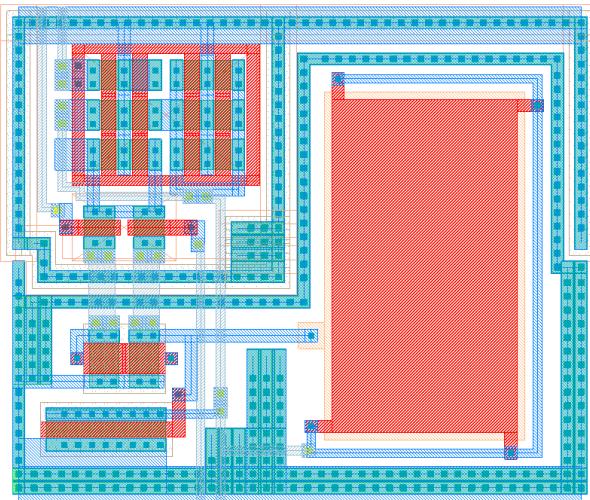
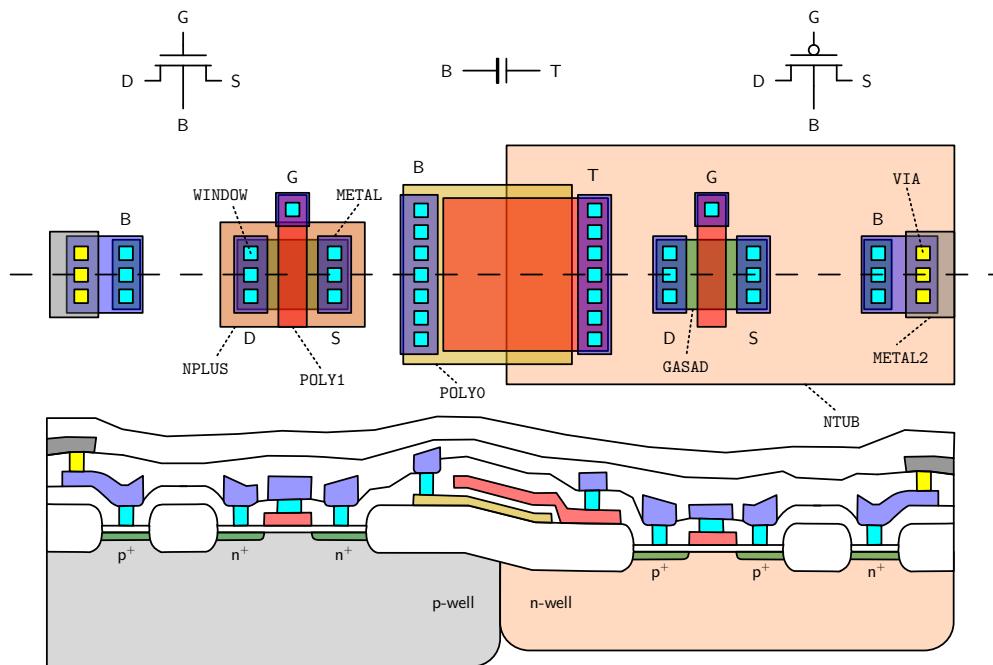
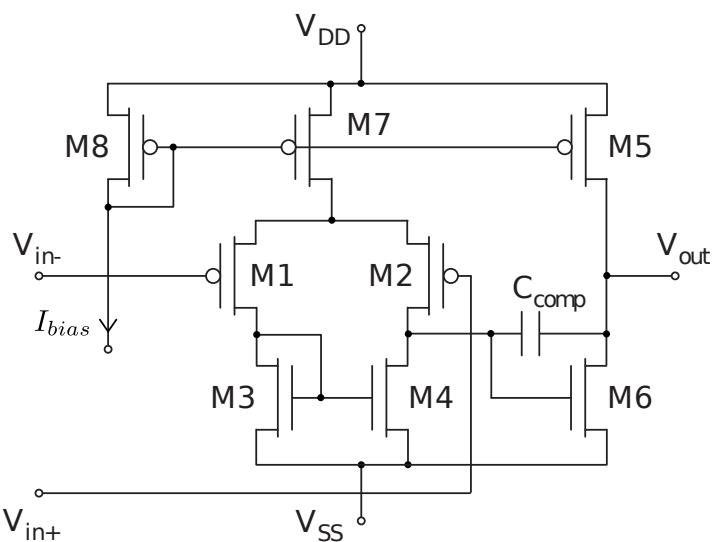
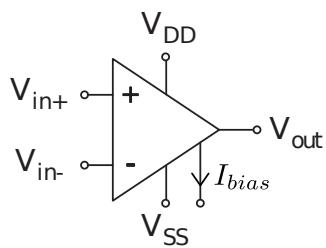
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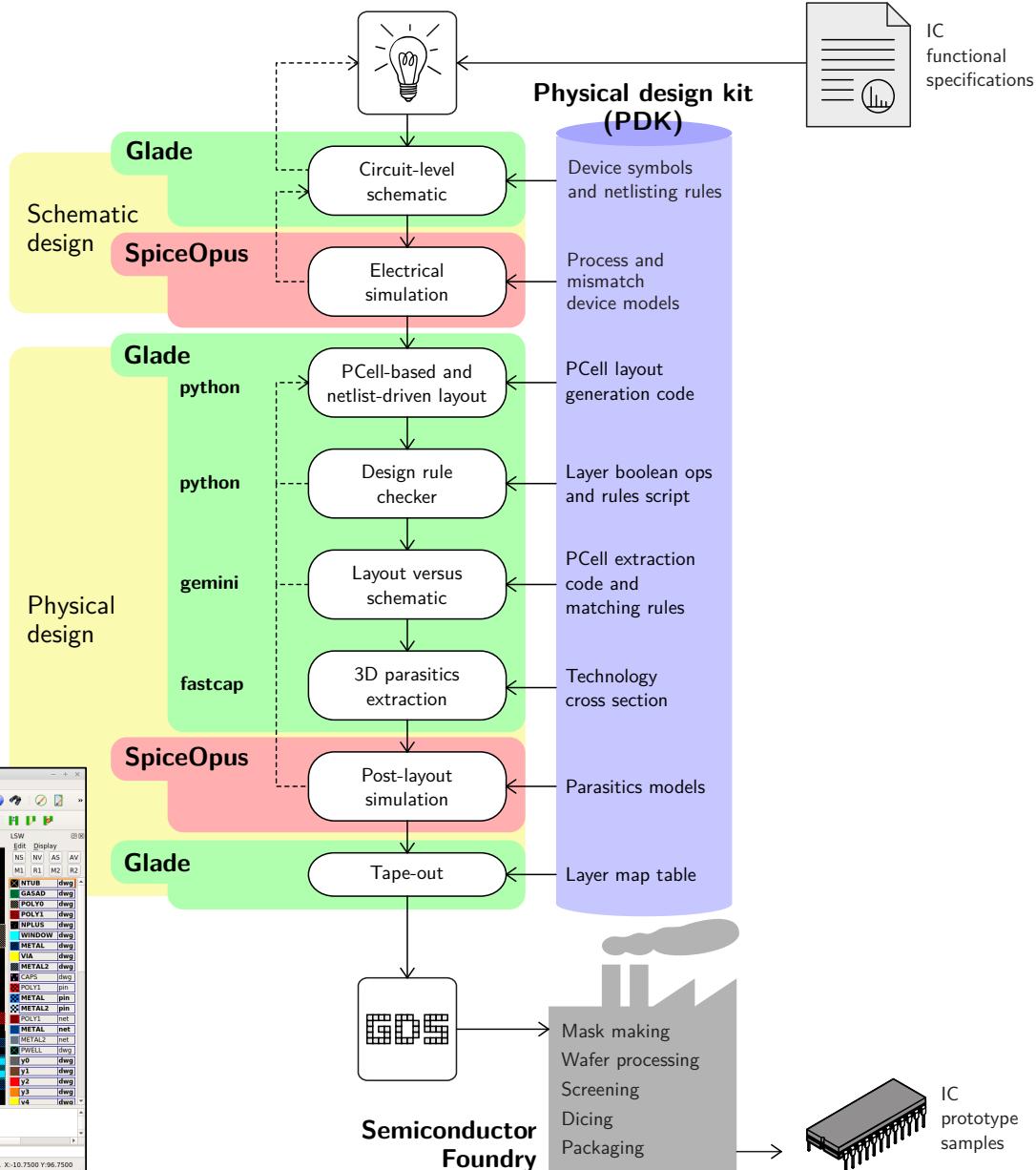
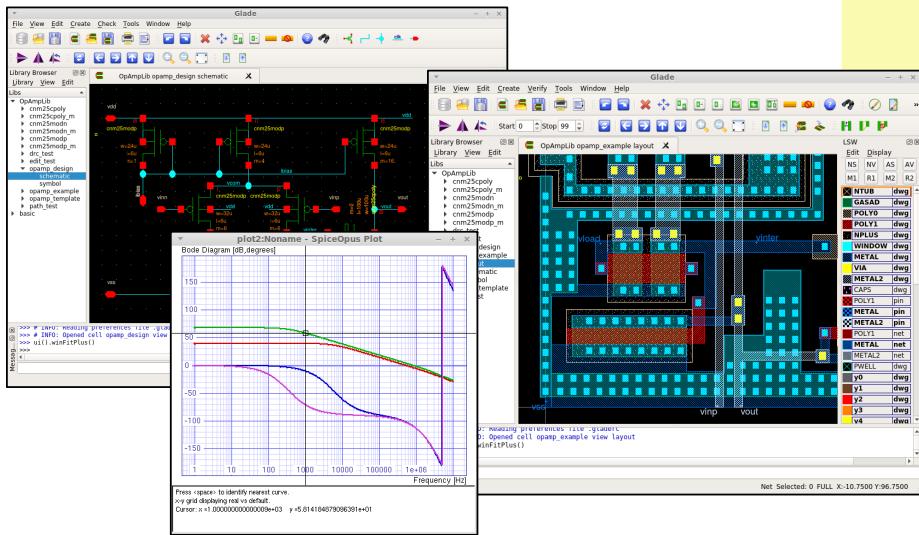
# Lab Exercises

- ▶ Two-stage Miller OpAmp design case
- ▲ Simple 2.5μm 2P2M CMOS technology (CNM25)



# Lab Exercises

- ▶ Two-stage Miller OpAmp design case
- ▲ Simple 2.5µm 2P2M CMOS technology (CNM25)
- ▲ Freeware and multi-OS (MS Windows, Linux) full-custom EDA tools
- ▲ Work at home and tutorial at lab...



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# Evaluation Methodology

► If  $Q_{\text{work,lab}} \geq \frac{3}{10}$  :

homework exercises

$$Q_{\text{overall}} = 0.1Q_{\text{exercises}} + 0.4Q_{\text{lab}} + 0.5Q_{\text{work}}$$

else or if  $Q_{\text{overall}} < \frac{5}{10}$  :

$$Q_{\text{overall}} = 0.1Q_{\text{exercises}} + 0.4Q_{\text{lab}} + 0.5Q_{\text{exam}}$$

▲ **Distributed** weights

▲ **Continuous** evaluation

▲ **No exam** need to be passed

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# Recommended Bibliography

- ▲ Self-contained theory in slides
- ▲ Practical problems solved at classroom
- ▲ Hands-on lab exercises

 <http://www.aicdesign.org>



## ► Additional reference material:

- P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press
- B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Education
- F. Maloberti, *Analog Design for CMOS VLSI Systems*, Kluwer Academic Publishers
  
- T. Tuma and A. Burmen, *Circuit Simulation with SPICE OPUS: Theory and Practice*, Modeling and Simulation Science, Engineering and Technology, Birkhäuser Boston
- A. Hastings, *The Art of Analog Layout*, Pearson Prentice Hall