Syllabus Guide

Francesc Serra Graells

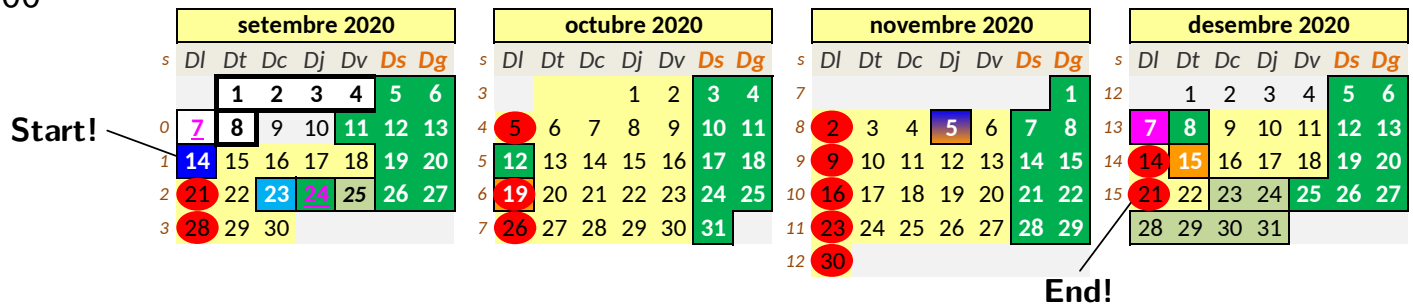
francesc.serra.graells@uab.cat
Departament de Microelectrònica i Sistemes Electrònics
Universitat Autònoma de Barcelona

paco.serra@imb-cnm.csic.es
Integrated Circuits and Systems
IMB-CNM(CSIC)

Basic Info

- **Who**:
  - Francesc Serra Graells (**theory** + **exercises** + **lab sessions**)
    IMB-CNM(CSIC)
    paco.serra@imb-cnm.csic.es
    tel. 93 5947700

- **When**:



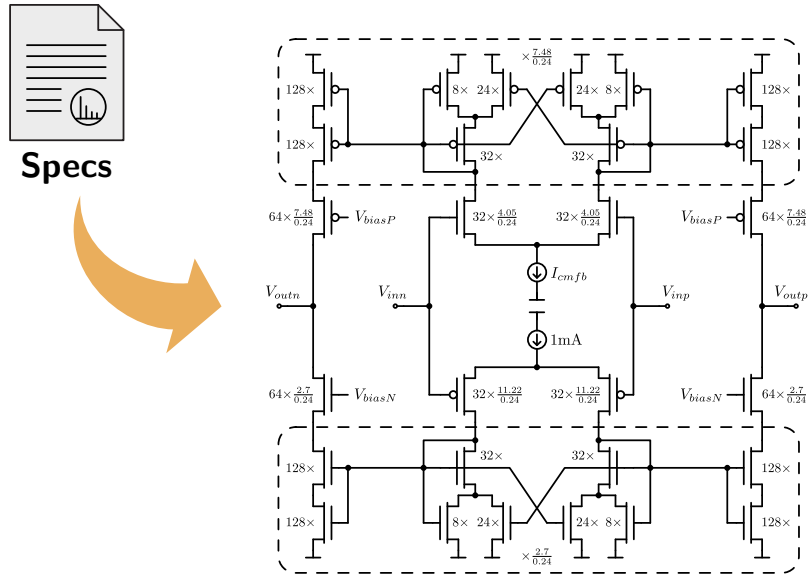
- **Where**:
  - Classroom: Q2/1005
  - Laboratory: **TBD**

- `http://cv.uab.cat`
- `http://www.cnm.es/~pserra/uab/damics`

- Classroom (Mondays 15:00h-18:00h)
- Laboratory (**TBD**)
- Work presentation (or remedial exam)

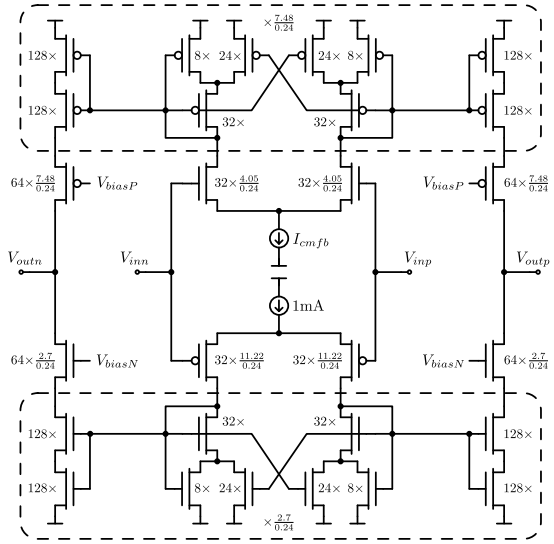
Objectives

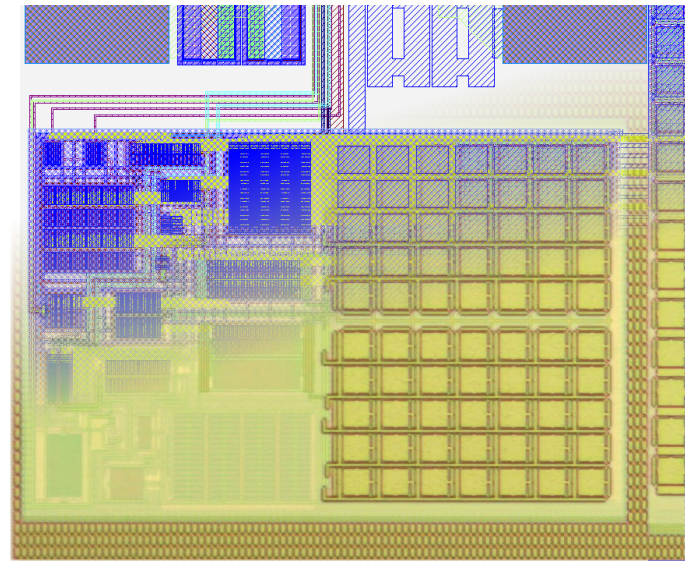
- Design techniques for **analog** and mixed integrated circuits in **CMOS** technologies



Objectives

- Design techniques for **analog** and mixed integrated circuits in **CMOS** technologies
- Design methodology and EDA tools for **full-custom** ASICs





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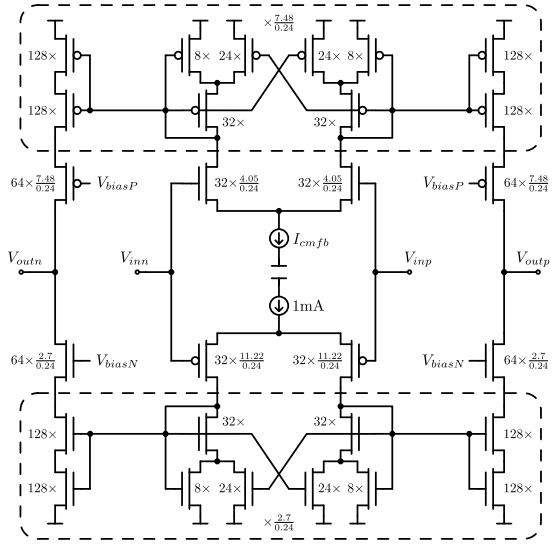
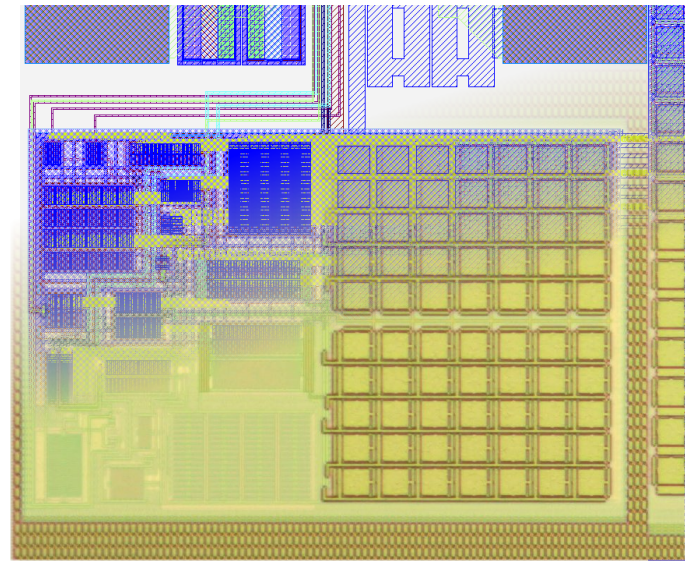
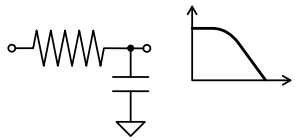


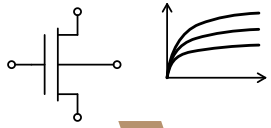


Prerequisites

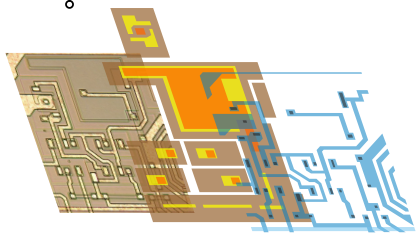
- Circuit theory



- Electronic devices



- Microelectronics technology



Theory Contents

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(Seminar: **Lab Exercices in CNM25**)

5 Low-Power OpAmps

- 5.1 Low-Voltage vs Low-Current
- 5.2 Subthreshold Operation
- 5.3 Class-AB Output Stages
- 5.4 Rail-to-Rail Topologies
- 5.5 Inverted-Based Pseudo-Differential Multi-Stage Architectures

6 OpAmp Application Examples

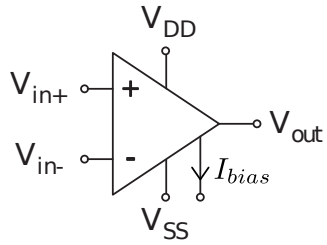
- 6.1 Pre-Amplification
- 6.2 MRC-Amplifiers for AGC
- 6.3 Continuous-Time Gm-C Filters
- 6.4 Switched-Capacitor Filters

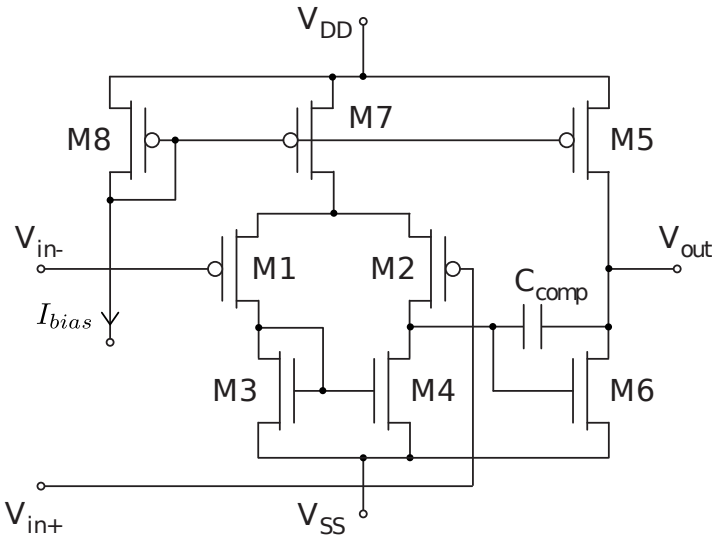
7 Integrated Data Converters

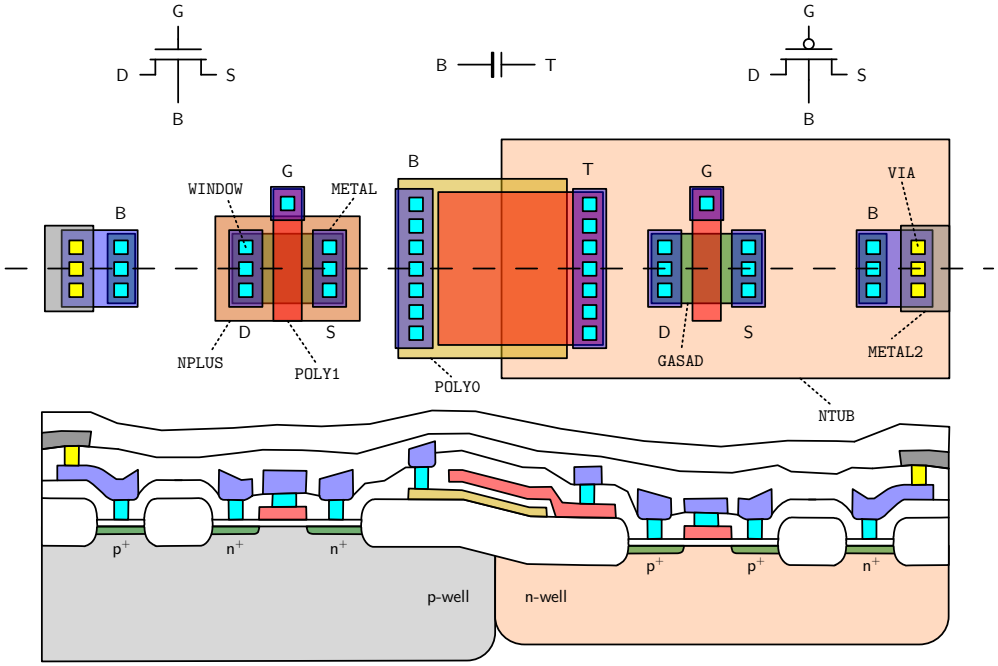
- 7.1 ADC vs DAC
- 7.2 Flash Architectures
- 7.3 SAR Topologies
- 7.4 Integrating Solutions
- 7.5 Delta-Sigma Modulators

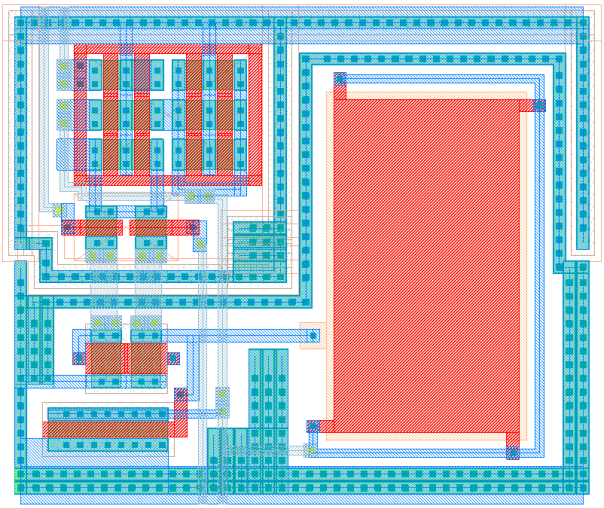
Lab Exercises

- Two-stage Miller **OpAmp** design case
- **Simple** 2.5µm 2P2M CMOS technology (CNM25)



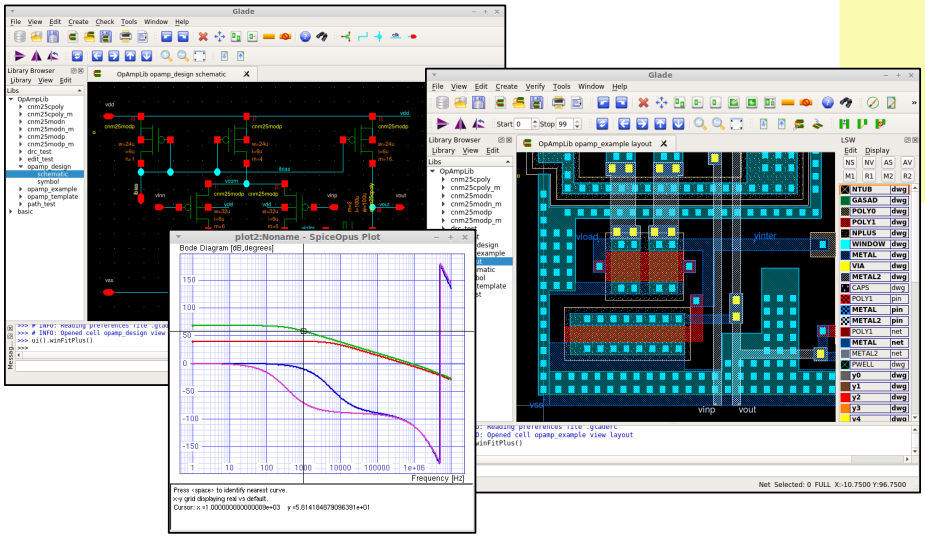


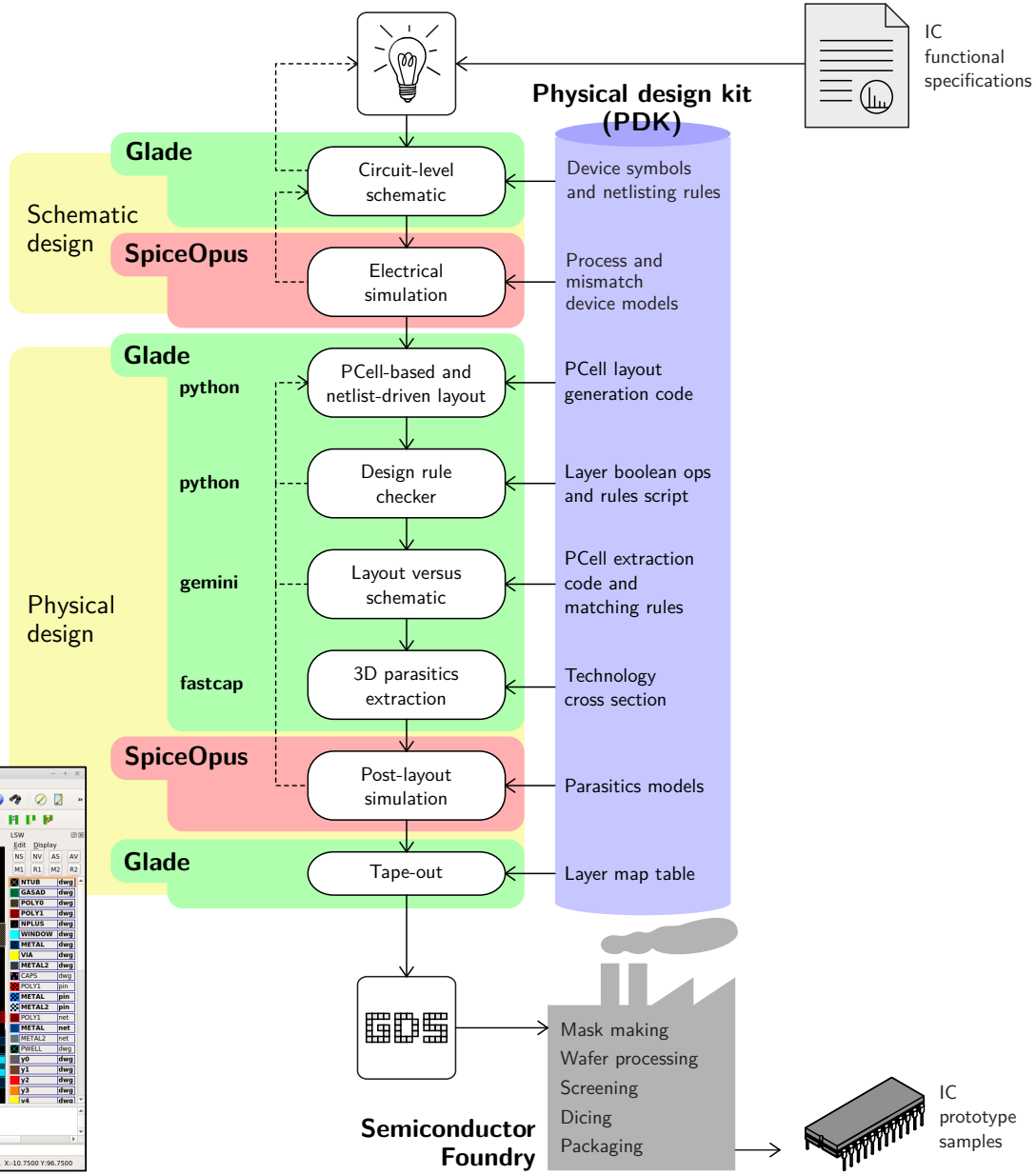




Lab Exercises

- Two-stage Miller **OpAmp** design case
- **Simple** 2.5µm 2P2M CMOS technology (CNM25)
- **Freeware** and **multi-OS** (MS Windows, Linux) full-custom EDA tools
- Work at **home** and tutorial at **lab**...





Evaluation Methodology

- If $Q_{\text{work,lab}} \geq \frac{3}{10}$:

$$Q_{\text{overall}} = 0.1Q_{\text{exercises}} + 0.4Q_{\text{lab}} + 0.5Q_{\text{work}}$$

homework exercises

else or if $Q_{\text{overall}} < \frac{5}{10}$:

$$Q_{\text{overall}} = 0.1Q_{\text{exercises}} + 0.4Q_{\text{lab}} + 0.5Q_{\text{exam}}$$

- **Distributed** weights
- **Continuous** evaluation
- **No exam** need to be passed

Recommended Bibliography

- Self-contained theory in slides
- Practical problems solved at classroom
- Hands-on lab exercises

http://www.aicdesign.org

- **Additional** reference material:
  - P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press
  - B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Education
  - F. Maloberti, *Analog Design for CMOS VLSI Systems*, Kluwer Academic Publishers
  - T. Tuma and A. Burmen, *Circuit Simulation with SPICE OPUS: Theory and Practice*, Modeling and Simulation Science, Engineering and Technology, Birkhäuser Boston
  - A. Hastings, *The Art of Analog Layout*, Pearson Prentice Hall