A Low-Power Neuromorphic CMOS Delta-Sigma Modulator Featuring Tunable Background Attenuation and Potentiostatic Asynchronous Readout for Smart Amperometric Electrochemical Sensors

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Introduction: Amperometric sensors

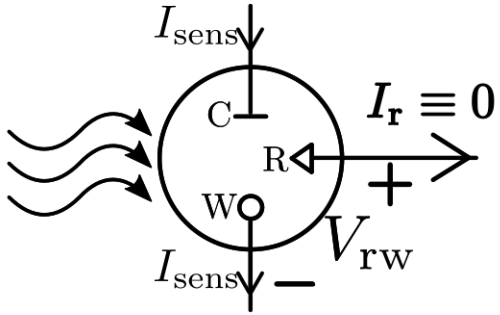
- Three electrodes:
  - **W**orking
  - **R**eference
  - **C**ounter

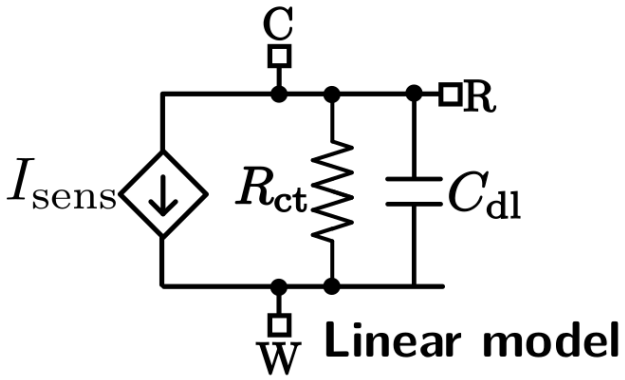
- Potentiostatic operation:
  - Constant $\mathbf{V_{RW}}$
  - null $\mathbf{I_R}$

- Signal current associated to the electrons involved in a **redox** process

$$0 + e^- \underset{\text{ox}}{\overset{\text{red}}{\rightleftharpoons}} R$$

- Dynamic range limited by background currents (resistive losses and capacitive currents)





Introduction: Objectives

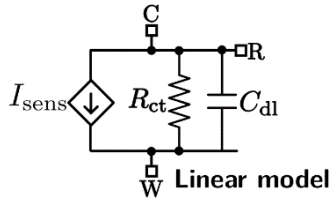
Neruromorphic, adaptive Delta-Sigma (ΔΣ) Modulator readout architecture:

- **Clockless data conversion** (sampling rate according to WE current dynamics)
- **Tunable** and **embedded data compression** (low-pass filtering of out-of-band background components)

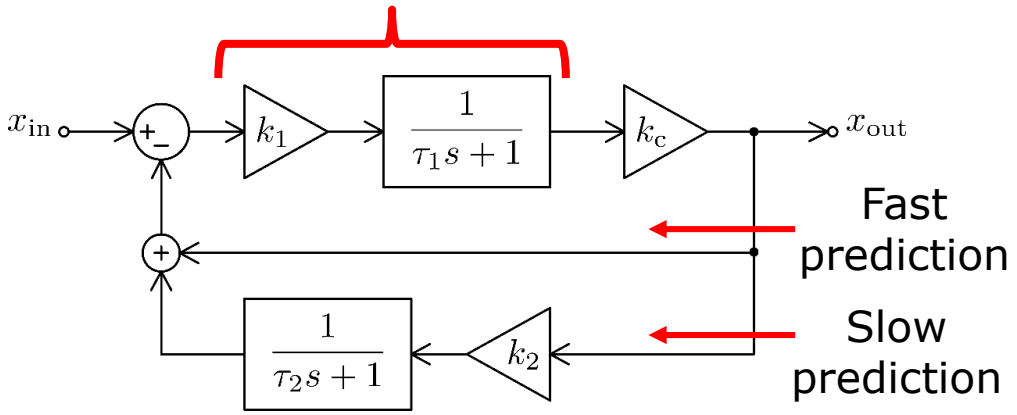
Sensor-in-the-loop Neuromorphic ΔΣ Modulation Architecture

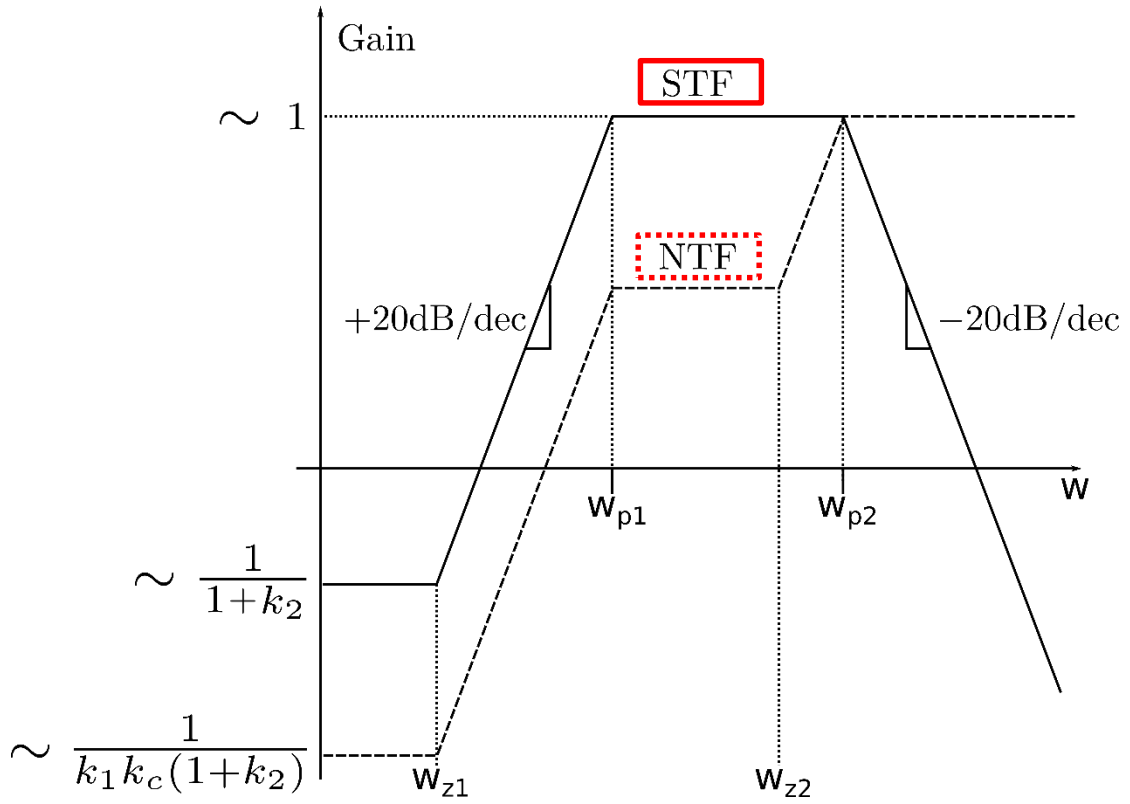
Linear model

- Sensor-in-the-loop architecture
- Dual-feedback scheme



$$\tau_1 = R_{ct}C_{dl}$$
$$k_1 = R_{ct}$$





- Band-pass response
- Stable for τ1 > τ2

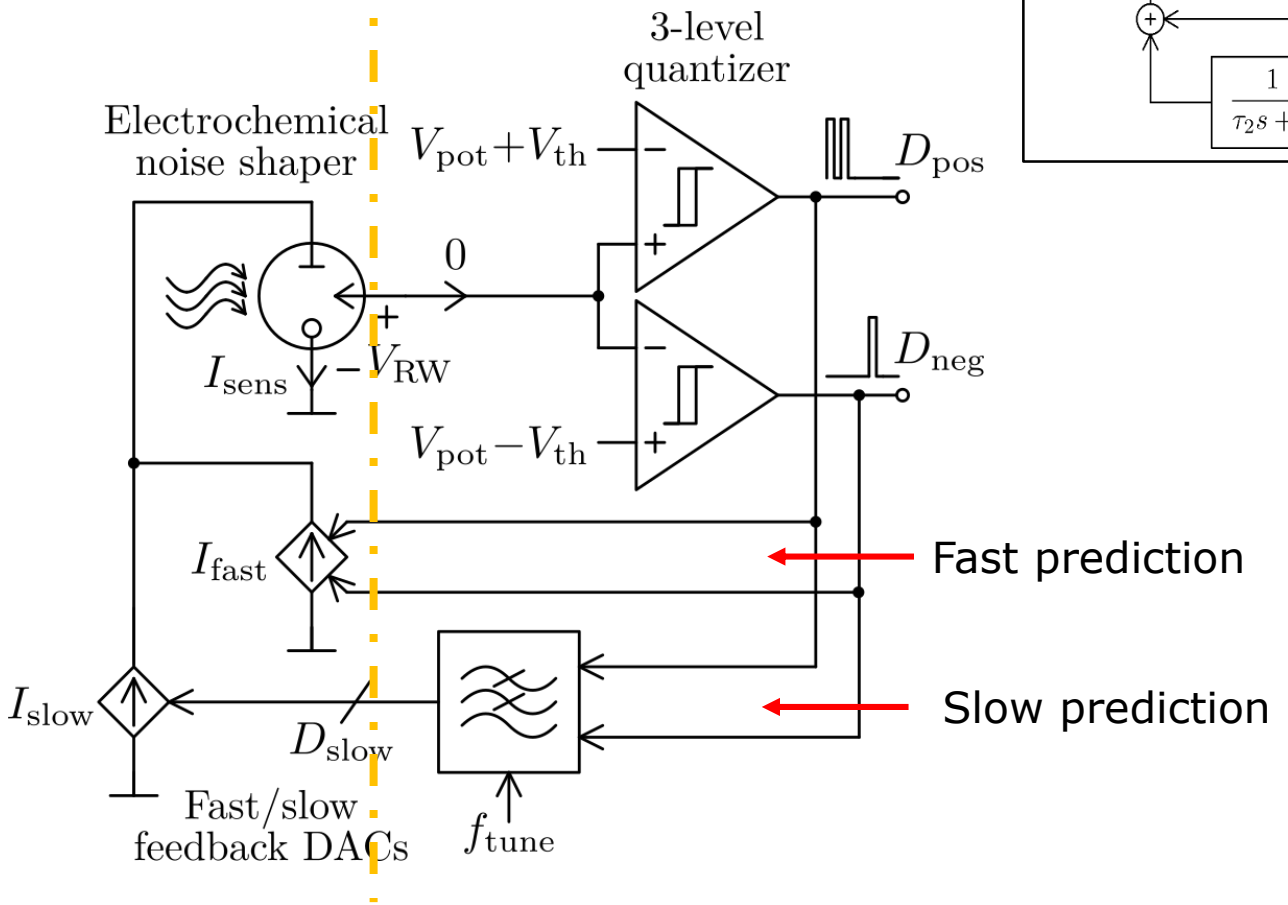
Sensor-in-the-loop Neuromorphic ΔΣ Modulation Architecture

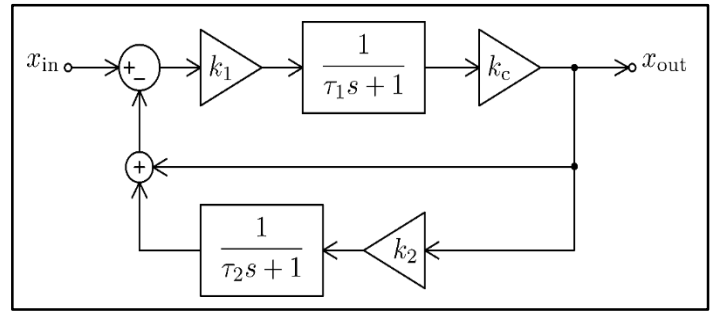
Electrical model

- 3-level quantization
- Tunable feedback low-pass filter
- Multi-bit slow feedback (Dslow)

Current domain

Voltage domain





Linear model

Asynchronous 3-level ΔΣ modulator circuits

CMOS circuits

Rail-to-rail folded cascode

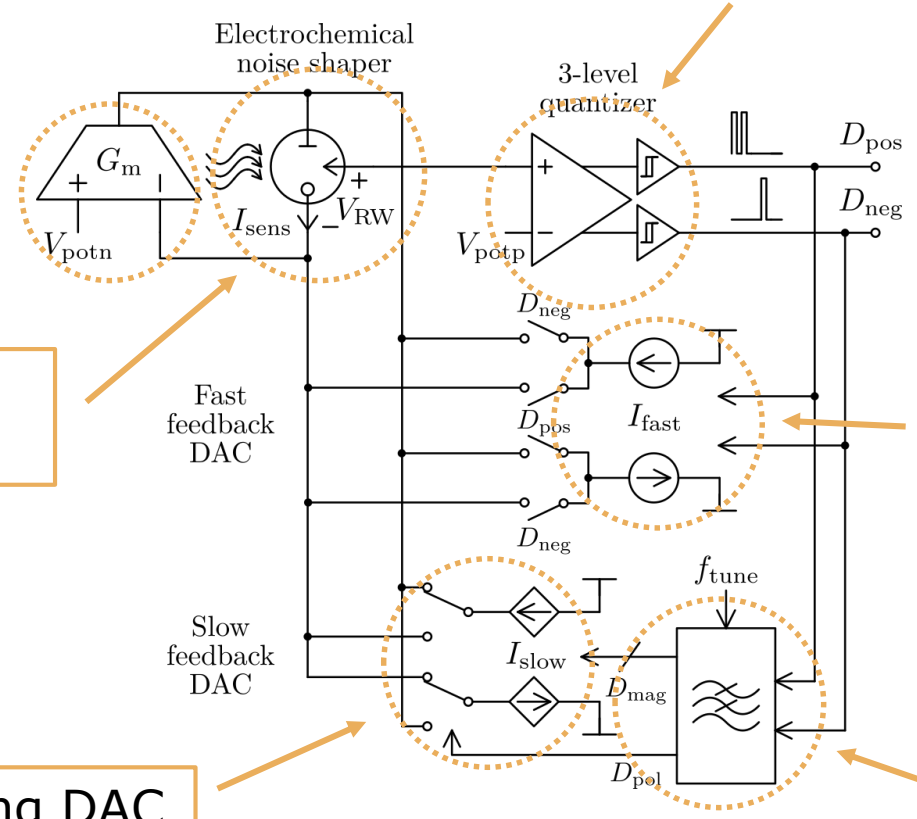
Differential hysteresis comparator

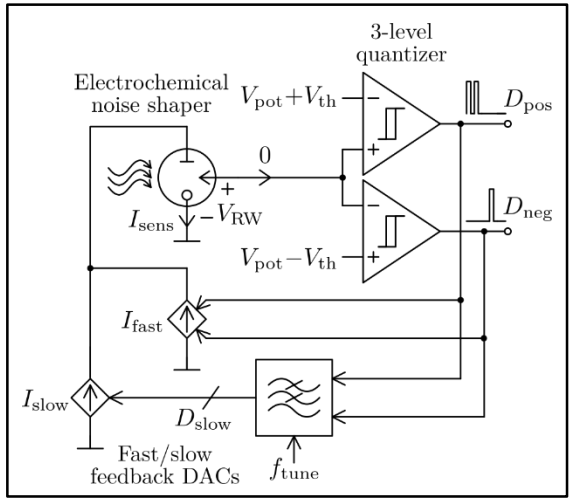
Differential potentiostat
(V_{RW} = Vpotp – Vpotn)

1-bit current DAC

N-bit current-steering DAC

N-bit digital low-pass filter

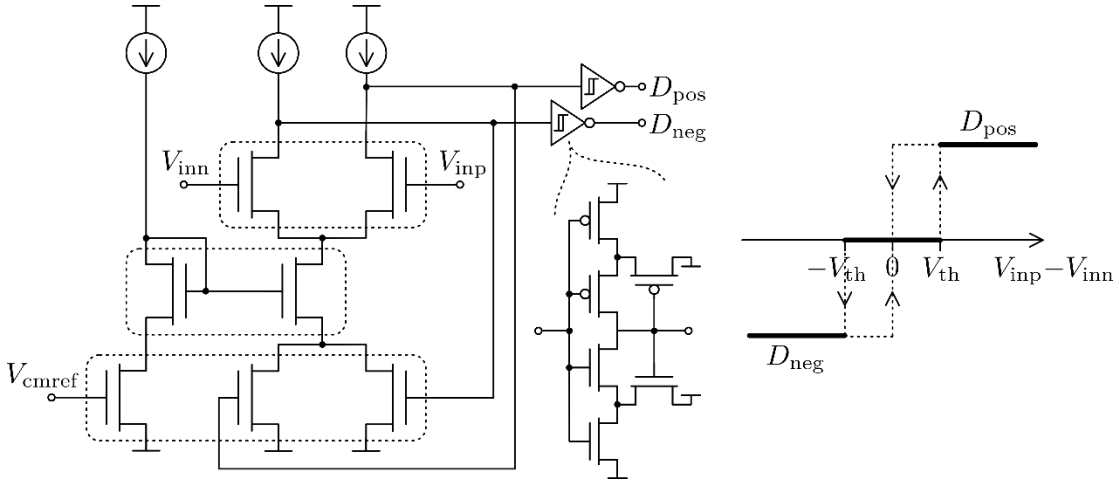




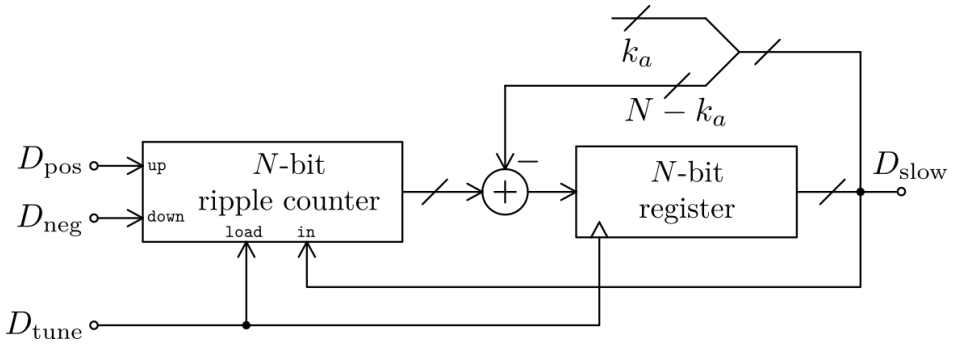
Electrical model

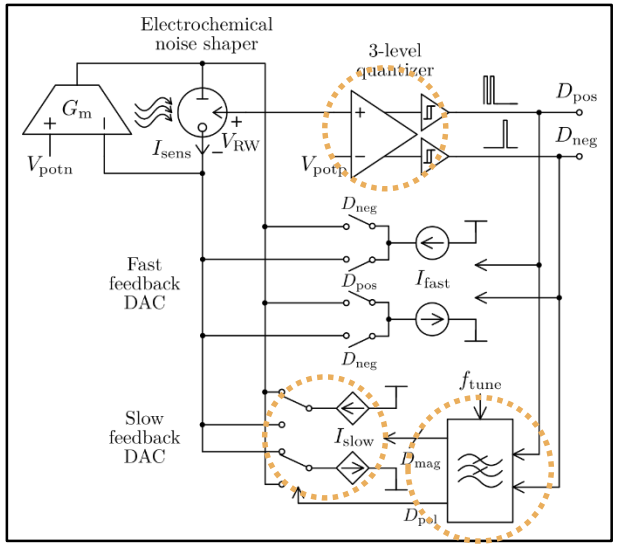
Asynchronous 3-level ΔΣ modulator circuits

Differential hysteresis comparator



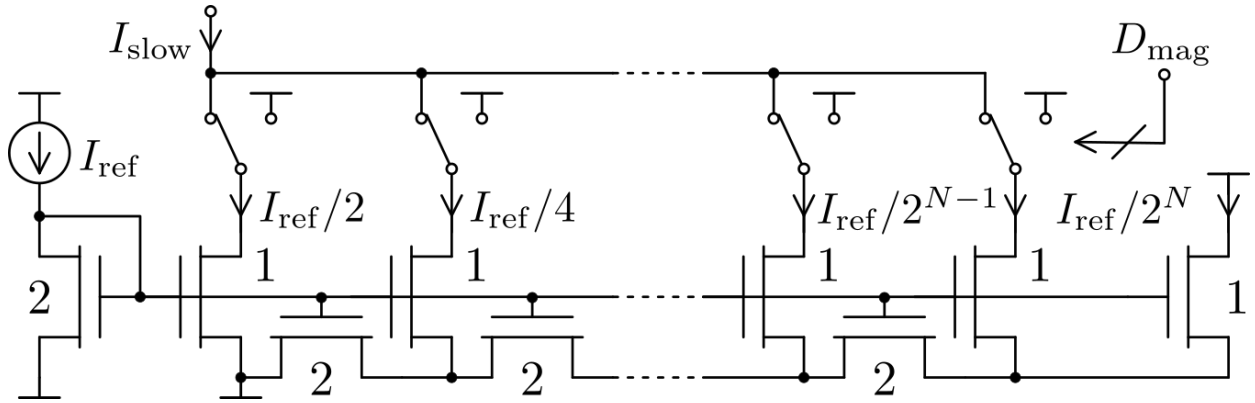
N-bit digital low-pass filter



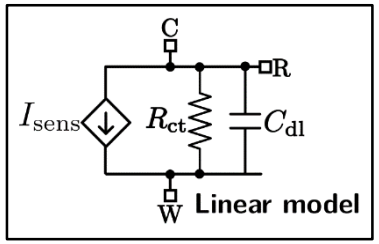


Circuit diagram

N-bit current-steering DAC

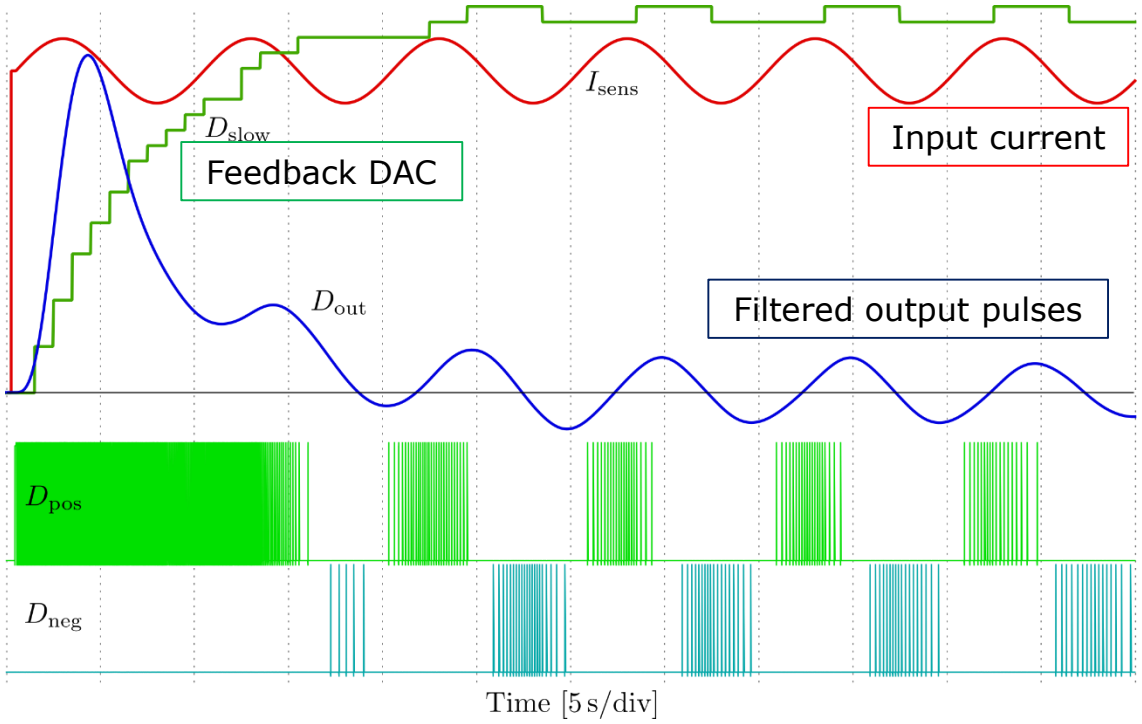


Simulation resuts in 65-nm CMOS technology



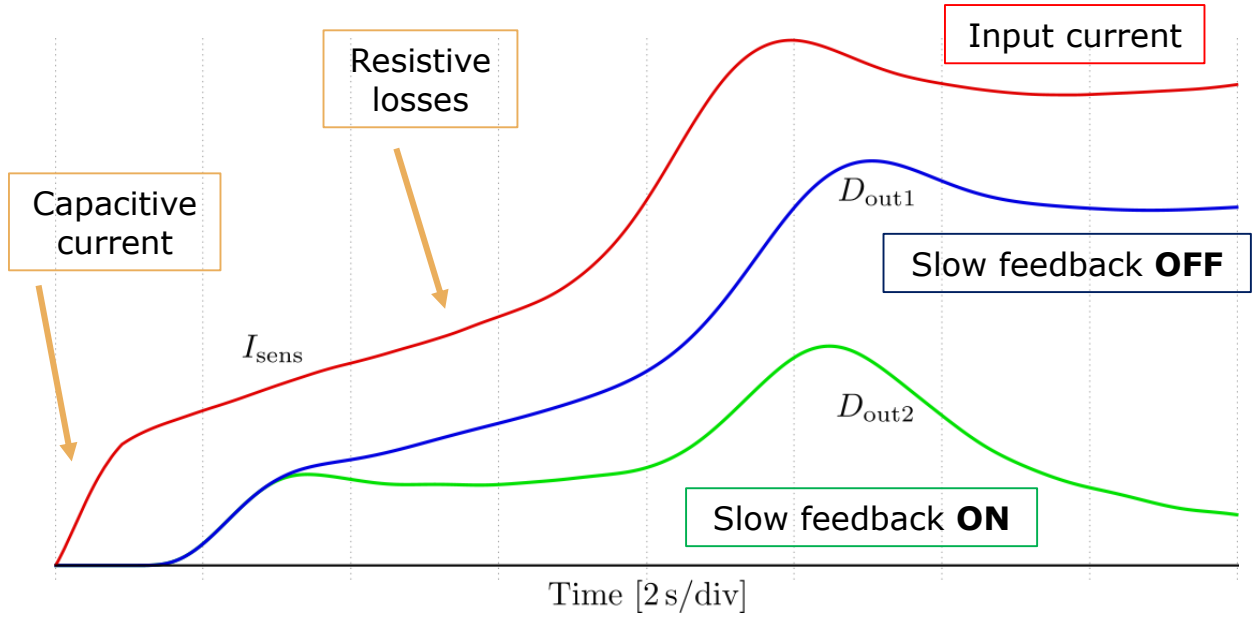
Sinusoidal input with offset

- Offset compensation
- Efficient data compression



Half voltammetry cycle

- Background current is compensation
- Dynamic range extended

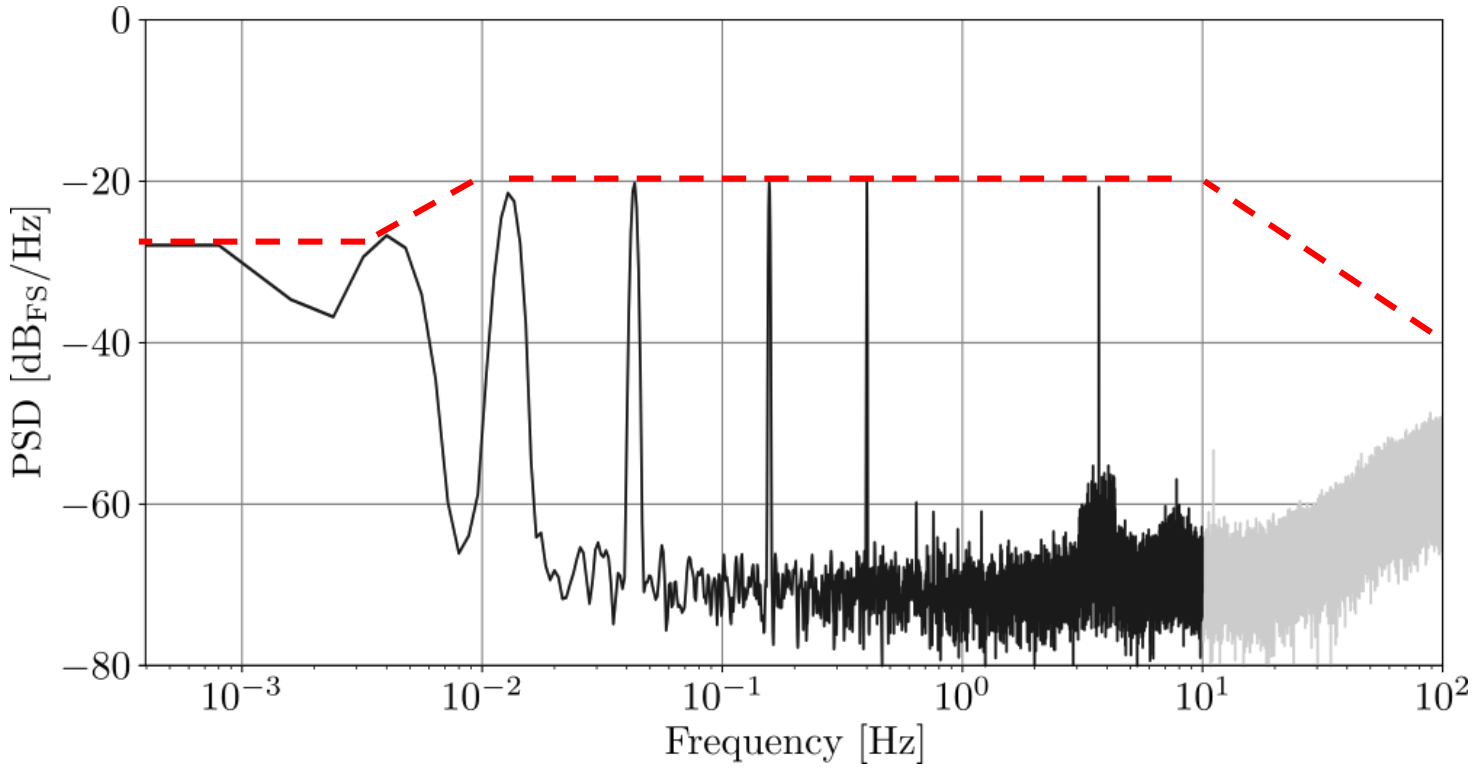


Simulation resuts in 65-nm CMOS technology

Power Spectral Density

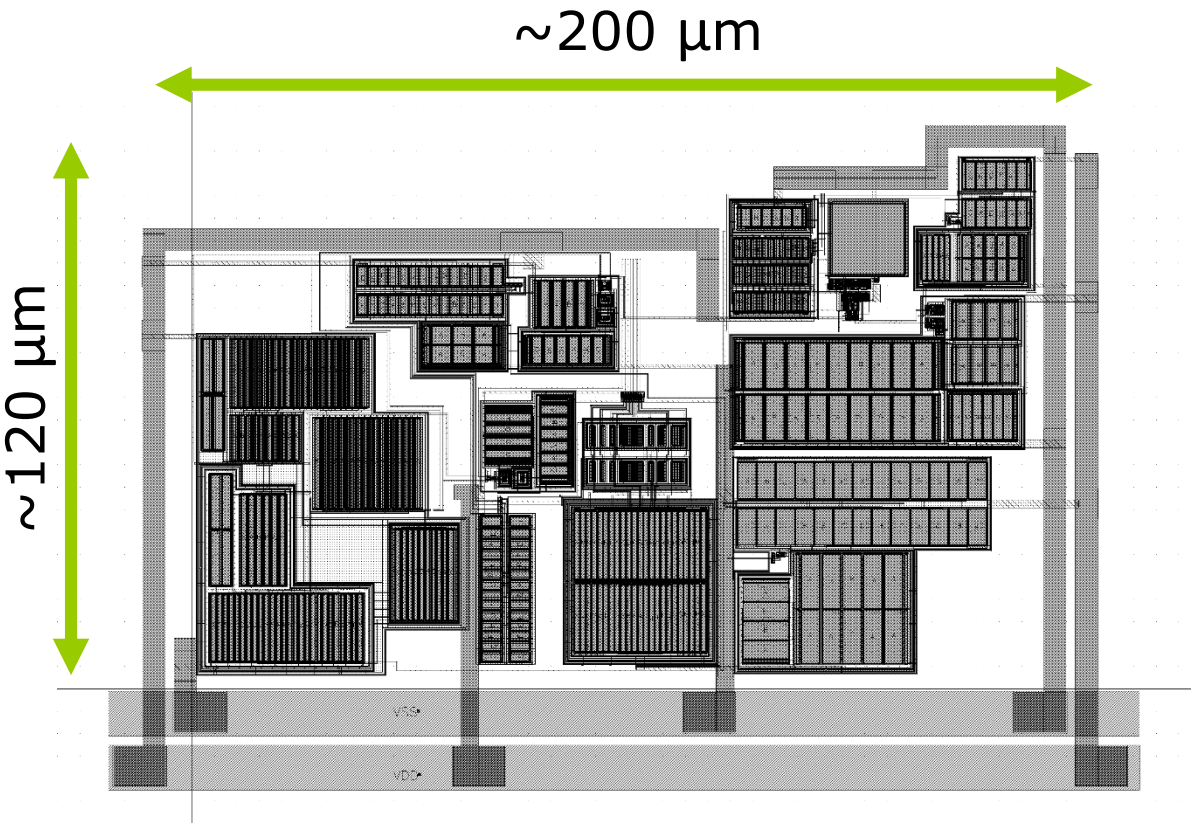
- 6-tone input + DC level
- Long simulation (> 1000s)

- Pass-band response
- Noise shaping



Conclusions

- Neuromorphic CMOS ΔΣ modulator:
  - Automatic **potentiostat regulation** of the desired potential (V_{RW})
  - **Asynchronous A/D conversion** of the signals from the sensor
  - **Configurable compression** of capacitive curents and sensor drifts
- So, what is **next**?
  - Electrical tests and characterization
  - Electrochemical experimentation
  - Think about future designs



...thank you for your attention!

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