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CAS

A 0.8mW 50kHz 94.6dB-SNDR Bootstrapping-free SC Delta-Sigma Modulator ADC with Flicker Noise Cancellation

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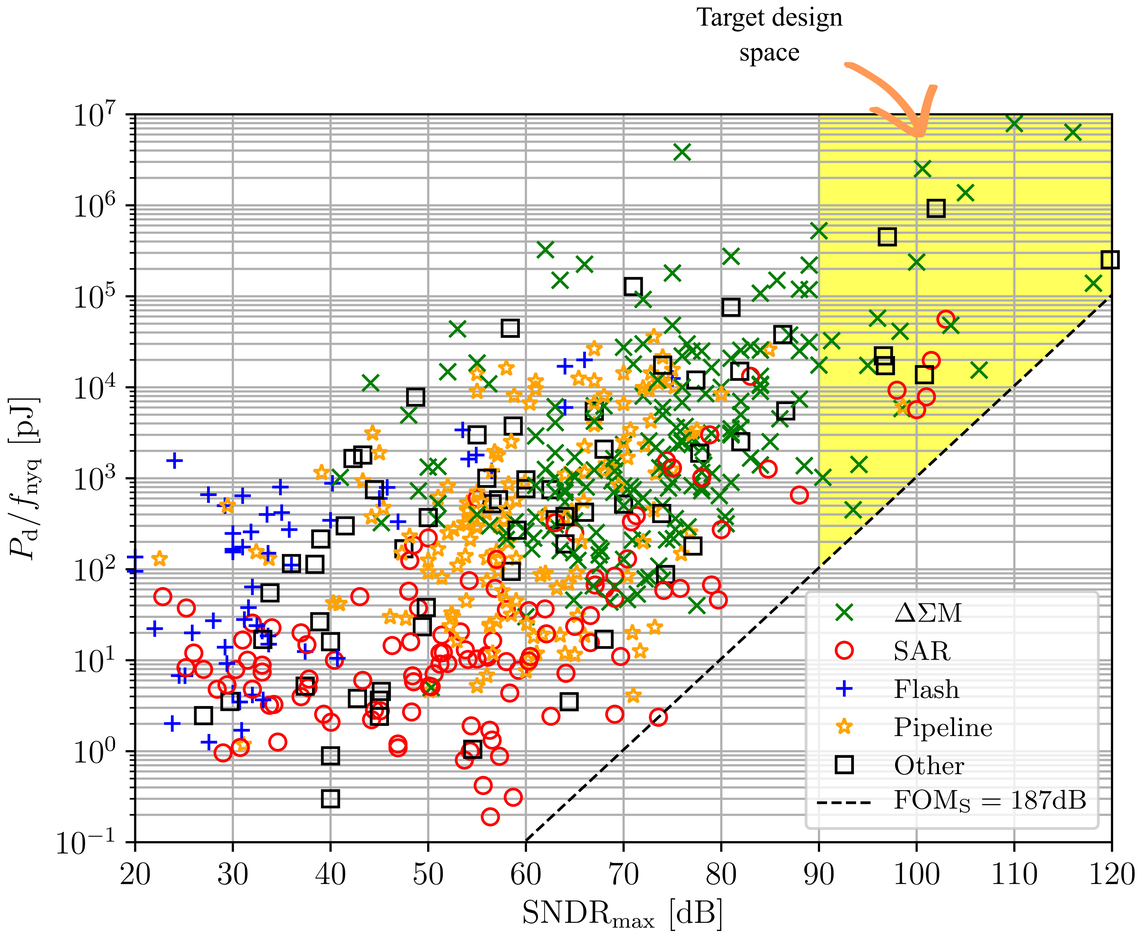
CSIC
Consejo Superior de Investigaciones Científicas

State-of-Art

- **Schreier FoM**:

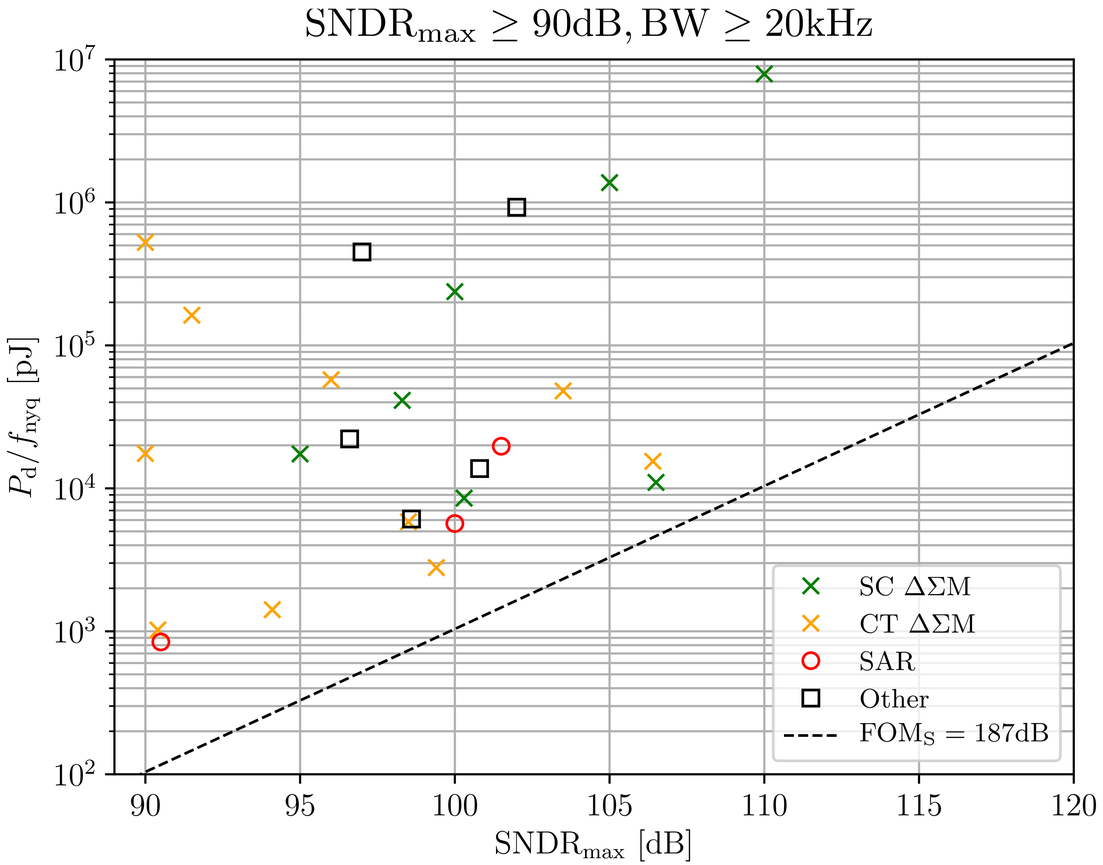
$$\mathrm{FOM_S} = \mathrm{SNDR_{max}} + 10\log\frac{f_{\mathrm{nyq}}}{2P_{\mathrm{d}}}\ [\mathrm{dB}]$$

- **Best FOMs achieved by:**
  - \+ SAR (moderate-high resolution)
  - \+ ΔΣM (high resolution)
- **High-resolution ADCs are scarce:**
  - \+ Increased complexity of CMOS design
  - \+ Most applications do not require so much resolution. Low-power consumption is preferable in many cases for multi-channelling purposes

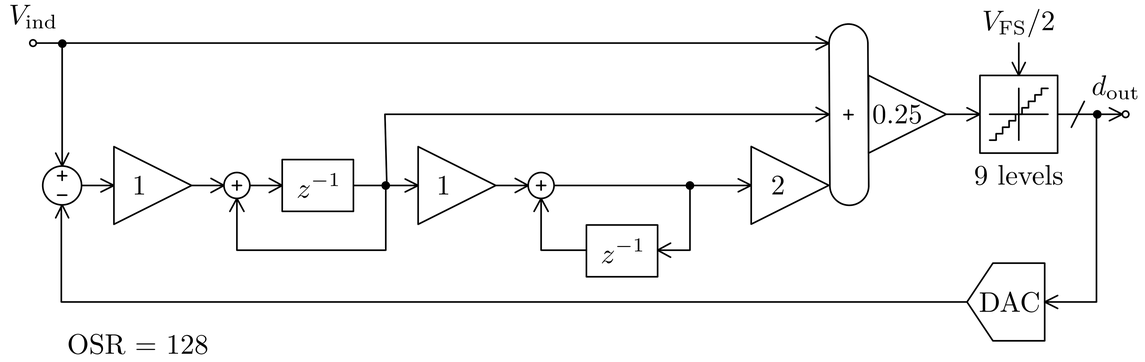


Target Design Space

- FOM not so fair for high-res. Designs must consider many things:
  - + Flicker noise, clock jitter, suppy coupling
  - + Switch non-linearity and charge injection
  - + OpAmp gain non-linearity
  - + Technology mismatching
- Also, FOM does not tell:
  - + PVT robustness
  - + Need for circuit calibration
  - + Internal supply bootstrapping
- Oversampled switched-capacitor (SC) ΔΣM preferred:
  - + No need for calibration
  - + Low sensitivity to CMOS technology compared to continuous-time (CT) ΔΣM



Low-Power Architecture



- **Second-order** loop filter
- **Feed-forward** path
- **9-level multi-bit** quantizer
- **Moderate oversampling ratio** (OSR = 128)
- **Quantizer input fullscale (FS) halved** to compensate passive adder attenuation

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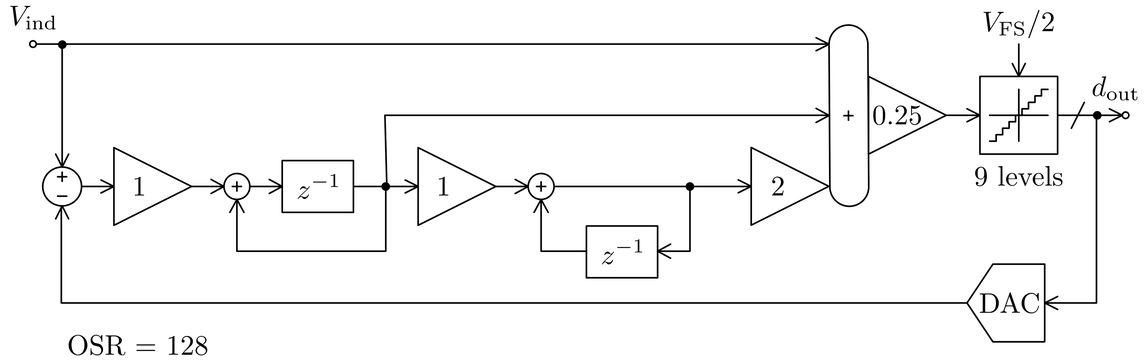

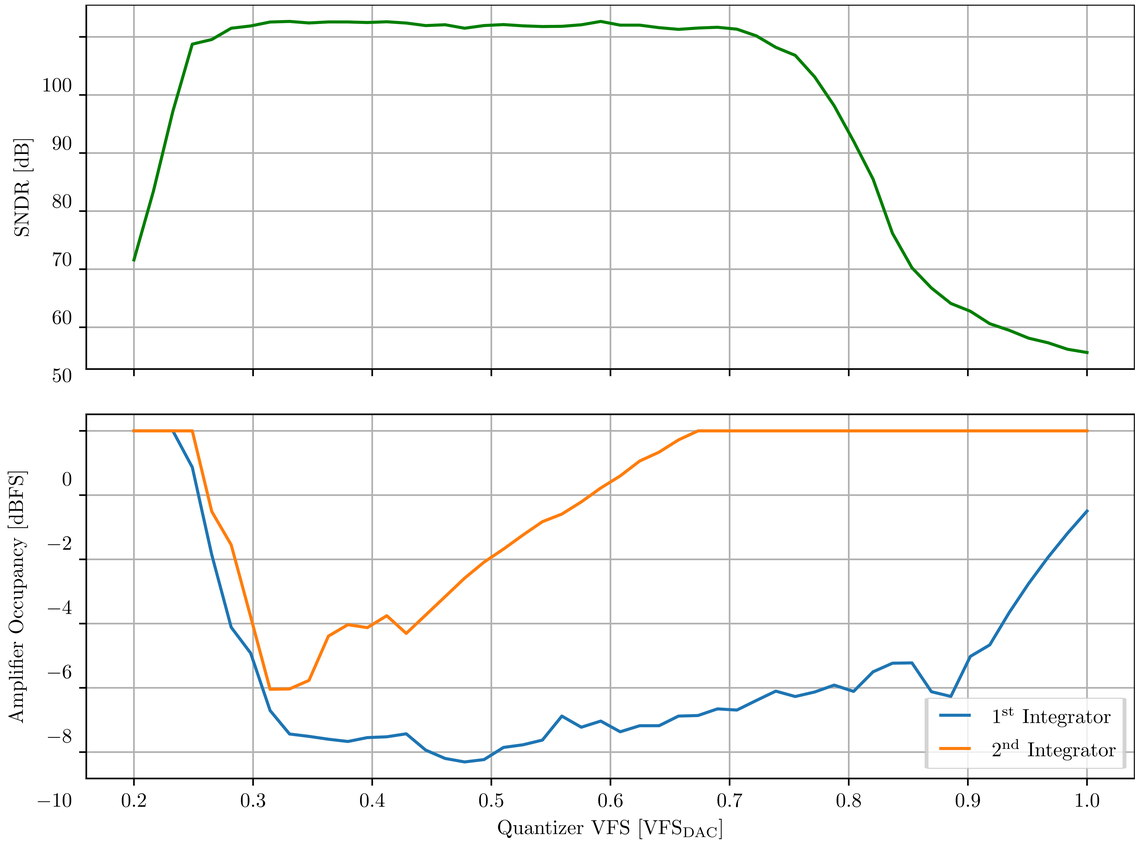

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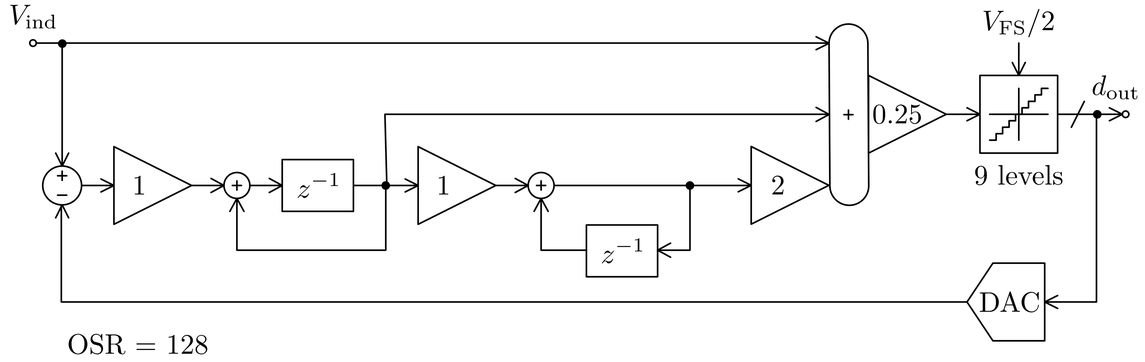
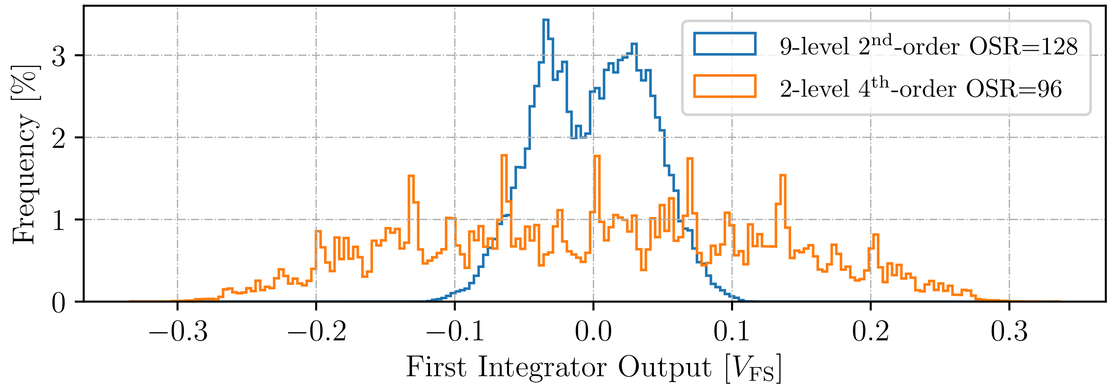
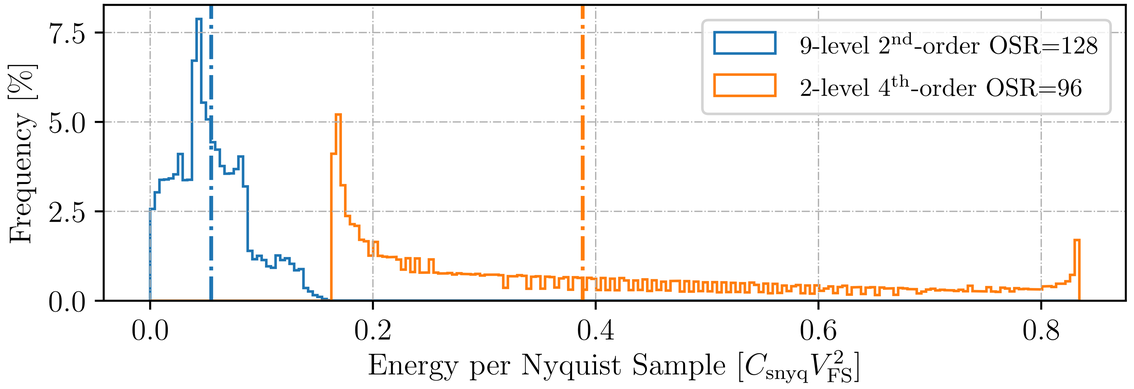


- This combination of multibit-quantization, low shaping-order and moderate oversampling **saves about 75% of the power associated with internal signal dynamics** compared with other implementations





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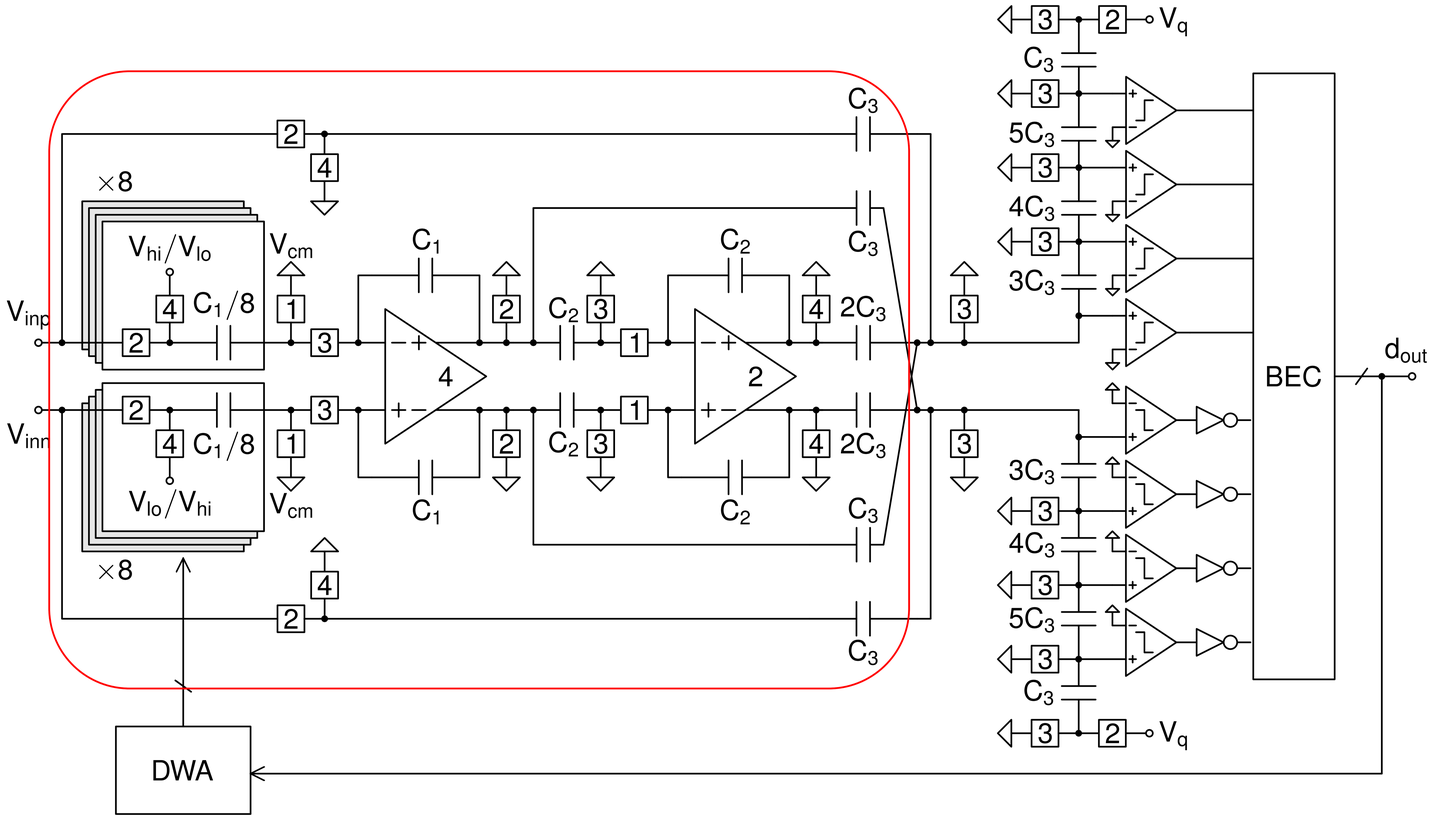

- **SC Integrators**
  - \+ Fully-differential switched OpAmp (SOA)
- **Resistor-less multi-bit quantizer**[1]
  - \+ Strong-ARM Comparator
- **Bubble error correction** (BEC)
- **Data-weighted averaging** (DWA) algorithm

[1] [11] J. Cisneros-Fernández, F. Serra-Graells, L. Terés, and M. Dei, "A Compact Switched-Capacitor Multi-Bit Quantizer for Low-Power High-Resolution Delta-Sigma ADCs"

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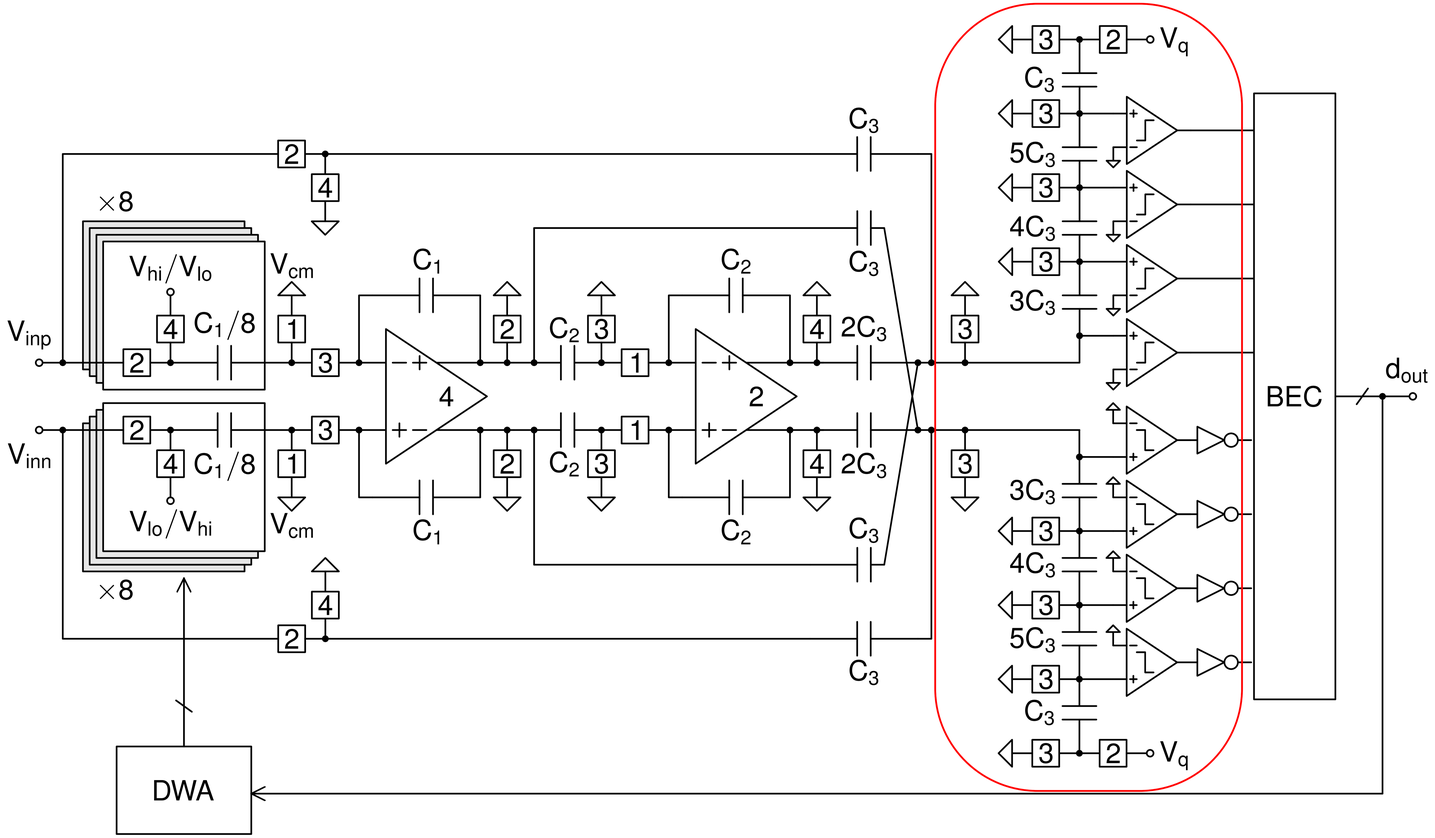

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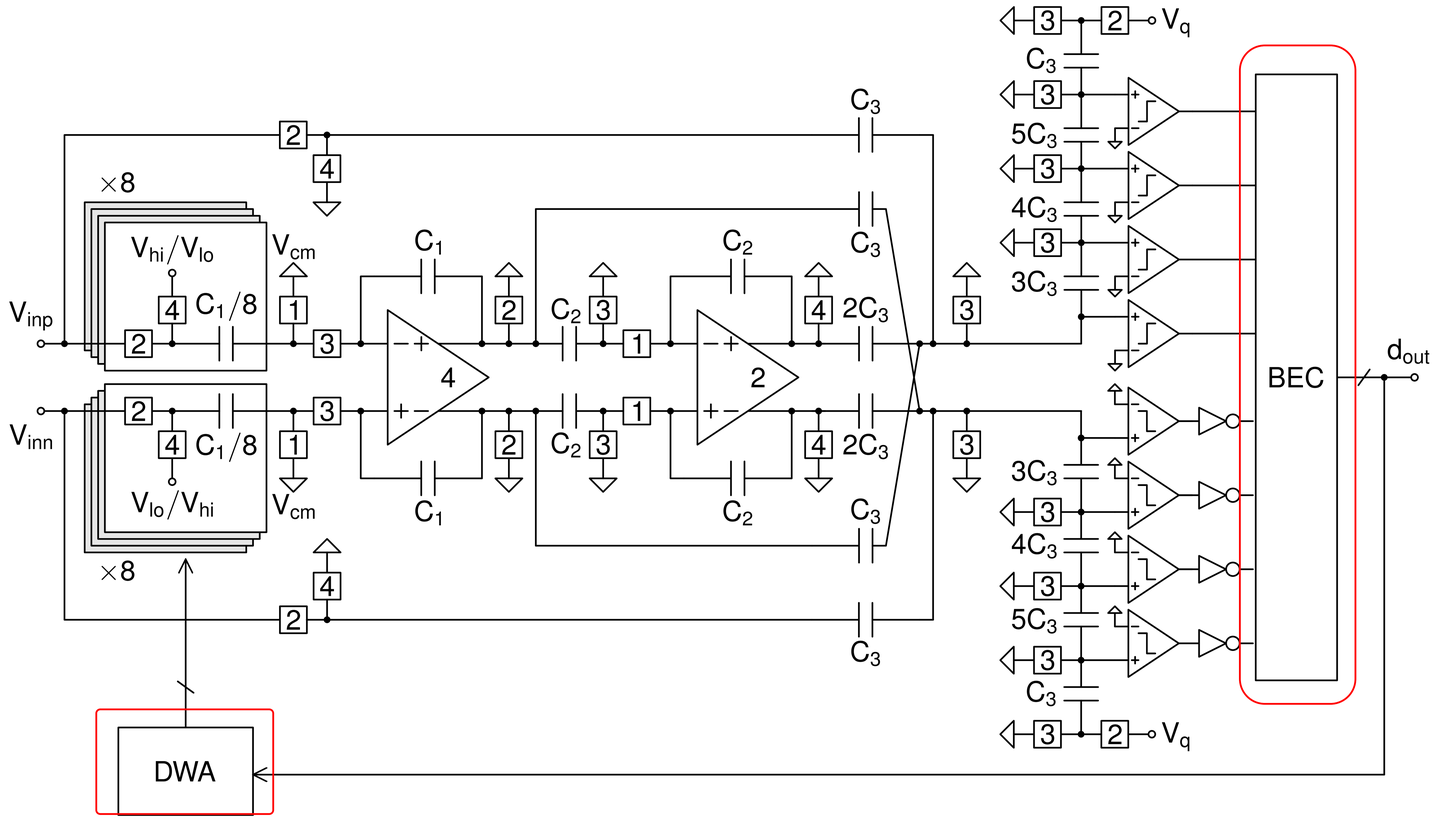

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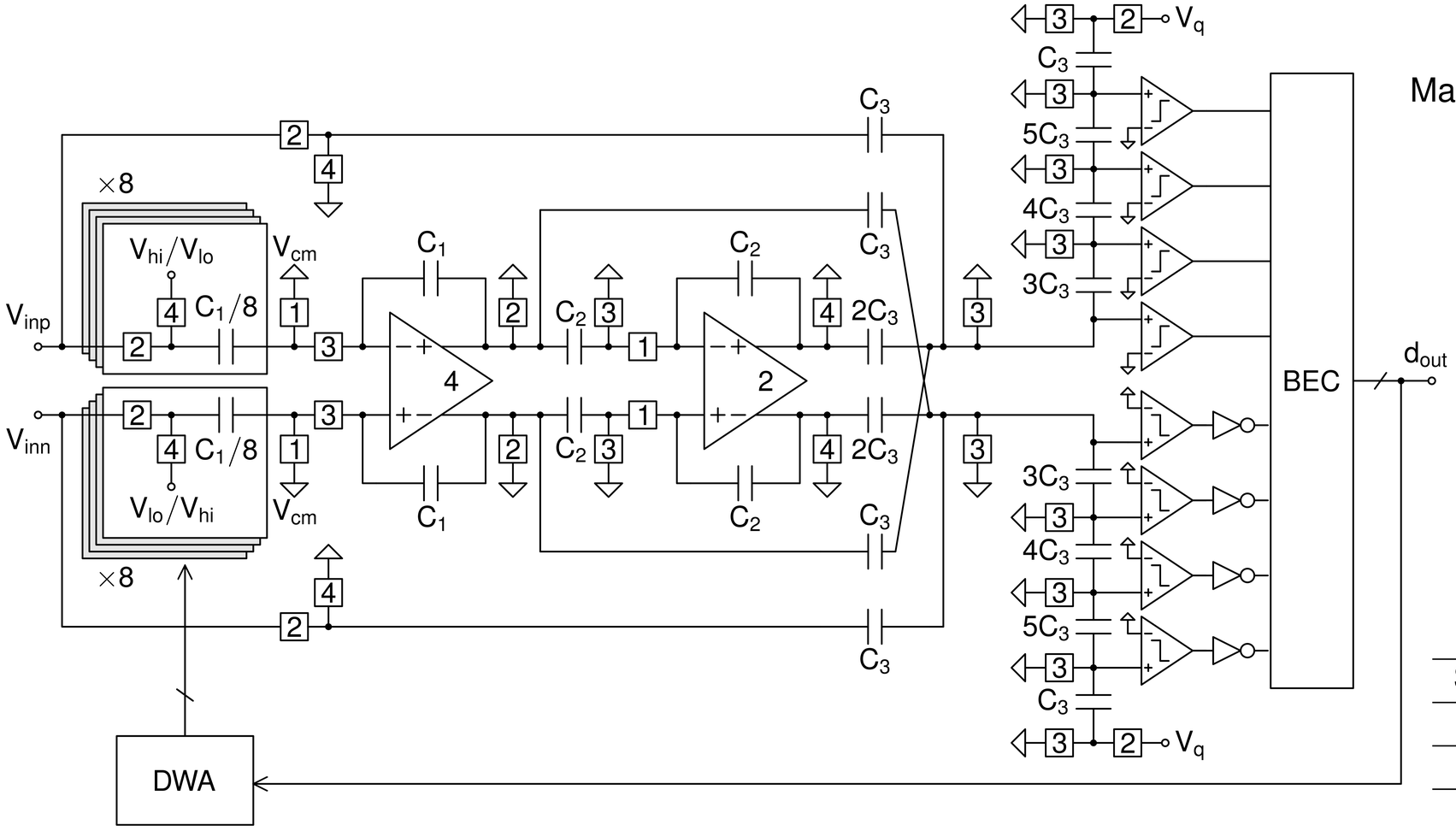
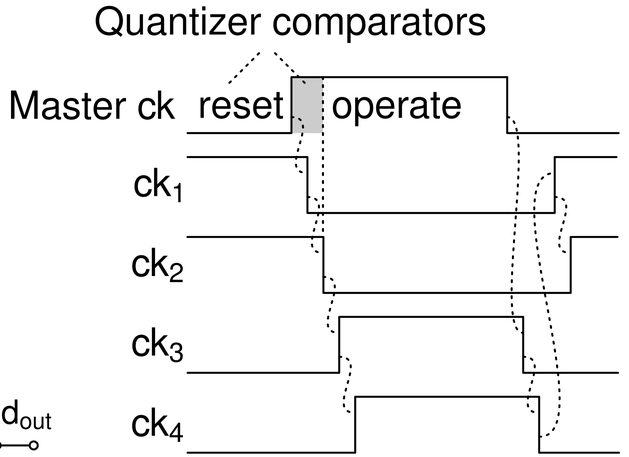




C_1	8 pF
C_2	2 pF
C_3	0.5 pF

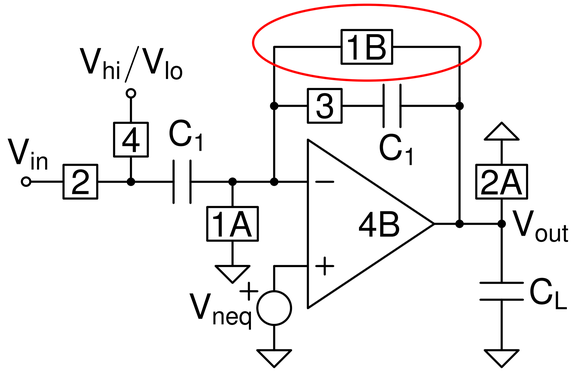
V_{cm}	0.9 V
V_{hi}	1.4 V
V_{lo}	0.4 V
V_q	0.65 V

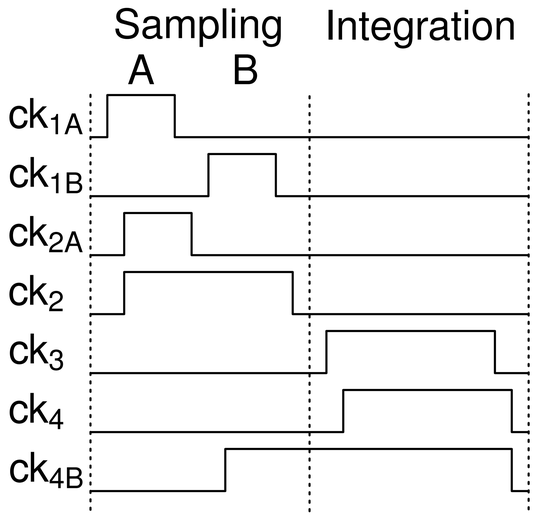
	-55°C	27°C	125°C
Slow	94.9	95.1	93.1
Typ.	96.2	96.5	93.2
Fast	94.8	92.4	93.6

$SNDR_{max}$ [dB]

Flicker-Noise Cancellation

- **Minimalist topology modification** (feedback switch)
- **Increased clock complexity**
- 3-phase CDS based operation:
  - Slewing phase
  - Noise sampling phase
  - Integration phase
- Shapping function obtained for OpAmp noise:
  - $V_{\mathrm{out}} = V_{\mathrm{in}} + (V_{\mathrm{neq}}[n] - V_{\mathrm{neq}}[n-1/2])$
- **Low-frequency noise** is virtually **removed**
- **OpAmp white-noise power will double** due to aliasing (CDS distance is half a period)





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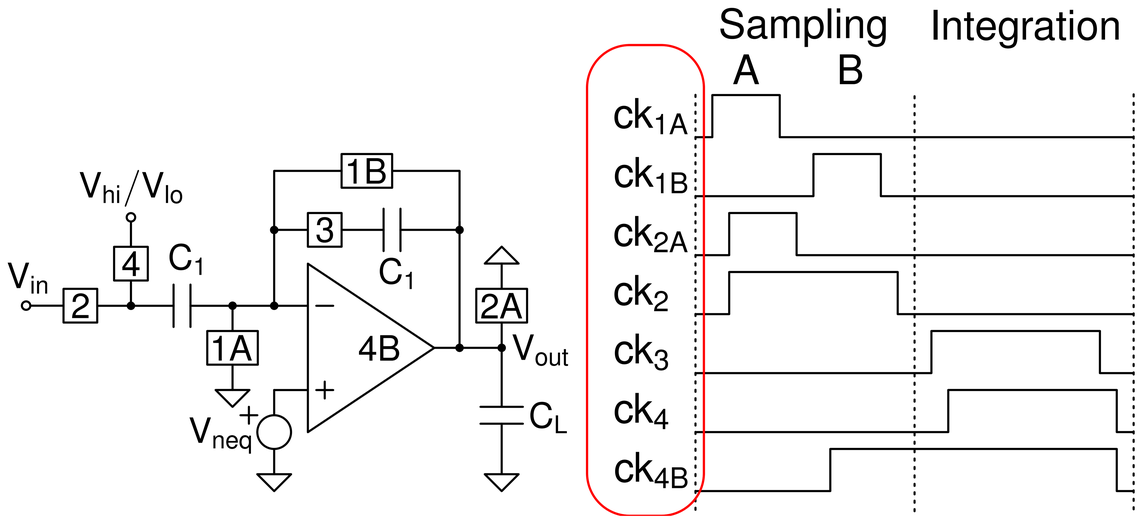

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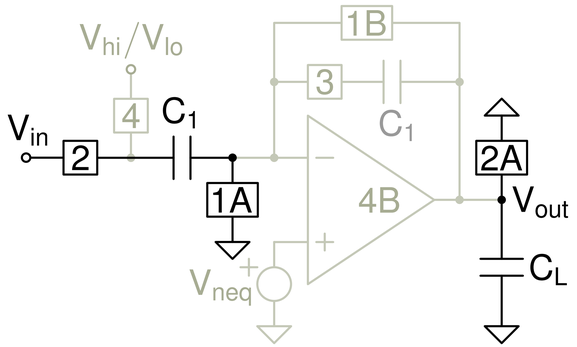

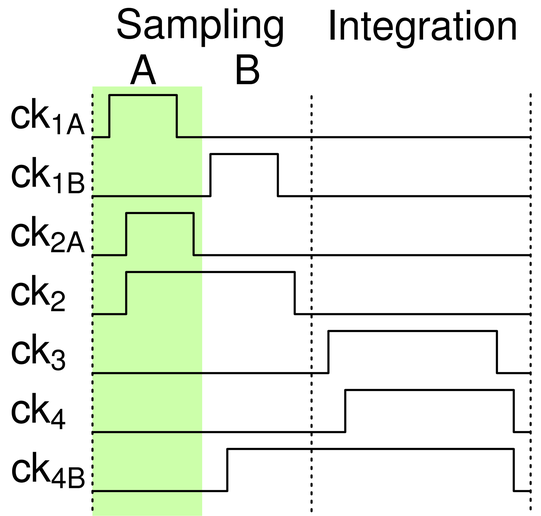

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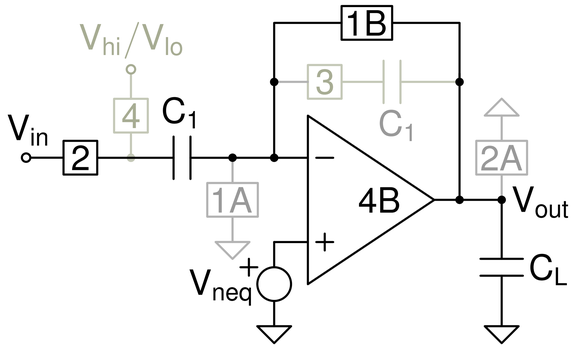

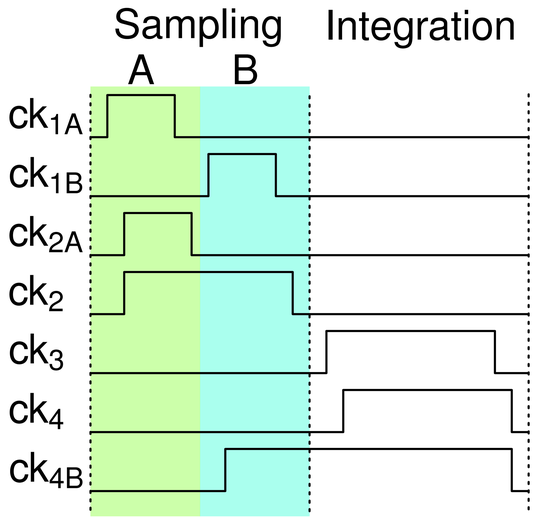

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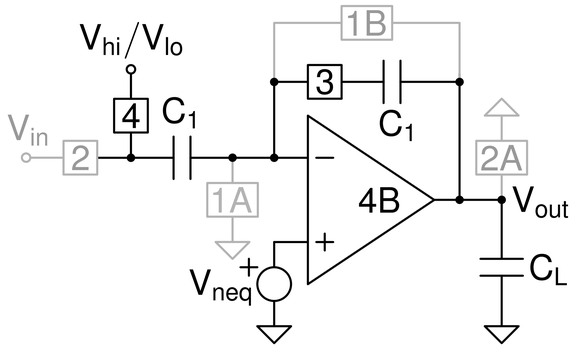
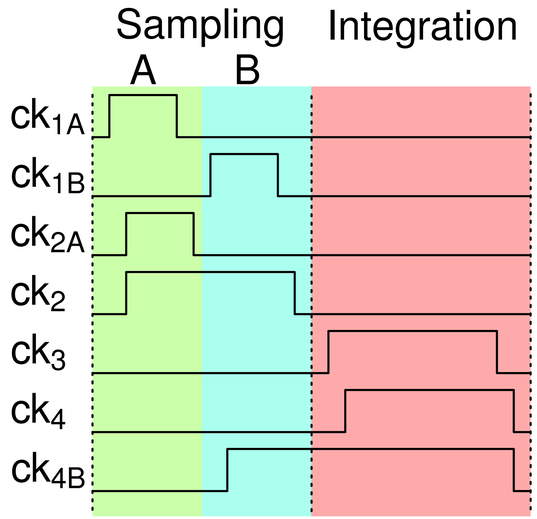


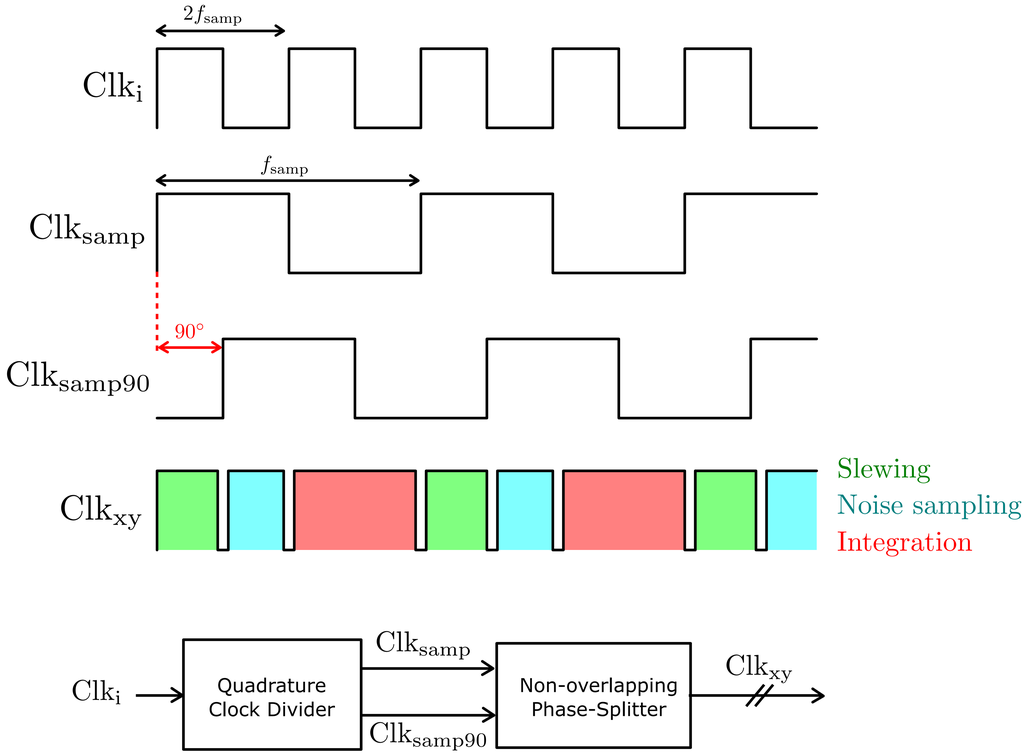


Clock Generation

- Sub-sampling phases time allocation:
  - ▼ A short slewing phase might prove insufficient to accurately sample the input. Also, it increases amplifier duty-cycle.
  - ▼ A short noise sampling phase might not allow amplifier start-up and also capture the switching glitches.
  - ▲ A **good trade-off is using 50% duty-cycle** for each one
- For a robust and simple clock generation

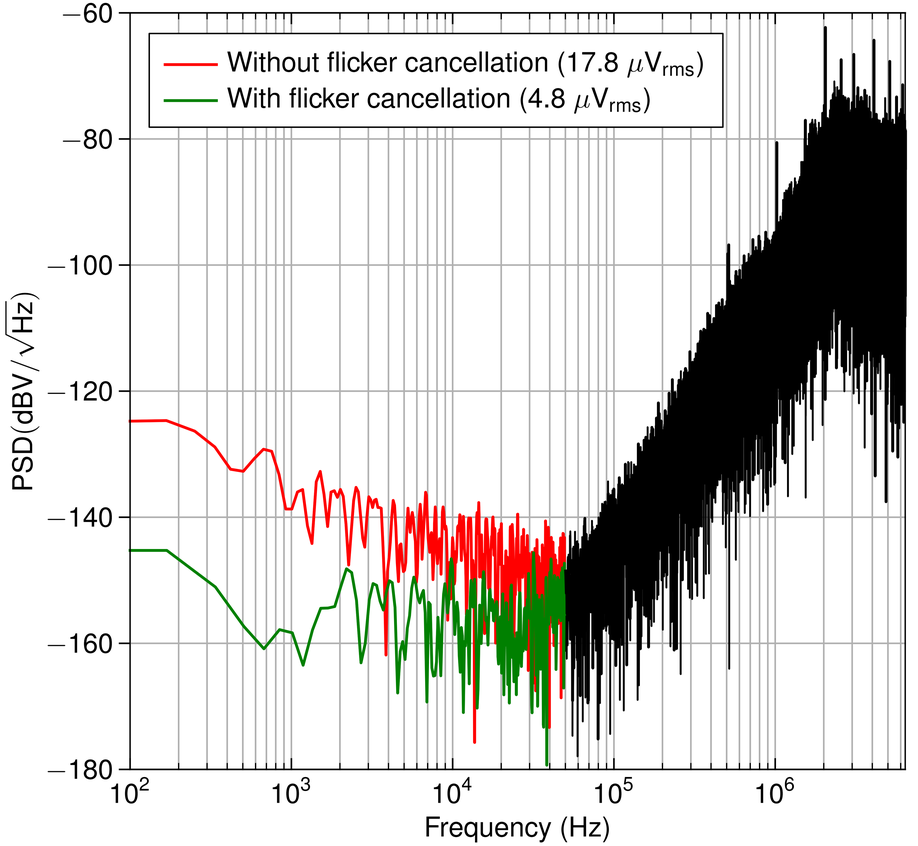
$$f_{\mathrm{clki}} = 2f_{\mathrm{samp}}$$

- Clock pairs [1,2] and [3,4] are in phase but delayed to **mitigate non-linear charge injection**. Unrelated to flicker-noise cancellation



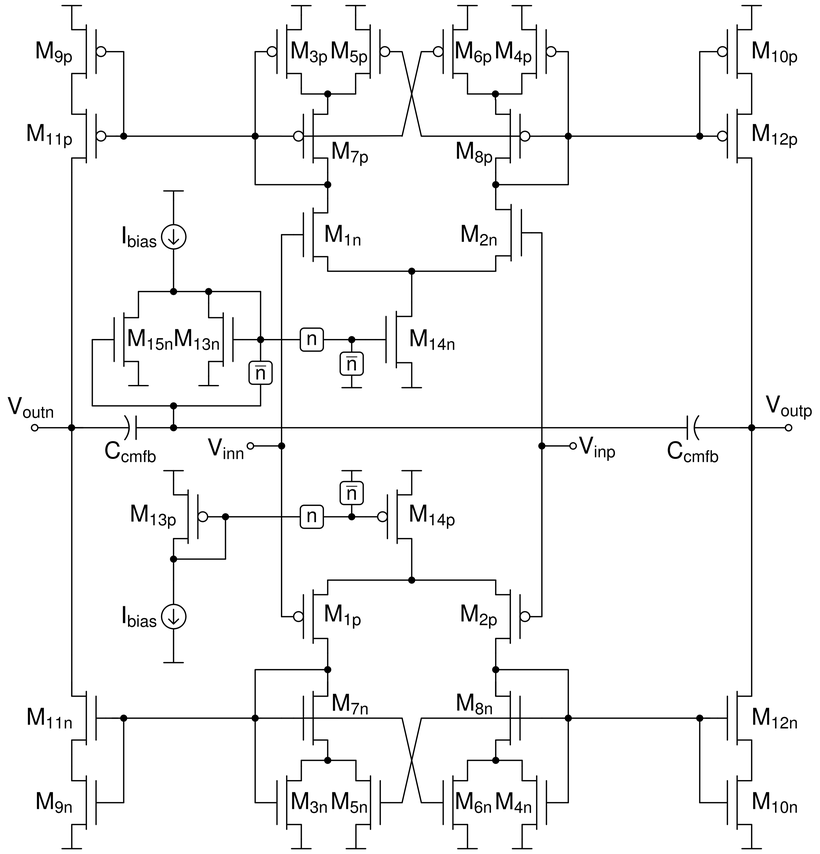
Flicker-Noise Simulation results

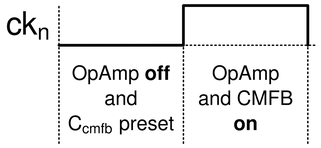
- ▲ **SNR improvement around 12 dB**
- ▼ **Power consumption** of 1st integrator **increased by 50%**
- ▲ $\mathrm{FOM_S}$ net improvement of 10 dB (even assuming total power is from 1st stage)



- Fully-differential Class-AB topology[2]:
  - High output dynamic currents ($I_{max} = k_{AB} I_{bias}$)
  - High PSRR, CMRR
  - Low PVT sensitivity
  - No compensation required
- Switched-OpAmp Operation fully compatible with SC CMFB
- Design trade-off around k_{AB}. Increasing k_{AB} results in:
  - Reduction of static power
  - Parasitic pole at lower frequency. Stability worsened

$$k_{AB} = 1 + \frac{B}{2C}, A = B + C$$





$(W/L)_{1n\text{-}2n}$	4×4/0.2
$(W/L)_{1p\text{-}2p}$	4×5/0.2
$(W/L)_{3n\text{-}4n}$	1×0.8/0.2
$(W/L)_{5n\text{-}6n}$	7×0.8/0.2
$(W/L)_{7n\text{-}12n}$	8×0.8/0.2
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$(W/L)_{13n}$	1×0.5/0.24
$(W/L)_{14n}$	8×0.5/0.24
$(W/L)_{15n}$	3×0.5/0.24
$(W/L)_{13p}$	2×4/0.48
$(W/L)_{14p}$	4×4/0.48
C_{cmfb}	0.4 pF
I_{bias}	30 μA

[2] [13] S. Sutula, M. Dei, L. Terés, and F. Serra-Graells, "Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single-Stage OTAs for Low-Power SC Circuits"

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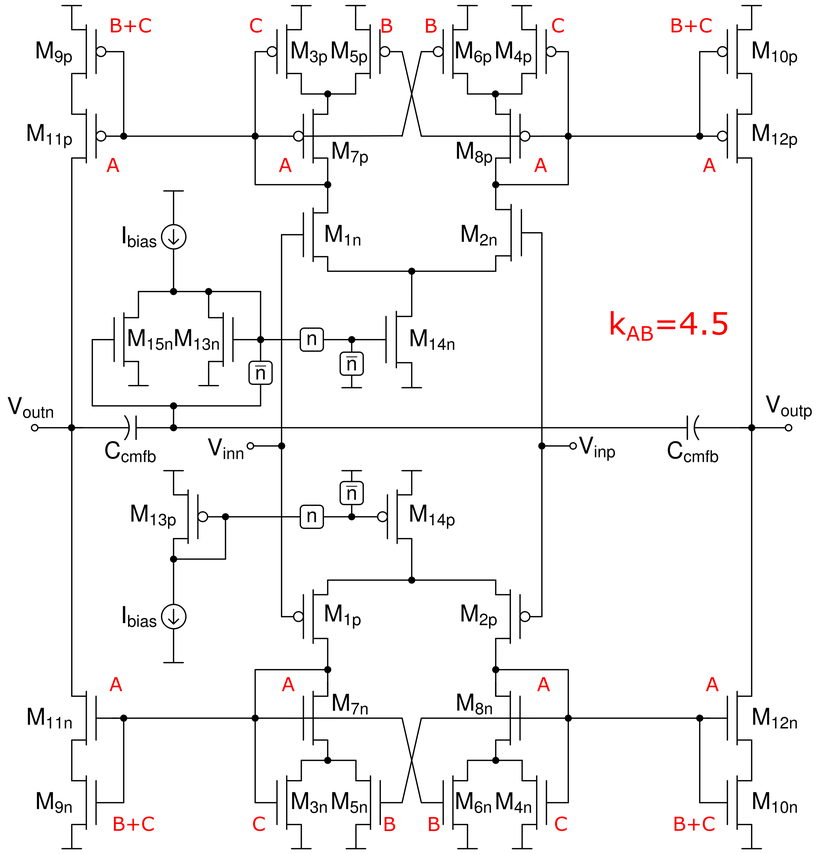

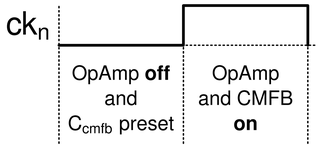

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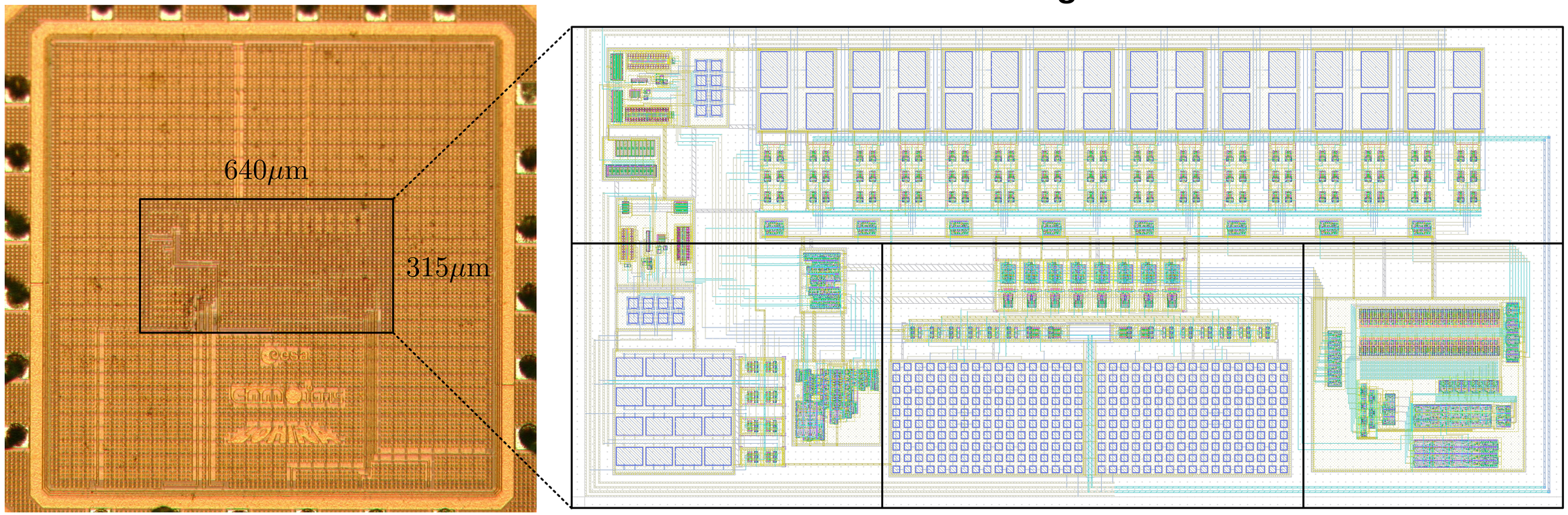
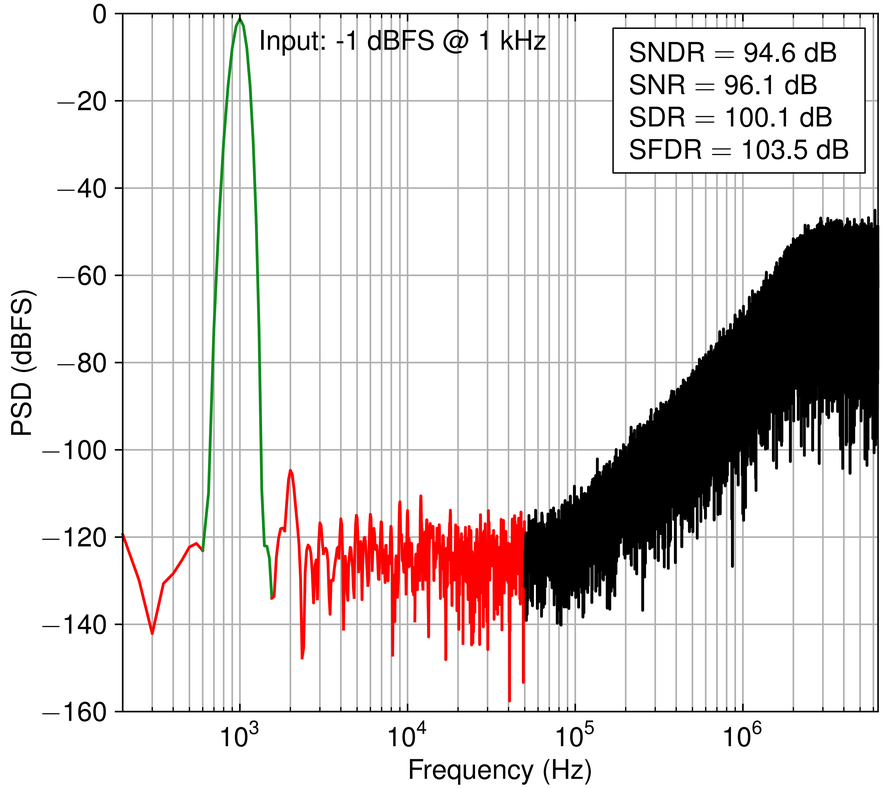
Chip Photo

+ 1.8V 0.18µm 6-metal CMOS technology



Measured Performance



- $\text{SNDR}_{\text{max}} = 94.6$ dB @ -1 dBFS, 1 kHz
- High spectral purity (SFDR = 103.5 dB)

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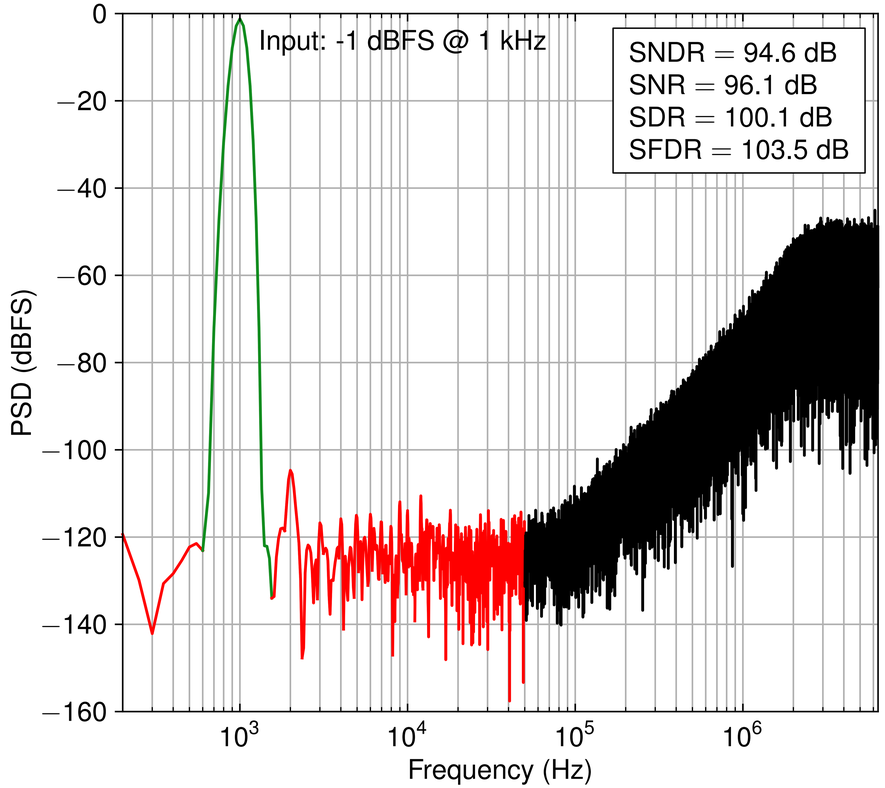

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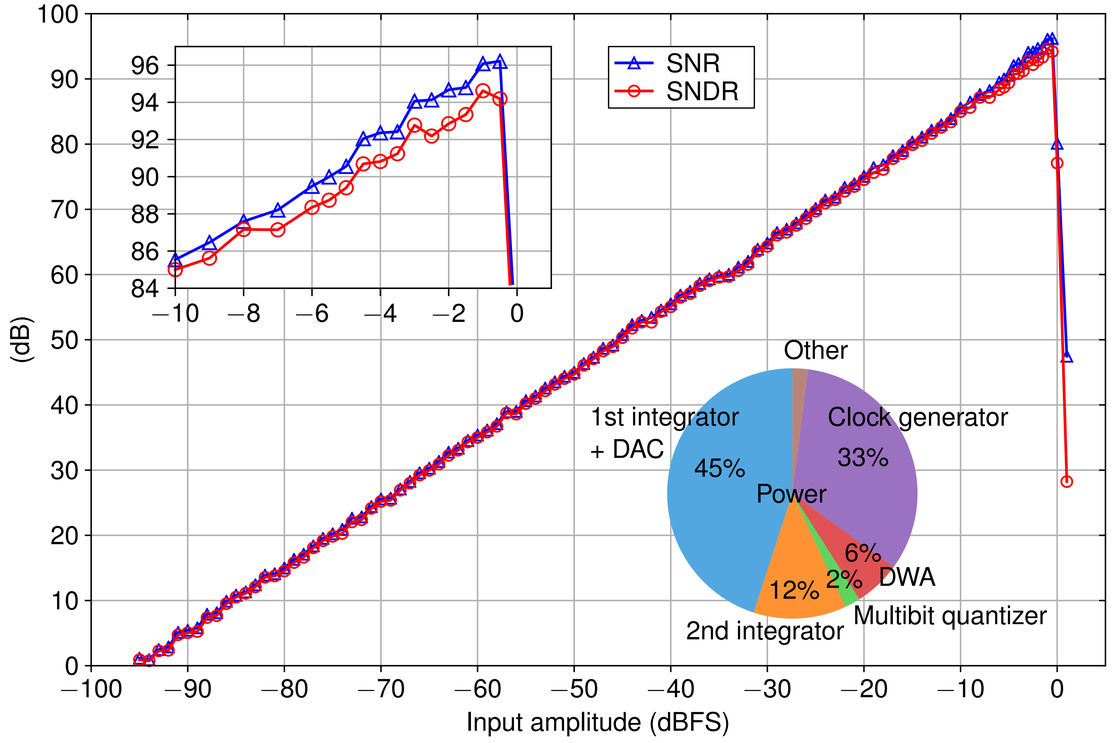
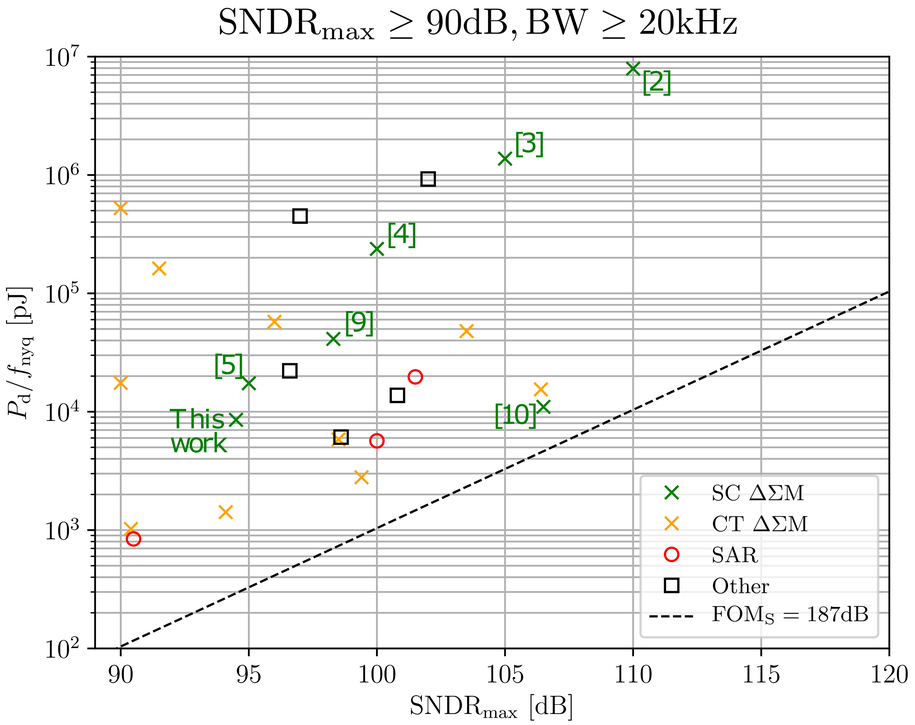


- Main power consumption from 1st integrator
- Clock generation also power hungry (driving buffers mainly)

Measured Performance

	[2]	[3]	[4]	[5]	[9]	[10]	This work	
Architecture	Loop	Loop	MASH	Loop	Zoom	Zoom	Loop	
shaping order	7^{th}	5^{th}	4^{th}	2^{nd}	3^{rd}	3^{rd}	2^{nd}	
quantization	3-level	17-level	multi-bit	18-level	2-level	4-level	9-level	
Technology	800	350	250	180	160	160	180	nm
Supply voltage	5	5		0.7	1.8	1.8	1.8	V
Diff. full scale	4		6.6		3.5		2	V_{pp}
Sampling rate	6.14	5.12	20	5	11.29	3.5	12.8	MS/s
Bandwidth	48	20	1000	25	20	20	50	kHz
Supply power	760	55	475	0.87	1.65	0.44	0.80	mW
Area	25	5.6	20.2	2.16	0.16	0.27	0.20	mm^2
$SNDR_{max}$	110	105	103*	95	98.3	106.5	94.6	dB
FOM_S	158.0	160.6	166.2*	169.6	169.1	183.1	172.6	dB
Bootstrap-free	Yes	Yes	Yes	No	No		Yes	
Resistor-less	Yes	Yes	Yes	Yes	Yes	No	Yes	



- Resistor-less implementation
- Bootstrapping-free
- Competitive $FOM_S = 172.6$ dB

Conclusions

- 9-level second-order single-loop SC ΔΣM ADC
- Features implementation of SC flash multi-bit quantizer
- Features implementation of variable-mirror Class-AB SOAs
- Proposed CDS-based flicker-cancellation mechanism
- Measured high-resolution (94.6 dB) and low-power (0.8 mW) experimentally
- Competitive 172.6 dB FOM_S obtained

Thanks for your attention!

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