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A 16bit 50kHz 177dB-FOMS Calibration-Free Bootstrapping-Free SC Delta-Sigma Modulator IP Block for Low-Power High-Resolution ADCs

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Next Generation of IoT Sensors

IEEE International Road map for Devices and Systems (IRDS)
More Than Moore White Paper, 2020 Edition
`https://irds.ieee.org/editions/2020`

- **18 billion** IoT devices are forecast by 2022!
- **Key markets** such as wearable point of care, food quality control, autonomous driving, environmental monitoring...
- To be **miniaturized**, **low cost** (even disposable), **autonomous** (non supervised) and **long lifetime** (energy efficient)
- Ubiquitous smart sensors will require **edge computing** capabilities:
  - + Local data processing to optimize **output bandwidth** in wireless communications

e.g. remote surveillance

  - + Local close-loop operation for **low-latency** response

e.g. epilepsy seizure alarm

Open Hardware for IoT Sensory Applications

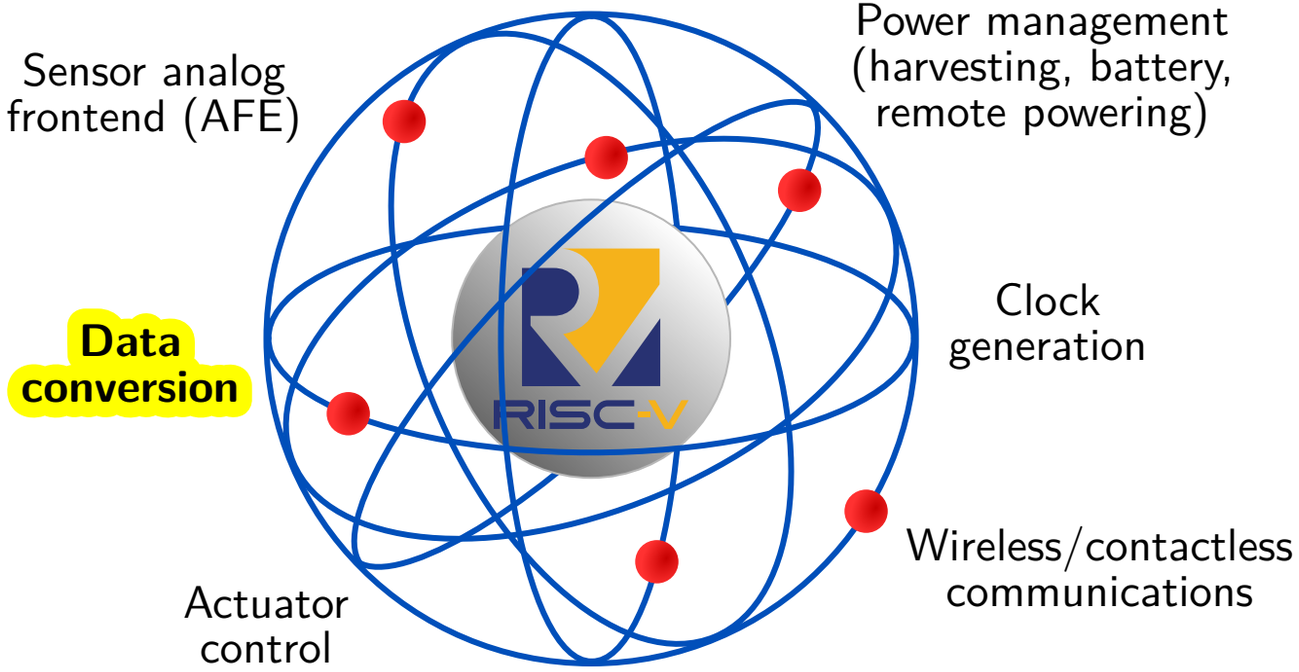
RISC-V International
https://riscv.org

- **CMOS integration** for miniaturized low-power low-cost (mass production) smart devices

▲ Low-power **open RISC-V** digital cores are ideal candidates for **software-defined** (e.g. DSP, NNs) IoT sensors

▼ Several **open mixed-signal** hard **IP blocks** still needed to complete the IoT SoC:

- \+ Sensor AFE (e.g. preamp, PGA, AGC, AA filter)
- \+ Data conversion (e.g. ADC, DAC, decimator)
- \+ Actuator control (e.g. power driver, PWM)
- \+ Clock generation (e.g. X-tal oscillator, VCO, PLL)
- \+ Wireless comm. (e.g. LNA, ASK, FSK, PA)
- \+ Power management (e.g. CP, LDO regulator)



- This paper focuses on **open ADC IPs**, which are required in almost every smart sensor...

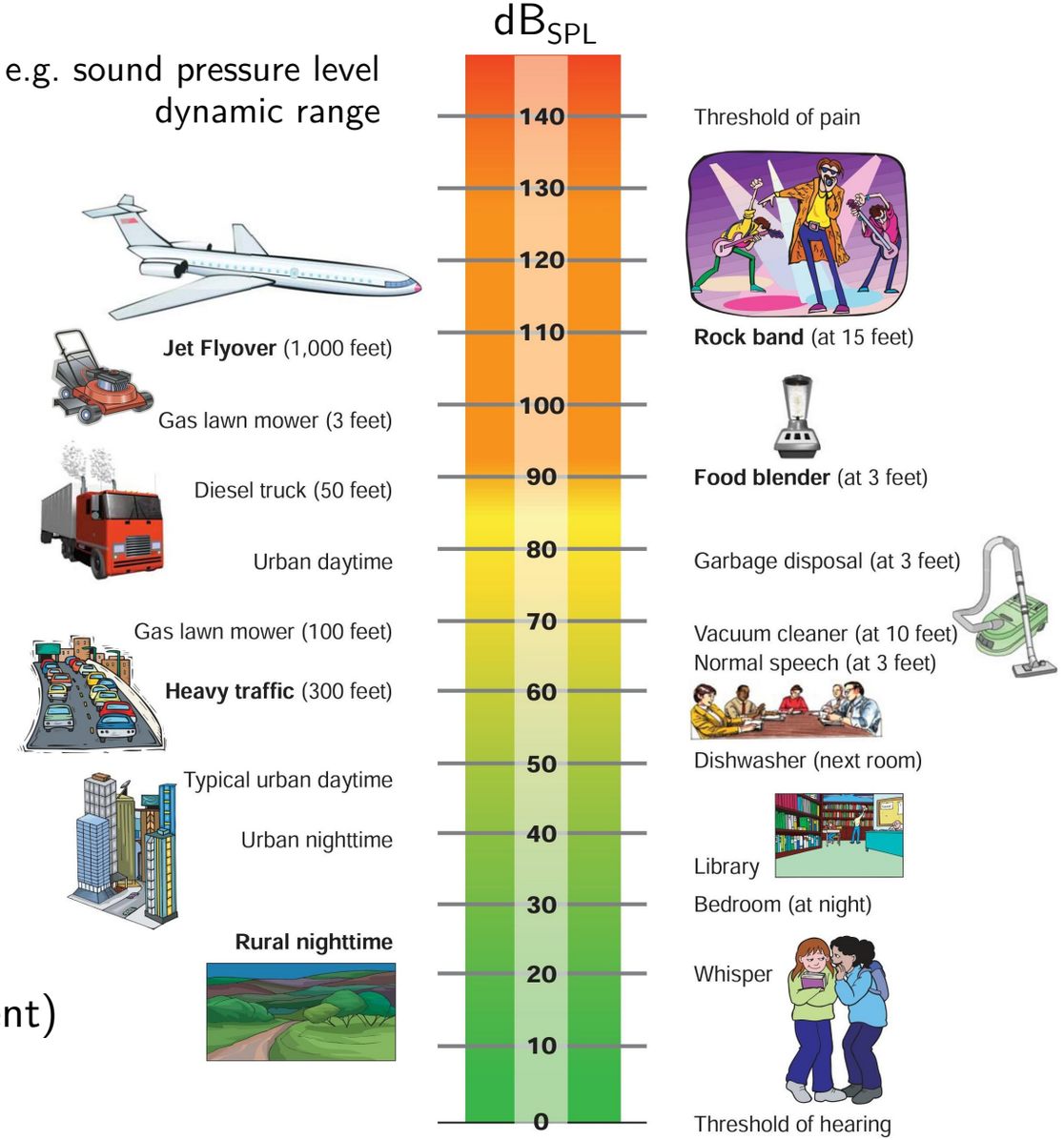
ADC Requirements for IoT Sensors

- Sensor **signal** characteristics?

Measurement	Bandwidth	Dynamic Range
Temperature	< 1 Hz	> 70 dB
Acceleration	< 25 kHz	> 100 dB
Light	< 100 Hz	> 100 dB
Acoustic	< 50 kHz	> 100 dB
Chemical	< 10 Hz	> 80 dB

- ▲ Low bandwidth (dozens of **kHz**)
- ▼ High dynamic range (exceeding **90dB**!)

- Each **analog frontend** adapts sensor signal domain (e.g. current) and dynamic range to the standard full scale (typ. 1V) so the same ADC can be reused for several sensors

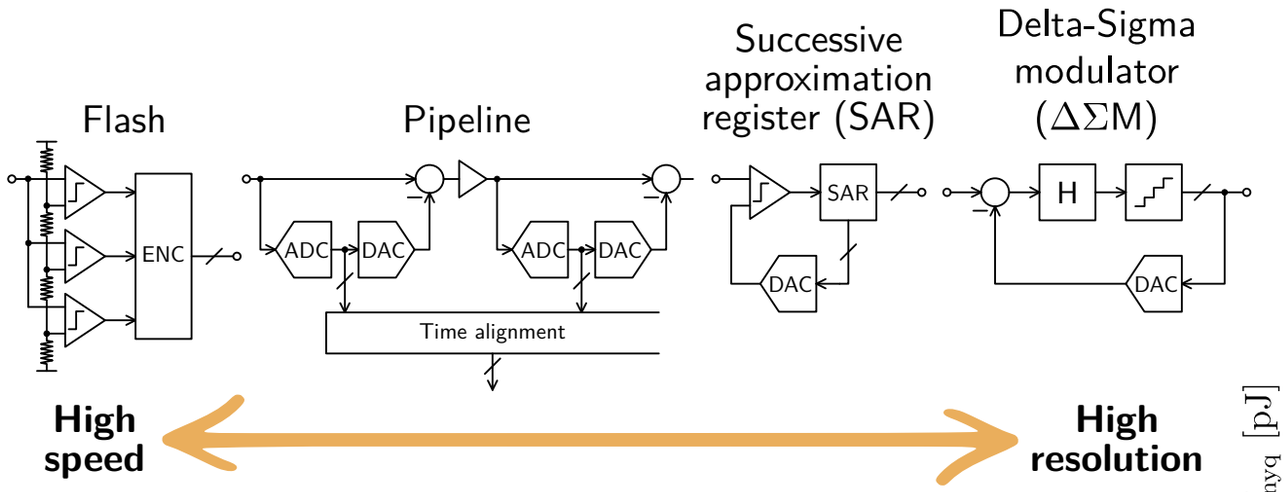


Arizona Department of Transportation, 2008

Which ADC to Choose?

ADC Performance Survey 1997-2019
https://web.stanford.edu/~murmann/adcsurvey.html

- Large variety of **architectures**:



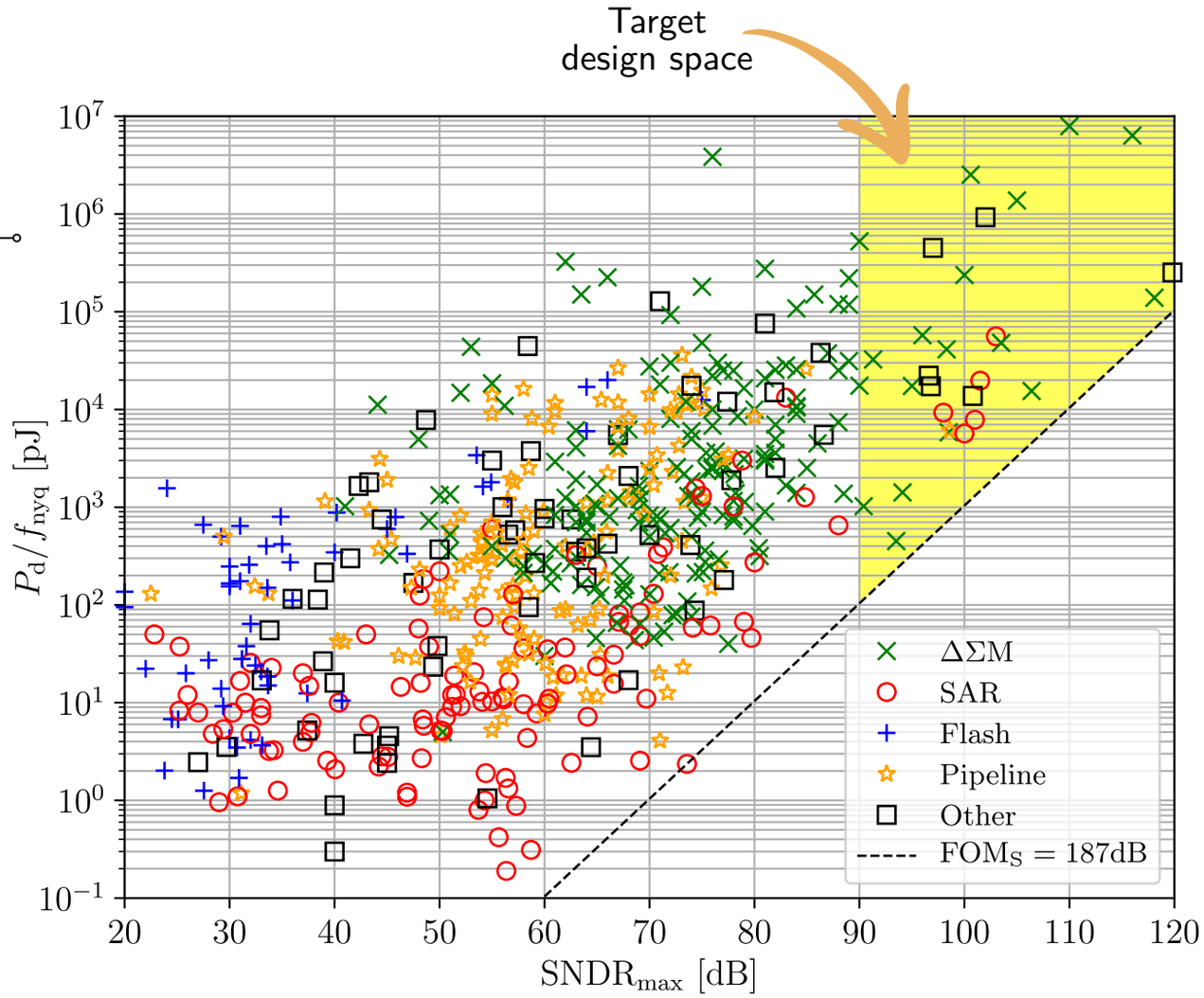
- Designers make use of the **Schreier** figure of merit:

$$\mathrm{FOM_S} \doteq \mathrm{SNDR_{max}} + 10\log\frac{f_{\mathrm{nyq}}}{2P_{\mathrm{d}}}\ [\mathrm{dB}]$$

$2 \times$ bandwidth (BW)

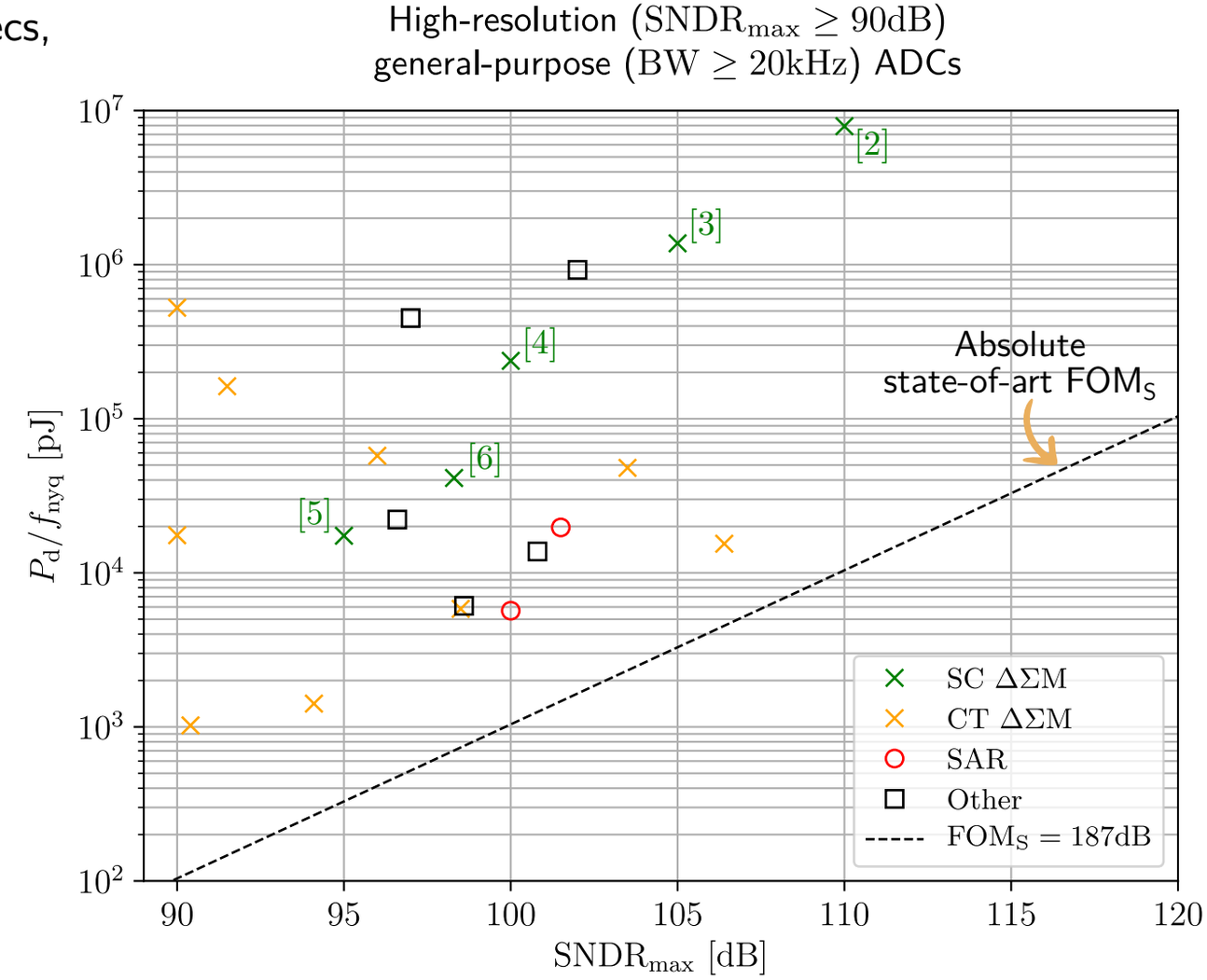
$\simeq 6 \times$ equivalent number of bits (ENOB)

Power consumption



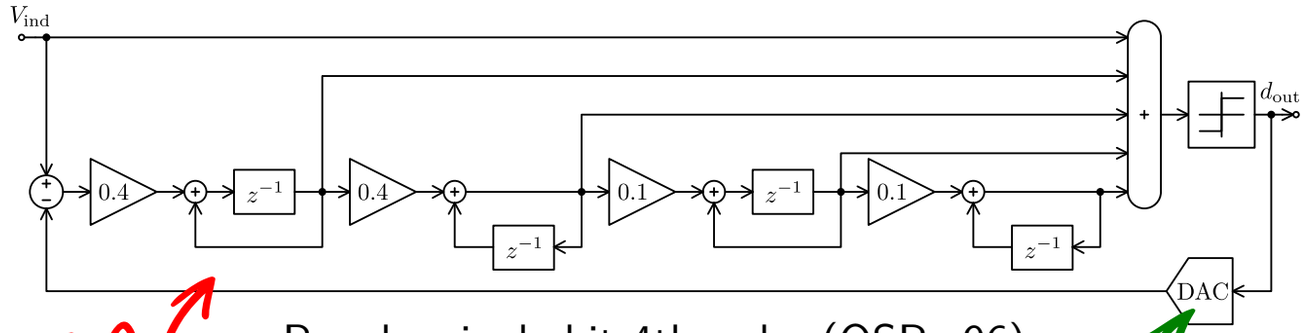
Why are High-Res ADCs Scarce?

- FOM_S not so fair when comparing distant $SNDR_{max}$ specs, as high-res CMOS circuit design must consider:
  - + **Flicker** noise, clock **jitter**, **supply** coupling
  - + Switch non-linearity and **charge injection**
  - + Technology **mismatching**
  - + OpAmp **gain non-linearity**
- Even for the same $SNDR_{max}$, FOM_S does not tell:
  - + **Robustness** against technology and temperature?
  - + Need for circuit **calibration**?
  - + Internal supply **bootstrapping**?
- Oversampled switched-capacitor (**SC**) **ΔΣM** preferred:
  - + **No calibration** needed (unlike SAR)
  - + **Low sensitivity** to CMOS technology compared to continuous-time (CT) ΔΣM



Low-Power ΔΣM Architecture Selection

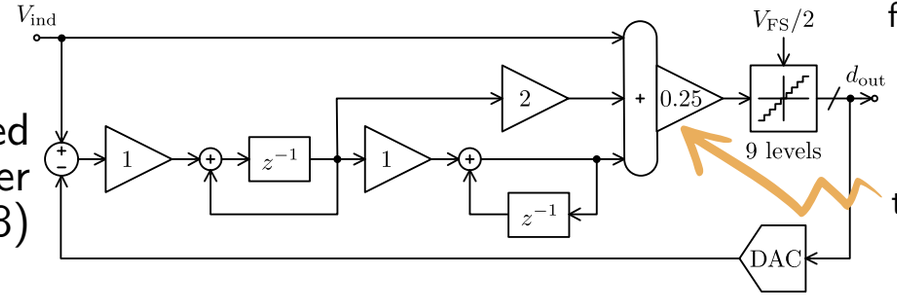
- **Single loop** more robust against technology mismatching than multi-stage noise shaping (MASH)
- **Feedforward path** to lower noise shaper occupancy
- **Power-aware** ΔΣM architecture selection?



Popular single-bit 4th-order (OSR=96)

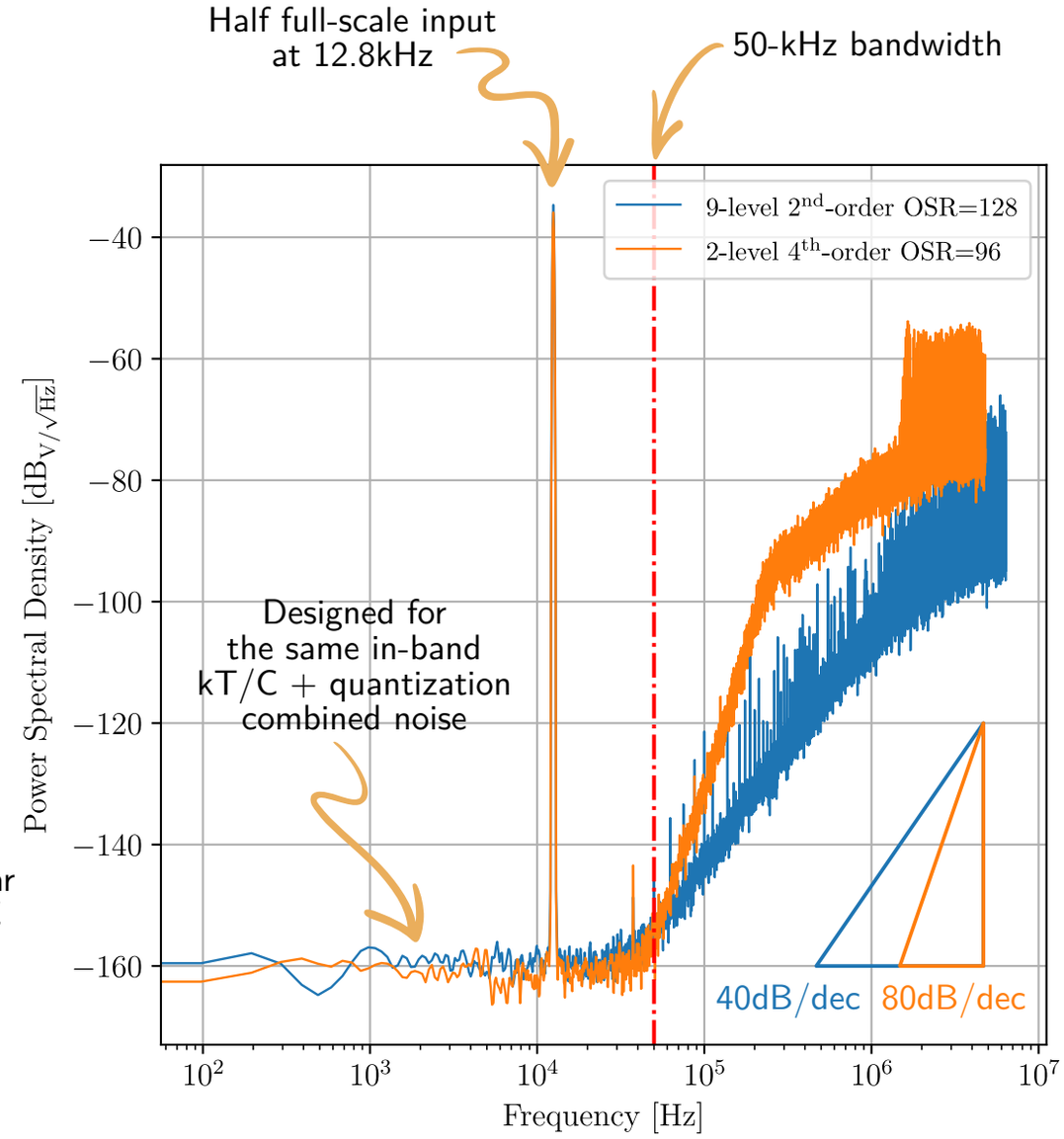
High order prone to instability

Inherently linear feedback DAC



Proposed 9-level 2nd-order (OSR=128)

Loss due to passive adder



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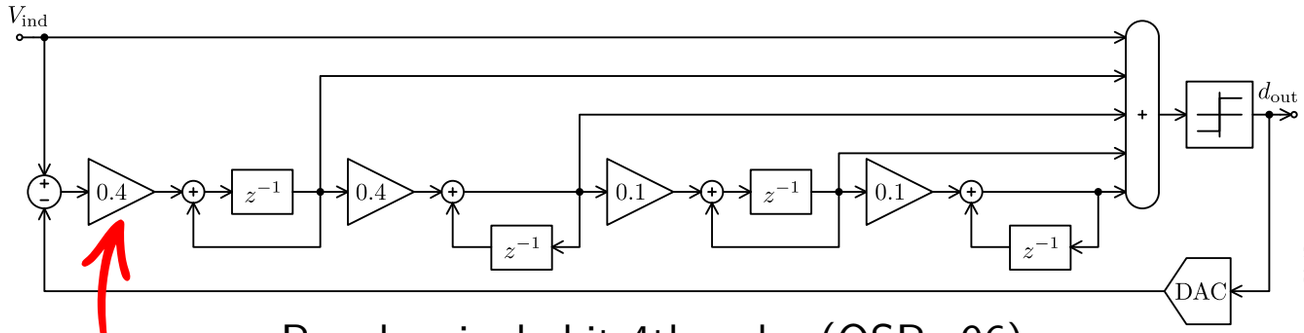
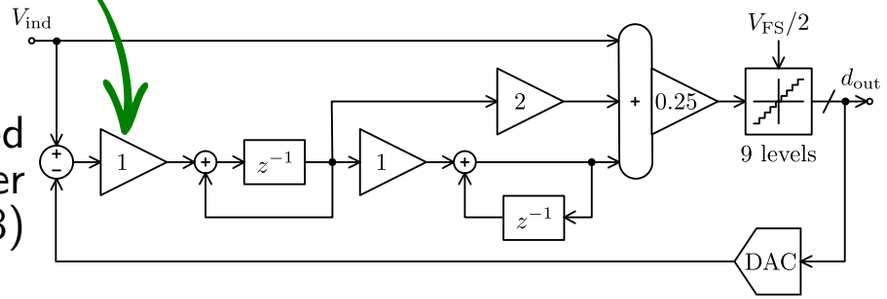


Popular single-bit 4th-order (OSR=96)

Fine input tracking enables unity gain = less **capacitance area** for same kT/C



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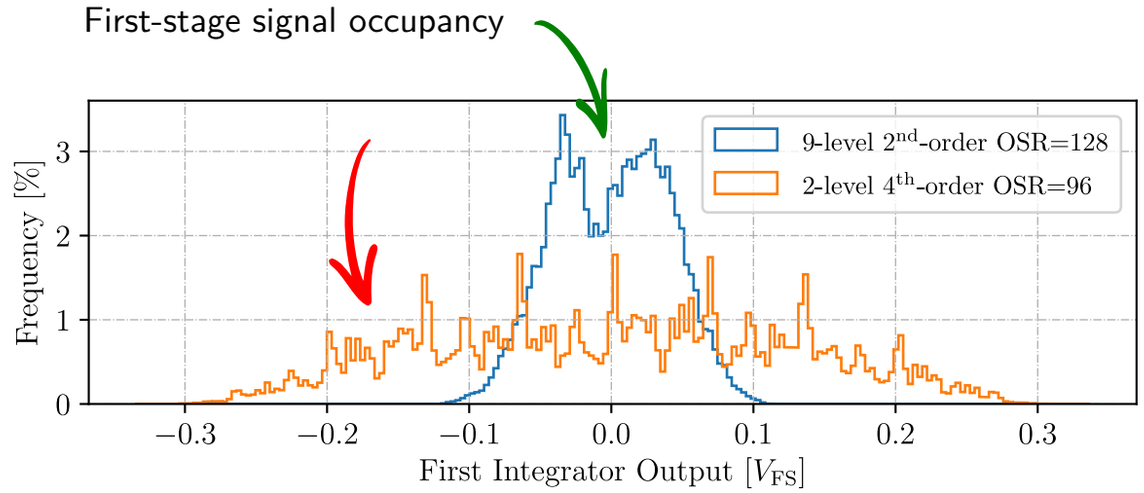
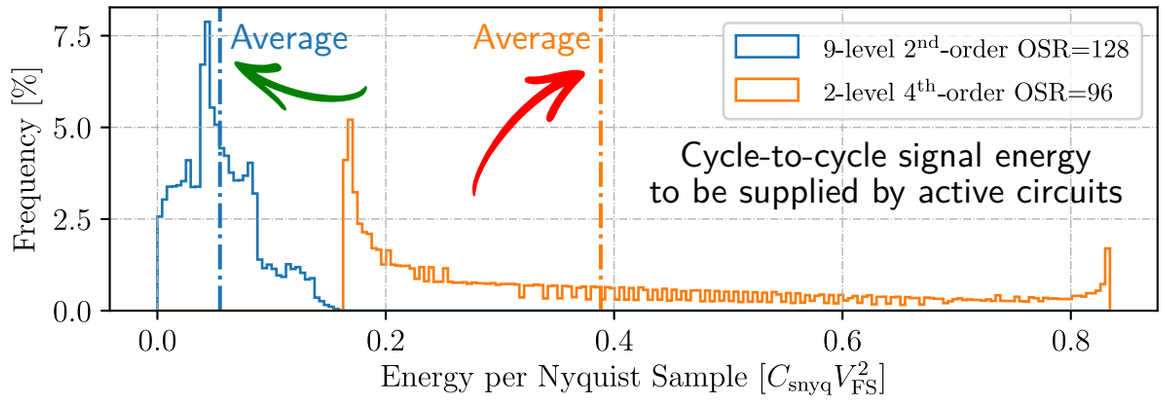
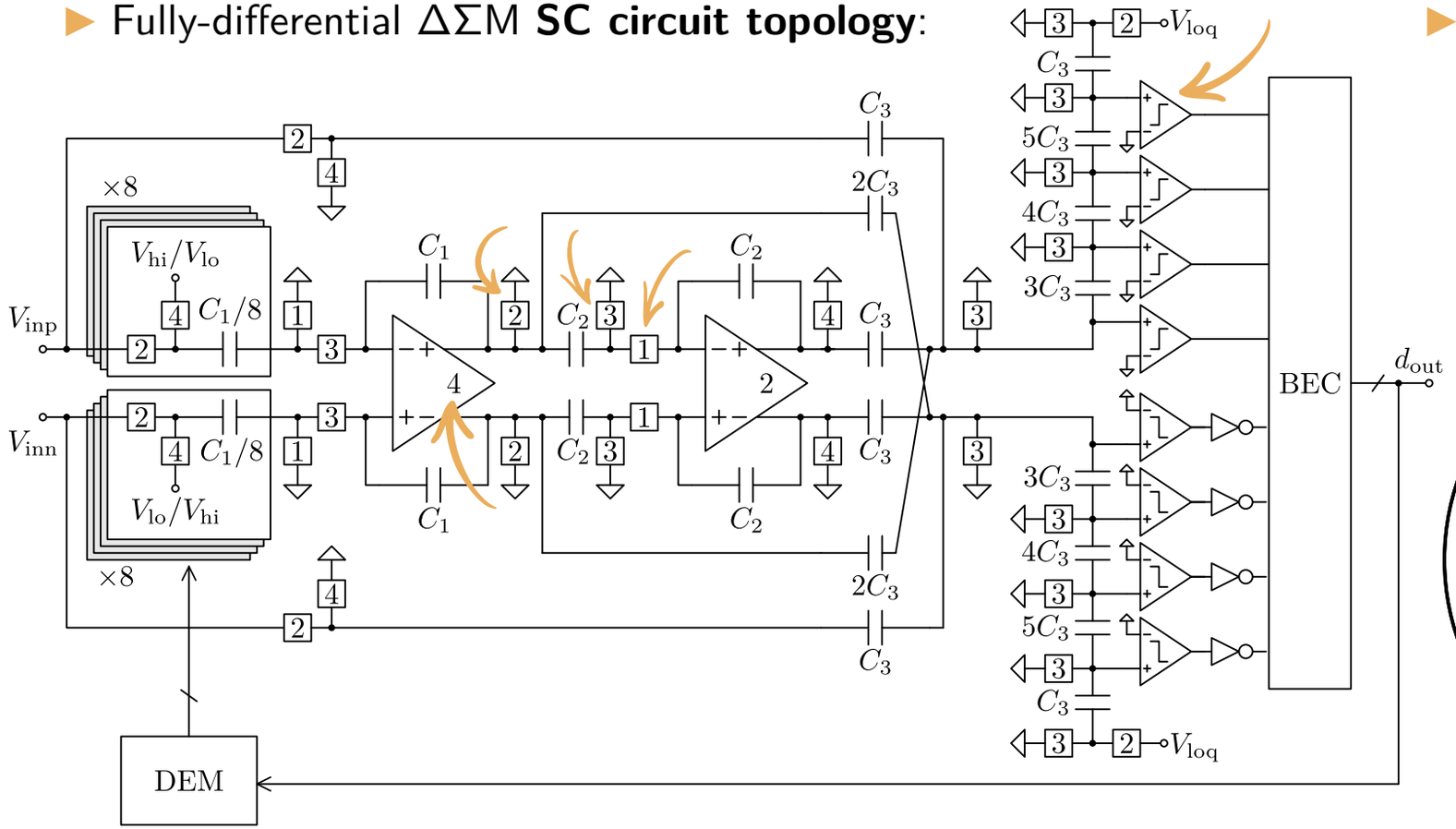




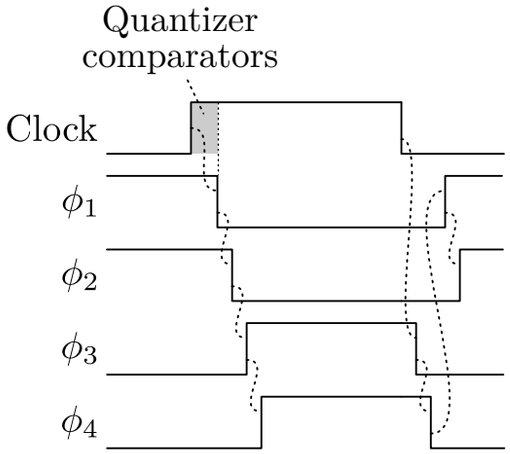
▲ Combination of multi bit + low order + moderate OSR can save >5x **dynamic power** (regardless CMOS circuits)

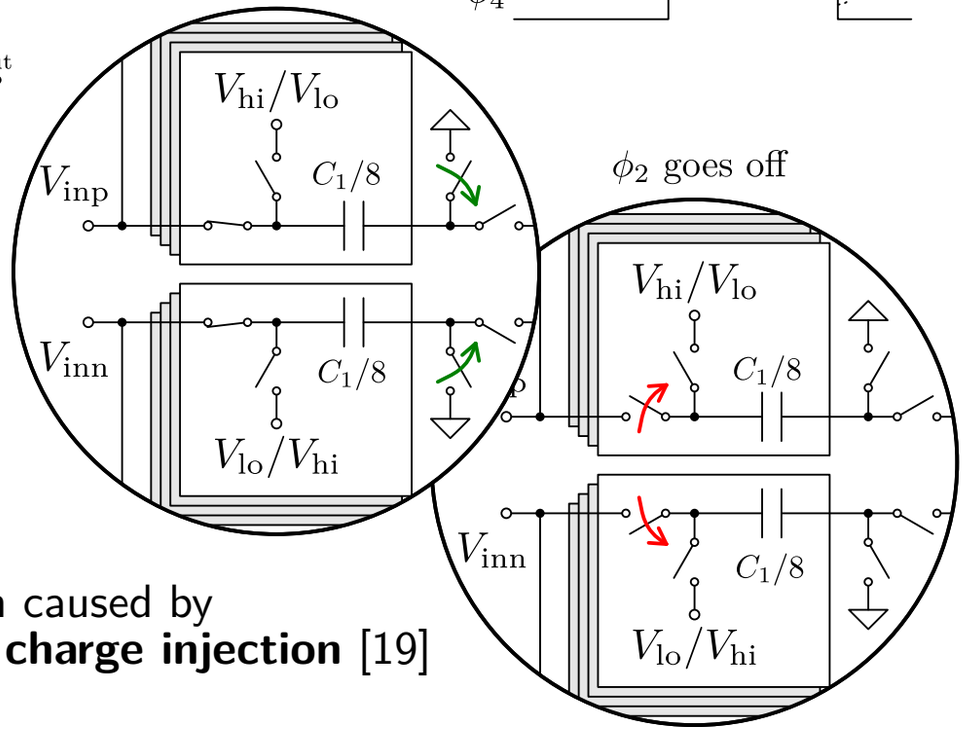
Low-Power ΔΣM Circuit Design

- Fully-differential ΔΣM **SC circuit topology**:



- **4-phase clock** splitting for the operation of the SC network:

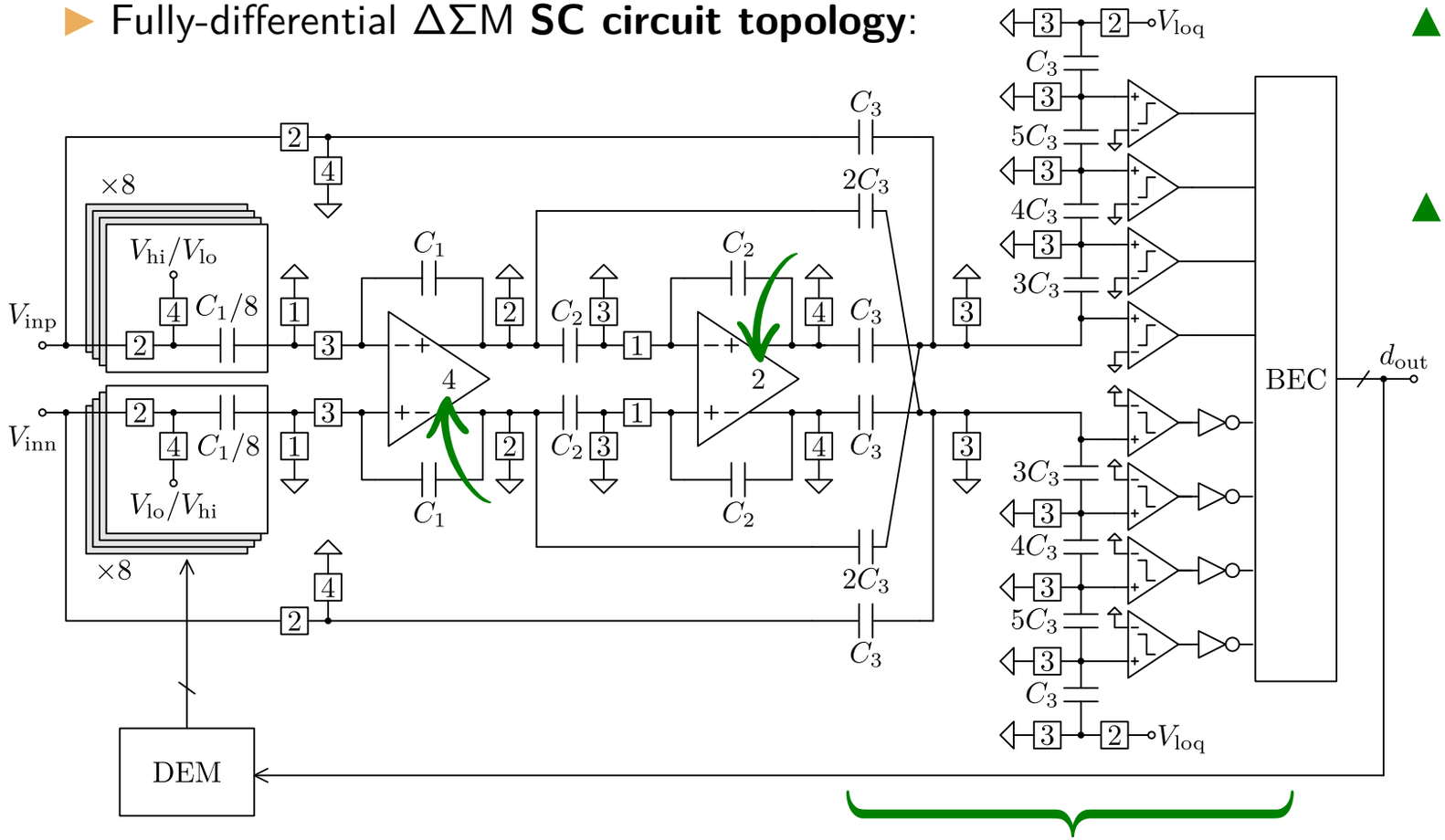




- Attenuation of distortion caused by signal-dependent switch **charge injection** [19]

Low-Power ΔΣM Circuit Design

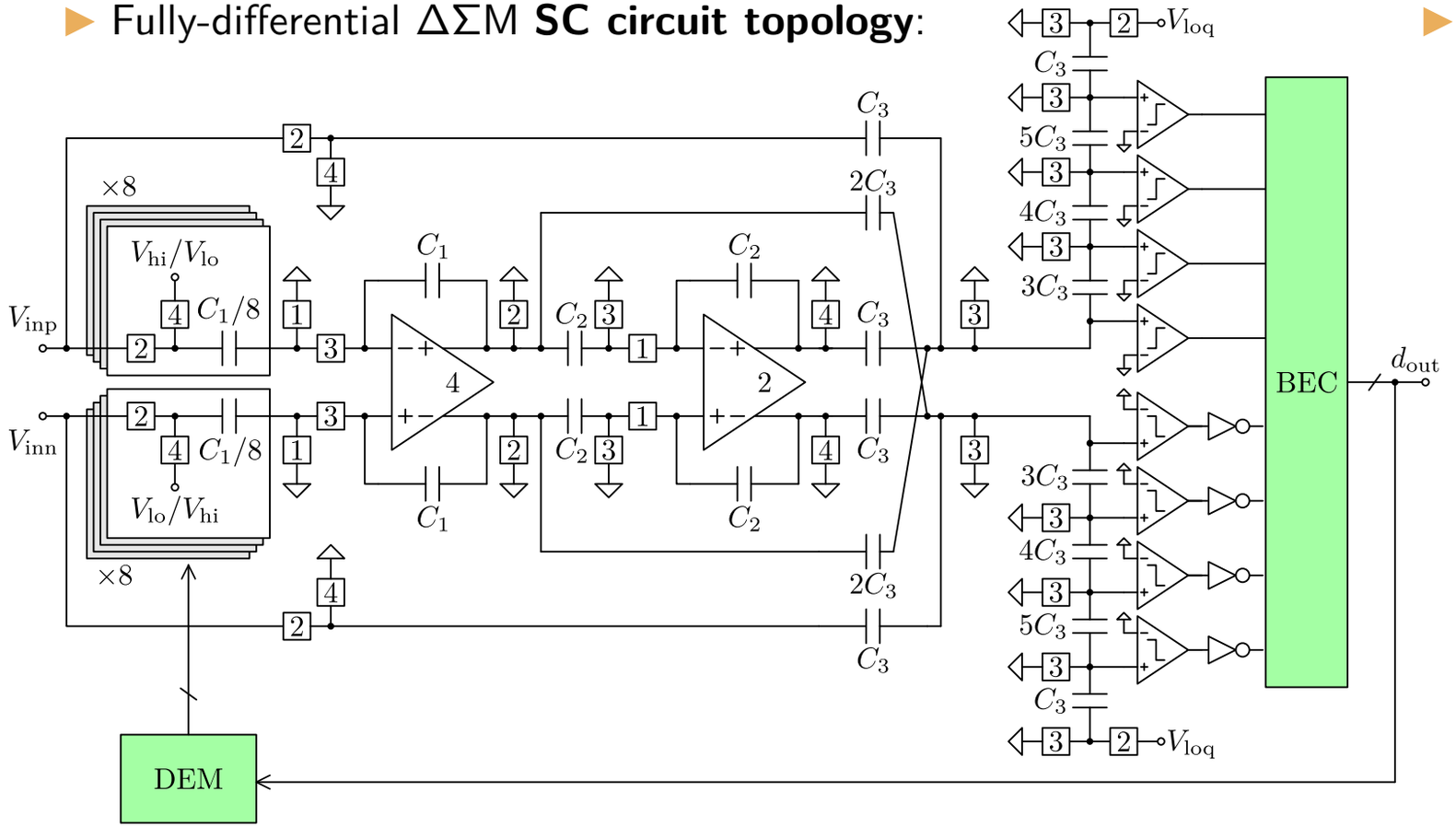
- Fully-differential ΔΣM **SC circuit topology**:



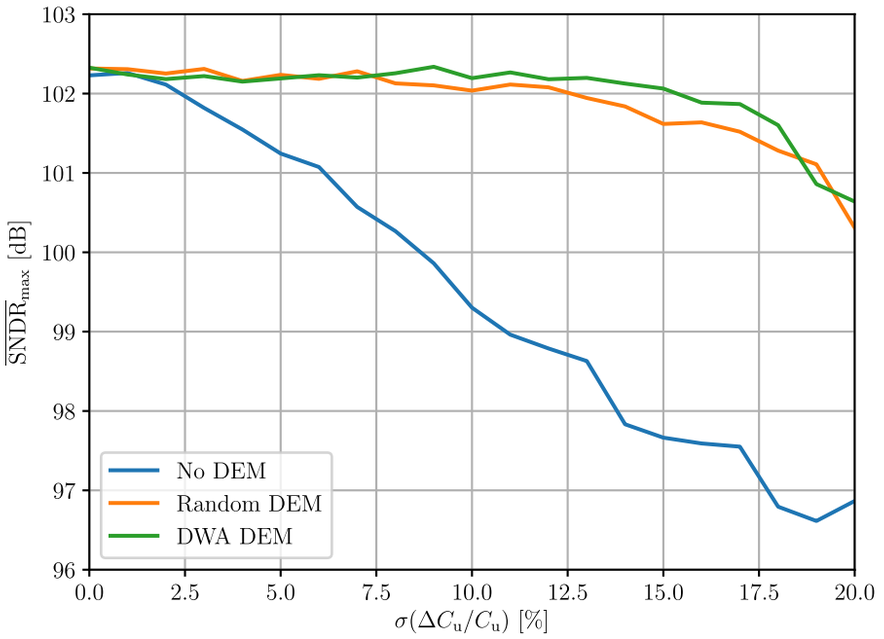
- **Switched-OpAmp** operation [20] saves 50% of static power and avoids internal supply bootstrapping that limits switch lifetime [21]
- 9-level **SC flash quantizer** proposed by these authors [22]:
  - \+ **Low power**
  - \+ **Compact** area
  - \+ High **modularity**
  - \+ **Single** comparator design
  - \+ **Compatibility** with multi-feedforward paths, clocked comparators and switched OpAmps

Low-Power ΔΣM Circuit Design

- Fully-differential ΔΣM **SC circuit topology**:



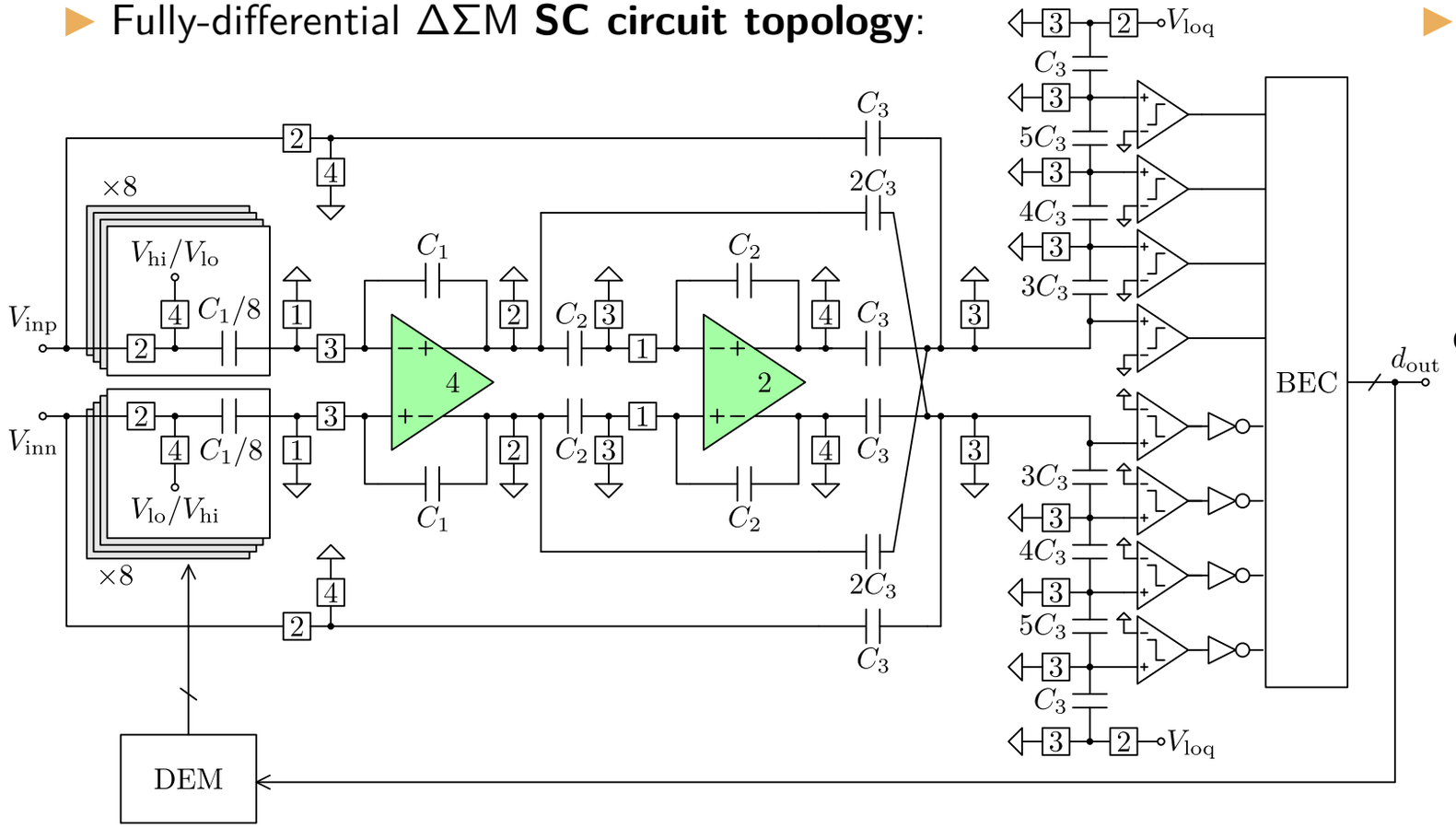
- Digital backend with bubble error correction (**BEC**) and data weighted averaging (**DWA**) to attenuate harmonic distortion



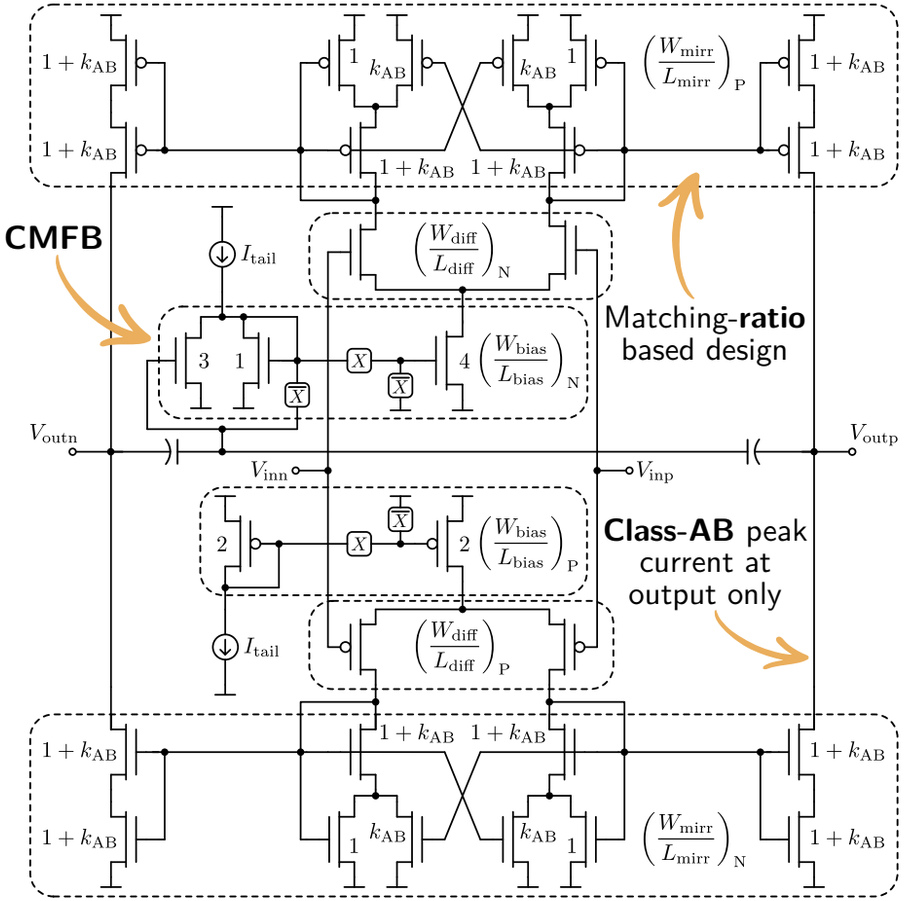
- Multi-bit feedback DAC can tolerate >**10%** of capacitive mismatching

Low-Power ΔΣM Circuit Design

- Fully-differential ΔΣM **SC circuit topology**:



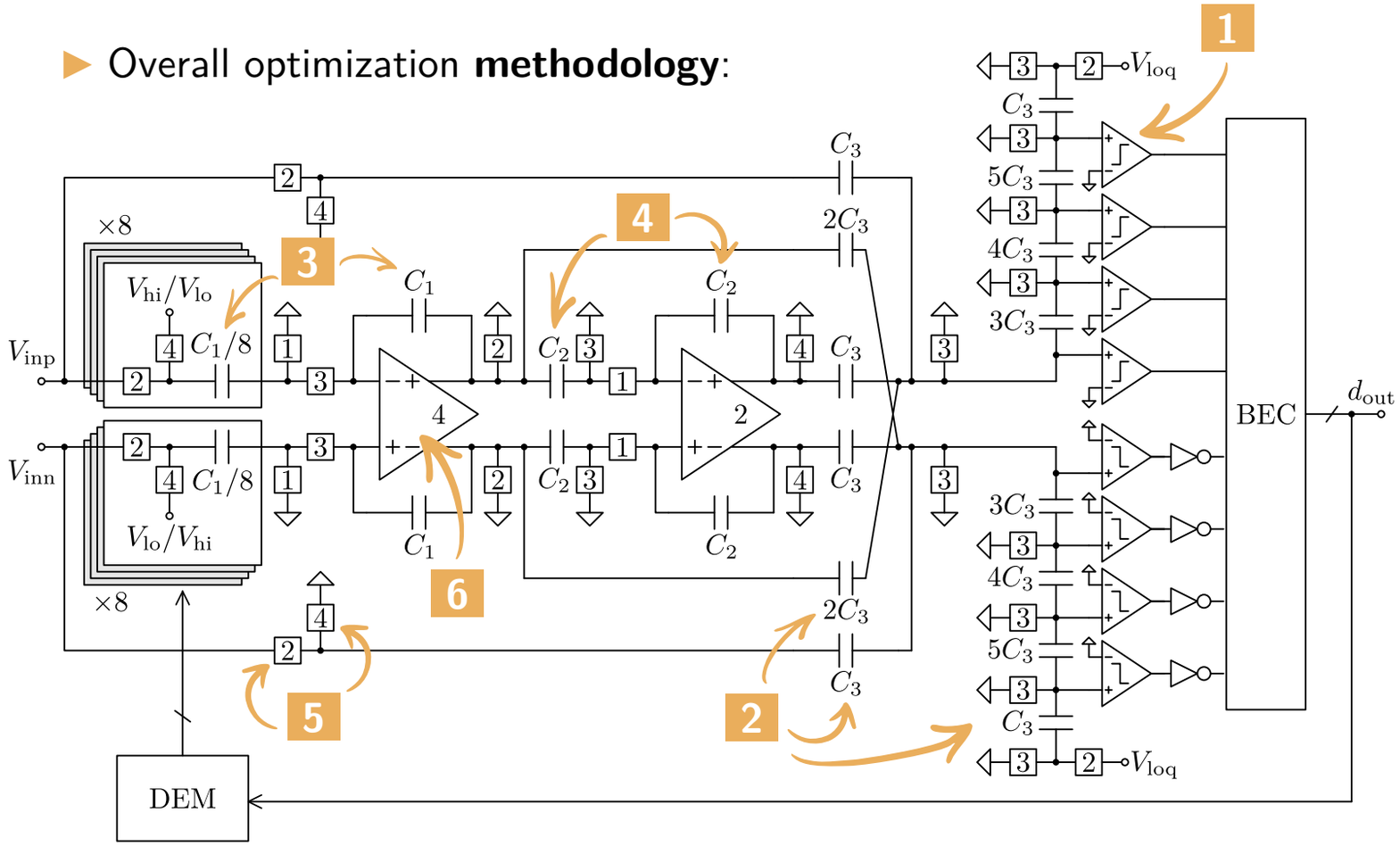
- Switched variable-mirror amplifier (**SVMA**) proposed by these authors [24]:



▲ **Class-AB single-stage** OpAmp with **low sensitivity** to PVT corners

Low-Power ΔΣM Circuit Optimization

- Overall optimization **methodology**:



1. Max offset (min area) allowed to comparators from Montecarlo simulation. Strong-arm **comparator** device sizing (single design) with speed trade-off.

2. Min C_3 to comparator input cap ratio needed from behavioral simulation. Sizing of all $\mathbf{C_3}$ elements.

3. Sizing of $\mathbf{C_1}$ applying 4x kT/C rule (2x fully diff. + 2x S/I phases).

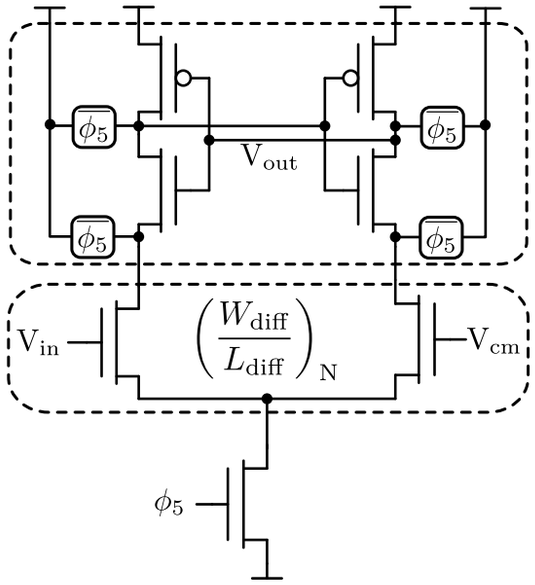
4. Sizing of $\mathbf{C_2}$ by layout and matching (kT/C not dominant).

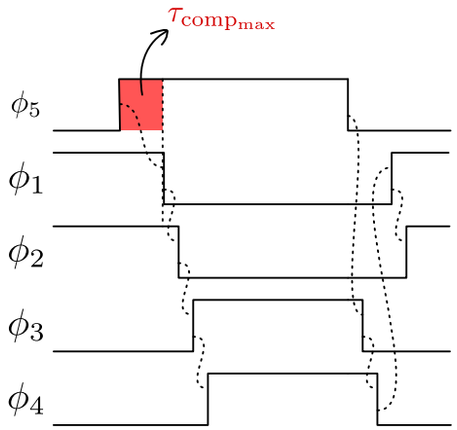
5. Minimum-length **MOS switches** with N/P ratios to equalize on-resistance. Constant switch-to-cap ratio so RC ~ 1/8 clock phase duration.

6. Min OpAmp performance needed from behavioral simulation. Class-AB **SVMA** individual optimization algorithm.

Comparator Optimization (1)

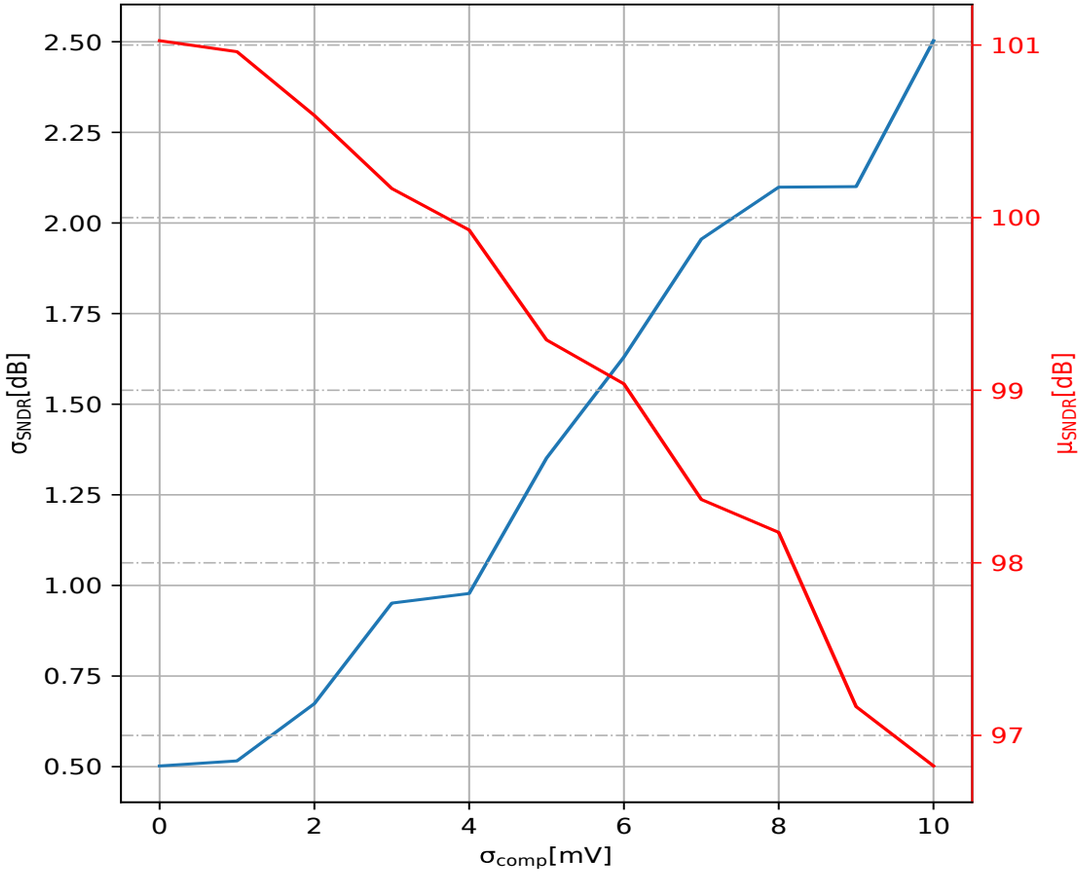
- **Strong ARM** comparator





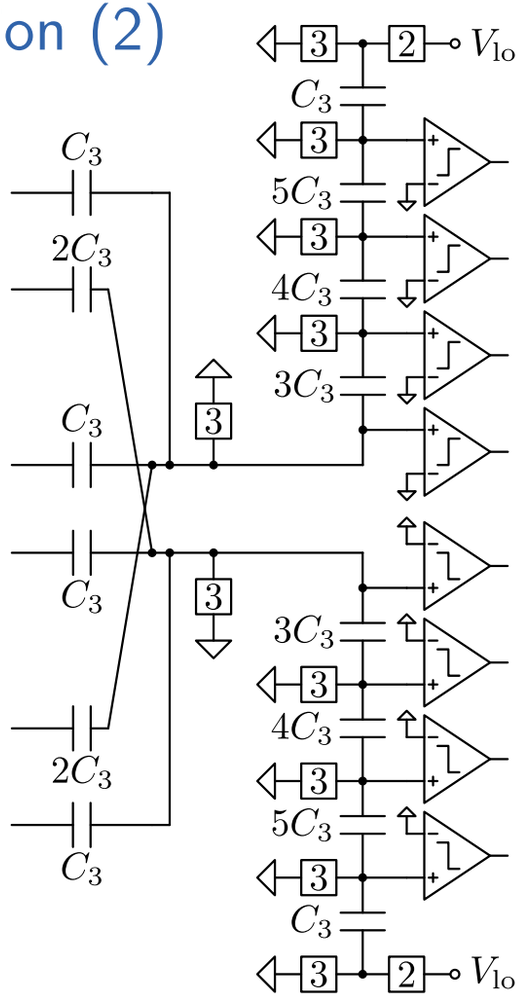
- **Simple** and **fast** latched topology
- **Differential pair** design trade-off:
  - \+ Large size for **offset** reduction
  - \+ Small size for minimum capacitive **parasitics**

- Technology mismatching: **offset** vs **resolution**



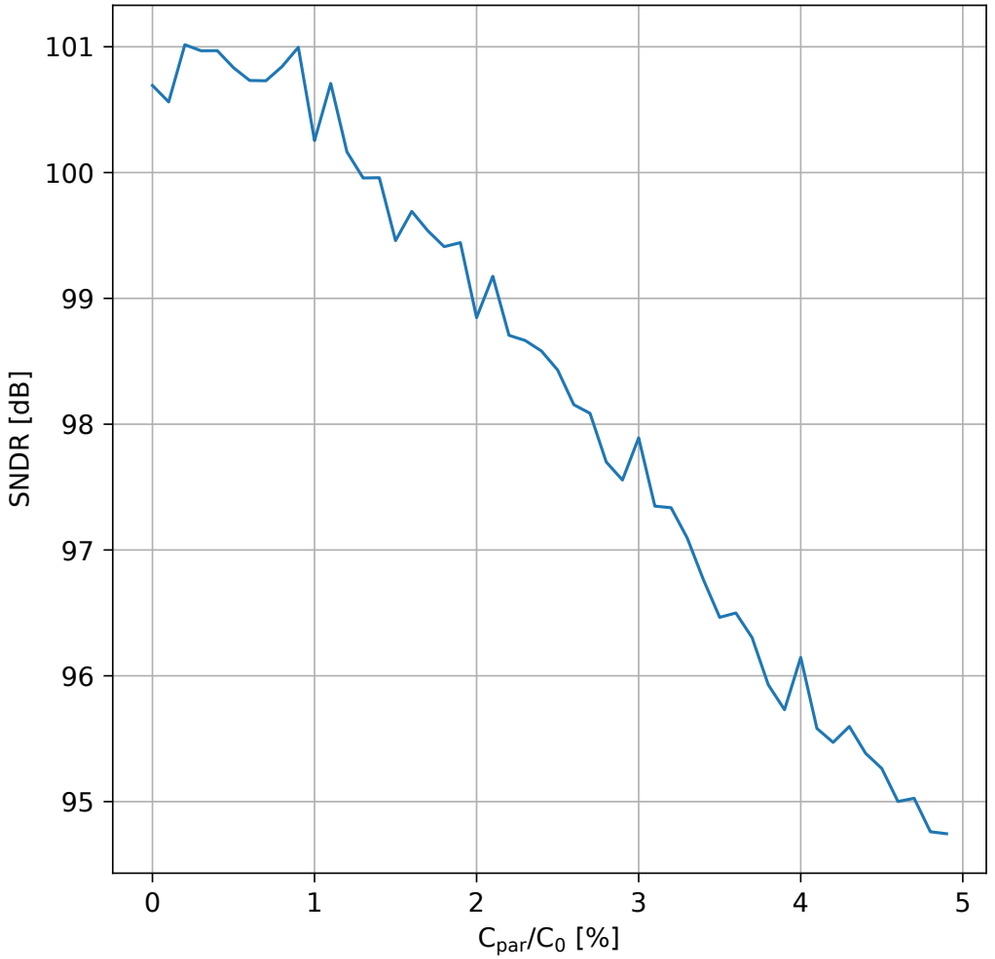
Quantizer Optimization (2)

- **Multi-bit** quantizer:



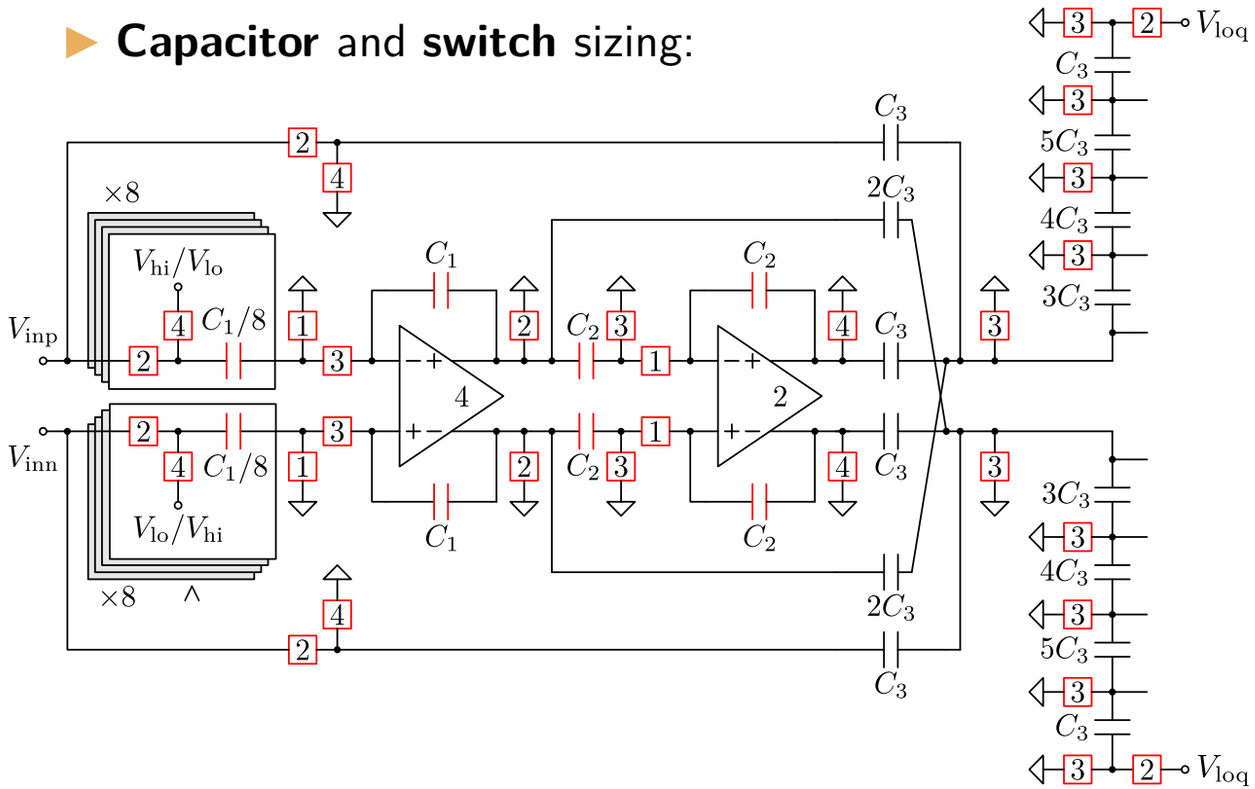
- **C_3** design trade-off:
  - \+ Large size for low sensitivity to **parasitics**
  - \+ Small size for **power saving** at OpAmps

- **Parasitic capacitance** effect on resolution



SC Network Optimization (3,4,5)

- **Capacitor** and **switch** sizing:



- **Sampling capacitor** design trade-off:

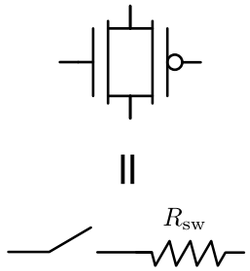
$$\sigma_{\text{n}}^2 = \frac{4KT}{C_1}$$

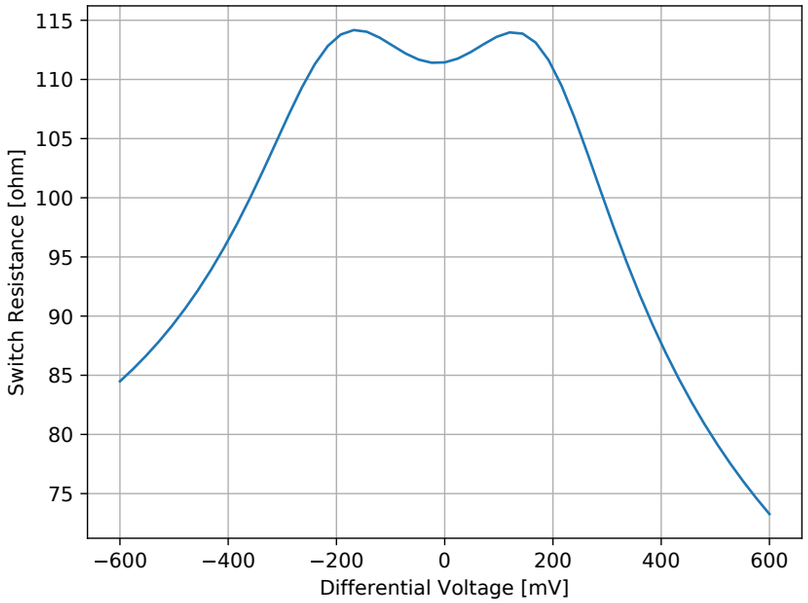
+ ADC effective **resolution**
+ OpAmp **power** consumption

- **Second-stage capacitor** noise requirements strongly relaxed: $C_2 = \frac{C_1}{M}$

- Design of **CMOS switches**:

+ P/NMOS sizing to maximize **resistance linearity**

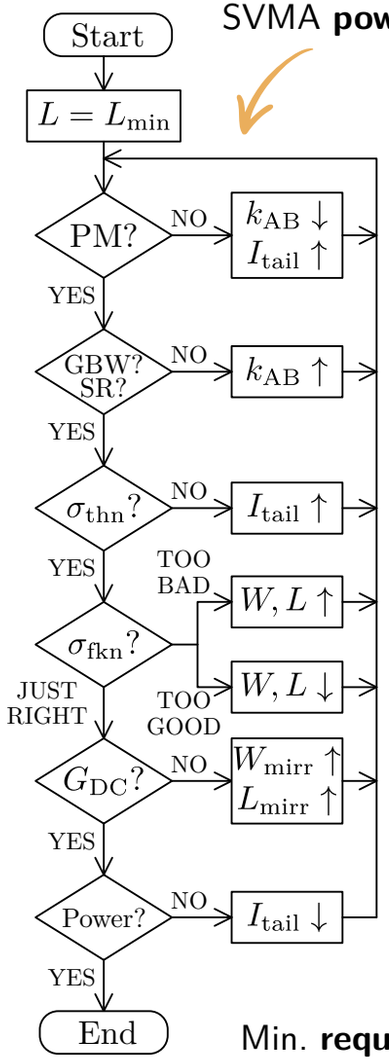




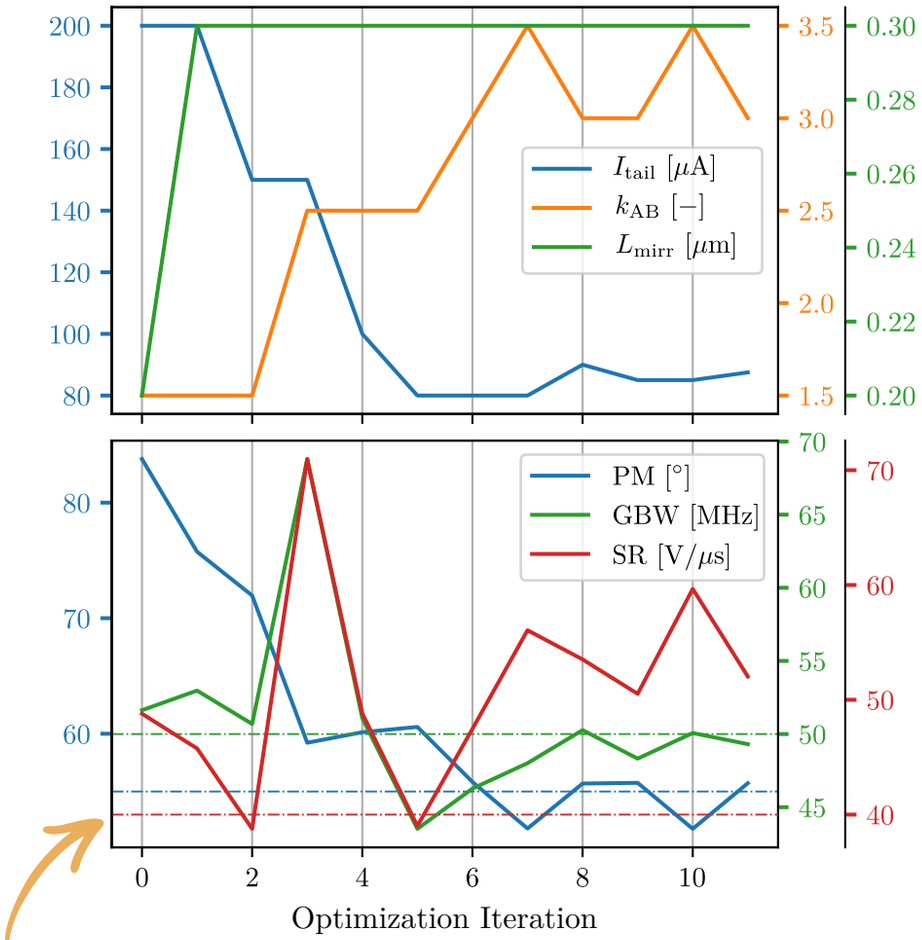
+ **Settling** rule of thumb: $\tau_{sw} = RC \leq \frac{T_{\text{samp}}}{8}$

OpAmp Optimization (6)

SVMA **power** optimization



First-integrator SVMA example



Min. **requirement** from behavioral simulations

Overall ΔΣM Robustness

- Low sensitivity of the ΔΣM IP block to **PVT corners** thanks to robustness of both architecture and CMOS circuits:

	−55°C	27°C	125°C
Slow	94.9	95.1	93.1
Typ.	96.2	96.5	93.2
Fast	94.8	92.4	93.6

SNDR_{max} [dB]

Deviations $<$ **1bit**

ΔΣM Hard IP Layout Design

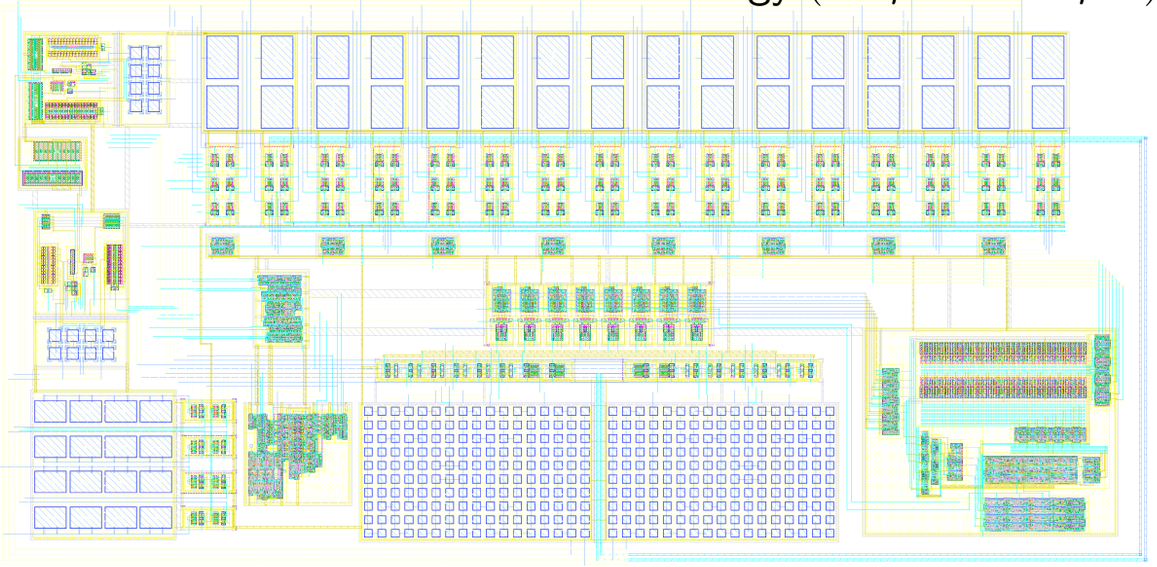
- Two hard IP CMOS implementations for **16-bit 50-kHz** common specifications

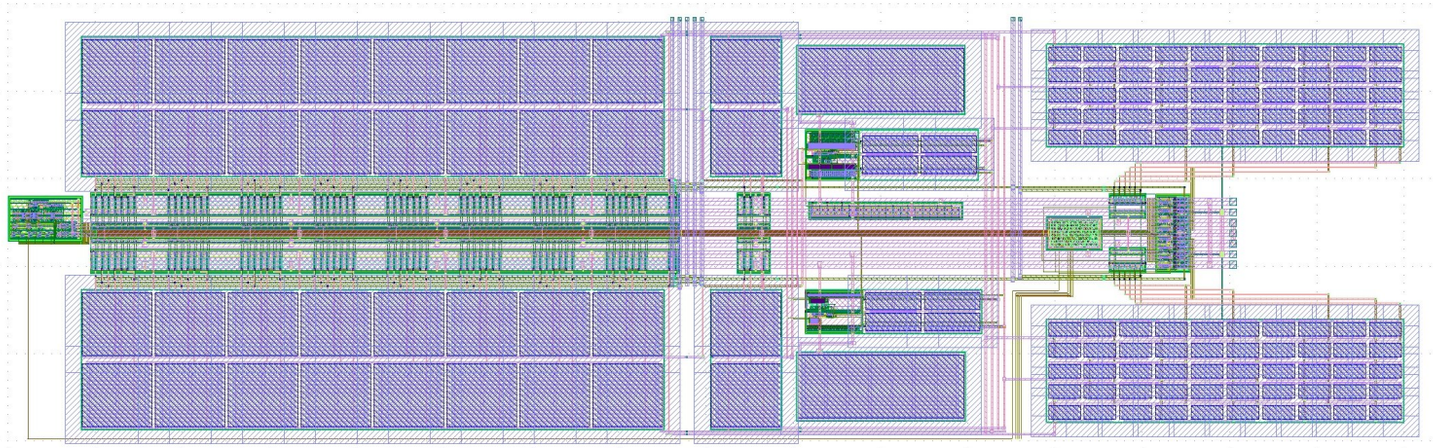
- **EDA** environment used:
  - + Open source Scientific Python (**SciPy**) for architecture design
  - + Commercial **Cadence Virtuoso** suite for full-custom schematic and layout design

- **Open** or **free** EDA alternatives exist but:
  - + Full-custom **PDK** typically unavailable and difficult to develop (DRC|XTR|LVS)
  - + **NDA** restrictions on CMOS process data

`https://peardrop.co.uk`
`http://opencircuitdesign.com`
`https://efabless.com`

XFAB 1.8-V 180-nm 6-metal MiM CMOS technology $(640\mu\text{m} \times 315\mu\text{m})$





TSMC 1.2-V 65-nm 8-metal MiM CMOS technology $(810\mu\text{m} \times 250\mu\text{m})$

ΔΣM Hard IP Layout Design

- Comparison of two **floorplan** strategies:
  - \+ XFAB layout is driven by device **matching**
  - \+ TSMC layout is driven by differential **symmetry**
- Standard **analog layout** guidelines [29] for device matching and signal decoupling
- These mixed-signal hard IP blocks still lack of the practical **digital backends**:
  - \+ **Decimator** filter for downsampling output data to (almost) Nyquist rate
  - \+ Standard lightweight register-based **interface** like AXI4-Lite [30]

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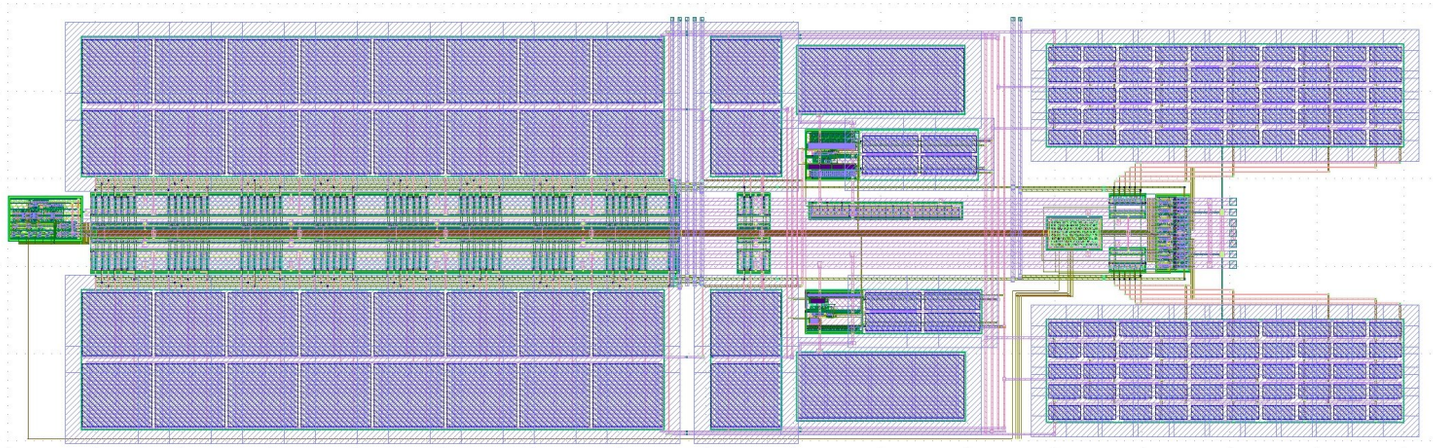

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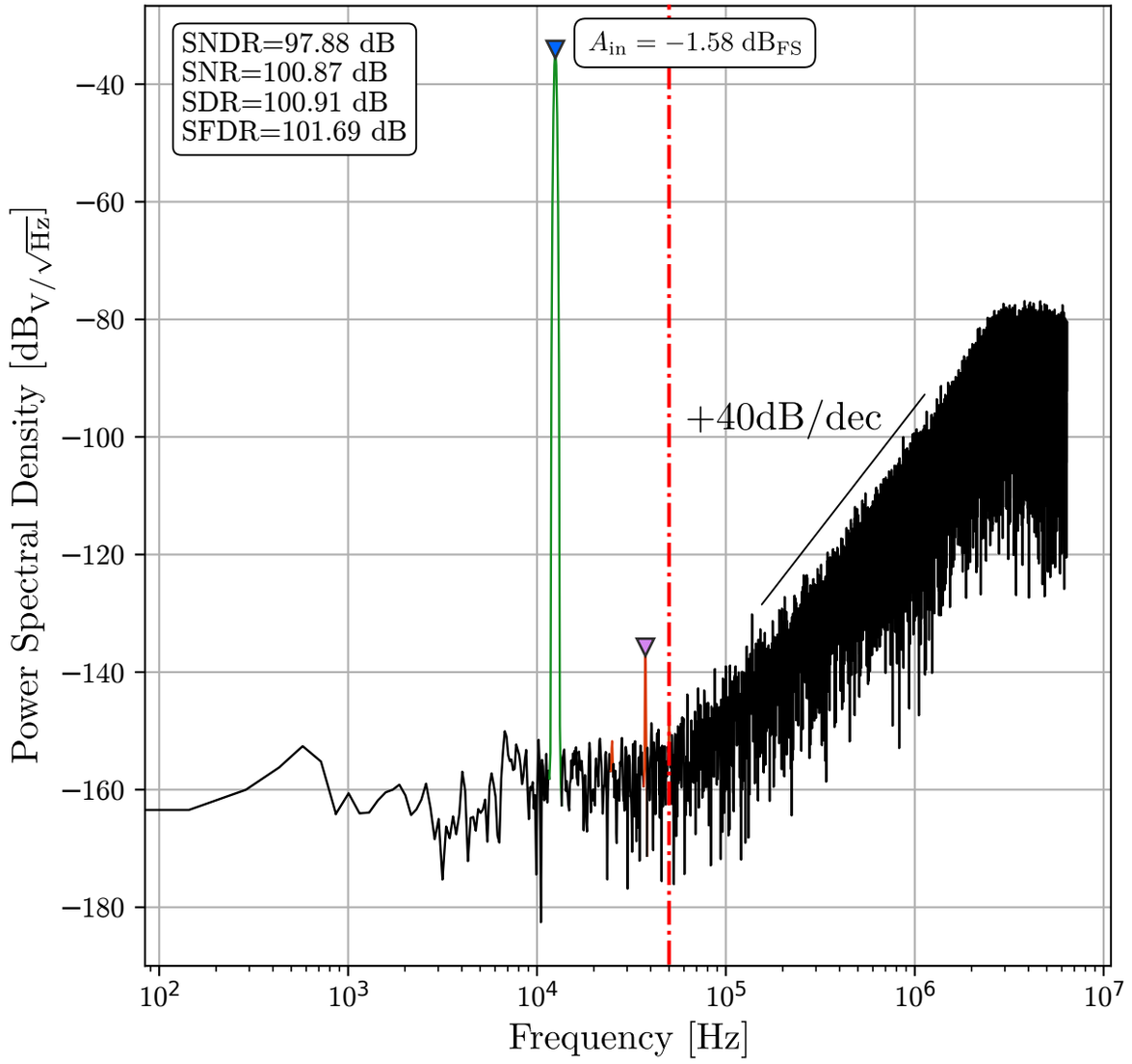
- **Post-layout** simulations return <1.5dB of $SNDR_{max}$ loss due to parasitics

TSMC 1.2-V 65-nm 8-metal MiM CMOS technology



ΔΣM IP Technology Scalability

- Challenge of **analog** CMOS **downscaling** due to:
  - + Increase of **process variability**
  - + Reduction of supply voltage (**full scale**)

Larger capacitors required to downscale kT/C noise and keep same dynamic range

Loss of device scalability benefits (**similar area**)

Loss of gm/I_D and parasitics benefits (**similar power**)

Comparison of high-resolution ($SNDR_{max} \geq 90dB$) general-purpose ($BW \geq 20kHz$) SC ΔΣ Modulators for ADCs

	[2]	[3]	[4]	[5]	[6]	This work†		
Technology	800	350	250	180	160	180	65	nm
Supply voltage	5	5		0.7	1.8	1.8	1.2	V
Diff. full scale	4		6.6		3.5	2	1.2	V_{pp}
Sampling rate	6.14	5.12	20	5	11.29	12.8		MS/s
Bandwidth	48	20	1000	25	20	50		kHz
Supply power	760	55	475	0.87	1.65	0.85	0.63	mW
Area	25	5.6	20.2	2.16	0.16	0.2		mm^2
$SNDR_{max}$	110	105	103*	95	98.3	100.3	98.0	dB
FOM_S	158.0	160.6	166.2*	169.6	169.1	178.0	177.0	dB
Bootstrap-free	Yes	Yes	Yes	No	No	Yes		
Calibration-free	Yes	Yes	Yes	Yes	Yes	Yes		

*FOM_S from DR instead of $SNDR_{max}$. †Post-layout simulation results.

ΔΣM IP Technology Scalability

▼ Challenge of **analog** CMOS **downscaling** due to:

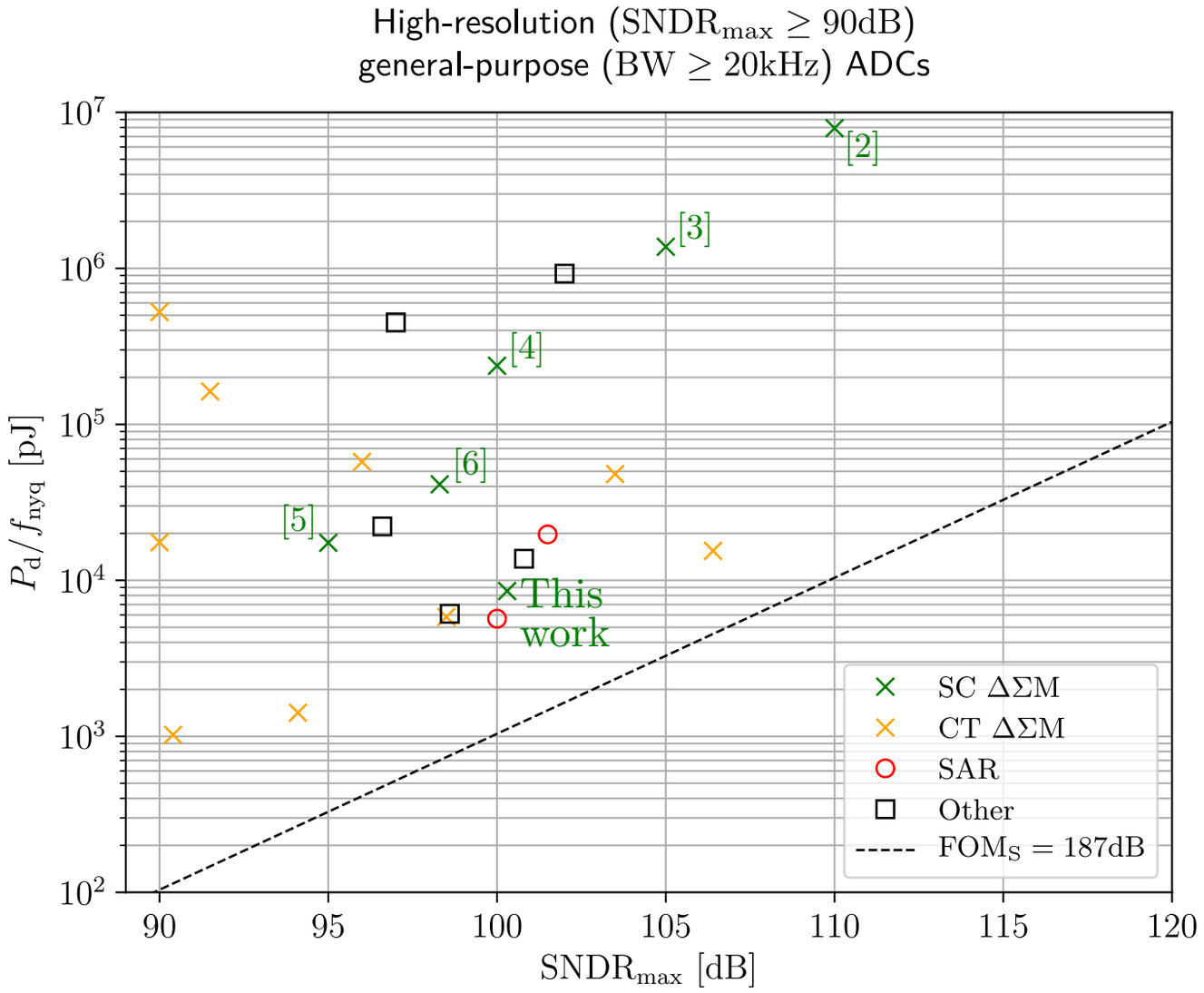
+ Increase of **process variability**
+ Reduction of supply voltage (**full scale**)

Larger capacitors required to downscale kT/C noise and keep same dynamic range

Loss of device scalability benefits (**similar area**)

Loss of gm/I_D and parasitics benefits (**similar power**)

▲ ΔΣM ADC IP block with **competitive FOM$_S$** and remarkable **PVT robustness**



Conclusions

- A **low-power high-res** SC ΔΣM ADC IP block has been presented for open-hardware IoT sensory devices
- Calibration-**free** bootstrapping-**free** resistor-**less** CMOS implementation
- Remarkable **FOM$_S$** and **robustness** vs process and temperature deviations
- Design **methodology** from architecture to circuit for **power optimization**
- **Scalability** examples in 1.8-V 180-nm and 1.2-V 65-nm CMOS technologies
- Current **open-hardware** restrictions:

Description Level	Modelling	NDA and/or Licensing
Architecture HDL code	• Quantization noise • Thermal noise • OpAmp-driven performance • Mismatching effects • Clock jitter	Open
Mixed-signal (transistor and RTL) schematic	As above, plus: • Flicker noise • Switch non-linearity and charge injection • Dynamic power consumption • PVT corners	• CMOS PDK (device electrical models and logic libraries) • EDA schematic, simulation and synthesis tools • IP standard backend (e.g. AXI4-Lite)
Physical layout	As above, plus: • RC parasitics • Crosstalk • Max. clock frequency • Floorplan	• CMOS PDK (pcells, verification rules and P&R libraries) • EDA physical and post-layout tools

Future Work

- Development of the ΔΣM IP **digital backend** (decimator + AXI4-Lite interface)
- Integration of the two ΔΣM hard IP examples in **180-nm** and **65-nm CMOS technologies**
- ΔΣM hard IP blocks characterization and test of radiation hardening (**Rad-Hard**)

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Thanks for your attention!