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CAS

A 1024-Ch GFET 10-bit 5-kHz 36-µW Read-Out Integrated Circuit for Brain µECoG

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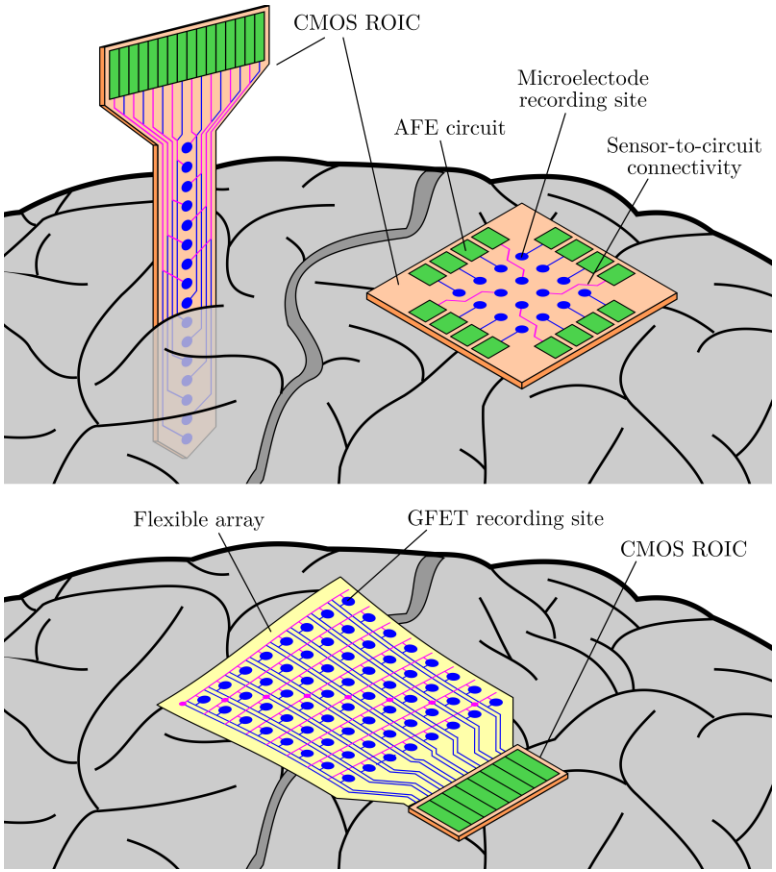
- Liquid-Gate GFET
- Time-Multiplexing
- ROIC
- DC Offset Cancellation
- CDS + PGA
- Chip
- Conclusions

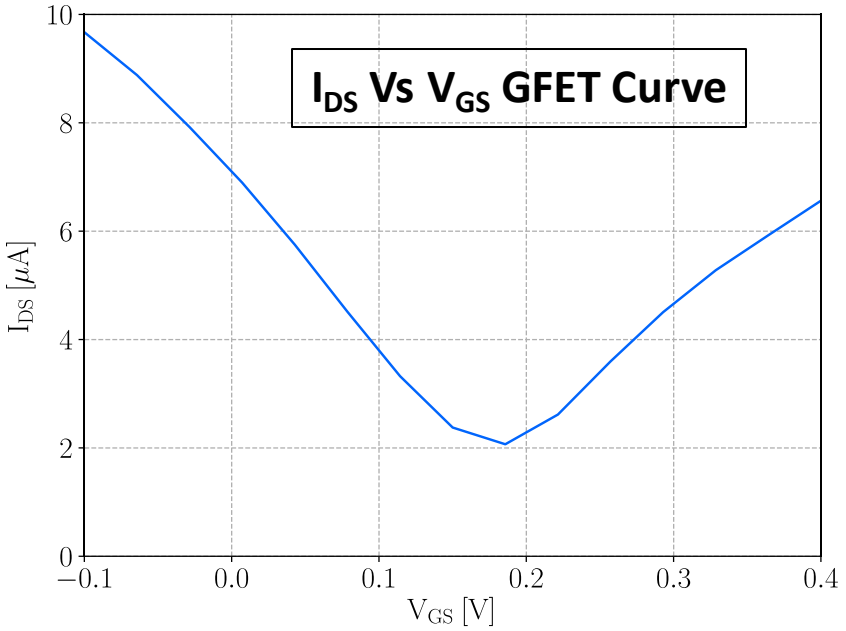
Introduction

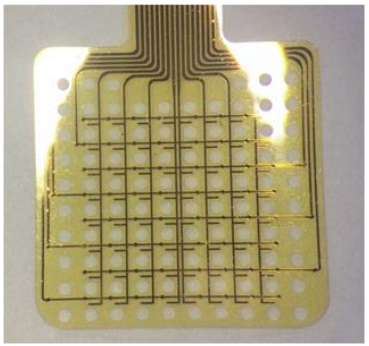
- **Low-power** ICs with **massive** number of channels needed for **neural recording**
- **Monolithical** high density in small areas, **high** fabrication **cost** and **low scalability**
- **Hybrid** (sensors+IC) device preferred **for large sensing area, low cost,** CMOS compatibility and **flexible substrates**
- **New Hybrid multiplexing scheme for low cost and large area flexible GFET active sensor arrays**



Liquid-Gate GFET

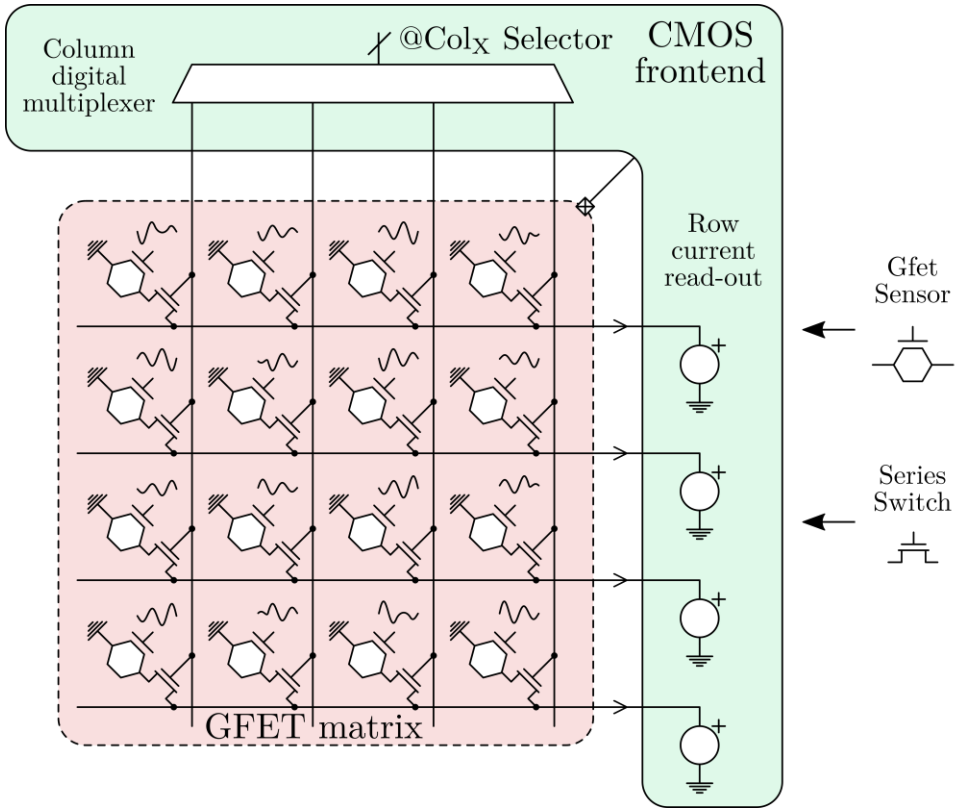
- ▲ **Liquid-gate** Graphene field-effect transistors (**GFETs**) are **good candidates for** micro-electrocorticography (**µECOG**)
- ▲ **Good** Signal-to-Noise Ratio (**SNR**) while keeping **biocompatibility**, **low dimensionality** and mechanical **flexibility**
- ▲ **Active sensor** with an expected transcoductance of **Gm = 0.1 mS** and **Rds** of **~2 kOhm**
- ▼ **GFET ambivalent conduction** requieres from **second technology** for **multiplexing**





Time-Multiplexing

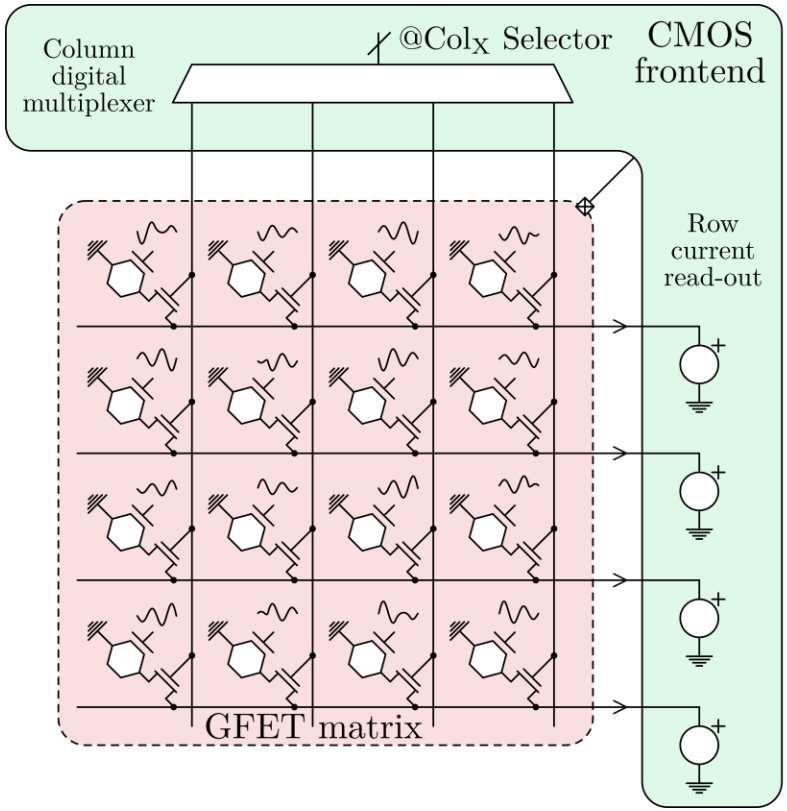
- **Classic Time-Domain Multiplexing**

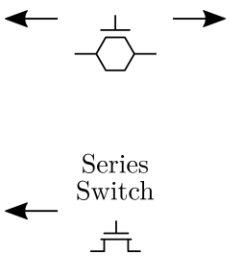


- ▼ **GFET + Switch** Technology integration
- ▲ At any time only **one device connected per row**

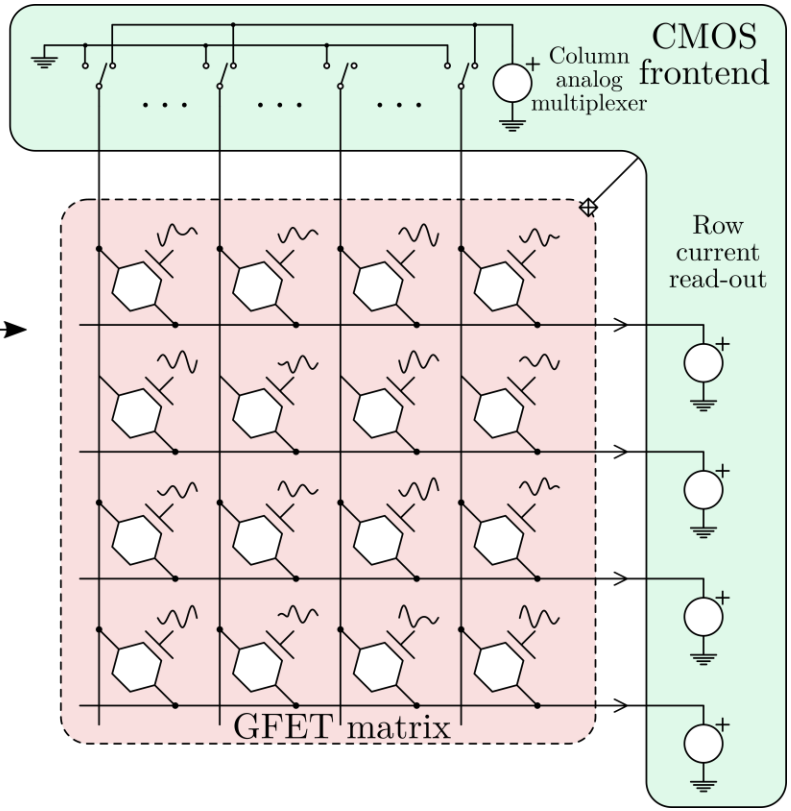
Time-Multiplexing

Classic Time-Domain Multiplexing





Proposed Time-Domain Multiplexing



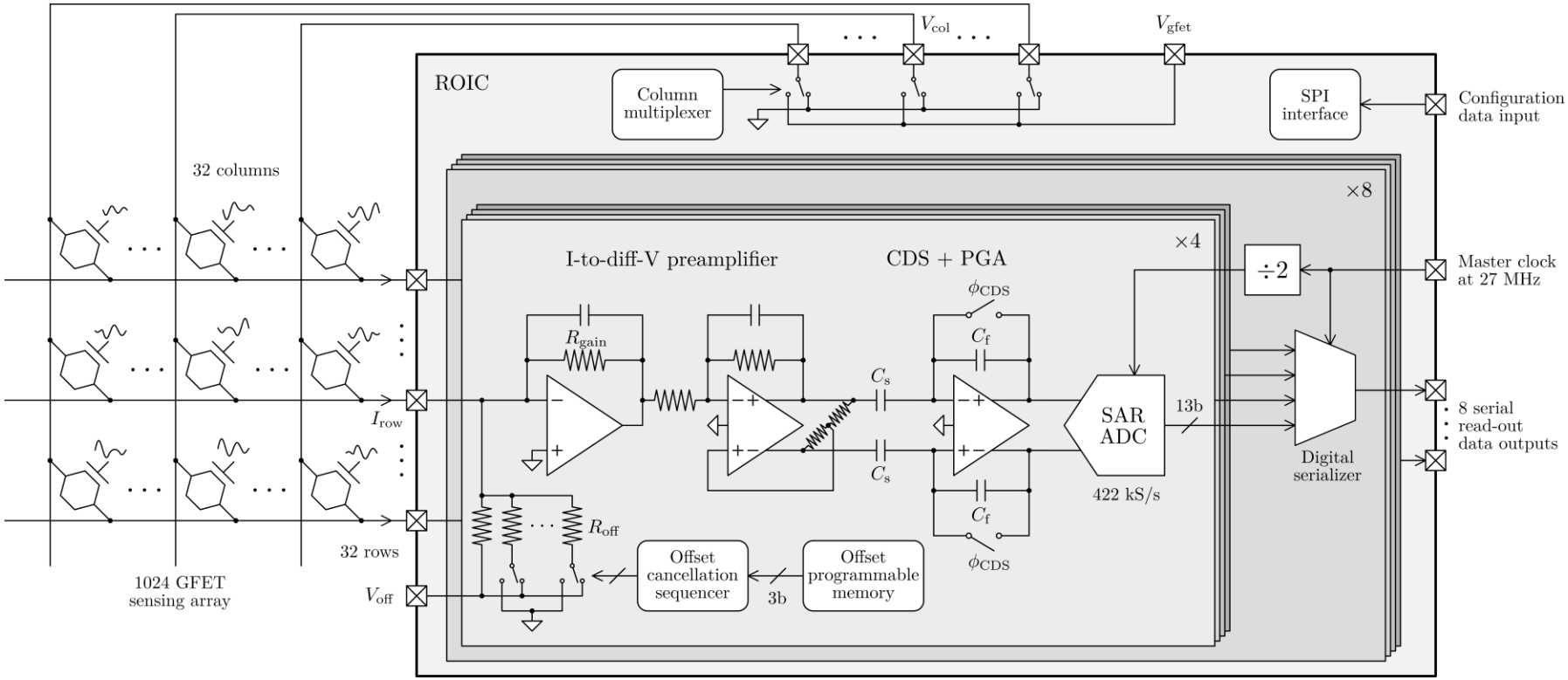
▼ **GFET + Switch** Technology integration

▲ At any time only **one device connected per row**

▲ **On-chip** cmos **switch** for multiplexing

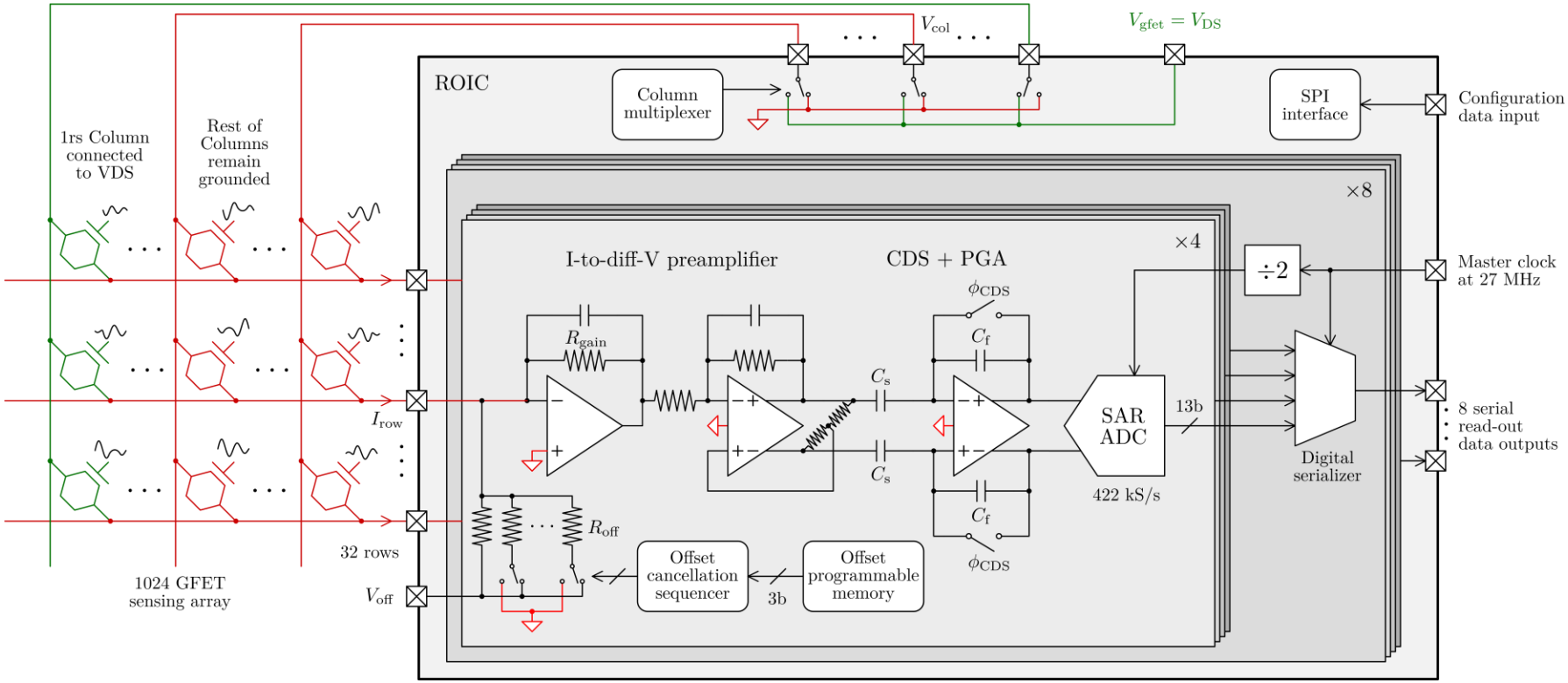
▼ **Pre-Amplifier Noise Figure Loss due to GFET permanent connection**

Architecture



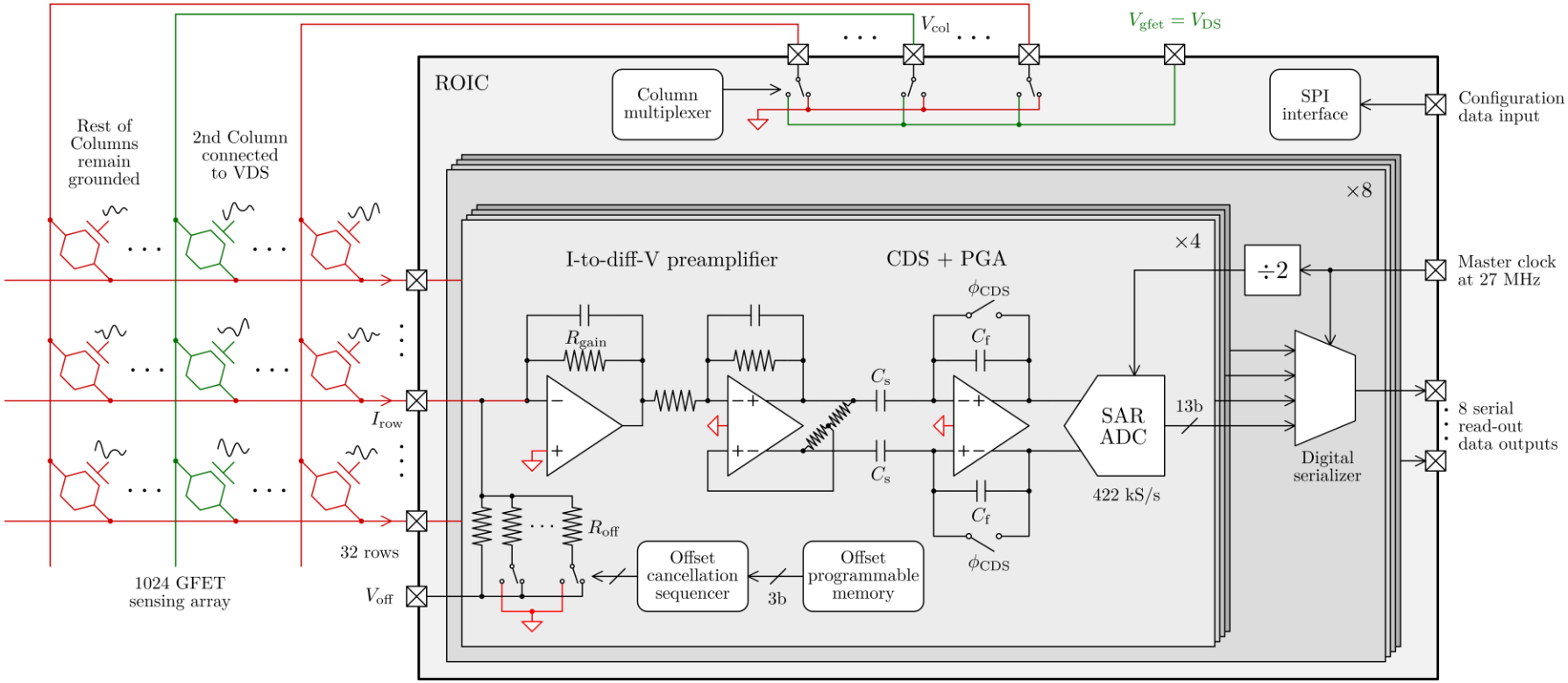
- **On-Chip** cmos **switch**
- **Transimpedance** Amplifier (R_{GAIN} = 25 kOhm)
- **Offset Cancellation 3-Bit R-DAC**
- **Single-to-Differential Amplifier**
- **Programable Gain Amplifier + CDS**
- **SAR ADC 10 Bit ENOB**

Operation



- **Channel multiplexing** controlled **by changing V_{DS}** of selected column
- **One Column** selected **at a given time (array power consumption** limited to **32 GFETS)**
- **Remaining Columns** biased to **ground by** the respective **Transimpedance amplifier**

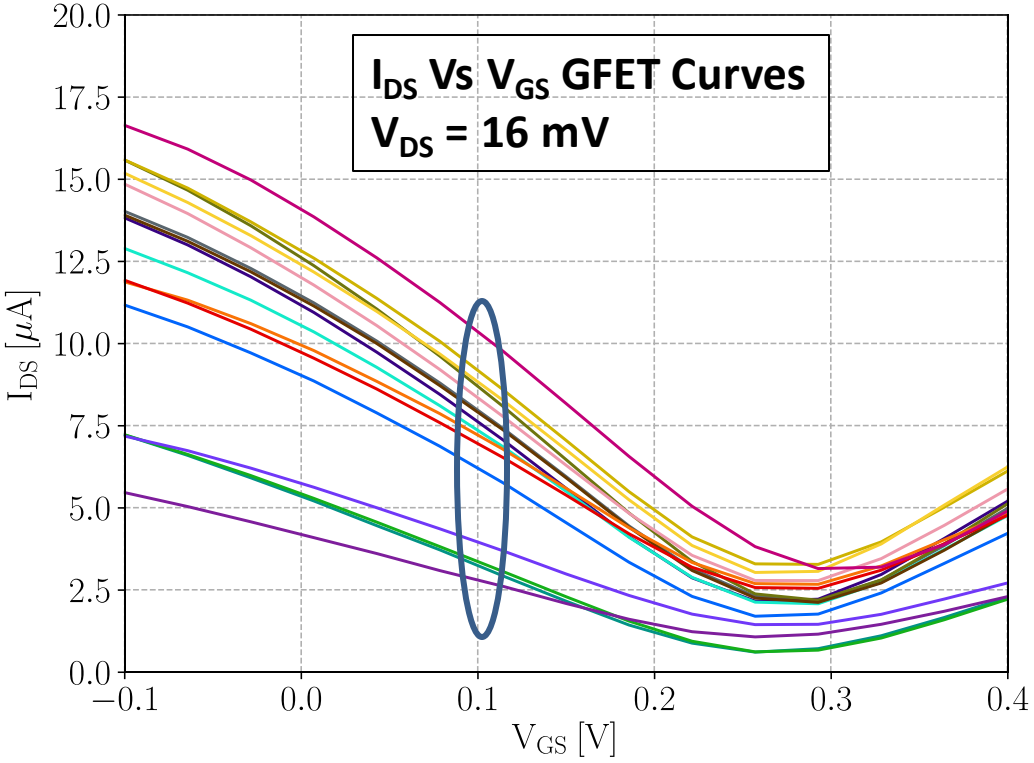
Operation



Two Challenges:

- **AFE Noise figure loss** due to GFET Up-Scaling
- **GFET R_{DS}** variability and **DC Offset**

DC Offset Cancellation

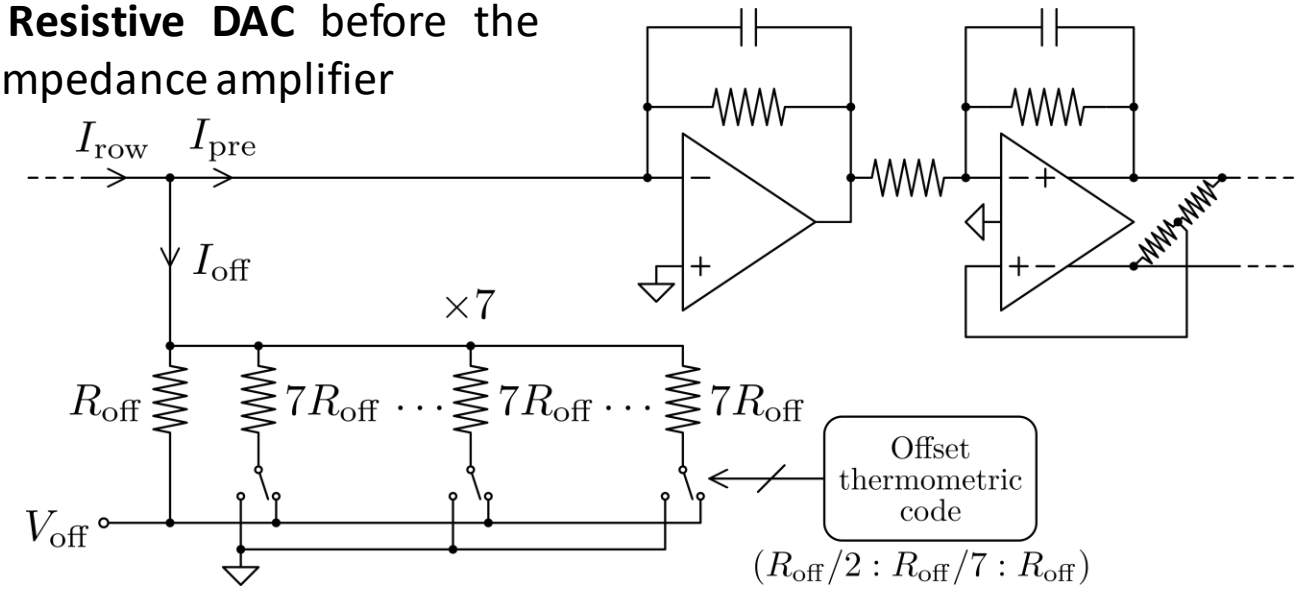


- **ROIC** is a **Fully DC coupled** adquisition system **with limited Input Full-Scale of 20 uA**
- **DC Offset: GFET R_{DS} = 2 kΩ** and a **V_{DS} = 100mV** a current of **50 µA** is expected
- **Bio-Signal**: **GFET G_m = 0.1 mS** and **V_{GS} = 10 mV** a maximum input current of **1 µA** is expected

- **Trade-Off: High Transresistance** needed for **Bio-Signal amplification but DC Offset** must be **cancelled to avoid saturation**

DC Offset Cancellation

- **3-Bit Resistive DAC** before the transimpedance amplifier



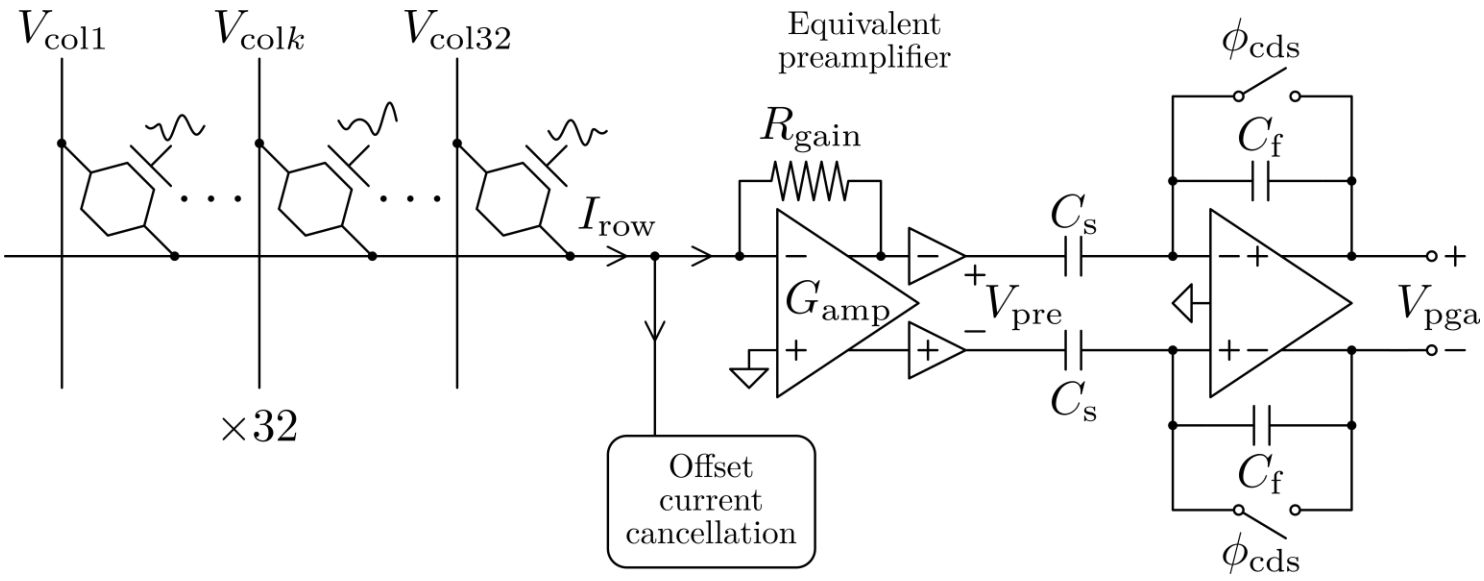
- **Prevents saturation** by subtracting the corresponding DC Current
- **Covering** a **mismatch** of **±30% on 5% Steps** from the Typ. 2 kΩ GFET
- **Individual** Offset **cancellation** configuration **for** each **recording site (Offset configuration map)**

CDS + PGA

- **Transimpedance noise figure loss** due to GFET permanent connection

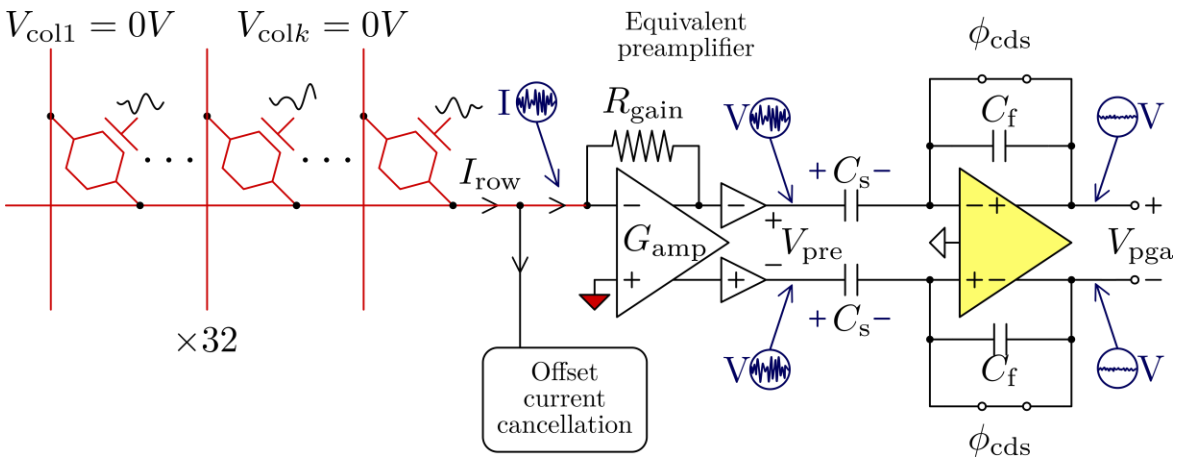
$$\mathrm{NTF} = \frac{1}{1+G_{\mathrm{amp}}H} \sim \frac{1}{G_{\mathrm{amp}}H} \quad \mathrm{H} = \frac{R_{\mathrm{gfet}}/32}{R_{\mathrm{gfet}}/32+R_{\mathrm{gain}}} \simeq \frac{1}{32}\frac{R_{\mathrm{gfet}}}{R_{\mathrm{gain}}} \simeq \frac{1}{400}$$

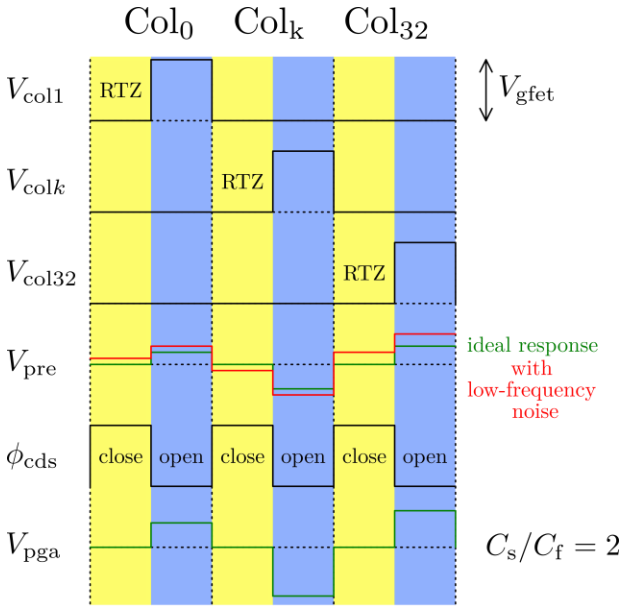
- **Analog-Front-End**



CDS + PGA

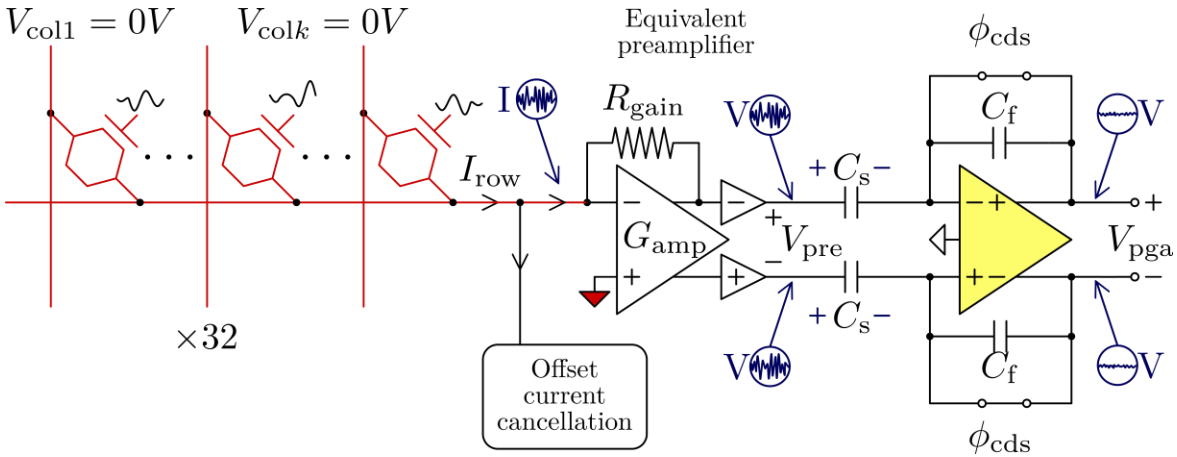
- **Return-to-Zero Phase**



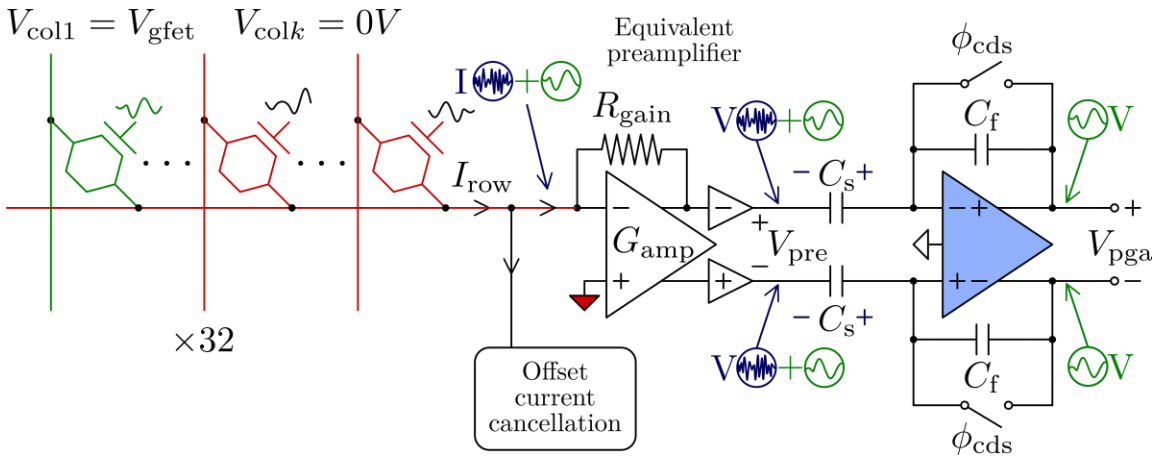


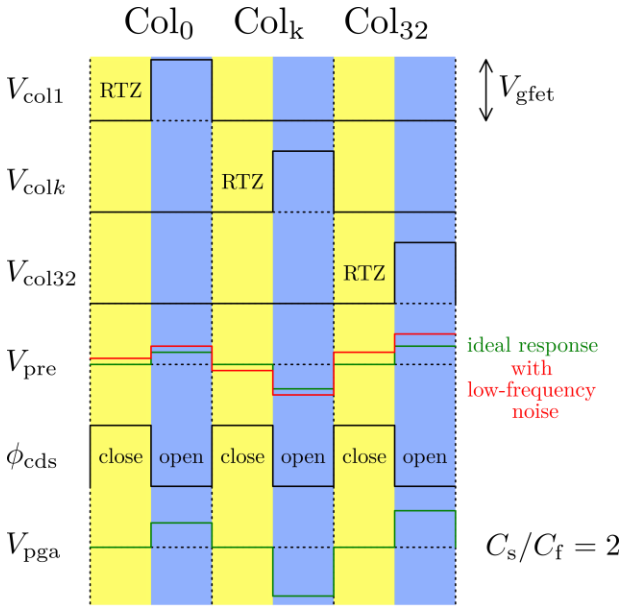
CDS + PGA

Return-to-Zero Phase



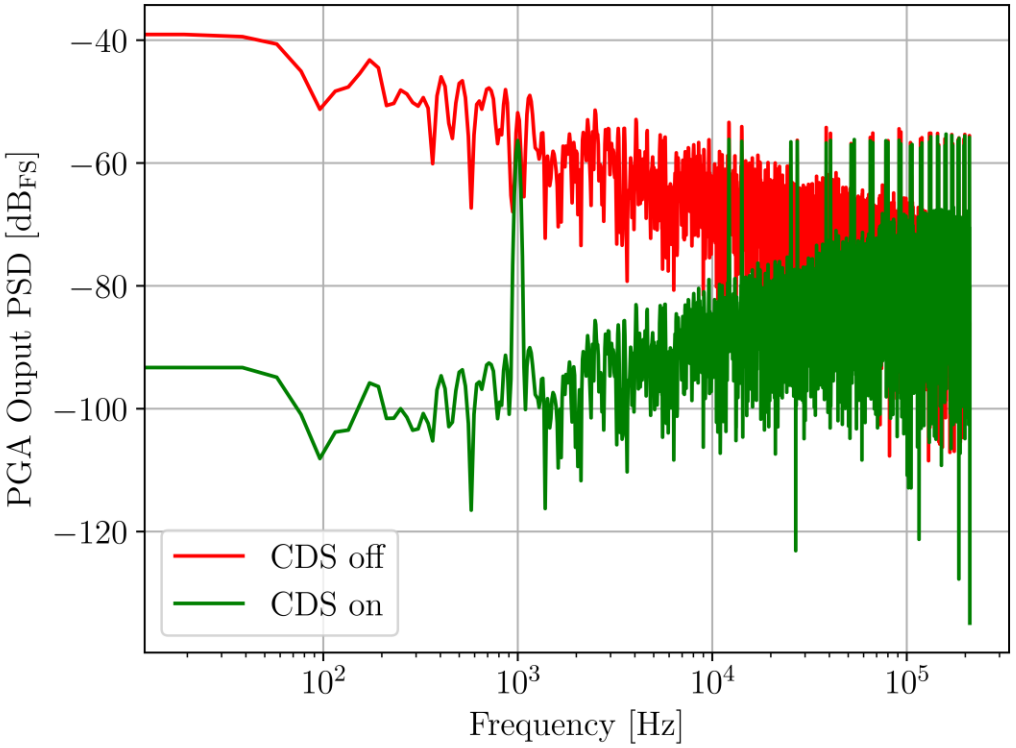
Amplification Phase





CDS + PGA

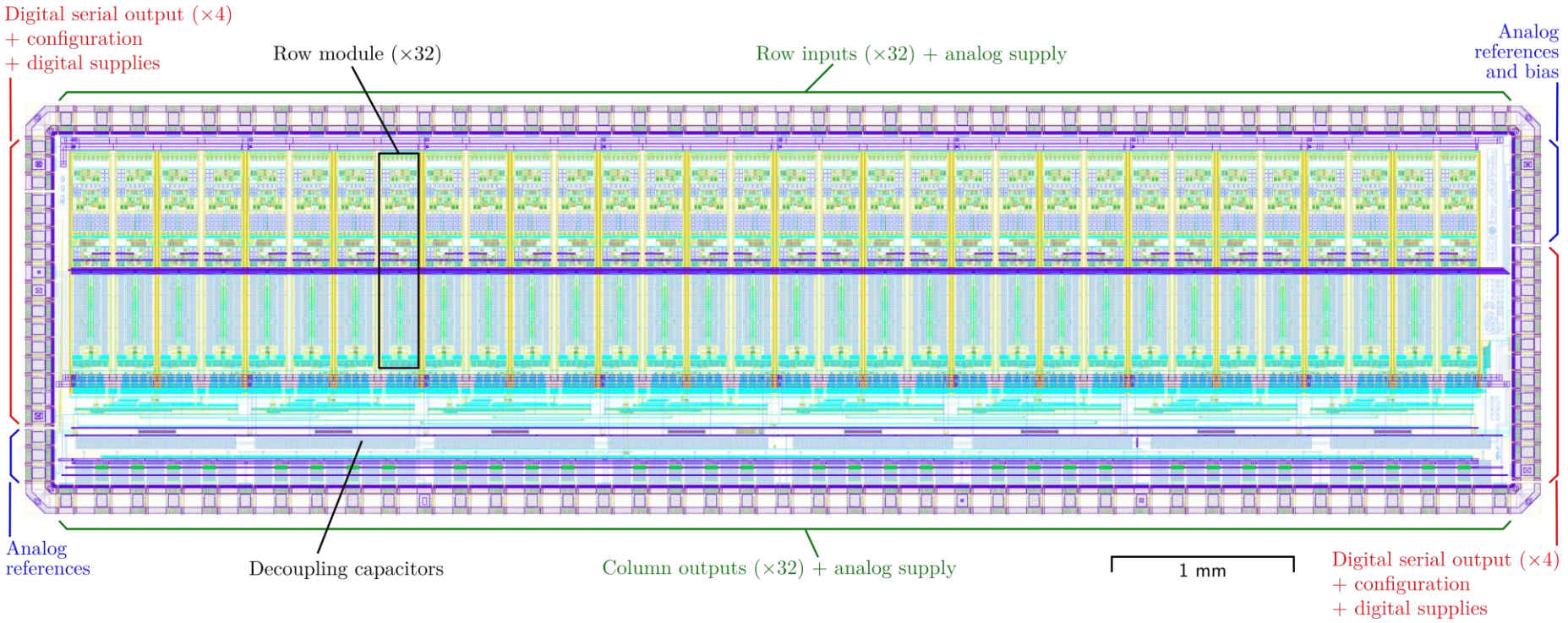
- **CDS PSD**



- **Low-Frequency Noise** from AFE **cancelled**
- **Overall AFE still DC Coupled**
- **CDS circuit reuses the discrete Switched-Capacitor PGA stage**

Chip

▲ **18.1 mm² ASIC** Integrated in **1.8V 0.18 µm 1P6M MIM XFAB**



Chip

1024-CHANNEL ROIC POST-LAYOUT SIMULATION RESULTS.

Parameter		Value	Units
Row preamp	transresistance	25	kΩ
	equiv. input offset	< 1	mV_{rms}
Row PGA	voltage gain	2 / 4 / 8 / 16	-
	CDS output noise	< 2	mV_{rms}
Row ADC	diff. full scale	2	V_{pp}
	sampling rate	422	kS/s
	per channel	13.2	
	dynamic range	13	ENOB
Digital I/O	input	1	SPI
	output	8	serial
	speed	27	Mbps
Supply	voltage	±0.9	V
	analog ref.	±0.5	
Power consumption	preamplifier	800	μW
	PGA	260	
	SAR ADC	80	
	per channel	36	
Silicon area	chip	18.7	mm^2
	per channel	0.018	

- High Transresistance
- 4 PGA Gains (1 Decade)
- 2Vp-p Differential FS from 1.8 V
- 6.6 kHz Bandwidth/Ch
- 1 SPI for PGA gain configuration, Offset cancellation map and TDM column Scan
- Output Data rate 216 Mbps
- Power consumption 36 µW/Ch
- Area 0.018 mm^2/Ch

Conclusions

- **1024-channel** modular µECoG **ROIC with liquid-gate GFETs**
- **Novel multiplexing scheme with strong sensor-to-circuit connectivity reduction** for **low-cost** integration and **low-power** operation
- **Mixed-signal ROIC architecture** capable for **GFET mismatch** and preamplifier **noise figure loss compensation**

Thanks for your attention!

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