Switch-Less Frequency-Domain Multiplexing of GFET Sensors and Low-Power CMOS Frontend for 1024-Channel µECOG

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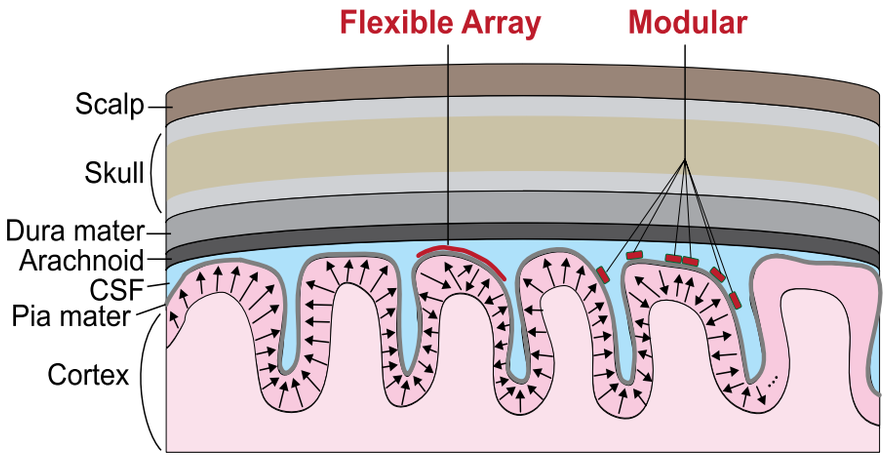
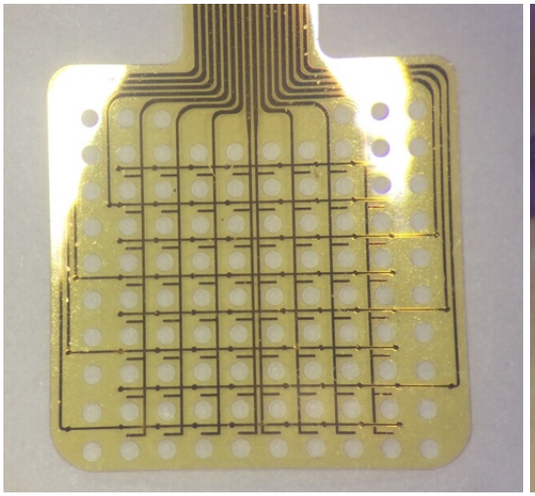
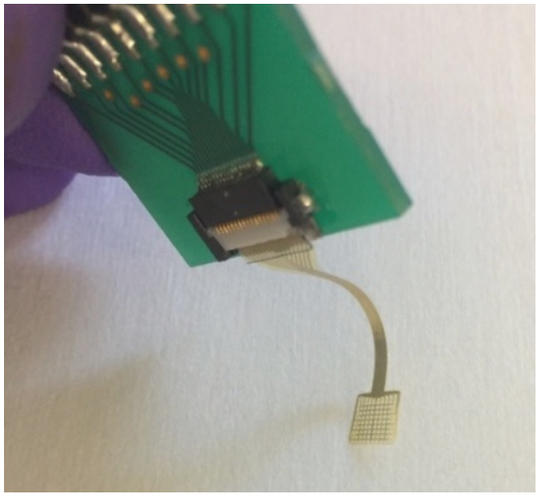
Introduction

- **Low-power** ICs with **massive** number of channels needed for **neural recording**
- **Monolithical** high density in small areas, **high** fabrication **cost** and **low scalability**.
- **Hybrid** (sensors+IC) device preferred for large sensing area, low cost, CMOS compatibility and flexible substrates = sensor **multiplexing**
- Liquid-gate Graphene field-effect transistors (**GFETs**) are good candidates for micro-electrocorticography (**µECOG**)

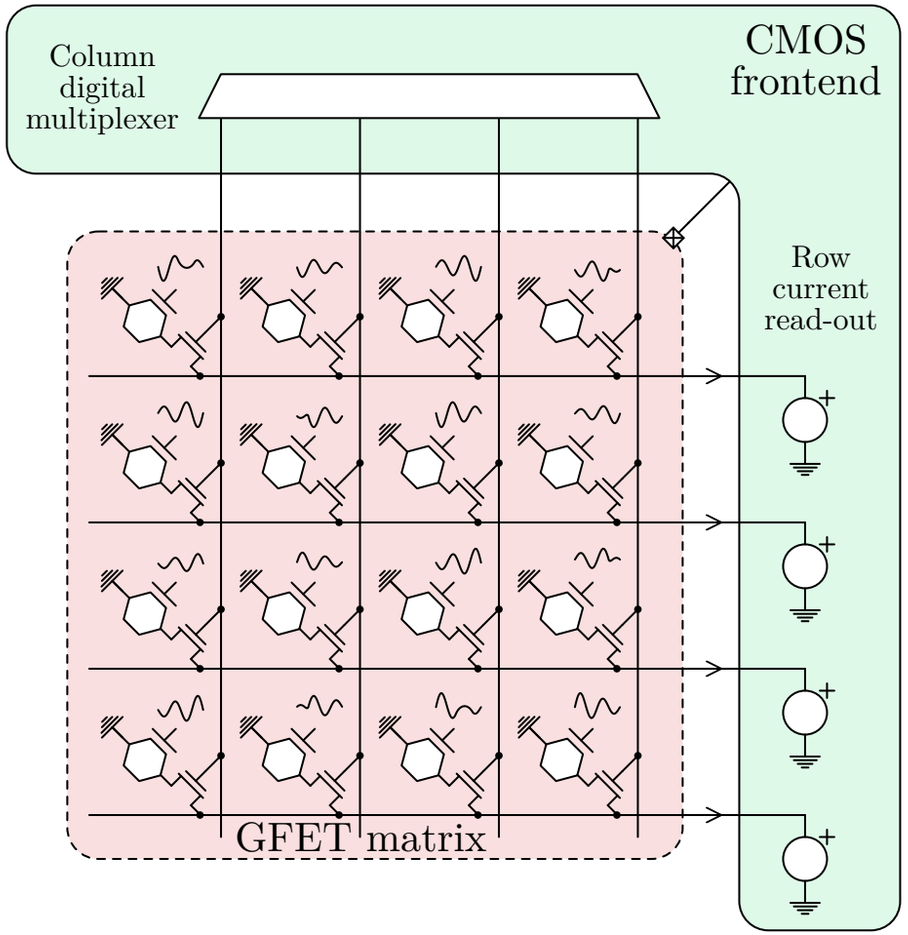






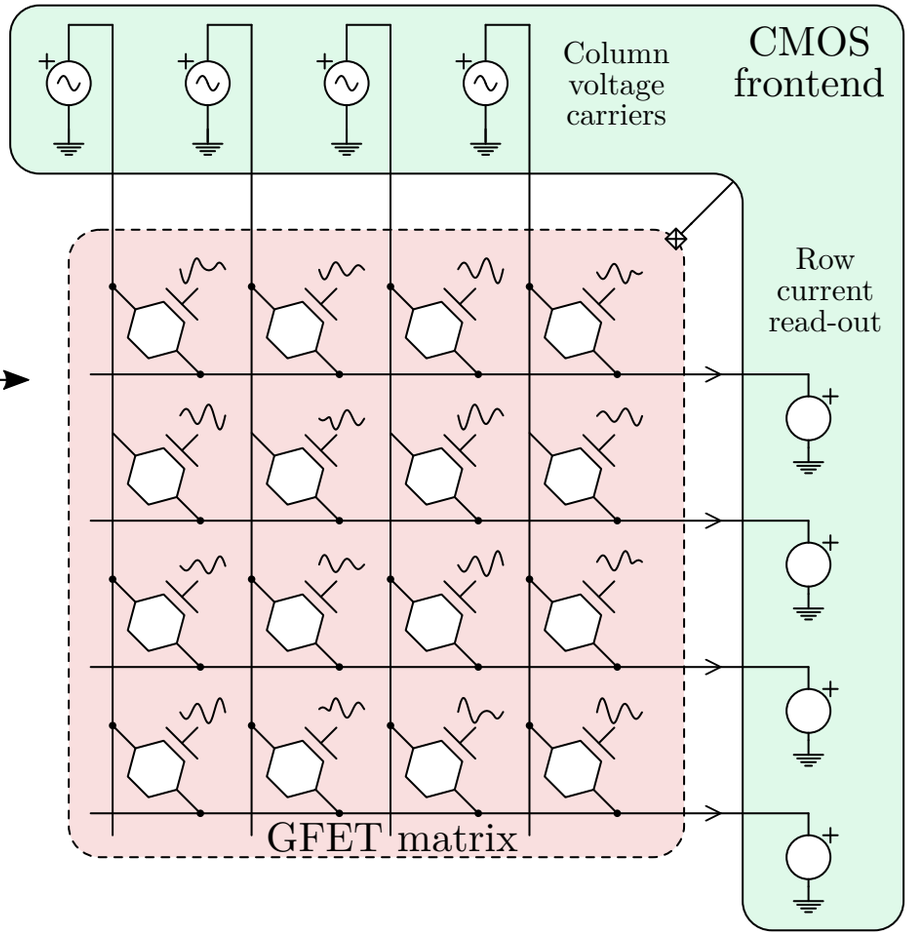
Frequency-Domain Multiplexing

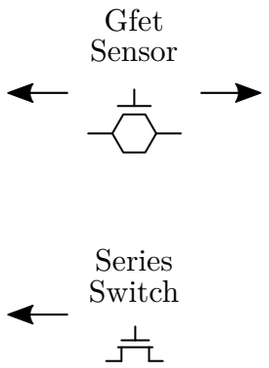
- Classic Time-Domain Multiplexing



- ▼ GFET + Switch technology integration
- ▼ GFET mismatch + transient operation
  =Multiplexing artifacs

- Frequency-Domain Multiplexing

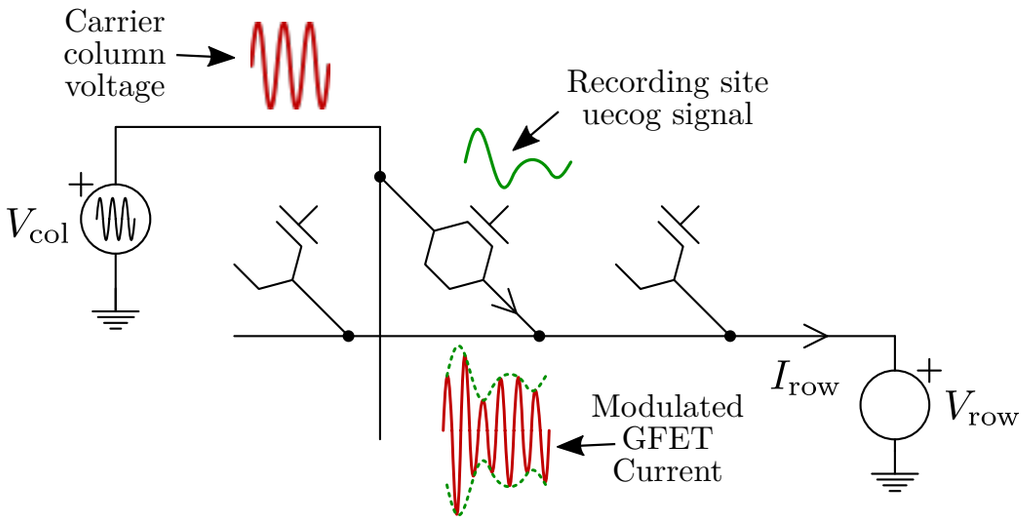




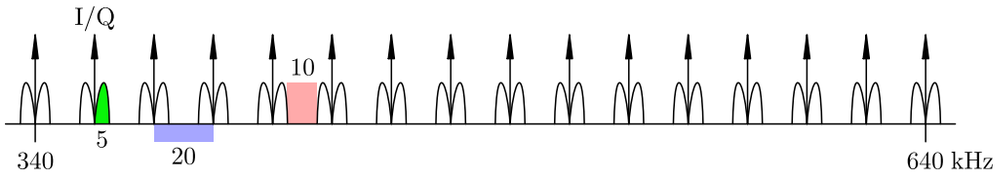
- Each **GFET** is permanently connected
- ▲ Switch-less and artifact-free

Frequency-Domain Multiplexing

- Each **GFET** is permanently connected and used as **transconductor+mixer**

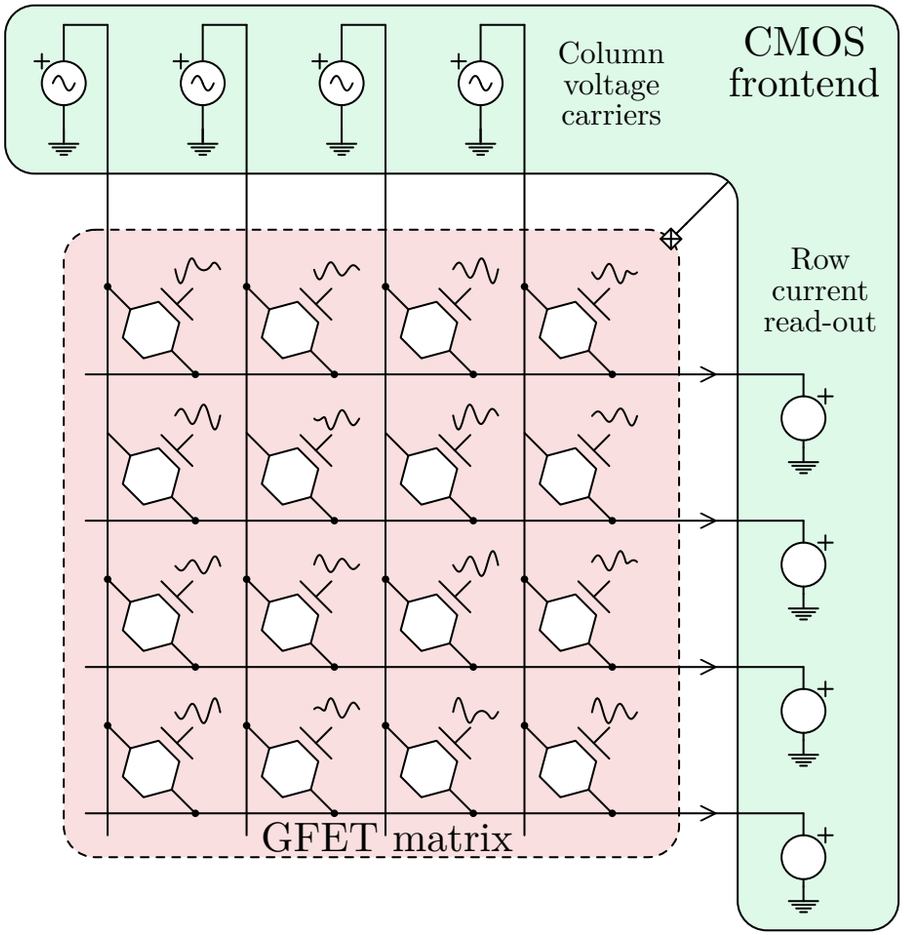


- **Irow** different channels frequency allocation



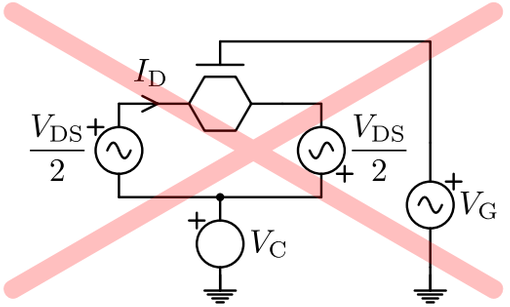
- Insensitive to CMOS **flicker** noise
- Low-noise **lock-in** demodulation

- Frequency-Domain Multiplexing

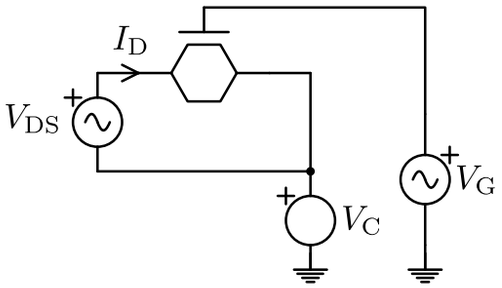


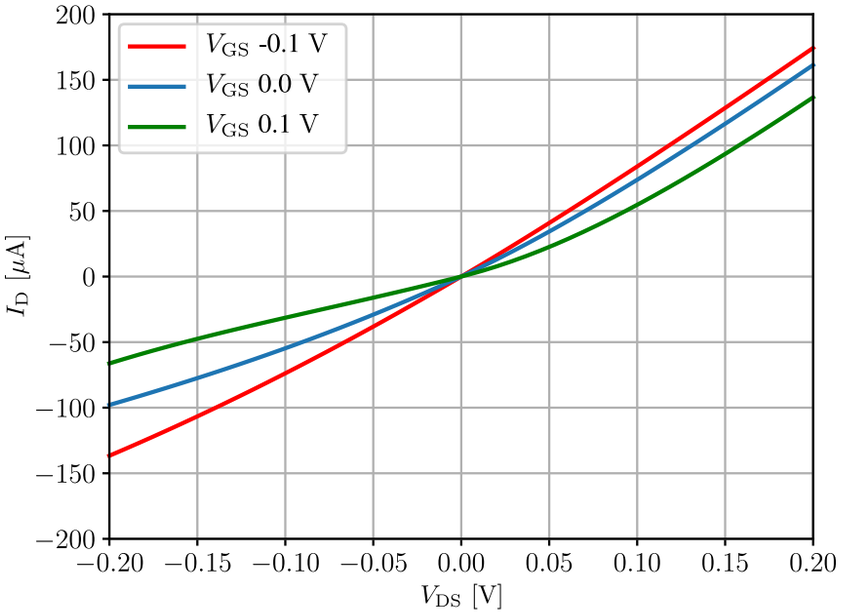
Frequency-Domain Multiplexing

Symmetrical operation



Asymmetrical operation





- GFET **asymmetrical** operation generates odd and even harmonics:

$$I_D|_{V_{G0}} \simeq G_{out}\left(V_{DS} + c_2 V_{DS}^2 + c_3 V_{DS}^3 + \cdots\right)$$

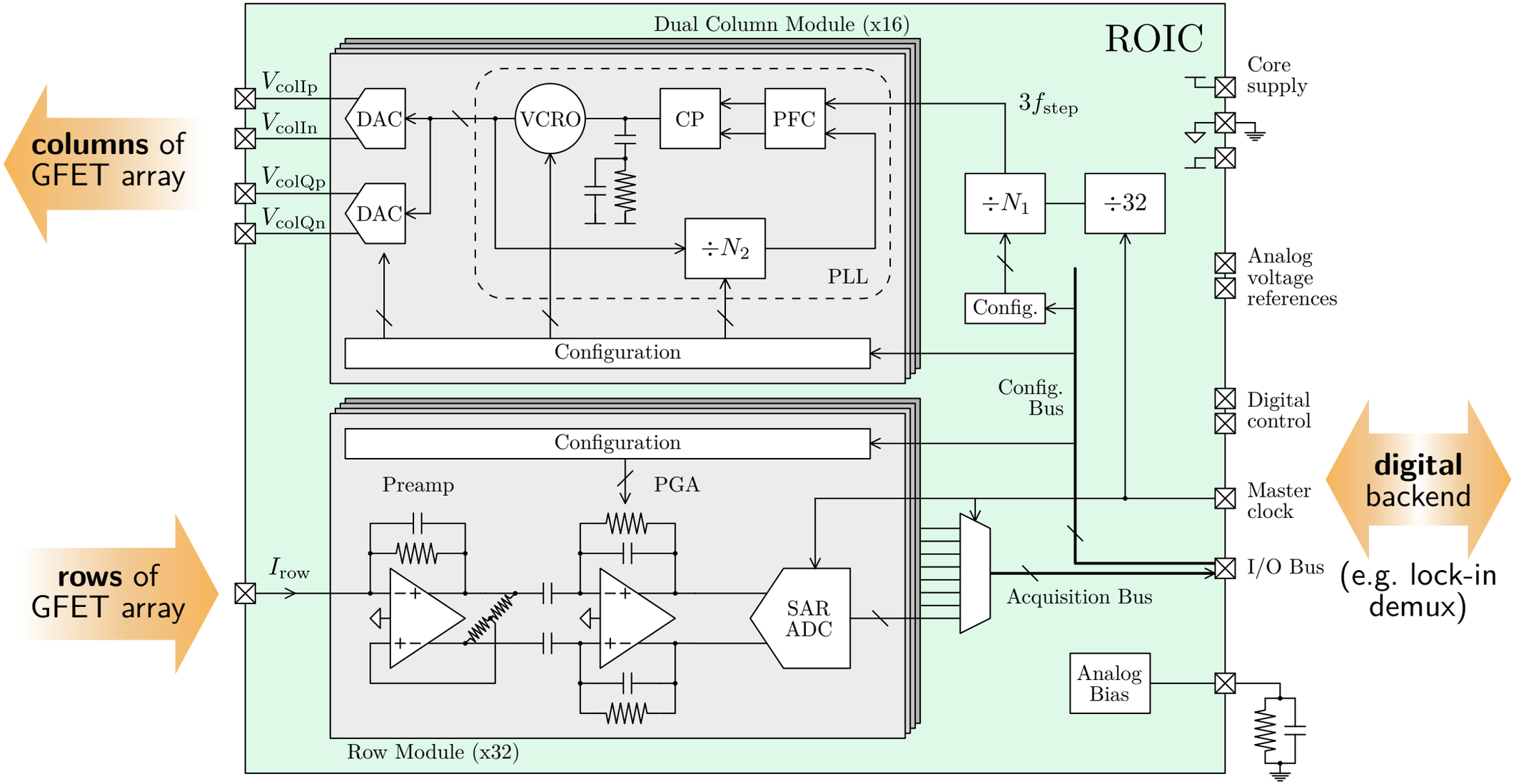
- FDM carrier **pre-distortion** to promote second-harmonic cancellation:
  - \+ Calibration not needed
  - \+ Compatible with I/Q generation

$$V_{col} = V_0\left[\sin(w_c t) + a_3 \sin(3 w_c t)\right]$$

I_{row}	DC	w_c	$2w_c$	$3w_c$	$\cdots$
$a_3 = 0$	$\frac{1}{2}c_2$	$1 + \frac{3}{4}c_3$	$-\frac{1}{2}c_2$	$-\frac{1}{4}c_3$	$\cdots$
$a_3 = \frac{1}{2}$	$\frac{5}{8}c_2$	$1 + \frac{3}{4}c_3$	0	$\frac{1}{2} - \frac{29}{32}c_3$	$\cdots$

1024-Channel ROIC Architecture

- **Modular** and **scalable** read-out IC (**ROIC**) for 32x32 GFET sensory arrays:



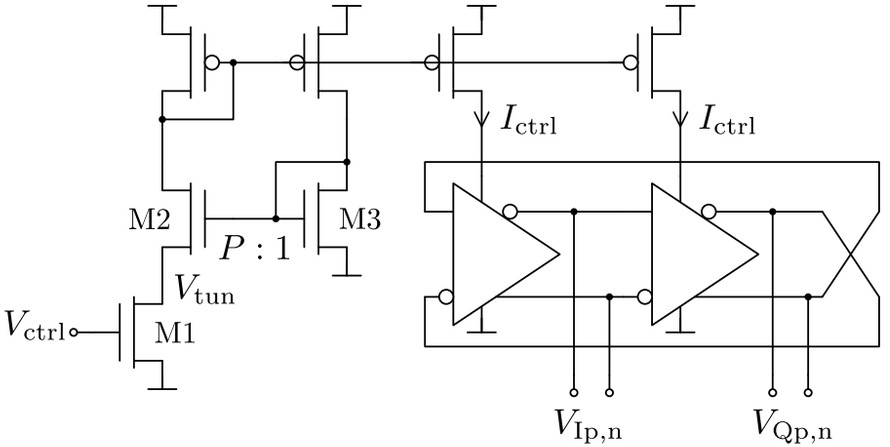
1024-Channel ROIC Architecture

- ROIC **specifications** from functional model in Scientific Python:
- ▲ Recording of local field potentials (**LFPs**) and high-frequency **spikes**
- ▲ Highly **configurable** to cover GFET process corners
- ▼ Main design **trade-offs** at system level:
  - \+ FDM freq. allocation vs GFET bandwidth
  - \+ FDM carrier amplitude vs GFET array power
  - \+ Row ADC sampling rate vs channel aliasing
  - \+ Row ADC DR vs number of array columns

Parameter		**Value**	**Units**
Array size		32×32	Ch
Channel	bandwidth	DC to 5	kHz
	full scale	5	mV
	resolution	5	μV
	dynamic range	60	dB
Col. FDM	I/Q carrier freq.	340 : 20 : 640	kHz
	guard spacing	10	kHz
	carrier amp.	10 to 50	mV_p
Row ADC	sampling rate	$\geq$ 1.6	MS/s
	dynamic range	$\geq$ 12	ENOB

Linear VCRO with Symmetrical Propagation Delay

- Two-stage current-starved voltage-controlled ring oscillator (**VCRO**) for the column PLL
- Quadrature (**I/Q**) generation



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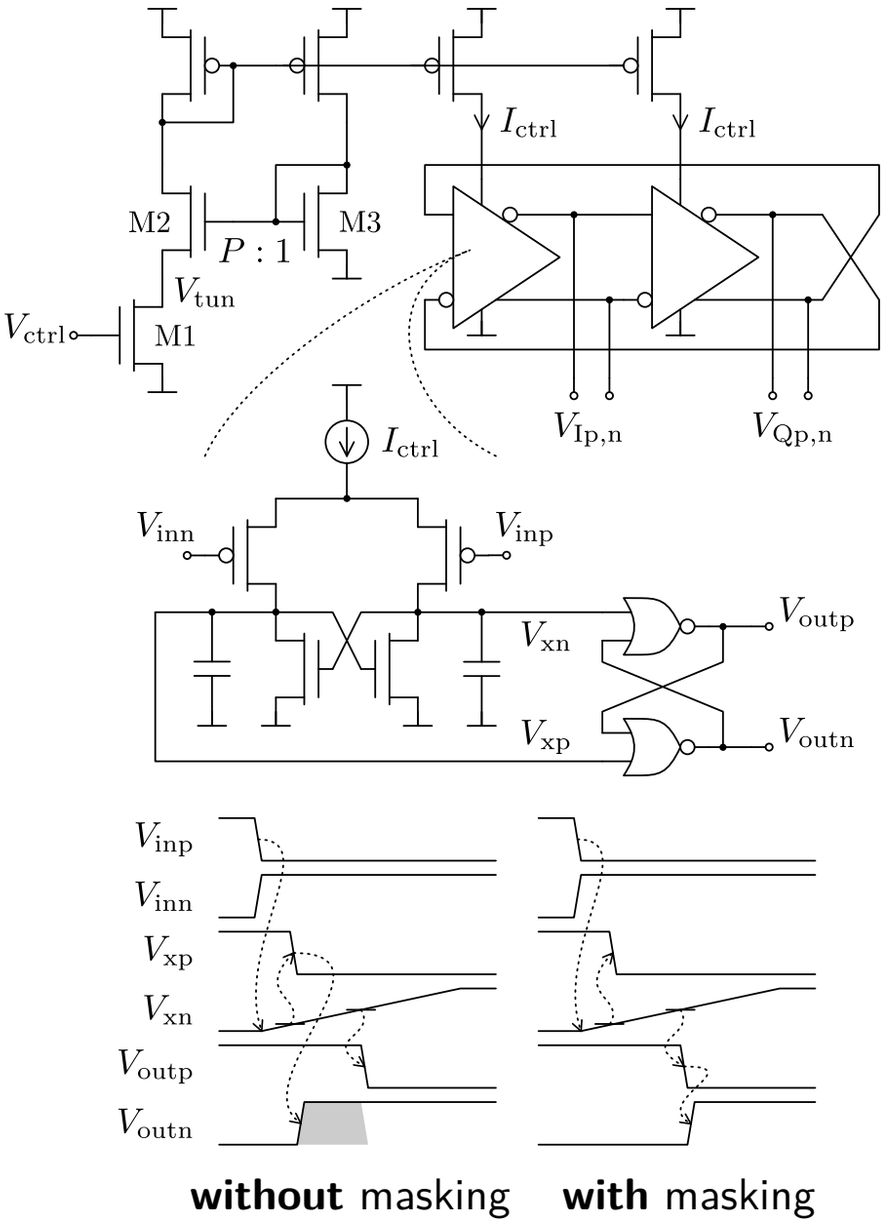
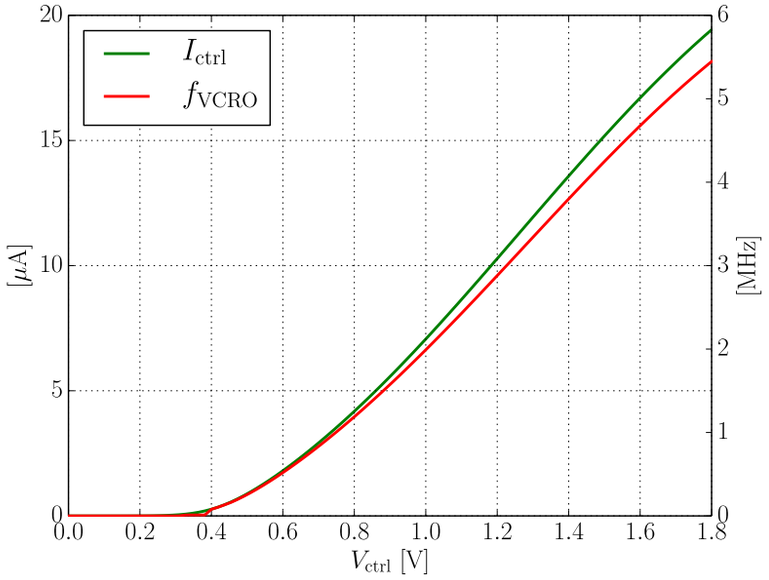
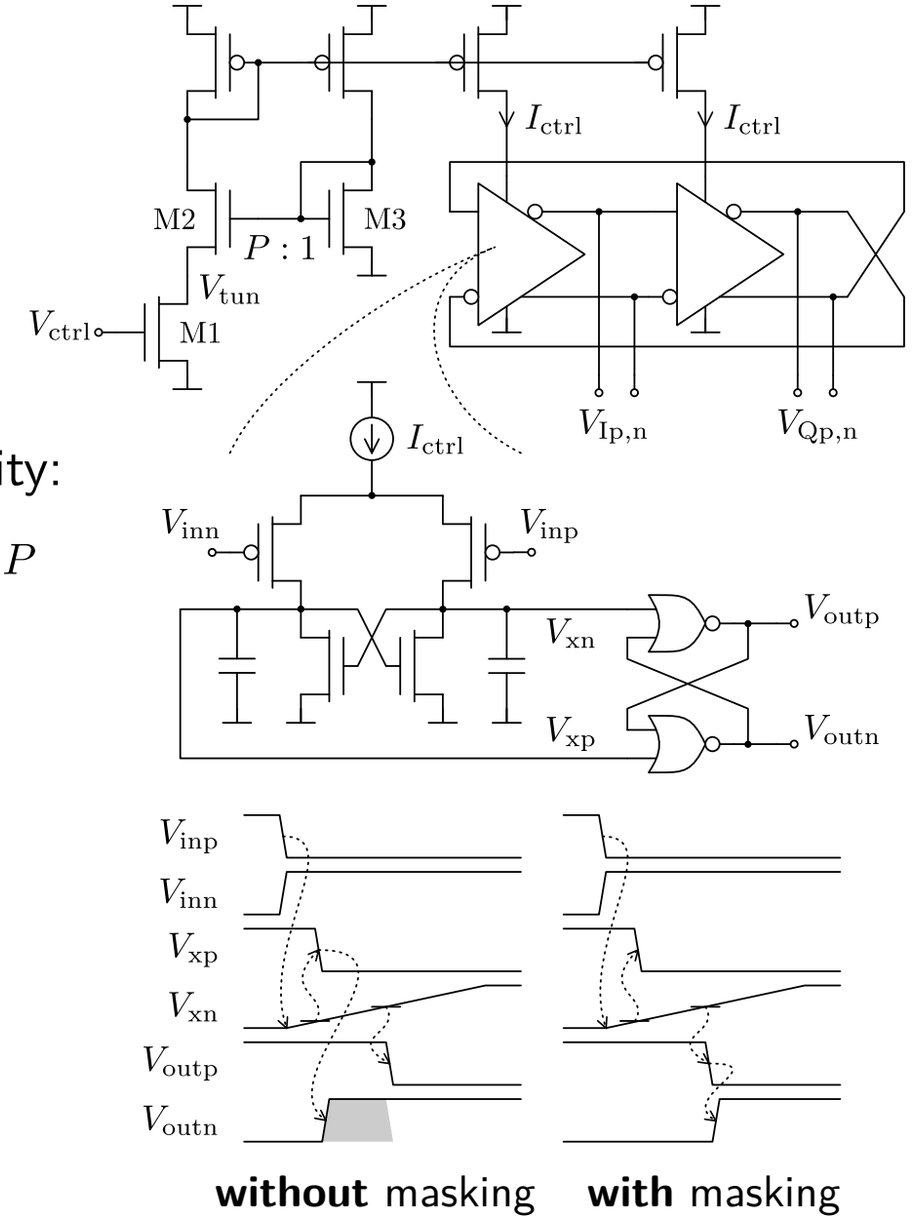


Linear VCRO with Symmetrical Propagation Delay

- Two-stage current-starved voltage-controlled ring oscillator (**VCRO**) for the column PLL
- Quadrature (**I/Q**) generation
- **Symmetrical** propagation delays by the addition of logical masking
- **Linear** V/I conversion to improve PLL stability:

$$I_{\text{ctrl}} = \beta_1 \left(V_{\text{ctrl}} - V_{\text{TH1}} - \frac{n}{2} V_{\text{tun}} \right) V_{\text{tun}} \quad V_{\text{tun}} = U_t \ln P$$

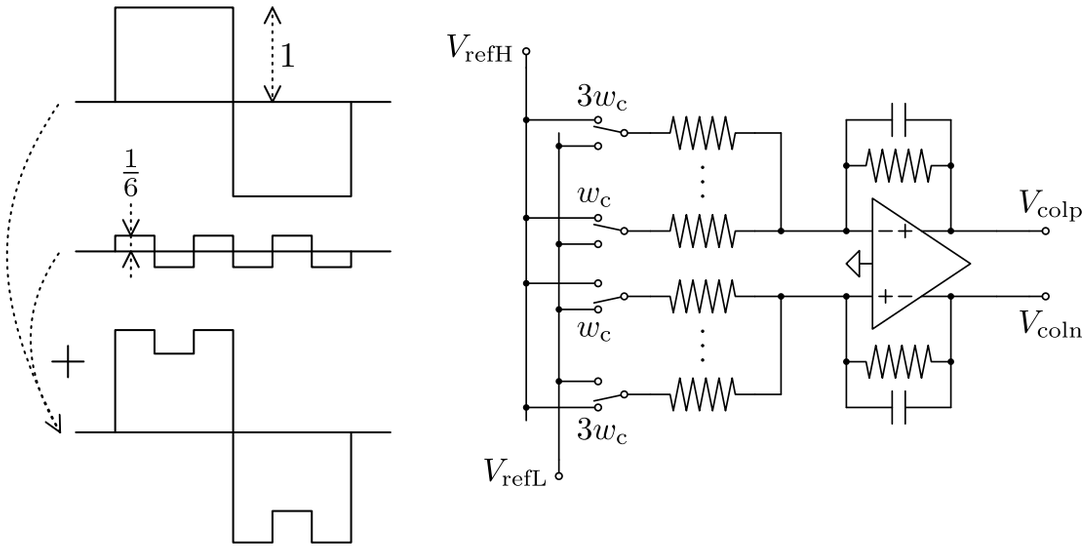




FDM Carrier DAC with Class-AB Column Driver

- Each PLL generates **I/Q square** waveforms at the FDM frequency $\mathbf{w_c/2\pi}$ and $\mathbf{3w_c/2\pi}$
- Synthesis of carrier **pre-distortion**:

$$\sqcap\!\sqcup(t) = \sin(w_c t) + \frac{1}{3}\sin(3w_c t) + \cdots + \frac{1}{k}\sin(kw_c t)$$



$$V_{colp}(t) = \sin(w_c t) + \frac{1}{2}\sin(3w_c t) + \cdots$$

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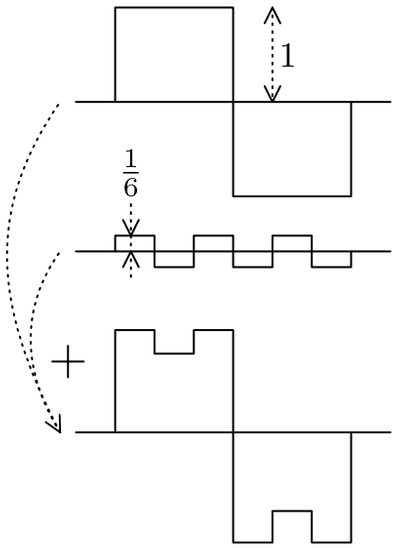
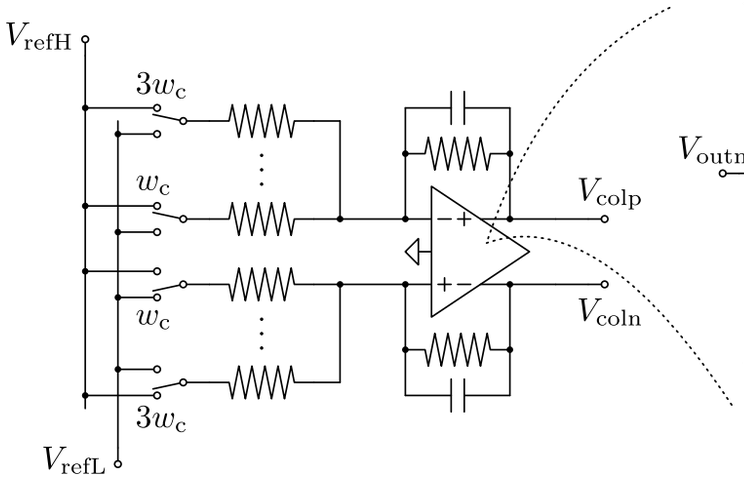
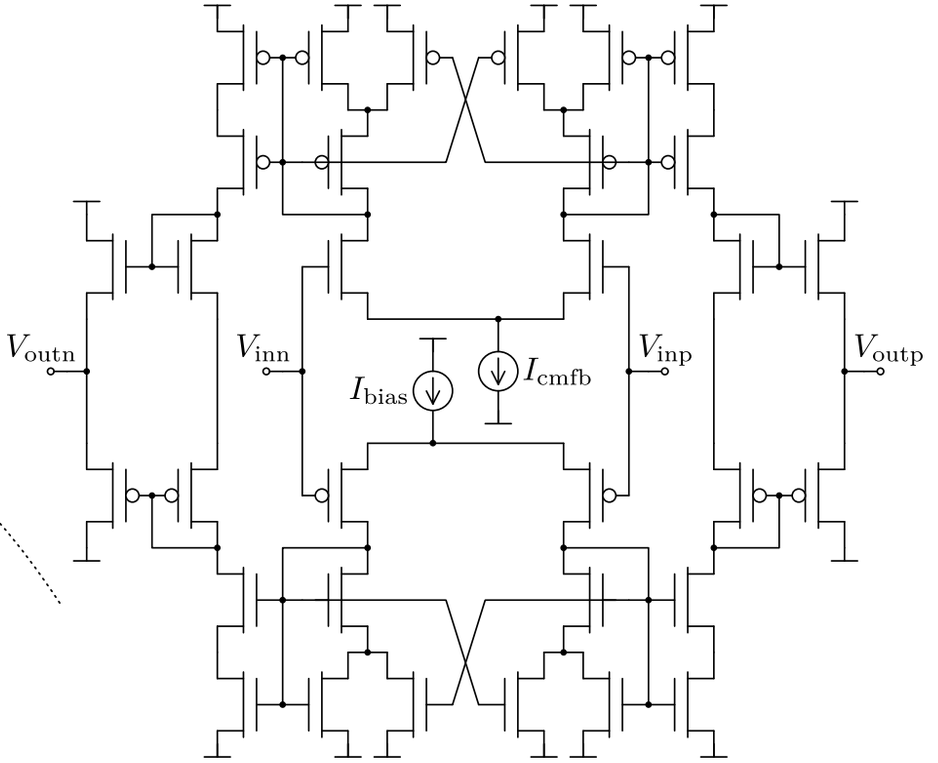




$$V_{colp}(t) = \sin(w_c t) + \frac{1}{2}\sin(3w_c t) + \cdots$$

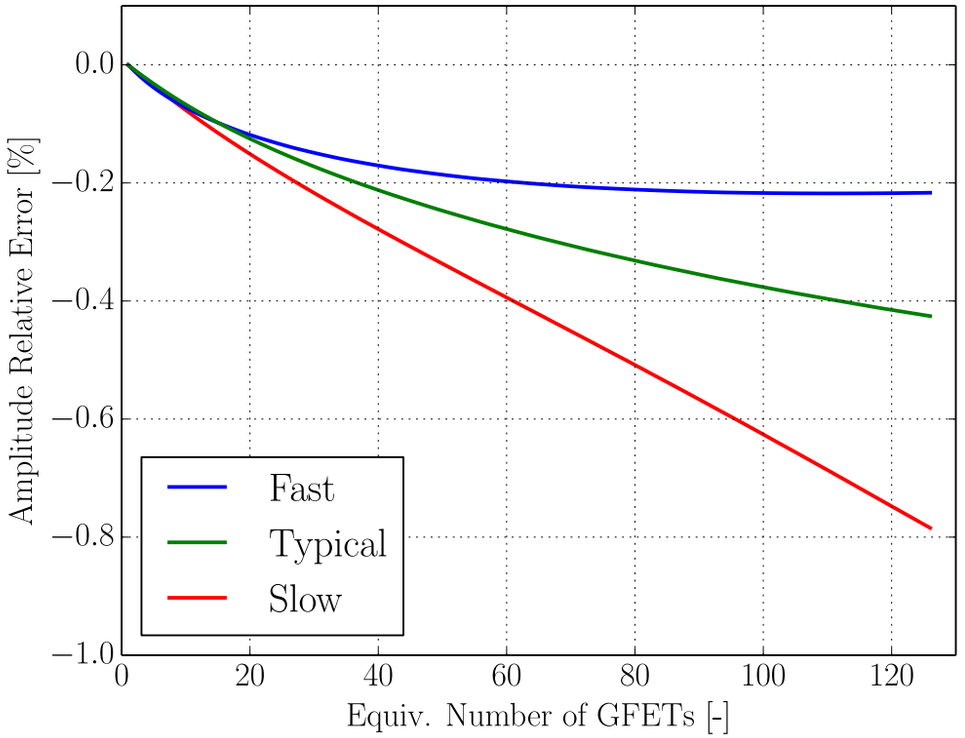
- Single-stage **Class-AB** variable-mirror amplifier (VMA):



+ Simple frequency compensation
+ Low PVT sensitivity

FDM Carrier DAC with Class-AB Column Driver

- Each PLL generates **I/Q square** waveforms at the FDM frequency $\mathbf{w_c/2\pi}$ and $\mathbf{3w_c/2\pi}$
- Synthesis of carrier **pre-distortion**
- Efficient V_{col} driving of the **low-impedance** (~60Ω) GFET array column:



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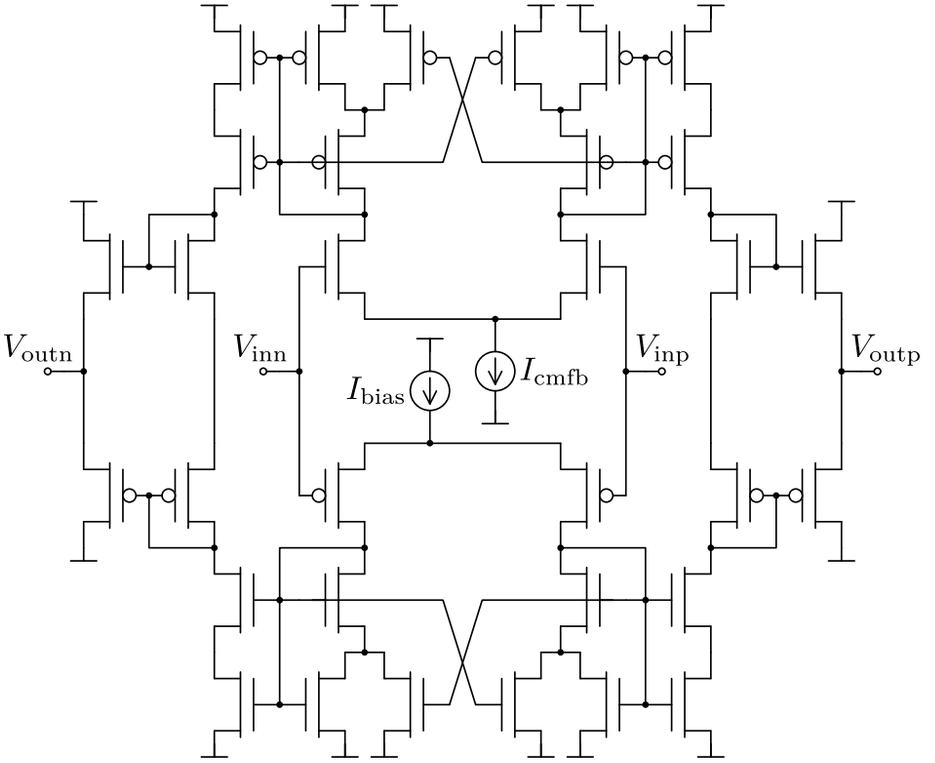

+ Simple frequency compensation
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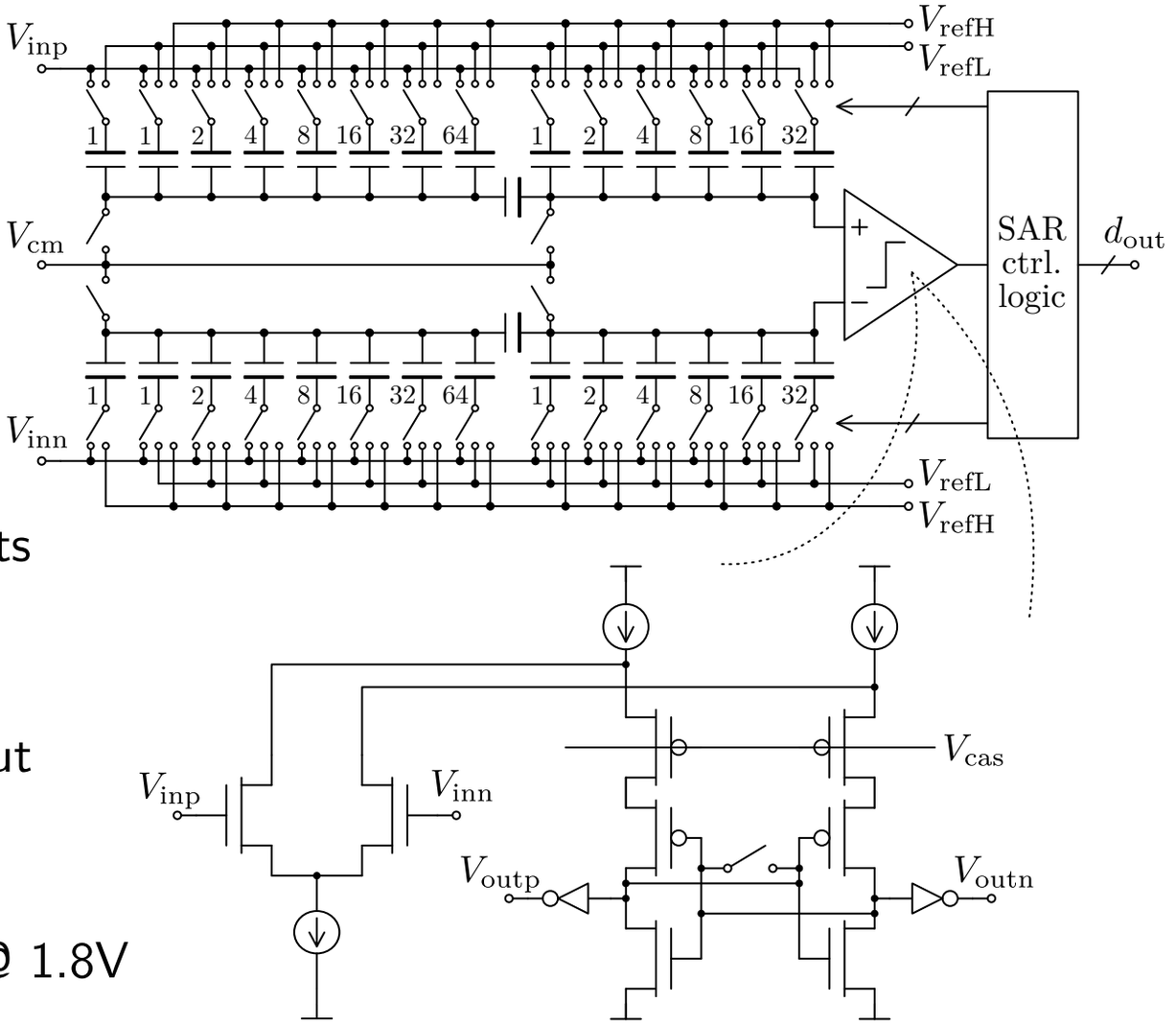
SAR ADC with Low-Kickback Comparator

- Segmented (6MSB+7LSB) **SAR ADC** for each array row:
  - \+ 2-V_{pp} differential full scale
  - \+ 60-fF unitary capacitor
  - \+ 1.8-MS/s sampling freq.

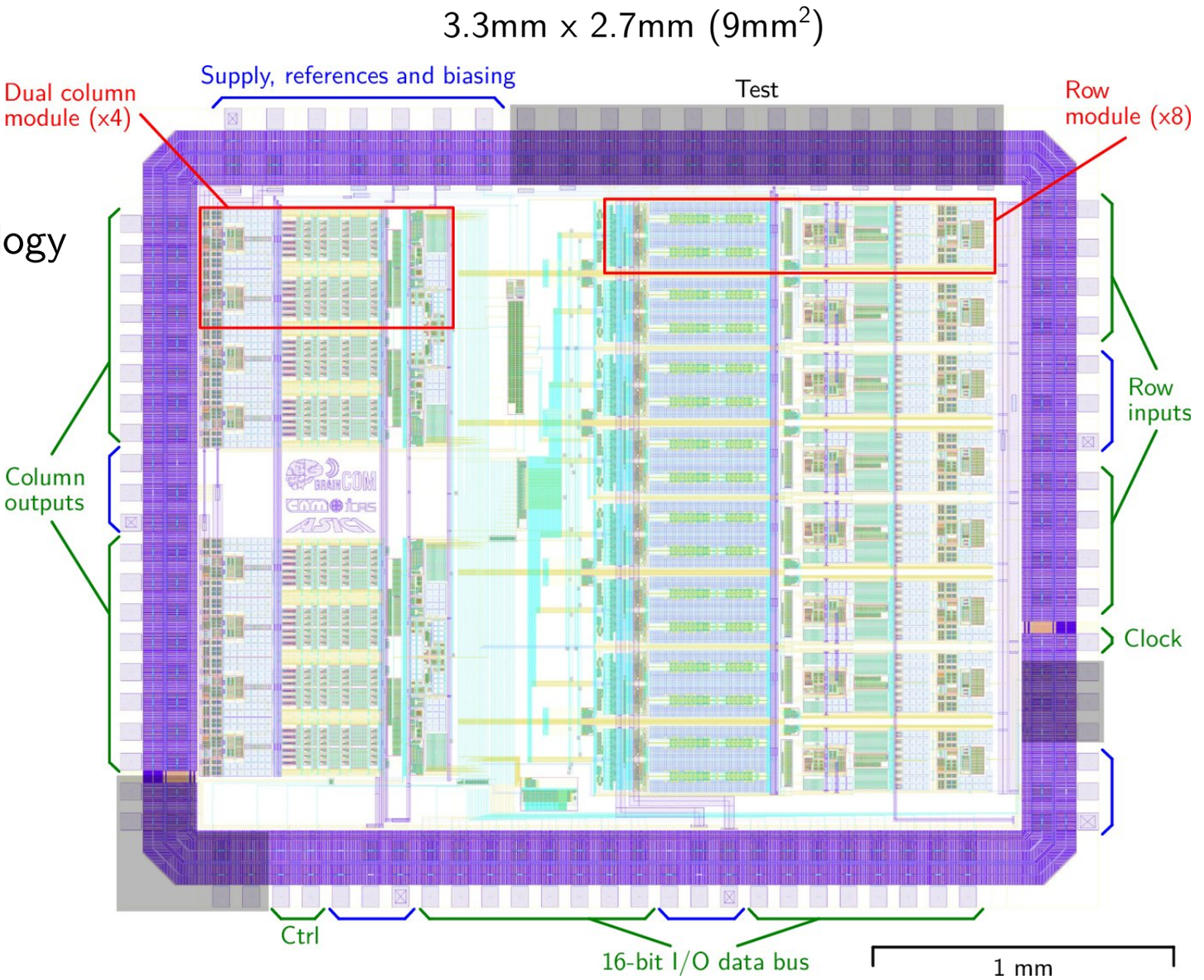
- **Low-power** operation usually allows kickback to reach high-impedance comparator inputs

- **Low kickback** can be achieved by combining folded cascode input and preset at metastability:
  - \+ 13-bit ENOB
  - \+ 125-µW power consumption @ 1.8V



Test Chip

- Integrated in 0.18-µm 6-metal CMOS technology
- To be tested with 8x8 GFET arrays
- 8x8 vs 32x32 ROIC = Num. of Modules



Test Chip

- Integrated in 0.18-µm 6-metal CMOS technology
- To be tested with 8x8 GFET arrays
- 8x8 vs 32x32 ROIC = Num. of Modules
- ▲ All CMOS building blocks designed for **1024-ch** specs
- ▲ In case of reducing system configurability, the **final ROIC** could be targeted for:
  - + < 50mW
  - + < 25mm^2

Parameter		**Value**	**Units**
Col. FDM	I/Q carrier freq.	340 : 20 : 640	kHz
		170 : 10 : 320	kHz
	carrier amp.	10 / 20 / 50 / 100	mV_p
Preamp	transresistance	5	kΩ
PGA	voltage gain	1 / 2 / 4 / 8	-
Row ADC	diff. full scale	2	V_{pp}
	sampling rate	1.8	MS/s
	dynamic range	13	ENOB
Master clock	frequency	27	MHz
Digital I/O	bus width	16	bit
Supply voltage	core circuits	±0.9	V
	pad ring	±1.65	
	analog ref.	±0.5	
Power consumption	PLL	32	µW
	DAC	648	
	Preamp	648	
	PGA	810	
	SAR ADC	125	
	total	70	µW/Ch
Silicon area		0.013	mm^2/Ch

Conclusions

- A **switch-lessartifact-free** frequency-domain multiplexing (**FDM**) of liquid-gate GFET sensors for large-scale µECOG
- **Flicker-freelock-in** channel demodulation in digital domain
- Modular read-out IC (**ROIC**) architecture for **1024 channels**
- Specific CMOS circuits for **low-power** operation
- An 8x8 **test chip** in 0.18-µm 6-metal CMOS technology

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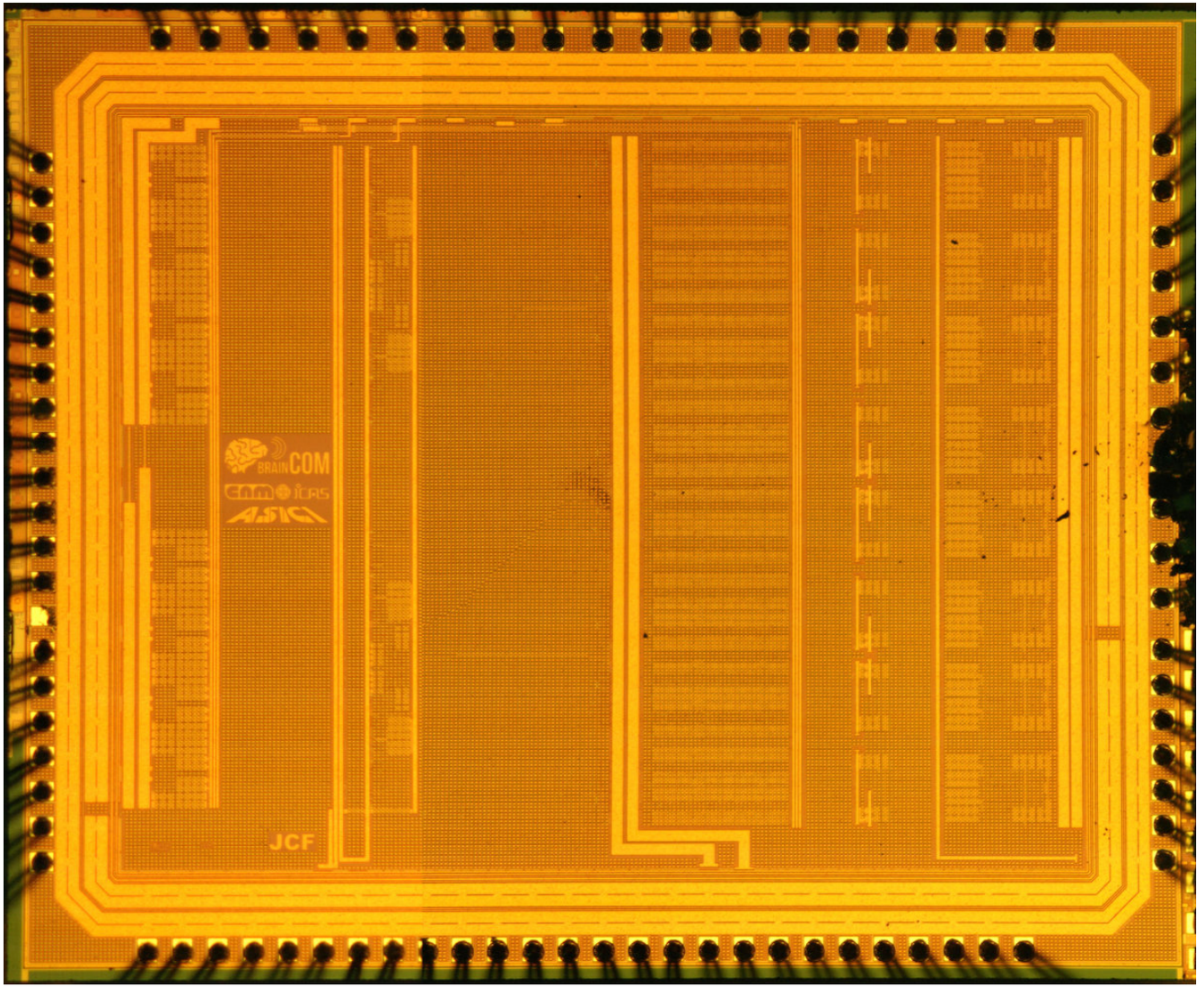
Conclusions

- To be tested in short...



Thanks for your attention!

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