A Compact Switched-Capacitor Multi-Bit Quantizer for Low-Power High-Resolution Delta-Sigma ADCs

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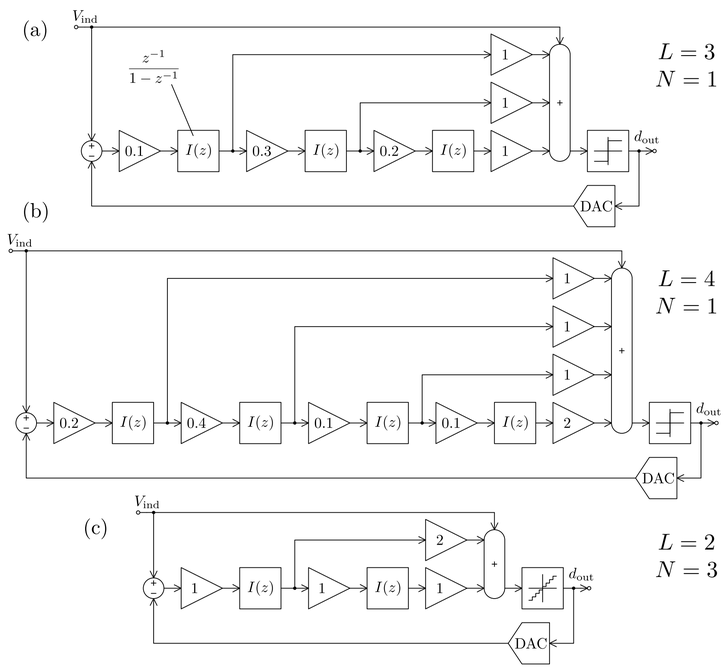
1 Introduction

- Reduced bandwidth (<1MHz) **high dynamic range** (>90dB) **ΔΣMs** for portable smart sensing
- **Power-aware** ΔΣM top-down design strategy?



Comparative examples of high-resolution single-loop ΔΣMs: single-bit third-order (a), single-bit fourth-order (b) and 3-bit second-order architecture (c).

2 ΔΣ Modulator Power Model

- **Min. dynamic power** consumption at the first integrator stage:

$$P_{\min} = \underbrace{C_{i1}\overline{|\Delta V_{out1}|}f_s}_{\overline{I_{DD}}} V_{DD} = \frac{C_{s1}}{a_1}\alpha_1 V_{DD}^2 \mathrm{OSR} f_{nyq}$$

+ state-signal **dynamics**: $\alpha_1 \doteq \dfrac{\overline{|\Delta V_{out1}|}}{V_{DD}}$

$$\mathrm{SNDR}_{peak}^{-1} = \mathrm{STNR}^{-1} + \mathrm{SQNR}^{-1}$$

$$\mathrm{STNR} = \frac{A_{peak}^2}{2}\frac{C_{s1}\,\mathrm{OSR}}{kT} = \frac{\alpha_{OL}^2 V_{DD}^2}{8}\frac{C_{s1}\,\mathrm{OSR}}{kT}$$

+ input full-scale **loss**: $\alpha_{OL} \doteq \dfrac{2A_{peak}}{V_{DD}}$

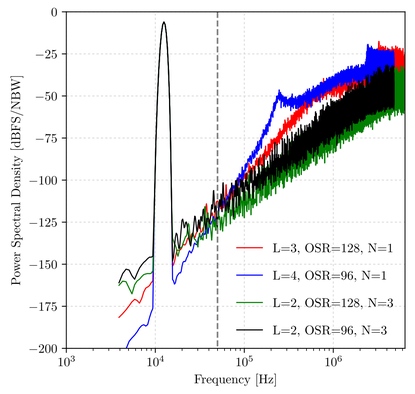
$$C_{s1} = \frac{8kT\,\mathrm{SNDR}_{peak}}{\alpha_{OL}^2 V_{DD}^2\,\mathrm{OSR}\,(1-\alpha_{QN})}$$

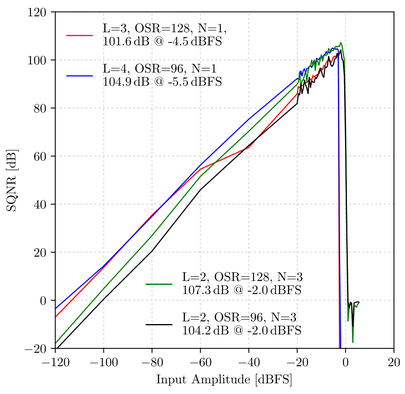
+ combined SNDR_{peak} **loss:** $\alpha_{QN} \doteq \dfrac{\mathrm{SNDR}_{peak}}{\mathrm{SQNR}} < 1$

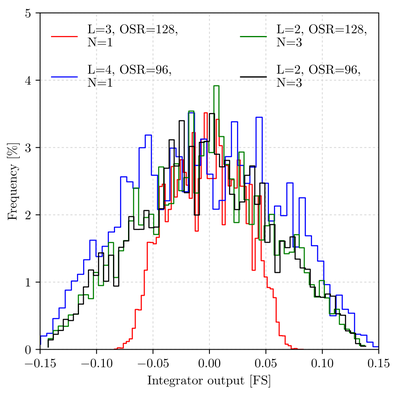
$$P_{\min} = \mathrm{SNDR}_{peak}\, f_{nyq}\, 8kT\, k_{mod}$$

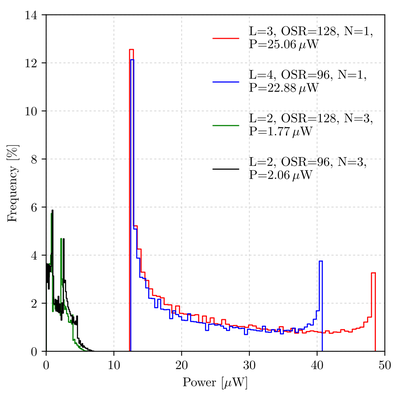
$$k_{mod} \doteq \frac{\alpha_1}{a_1\,\alpha_{OL}^2\,(1-\alpha_{QN})}$$

Parameter	L=3 OSR=128 N=1	L=4 OSR=96 N=1	L=2 OSR=128 N=3	L=2 OSR=96 N=3
a_1	0.1	0.2	1	1
α_1	0.0411	0.0859	0.0823	0.0821
α_{OL}	0.596	0.531	0.794	0.794
α_{QN}	0.449	0.206	0.120	0.246
k_{mod}	2.103	1.921	0.148	0.173





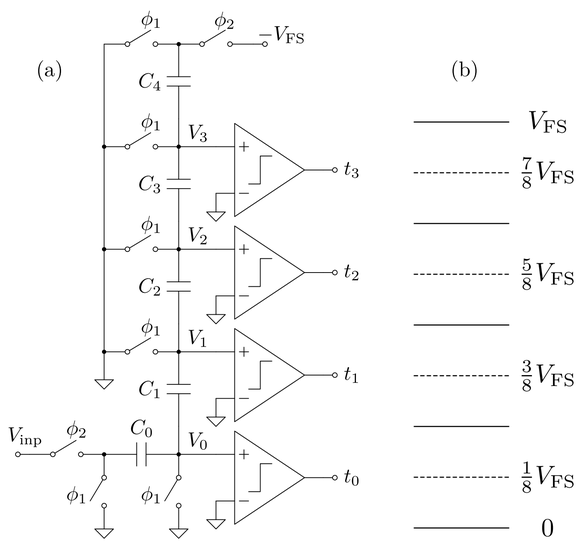




▲ **Multi-bit** quantization with **low-order** noise shaping and **moderate OSR** can save **x10** dynamic power consumption

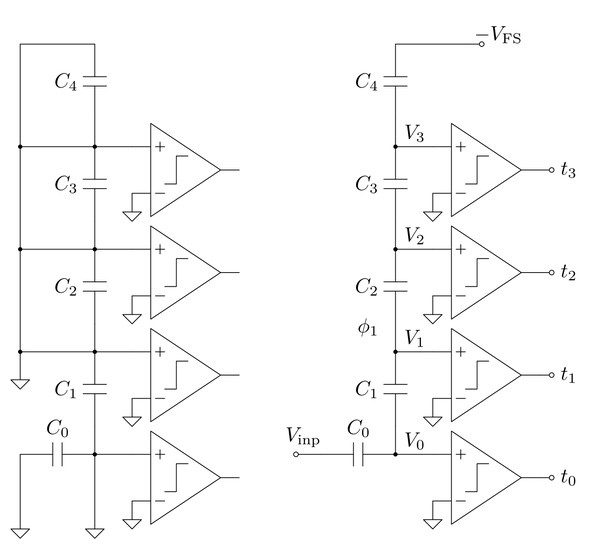
3 Compact SC Multi-Bit Quantizer

- The proposed flash topology is based on a **ladder network** of matched capacitors:



Half-circuit SC topology of the proposed multi-bit quantizer for the 9-level design case (a) and equivalent thresholds (b).

- Non-overlapped clock **operation** of the presented SC quantizer:



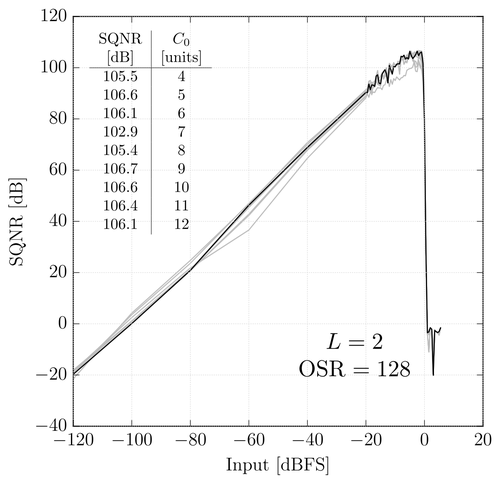
Resetting of all capacitors $C_{0\cdots4}$ during ϕ_1

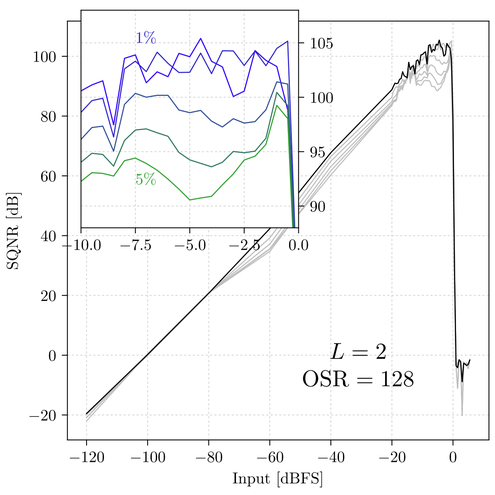
Input S/H, indiviual level shifting of $V_{0\cdots3}$ and parallel quantization during ϕ_2

- Implementation of the equivalent **quantization thresholds**:

$$\frac{C_j}{C_0} = \begin{cases} \dfrac{4(j+n)^2-1}{4n(1+2n)} & j \in [1\ldots n-1] \\ \dfrac{1}{(1+2n)\left(1-4n\sum_{i=0}^{n-1}\frac{1}{4(j+n)^2-1}\right)} & j = n \end{cases}$$

+ **Matching-ratio** based design
  e.g. $\frac{C_{1\cdots4}}{C_0}=\{\frac{11}{16},\frac{143}{144},\frac{65}{48},\frac{5}{24}\}$ for n=4 (9 levels)
+ Low signal **attenuation**
  e.g. $\frac{V_j}{V_{inp}} > \frac{V_{n-1}}{V_{inp}} = \frac{2n-1}{4n-1} \sim -6$dB





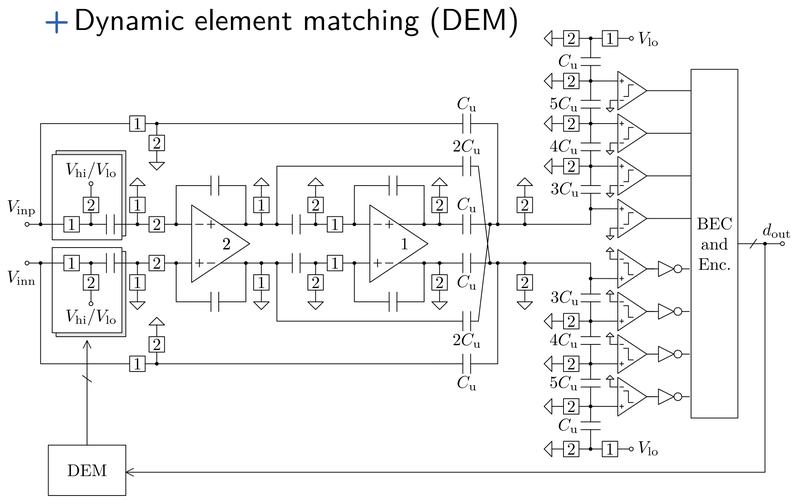
▲ **Compact** and **modular** circuit topology with straightforward scalability

▲ All flash comparators latch at the **same input threshold** to simplify CMOS circuit optimization

▲ Robustness against technology mismatching ensures low sensitivity to **layout granularity** and **parasitic capacitance**

4 Design Example

- A **50-kHz 16-bit 9-level 2nd-order** ΔΣM case of study:
  + 2-V_{pp} differential input full scale with V_{lo}=0.4V and V_{hi}=1.4V at 1.8-V supply
  + 12.8-MHz sampling rate (OSR=128)
  + Switched OpAmps
  + Bubble error correction (BEC)
  + Dynamic element matching (DEM)

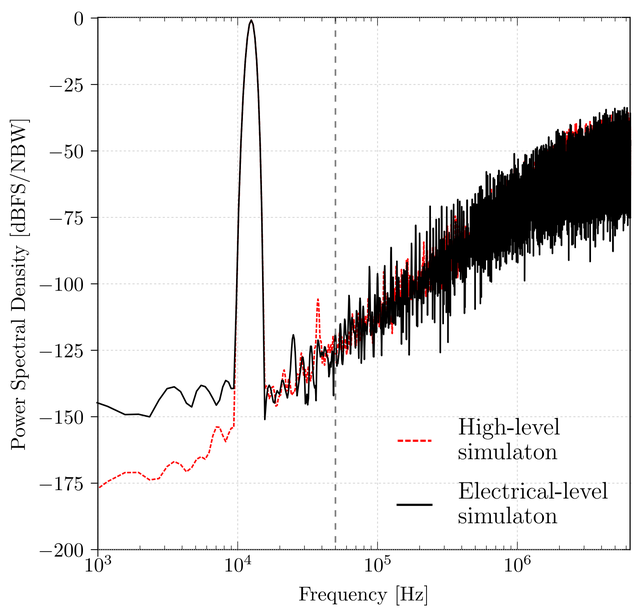


Simplified schematic of a 9-level second-order SC ΔΣM circuit using the proposed multi-bit quantizer.

- Quantizer $\frac{C_{1\cdots4}}{C_0}=\{\frac{11}{16},\frac{143}{144},\frac{65}{48},\frac{5}{24}\}\simeq\{\frac{3}{4},\frac{4}{4},\frac{5}{4},\frac{1}{4}\}$ with unitary capacitance C_u=0.5pF

▲ 4-element C_0 to weight the nested feedforward paths

▲ Good **SQNR matching** between behavioral and electrical simulations at transistor level



Output PSDs for the 9-level second-order SC ΔΣM circuit example obtained from behavioral and electrical simulations at -1dB$_{FS}$ input.

5 Conclusions

▲ A **power model** for single-loop ΔΣM to show the importance of **multi-bit quantization** when facing high-resolution ADC specifications

▲ A **SC topology** proposal for multi-bit flash quantizers exhibiting:
  + **Compact** implementation
  + High circuit **modularity**
  + **Single** comparator CMOS design
  + **Low-power** operation
  + Compatibility with **multi-feedforward** ΔΣM architectures
  + Compatibility with **SC low-power** techniques like clocked comparators and switched OpAmps

▲ A practical 50-kHz 16-bit 9-level 2nd-order ΔΣM **design example** with transistor-level simulations

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