A 6.5-μW 70-dB 0.18-μm CMOS Potentiostatic Delta-Sigma for Electrochemical Sensors

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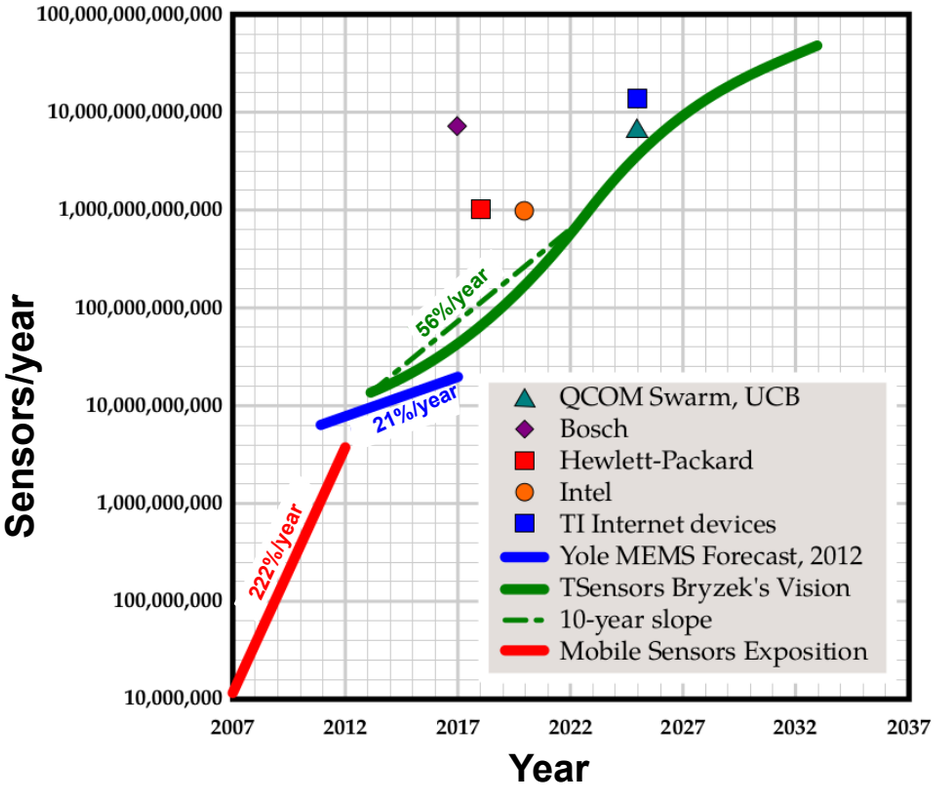
Sensors Market Vision

- Several organizations created visions for continued growth to trillion(s) sensors
  - $15 trillion by 2022
- **Electrochemical sensors** are growing exponentially due to potential of miniaturization and mass production
  - **Monolithic** or **hybrid** integration onto CMOS platforms
  - Applications in biosensors, quality control, ...



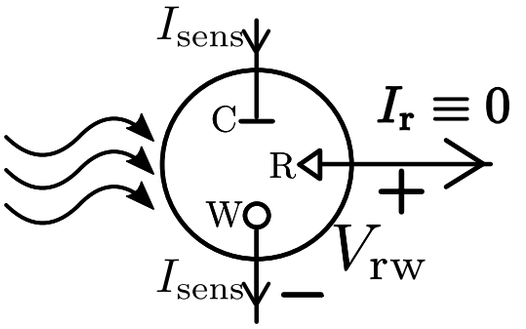
Expected sensor production growth per year

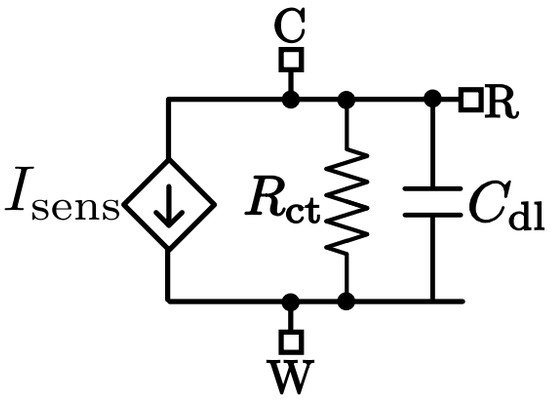
www.tsensorssummit.org

Amperometric Electrochemical Sensors

- ▲ Interaction with microorganisms
- ▲ **Selectivity** by functionalization
- ▼ Reduced **speed** and **life** time
- ▼ **Potentiostatic** and **amperometric** operations
- ▶ **Three electrodes:**
  - **W**orking
  - **R**eference
  - **C**ounter
- ▶ Measurement independent of the **R** and **C** impedances.
- ▶ Current associated to the electrons involved in a **redox** process

$$\mathrm{O} + e^- \underset{\mathrm{ox}}{\overset{\mathrm{red}}{\rightleftharpoons}} \mathrm{R}$$

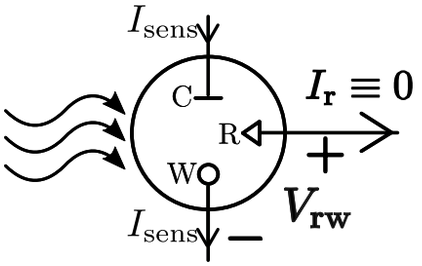




- Electrochemical **time constant:**

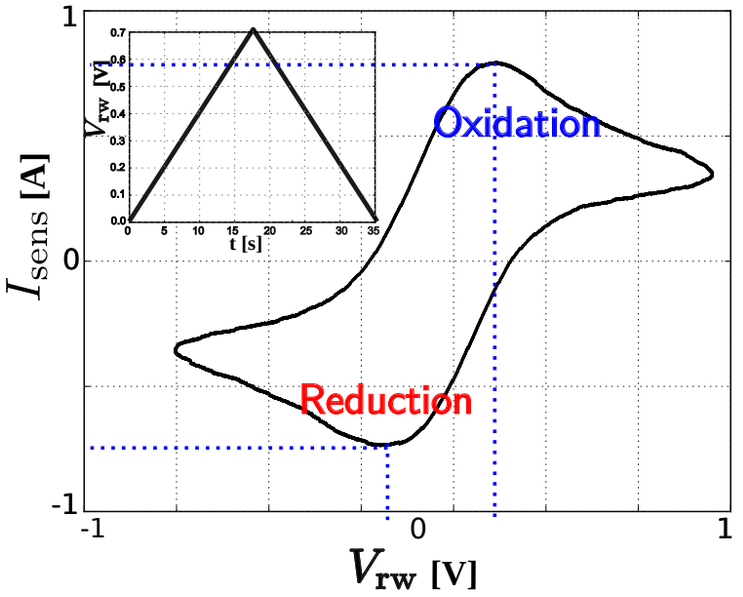
$$\tau_{\mathrm{ch}} = R_{\mathrm{ct}} C_{\mathrm{dl}} \approx 10^{-1}\mathrm{s}$$

Amperometric Electrochemical Sensors

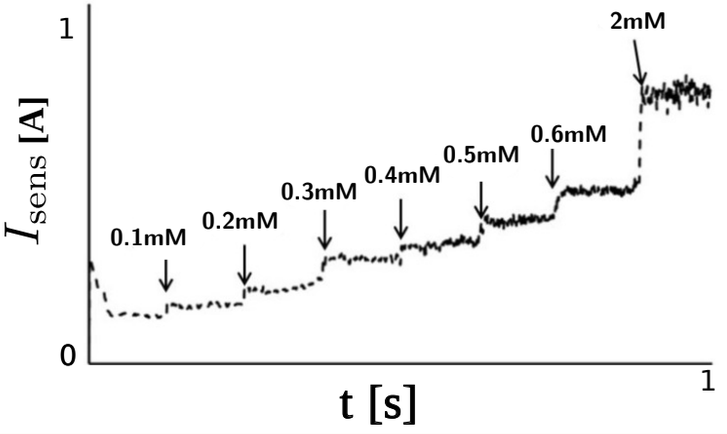


- Different **detection methods** are required

- **Cyclic Voltammetry (CV)**
  - Sensor performance, rapid location of redox potentials, ...
  - **Sweeping** electrode potential V_{rw} and **measuring** resulting current I_{sens}
  - Potentiostat must sink/source current



- **Chronoamperometry (CA)**
  - V_{rw} fixed and I_{sens} monitored as a function of time while concentration is swept



Classic circuit implementation

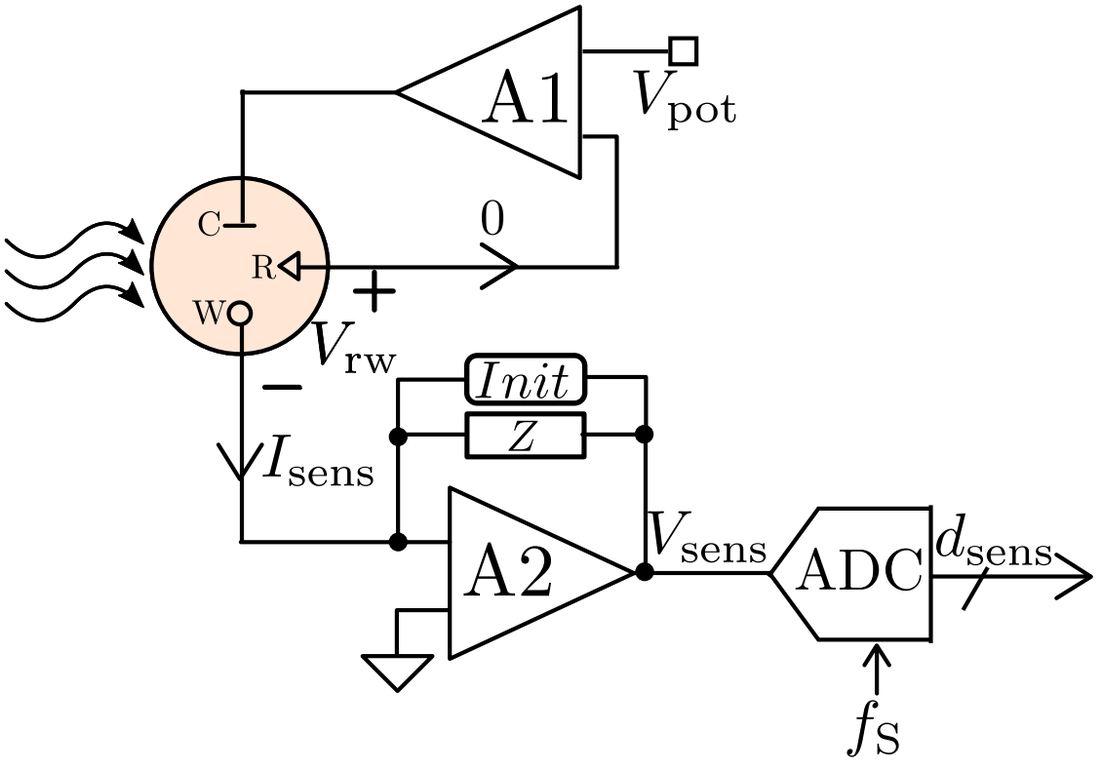
- **Potentiostat**
  - A_1 establishes the control loop to accomplish potentiostat operation

$$V_{\mathbf{rw}} = V_{\mathbf{pot}} \quad \& \quad I_{\mathbf{r}} \equiv 0$$

- **Amperometry**
  - A_2 converts sensor current to voltage for digitization and readout

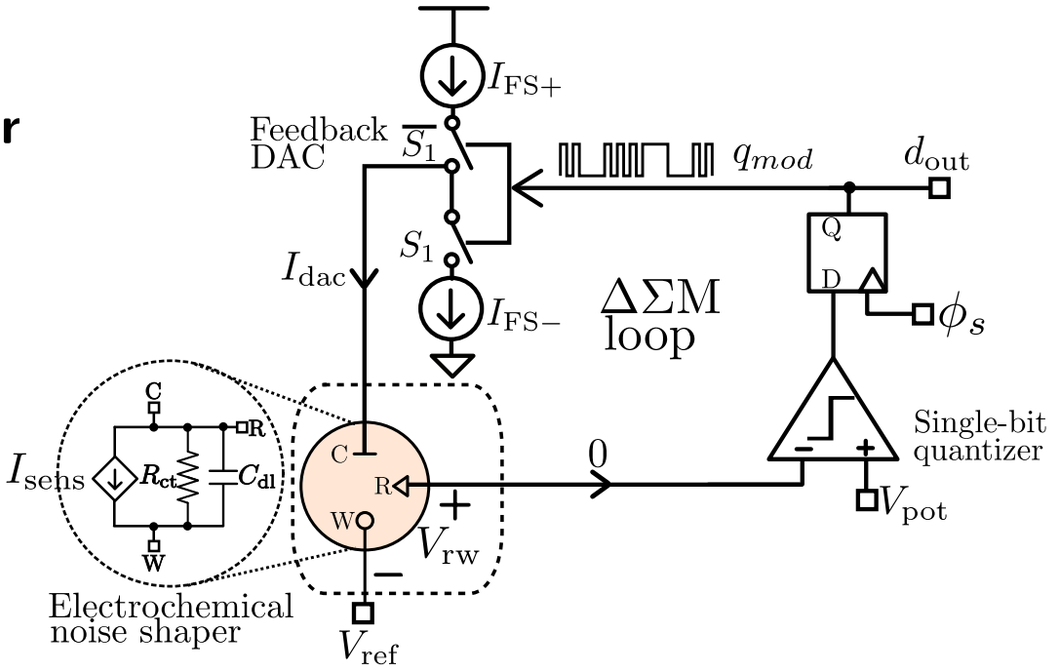
- ▼ Requires multiples OpAmps + ADC

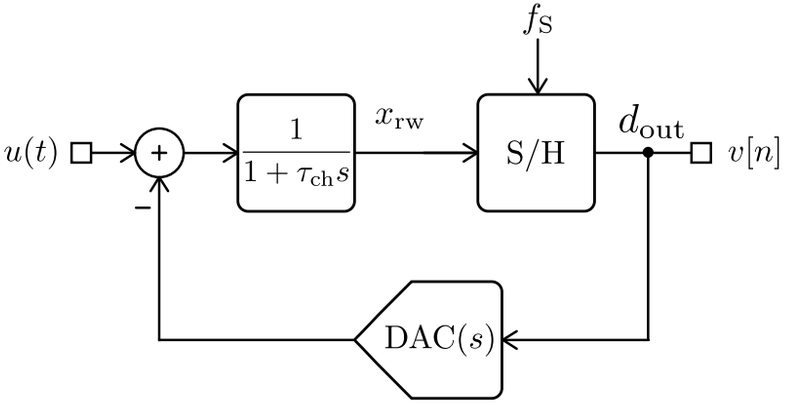
- ▼ Large **area** and **power consumption**



Potentiostatic ΔΣM

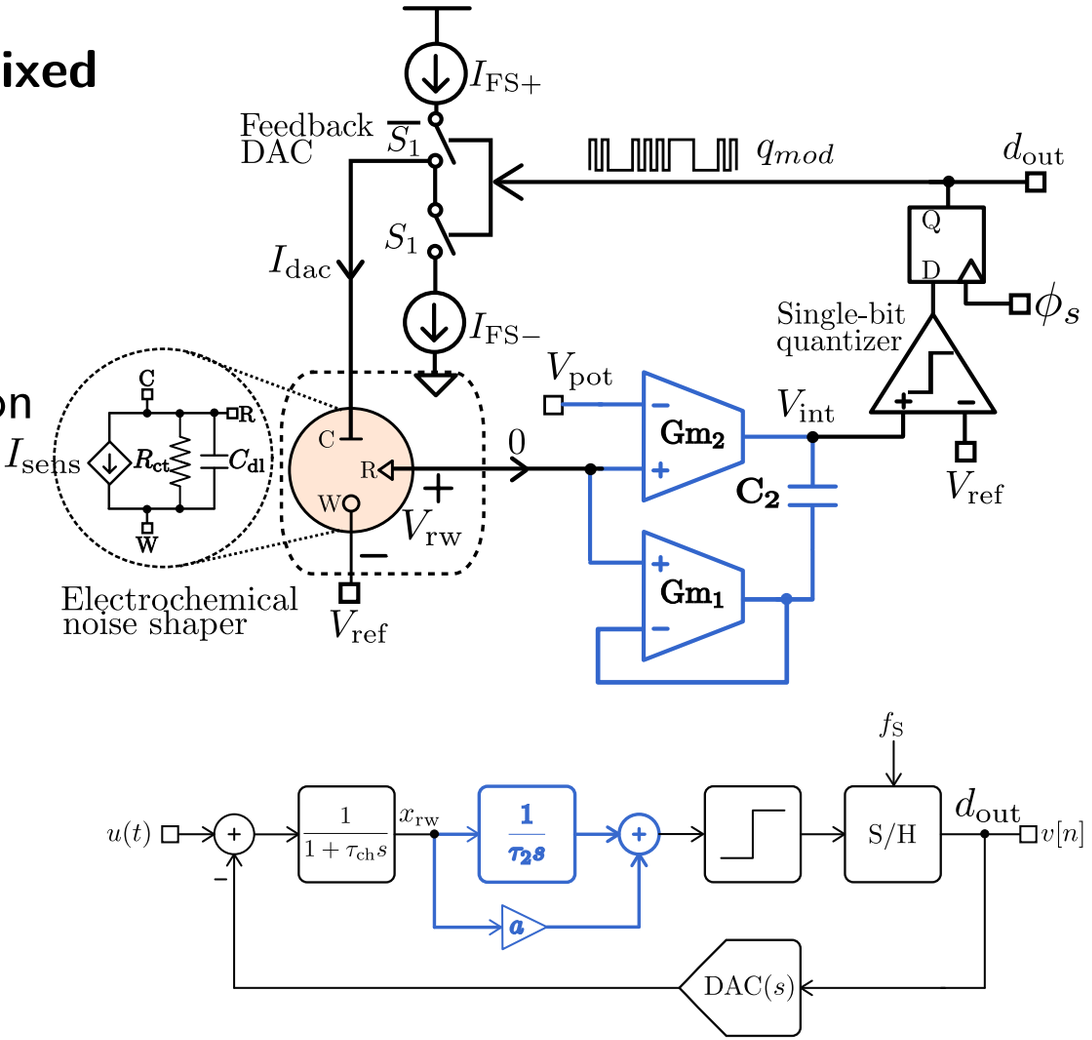
- Behaviour similar to **low-pass first-order single-bit CT** $\Sigma\Delta$M A/D modulator
- Error current converted into voltage and shaped in frequency by the **electrochemical sensor** itself
- ▲ High oversampling ratios (**OSR>100**) can be easily obtained with kHz-range clock frequencies f_S
- ▲ **Amperometric** read-out through the $\Delta\Sigma$ modulation of output bit stream q_{mod} by chemical input I_{sens}





From 1st order to 2nd order ΔΣM

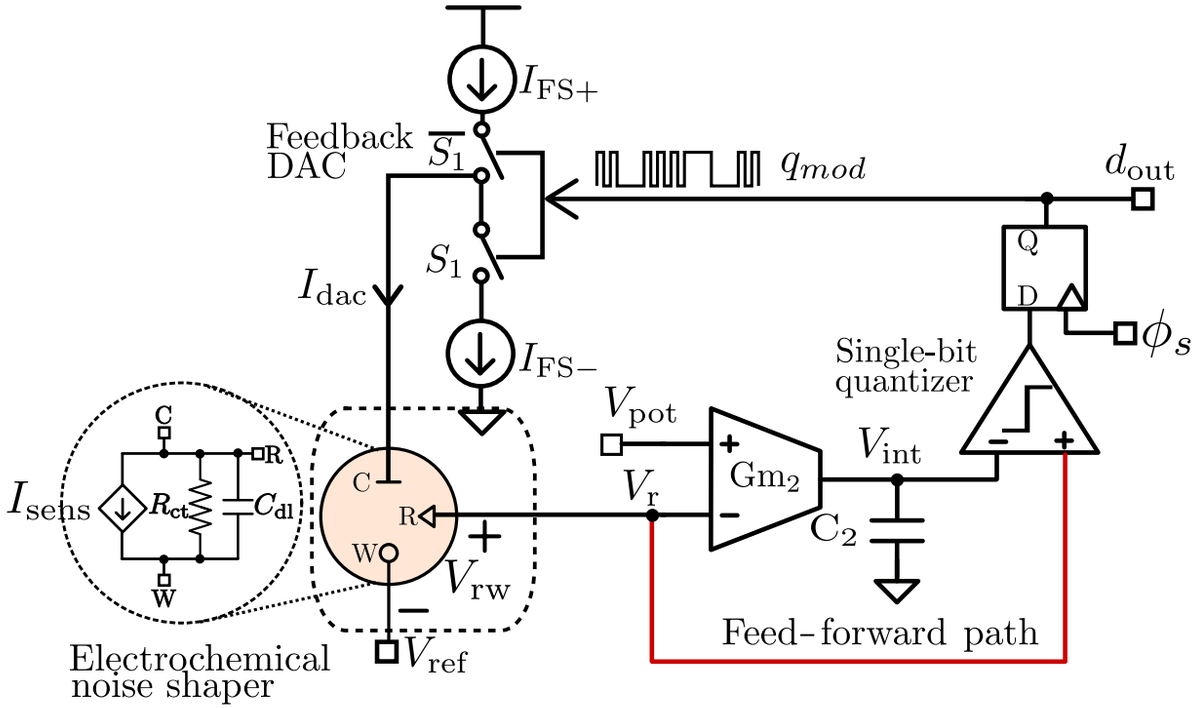
- From electrochemical only τ to **hybrid/mixed EC/electronic τ_s**
- Electronic time constant **C_2/Gm_2**
  - Allows **precise potentiostatic** operation
  - **Tones** and pattern noise **suppression**
- Feed-Forward through **Gm_1**
  - Stabilize the loop

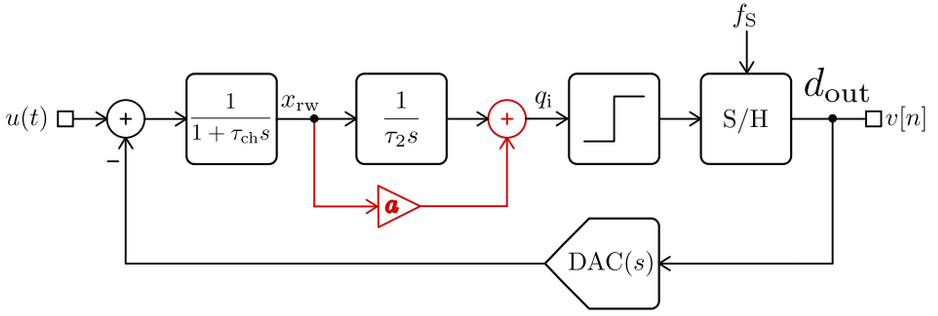


[5] J. Aymerich, M. Dei, L. Terés and F. Serra-Graells, "Design of a Low-Power Potentiostatic Second-Order CT Delta-Sigma ADC for Electrochemical Sensors," 2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)

From 1st order to 2nd order ΔΣM

- **Improved architecture**
  - Direct path from Vr to input the single-bit quantizer
  - Area and power consumption





- **Low-power** CMOS circuits
- **Large flexibility** on the selection of **potentiostatic voltage**
  - Wide common-mode voltage range

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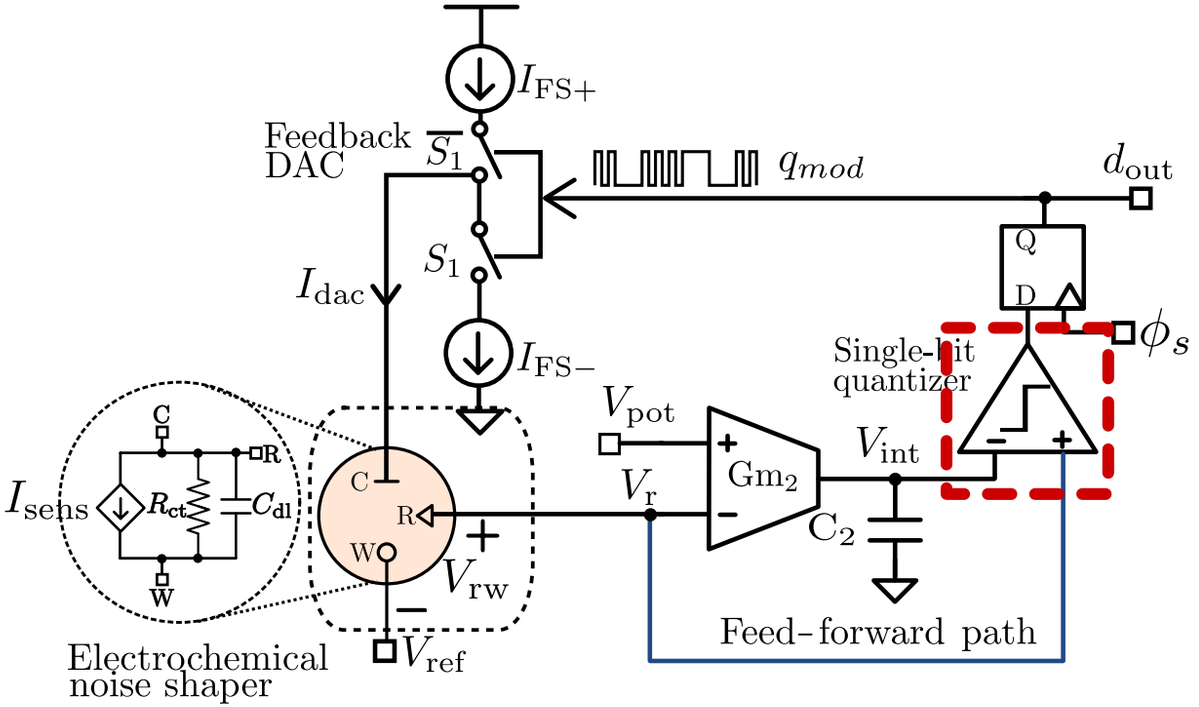
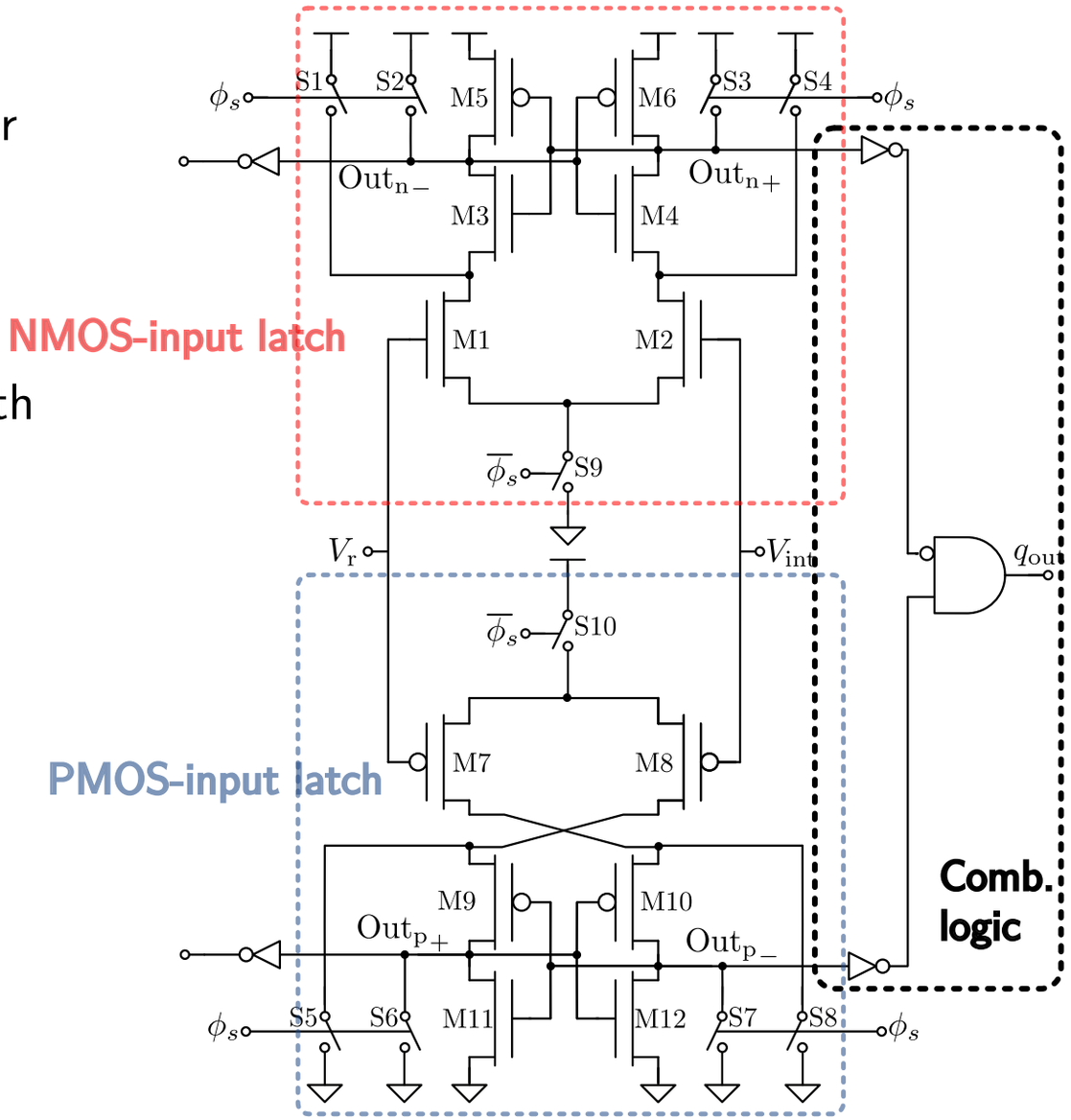


- **Large flexibility** on the selection of **potentiostatic voltage**.
  - **Single-bit quantizer**: Wide input common-mode voltage range
  - **Transconductance Gm_2**: Wide input/output common-mode voltage range

Single-bit quantizer

- Rail-to-rail complementary latch comparator
  - High-input impedance
  - Zero-static power consumption
  - Combinational logic allows to merge both NMOS-PMOS-input comparators



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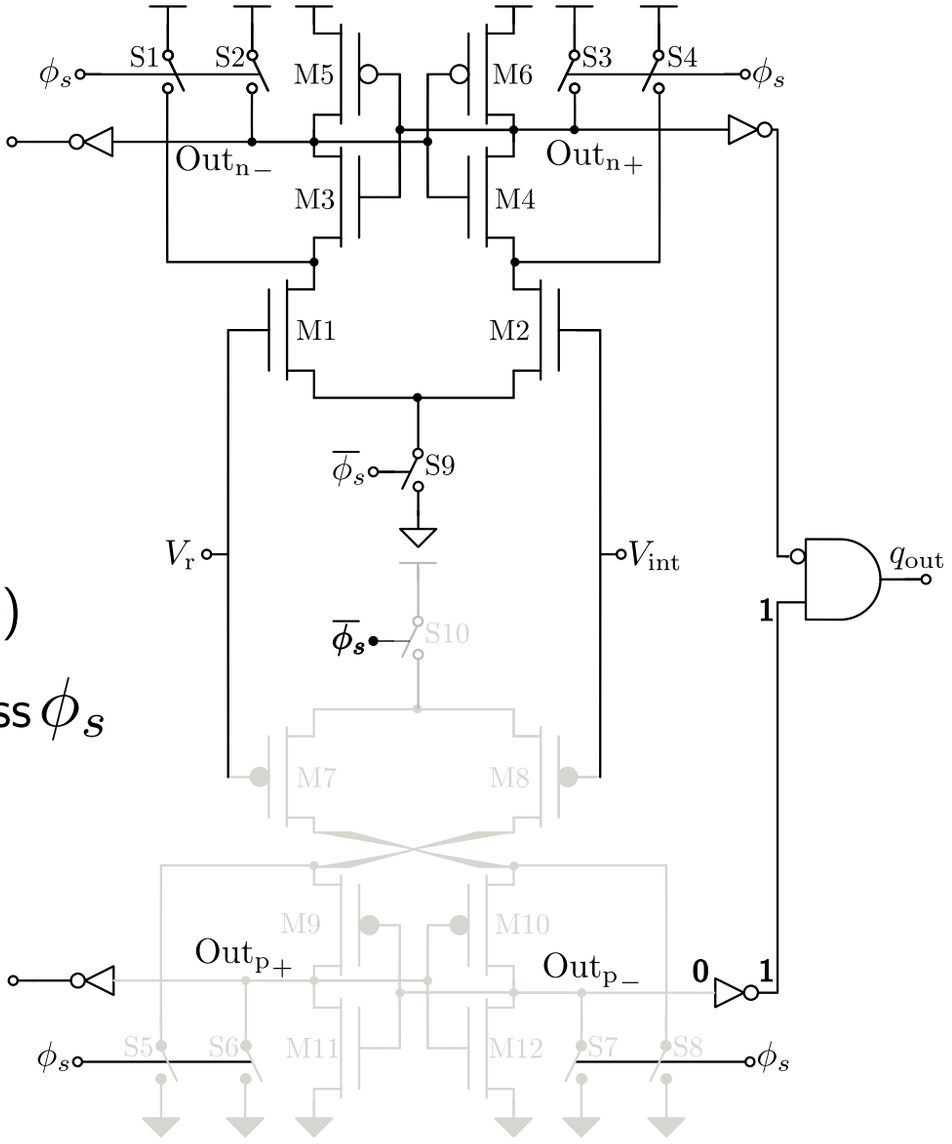
  - Outp nodes remain at the negative rail regardless ϕ_s



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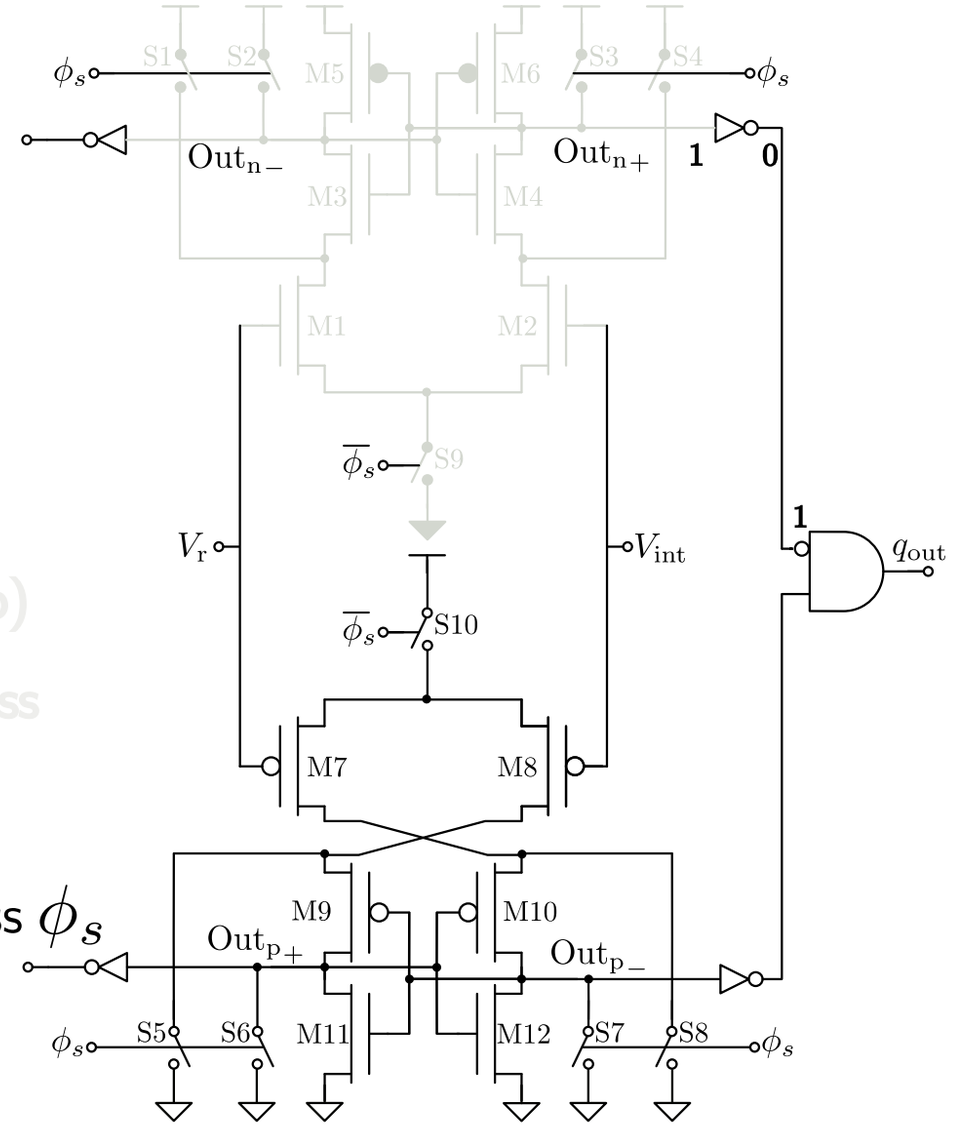
  - Outp nodes remain at the negative rail regardless
- **NMOS OFF:** Input common-mode < (VTHn)
  - Outn nodes remain at the positive rail regardless ϕ_s



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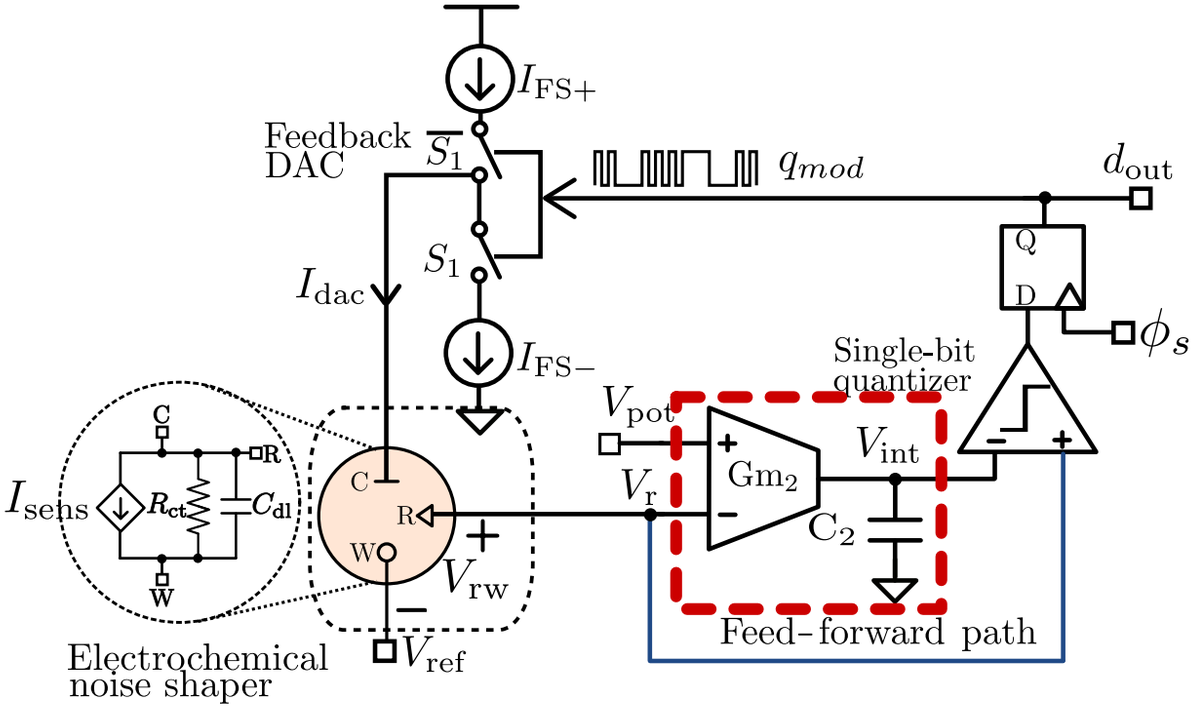

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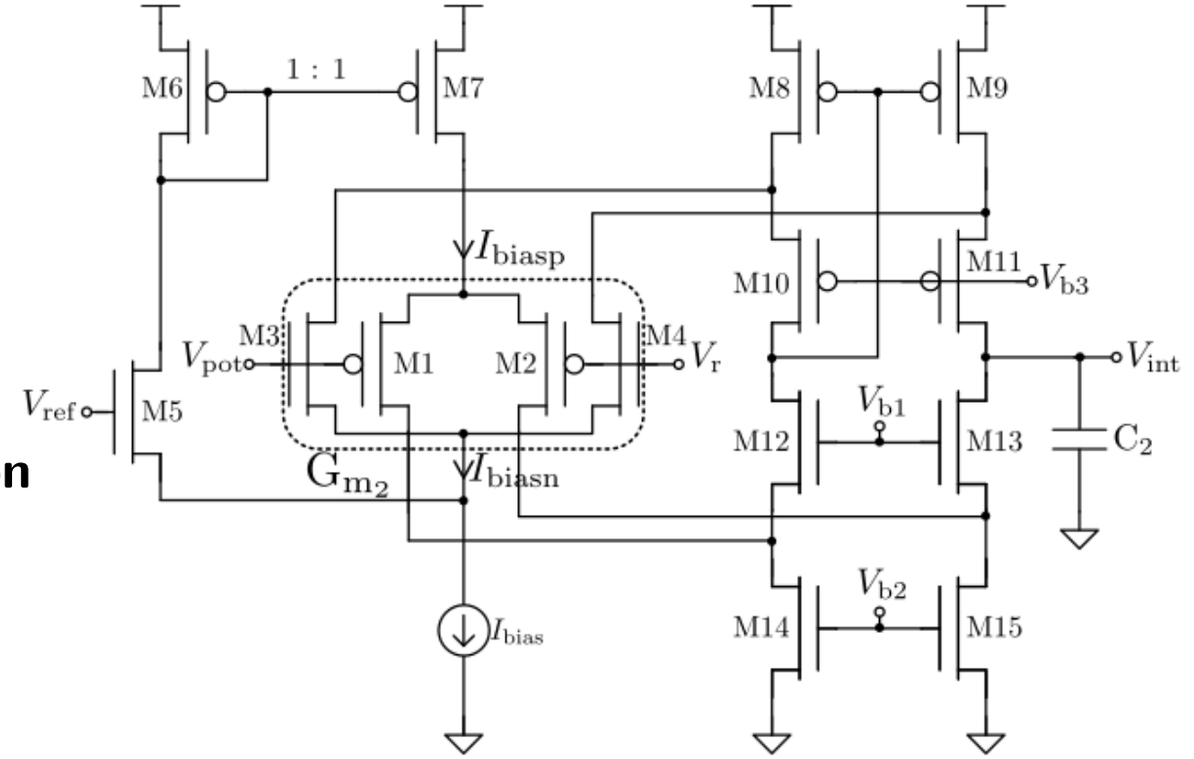
Gm-C Integrator

- **Constant gm** over the input common-mode voltage
  - Avoid variations in the electronic integrator time constant
  - **M1 - M4** operated in **weak inversion**

$$\mathrm{gm}_2 = \frac{I_{\mathrm{biasn}} + I_{\mathrm{biasp}}}{nU_{\mathrm{T}}}$$

  - Sum of the tail currents constant



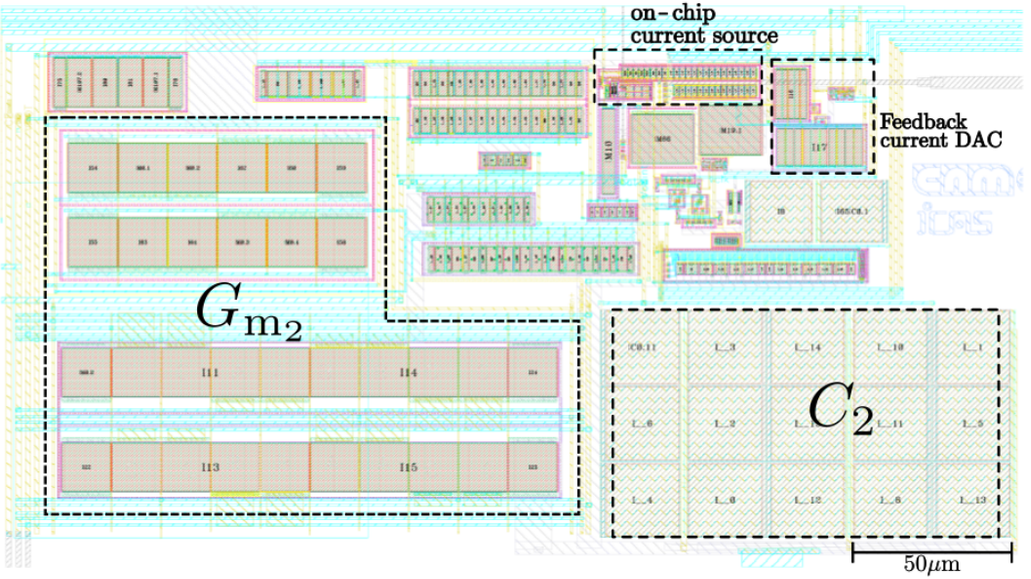
- **Wide output swing**

$$2V_{\mathrm{ov}} < V_{\mathrm{int}} < V_{\mathrm{dd}} - 2V_{\mathrm{ov}} \qquad V_{\mathrm{ov}} \longrightarrow \text{Overdrive voltage}$$

Low-power 0.18-μm CMOS Design

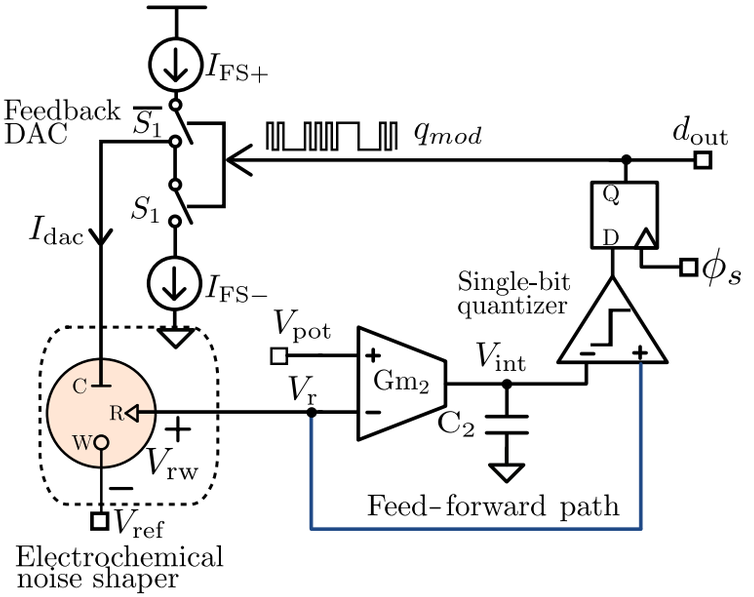
- Layout area: **0.063mm²**

- **Gm-C integrator** occupy most of the area
  - to minimize **offset**, i.e potentiostatic error (Vr - Vpot)
  - **slow** integrator **time constant** (sampling frequency @ 1kHz)



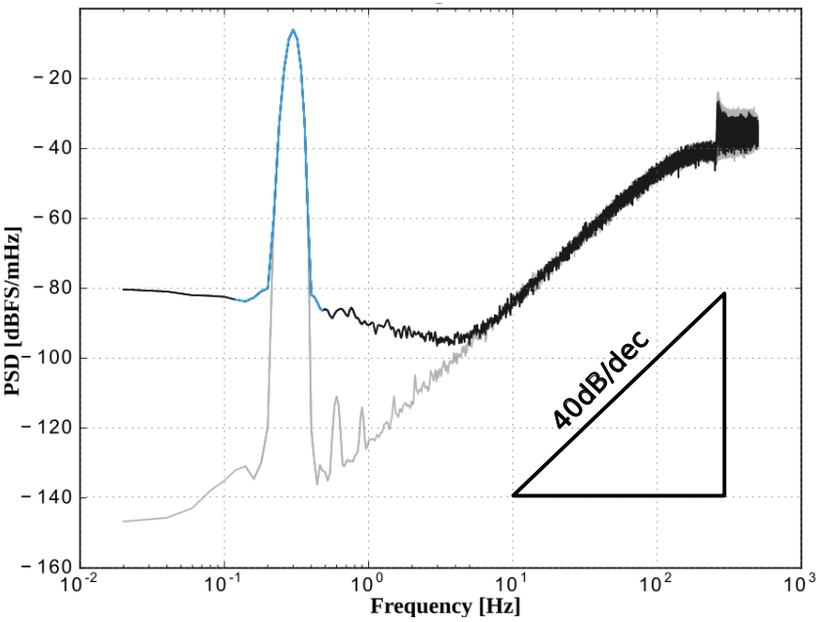
- **Large Feedback DAC**
  - To minimize **low-frequency noise**. (DAC noise added directly to the input, it is not shaped by the delta-sigma loop-filter)

- **Ongoing run** XFAB-XH018

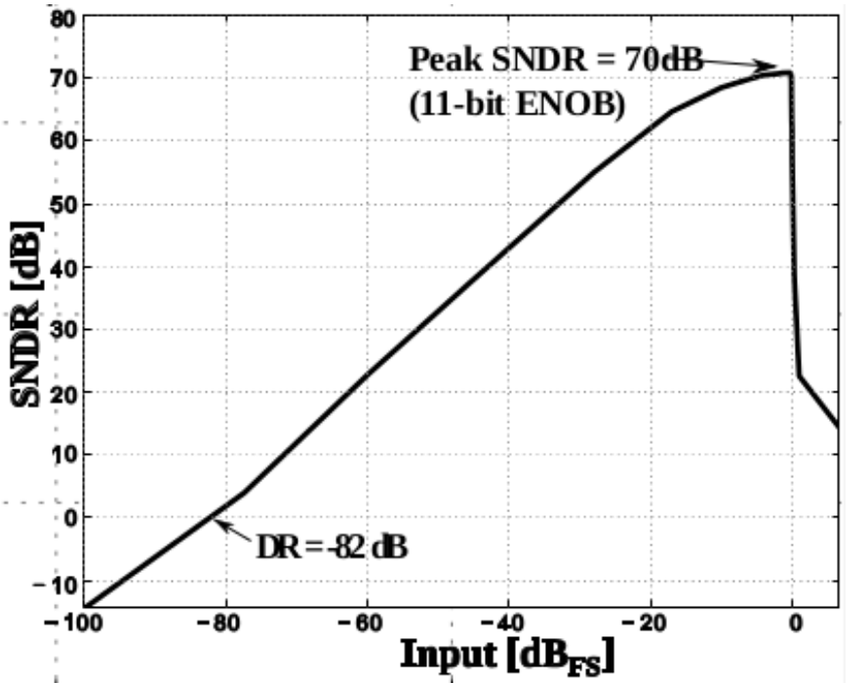


Post-Layout Simulations

- **Output spectrum** comparison w/ and w/o electronic transient
  - $f_S = 1k\text{Hz}$
  - $\tau_{\text{ch}} = 0.15\text{s}(OSR \approx 500)$
  - $I_{\text{FS}} = 1.25\mu A$



- **70-dB** dynamic range for 1.25uA current full scale. (280pA RMS, noise)



- **Higher resolution** is achievable enlarging the area of the feedback DAC

AREA PENALTY AGAINST DYNAMIC RANGE.

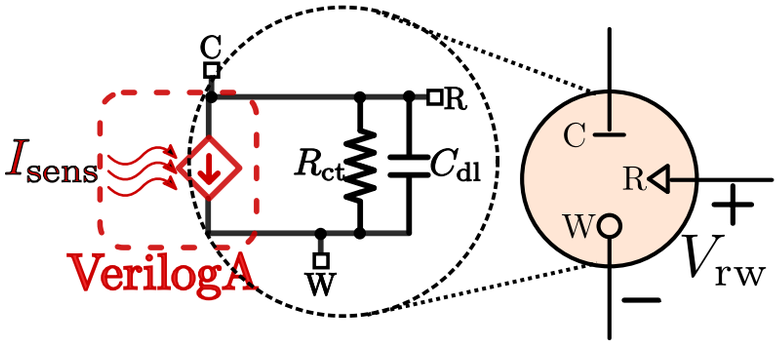
DAC + bias current Area estimation	Total area increased	SNDR	ENOB
$1400\mu\text{m}^2$	—	70-dB	11
$5600\mu\text{m}^2$	7%	75.5-dB	12
$22400\mu\text{m}^2$	33%	81-dB	13

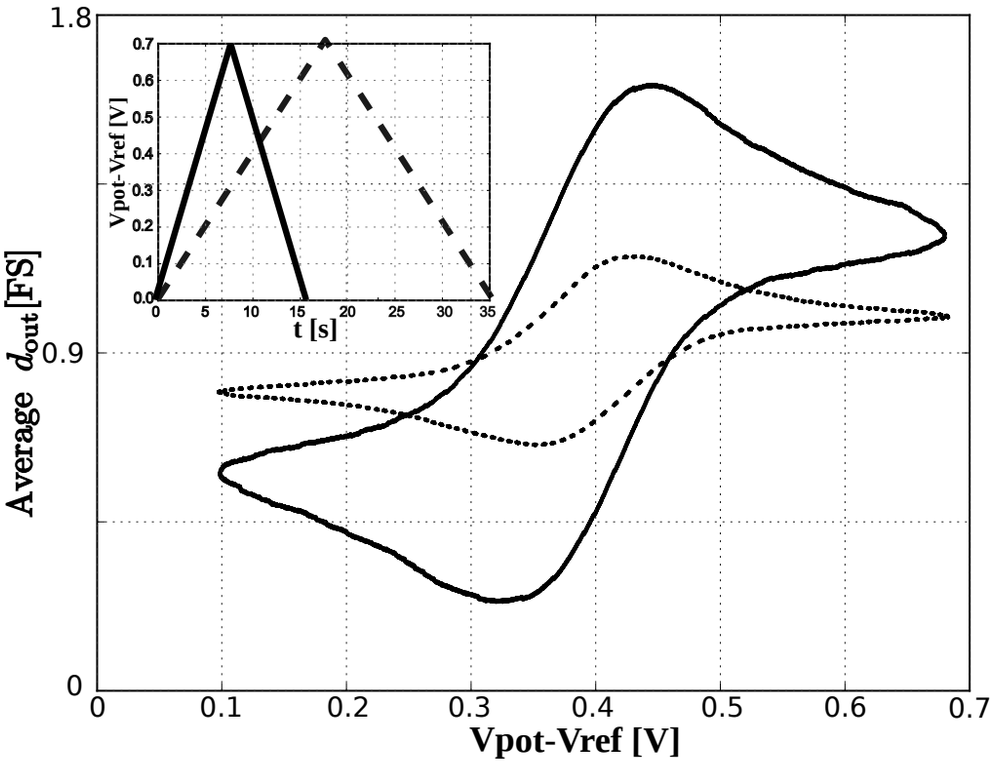
Post-Layout Simulations

- **Cyclic Voltammetry**

  - **Triangular waveform** is applied to the reference electrode while the sensor current is measured simultaneously

  - **VerilogA model**: Vrw-Isens DC look-up tables based on two experimental measurements of ferricyanide CVs





Ferricyanide Cyclic Voltammetry

Simulation Results

- **Performance simulation results**

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}	1.8	V
Potential range	$V_{pot} - V_{ref}$	± 0.7	V
Input full scale	I_{FS}	± 0.2 to ± 2	μA
Oversampling ratio	OSR	500	–
Sampling frequency	f_S	1	kHz
Layout area	–	0.0063	mm^2
SNDR at $1.25\mu A_{FS}$	SNDR	70	dB
Power at $2\mu A_{FS}$	P_D	6.5	μW

- **Power consumption** mainly determined by feedback current DAC

  $P_{DAC} = 5\mu W$

- Rest of circuit blocks

  $P_{DAC} = 1.5\mu W$

Conclusions

- **Compact architecture** thanks to the electrode-electrolyte interface used as an integrator stage in the $\Delta\Sigma$ structure
- **Minimalist** analog circuits fully integrable in purely digital CMOS technologies
- **High resolution** with kHz-range clock frequencies: $\mathrm{SNDR} = 70\mathrm{dB@}1k\mathrm{Hz}$
- **Low-power ($1.5\mu\mathrm{W}$)** operation compared to sensor consumption

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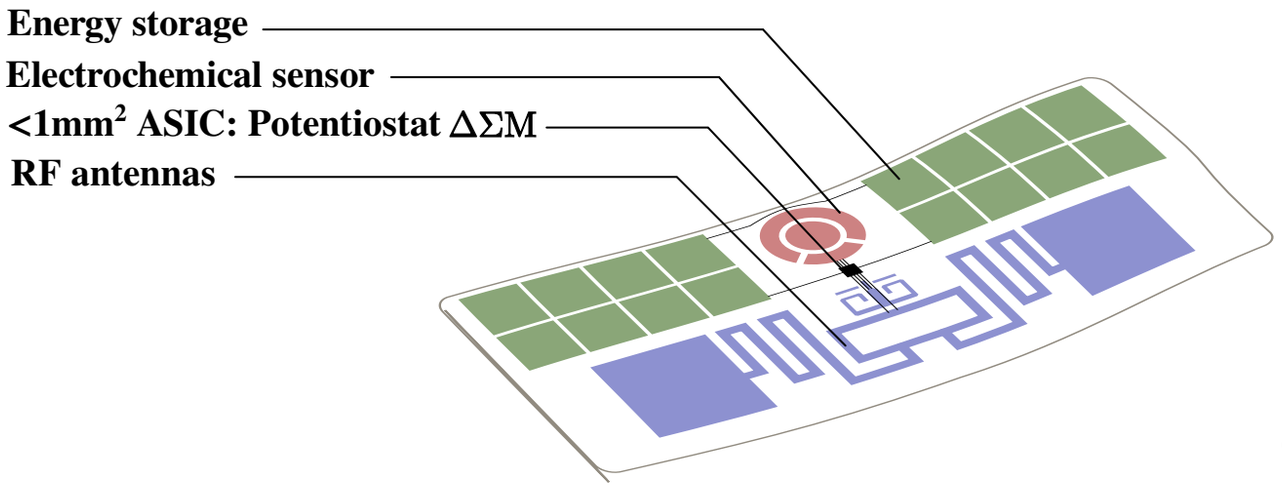
Future work

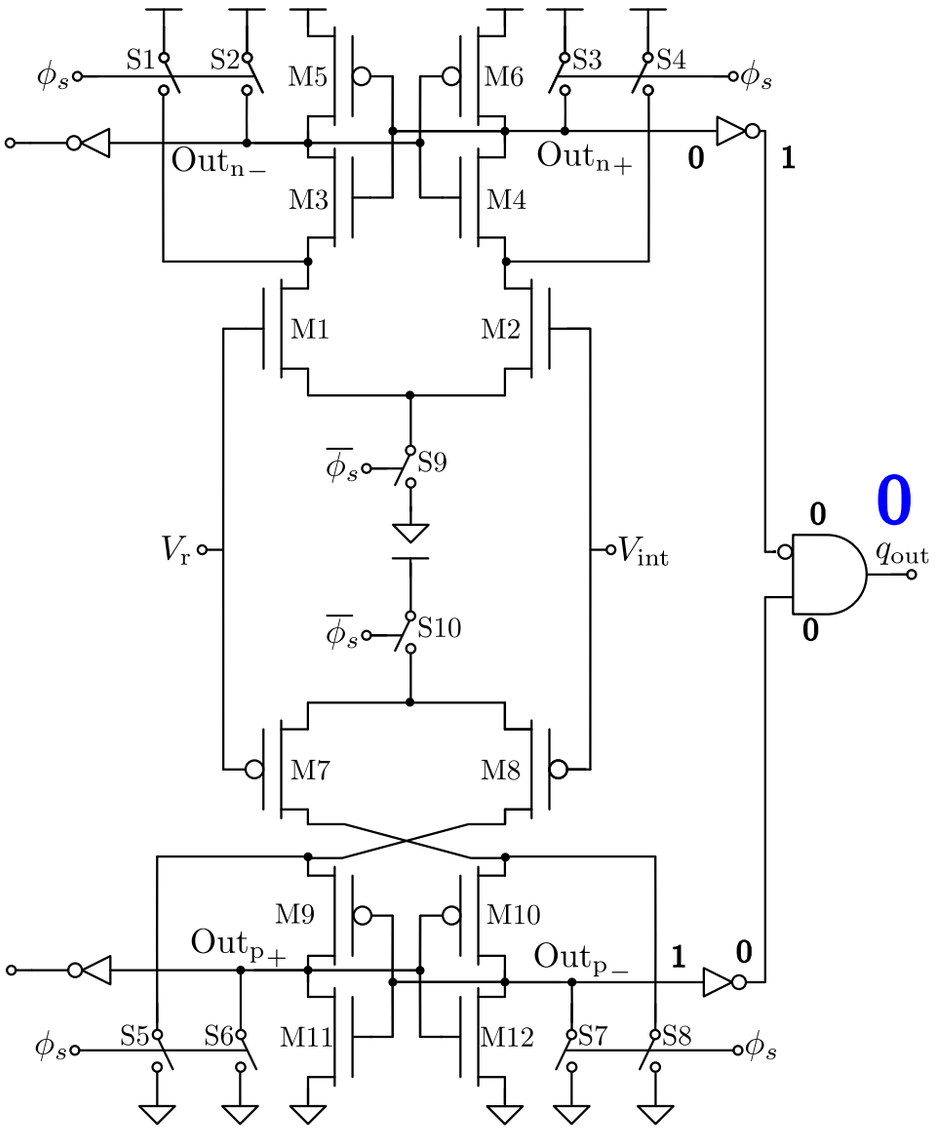


Smart tags for food quality control

Wireless contact lens for health monitoring

Single-bit quantizer

- Rail-to-rail complementary latch comparator
  - Zero-static power consumption
  - Combinational logic allows to merge both NMOS-PMOS-input comparators
- **PMOS and NMOS ON**
  - Vint $>$ Vr



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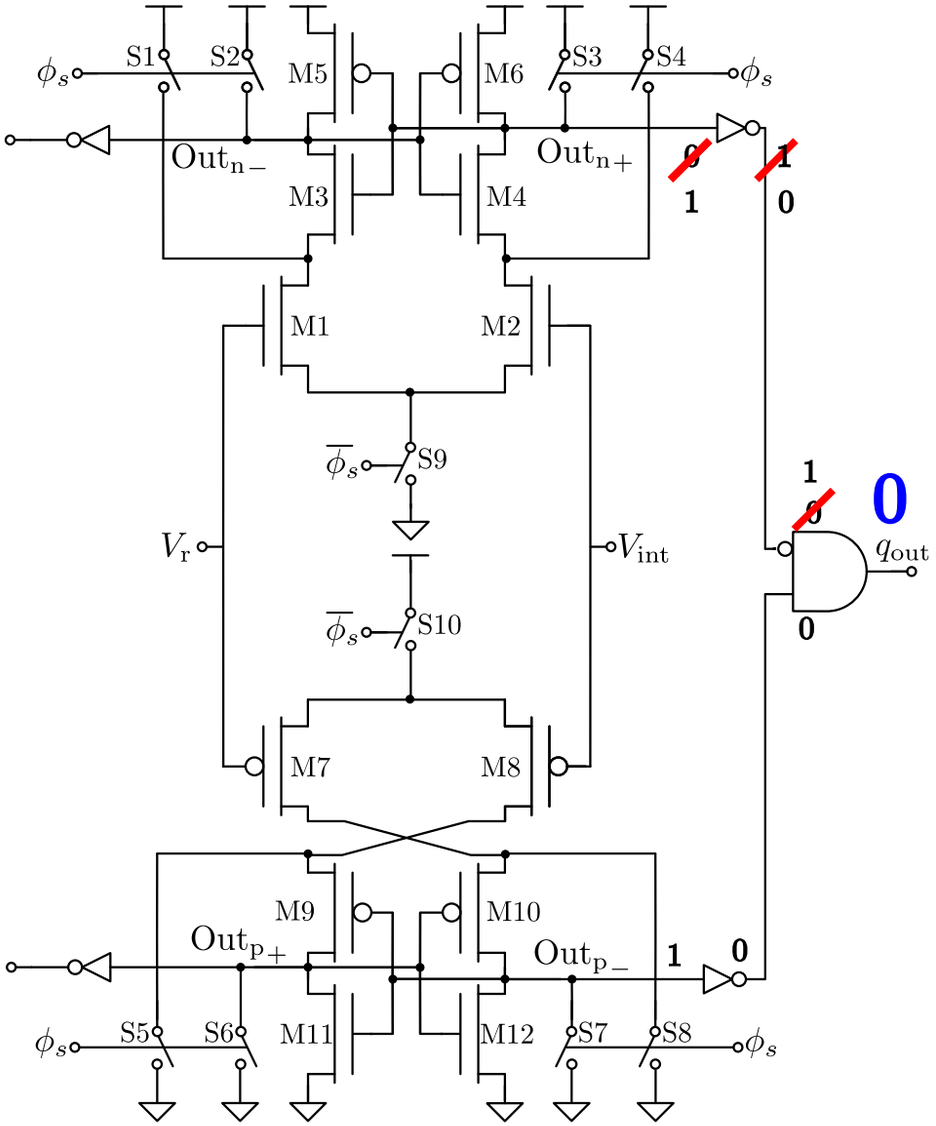

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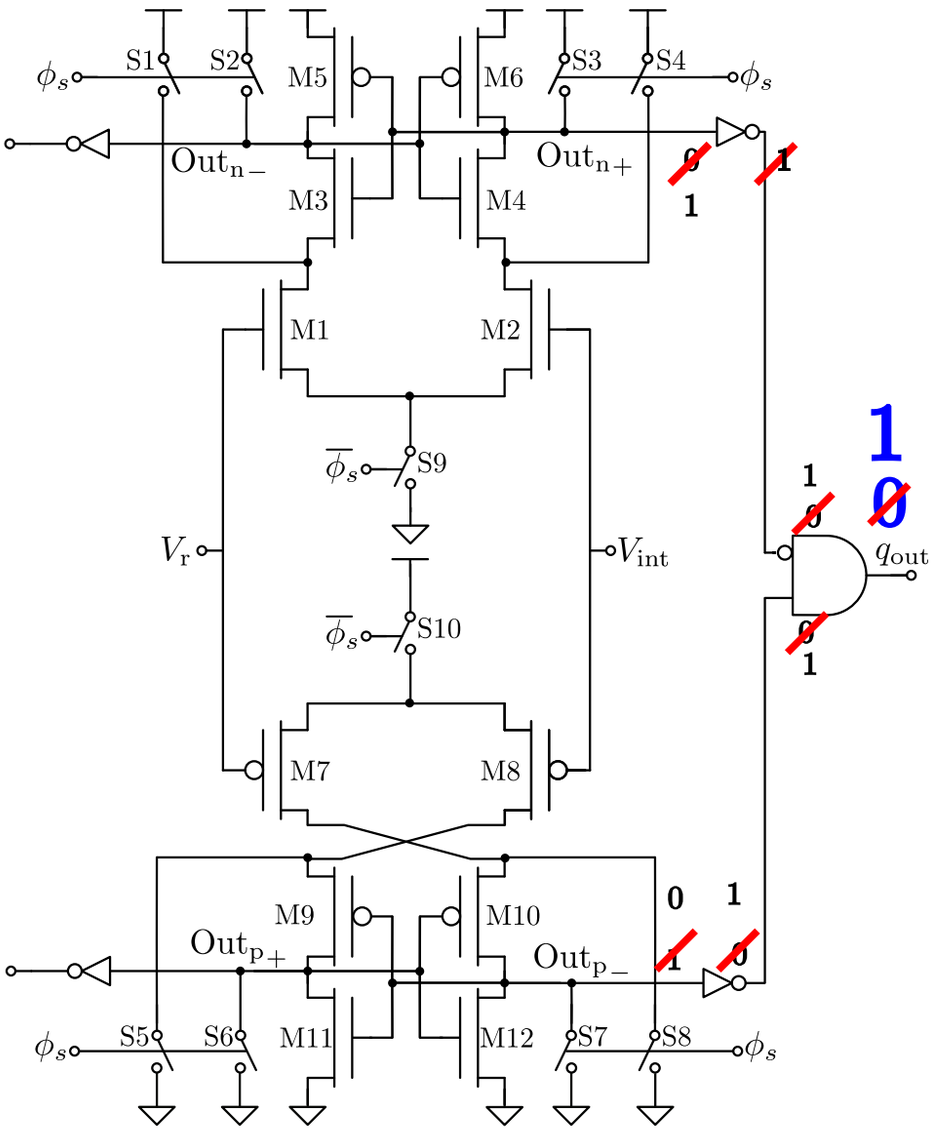

Power Consumption Comparison

						[This work]
Technology	0.18 µm	0.5 µm	0.13 µm	0.18 µm	2.5 µm	0.18 µm
ADC structure	Current to frequency	Delta-sigma	Single-Slope	Delta-sigma	Delta-sigma	Delta-sigma
Sampling frequency	-	100 kHz	1.25 kHz	-	1 kHz	1 kHz
FS current	**150 nA**	**16 µA**	**600 nA**	**1.65 µA**	**2 µA**	**2 µA**
Power consumption	**3 µW**	**241 µW**	**56 µW**	**920 µW**	**25 µW**	**5 µW**
@ supply voltage	@ 1.2 V	@ 1.2 V	@ 2 V	@ 1.8 V	@ 5 V	@ 1.8 V