A 128×128-pix 4-kfps 14-bit Digital-Pixel PbSe-CMOS Uncooled MWIR Imager

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1 Introduction & Current State

2 Digital Pixel Sensor Circuits

3 Imager Integration in 0.18-µm CMOS Technology

4 Post-Layout Simulation Results

5 Conclusions

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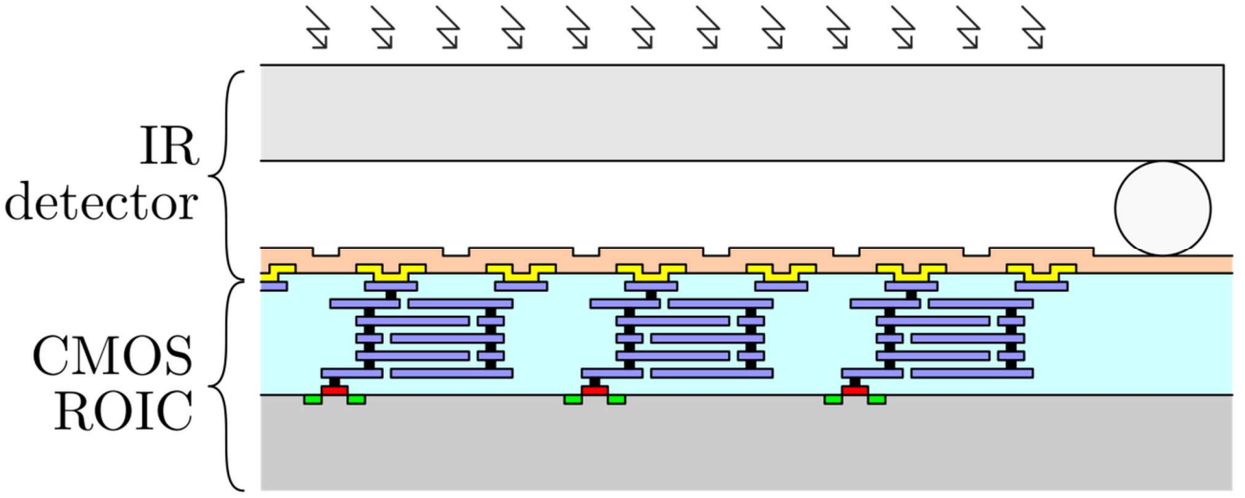
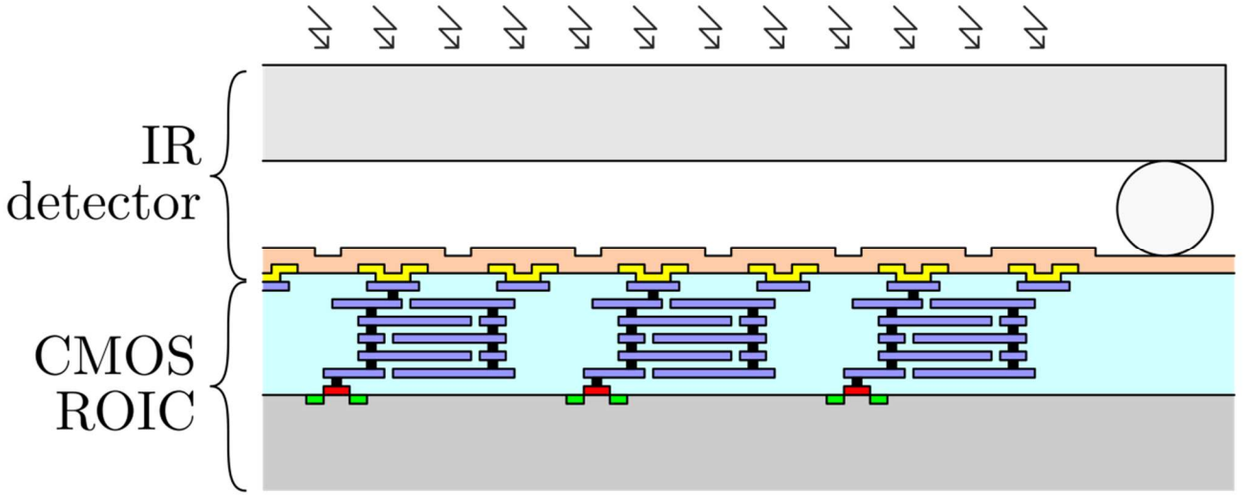
IR Imagers Detector

- Thermal microbolometers
  - LWIR
  - ▲ Low-cost CMOS integration
  - ▲ Room-temperature
  - ▼ Low sensitivity
  - ▼ Limited frame rates
- Quantum-well IR photodetectors
  - SWIR
  - ▼ Expensive hybrid integration
  - ▼ Cryogenic cooling
  - ▲ High sensitivity
  - ▲ High speed
- PbSe VPD IR technology
  - MWIR
  - ▲ Monolithic
  - ▲ Room-temperature
  - ▲ High bandwidth
  - ▲ High speed

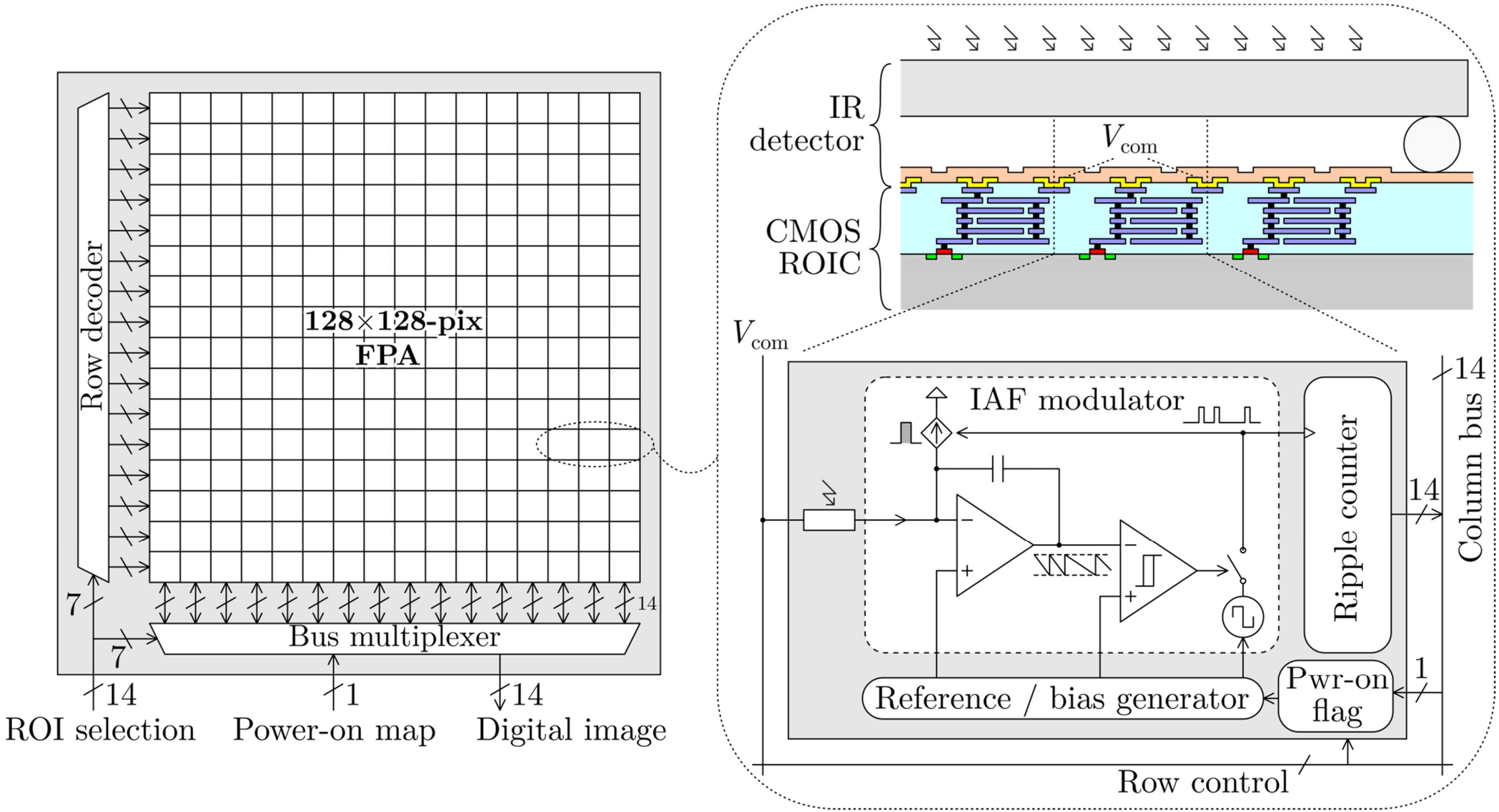


IR Imagers ROIC

- DPS requirements
  - Digital output
  - Low-crosstalk
  - Reduced noise bandwidth
  - Dynamic range enhancement
  - Reduced pixel pitch
  - Low power consumption
- DPS implementation
  - Massive parallel A/D conversion
  - In-pixel references generation
  - Challenging design



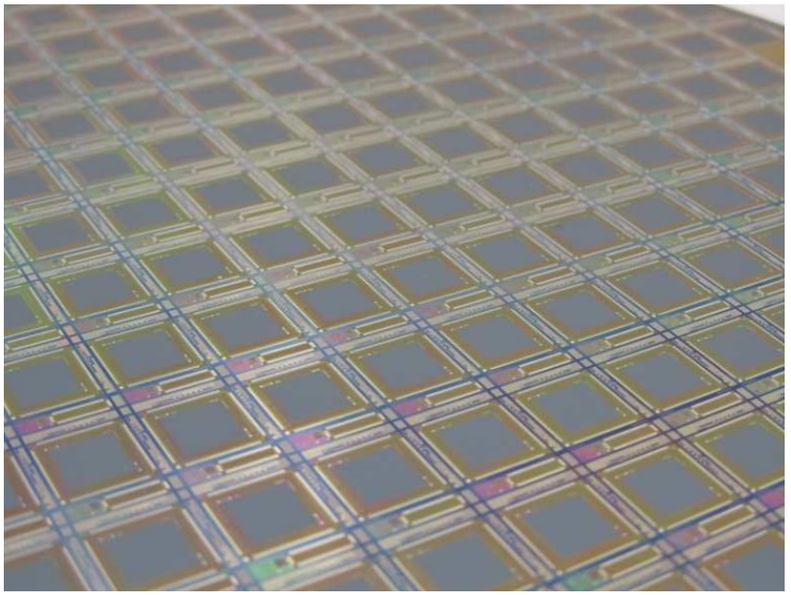
CMOS-ROIC for an IR Imager using PbSe detector

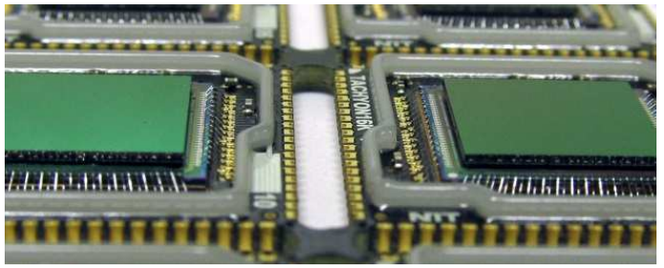


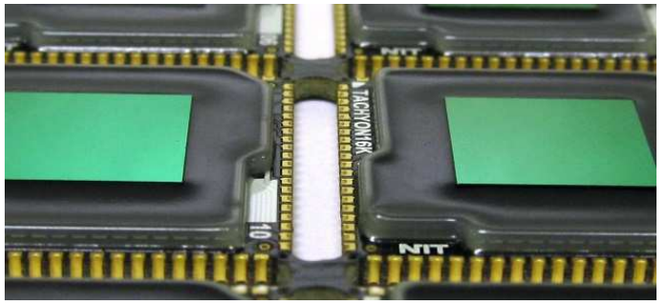
Current State

- ROIC samples available ready for detector post-processing steps.
- To be packaged and integrated to the camera.

- Presented work is actually the ROIC final version.
- A previous version is already in production.







66mm × 62mm × 62mm

- Main applications:
  - Industrial process monitoring and control.
  - Defense and security.
  - …

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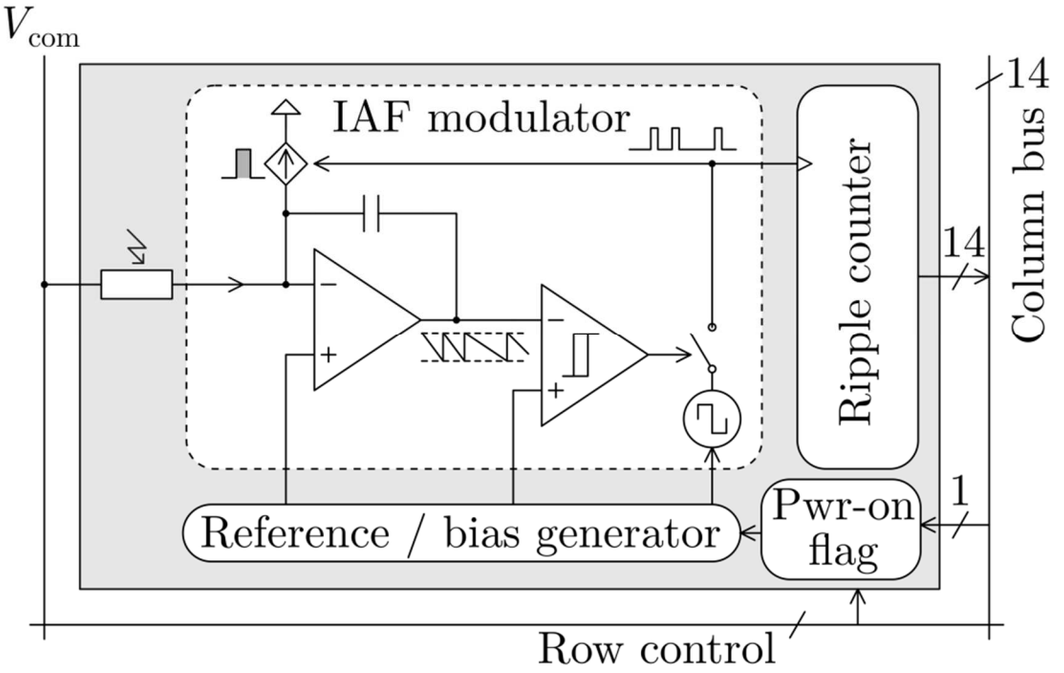
Digital Pixel Sensor Circuits

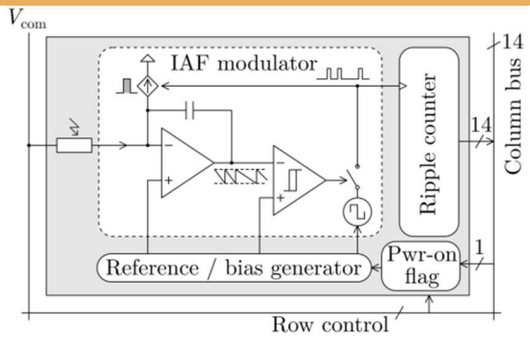
- PbSe Detector
  - 2-4 Mohm; DC biasing ~ 1 V
    dark current ~ 0.25-0.5 μA
  - Input signal full scale ~ 2 μA
  - Parasitic capacitance 0.2-1 pF

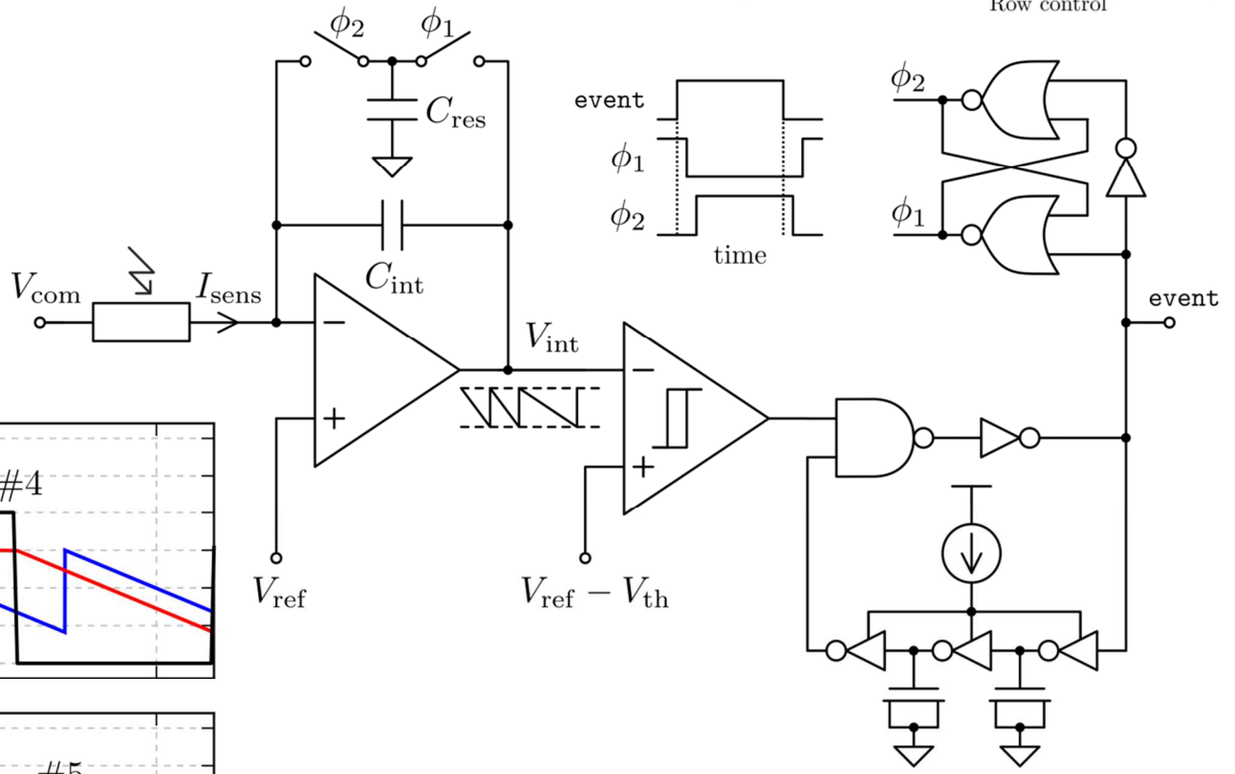


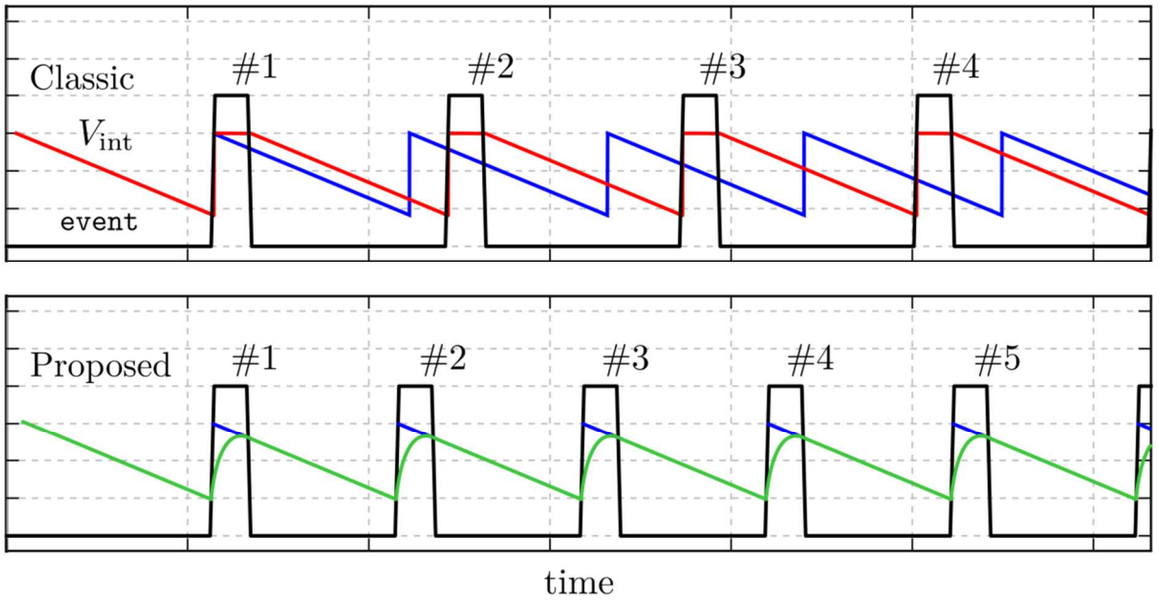
- ROIC DPS
  - In-pixel A/D conversion
    - Low power IAF modulator (up to 20Meps)
    - Digital counter (14-bit)
  - Ring oscillator
  - Local generation of reference voltages and biasing currents
  - Individual (or global) power-on → ROI

In-pixel IAF Modulator

- Low-power ideal transfer function
  - Lossless reset scheme
- Overloading protection
  - Ring oscillator



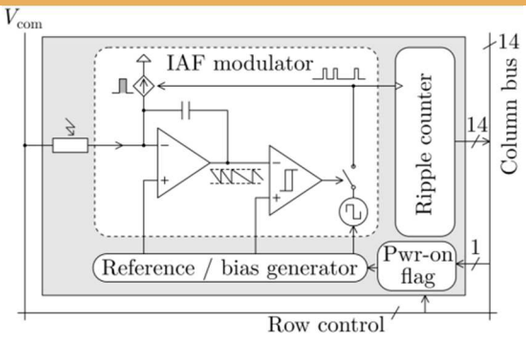


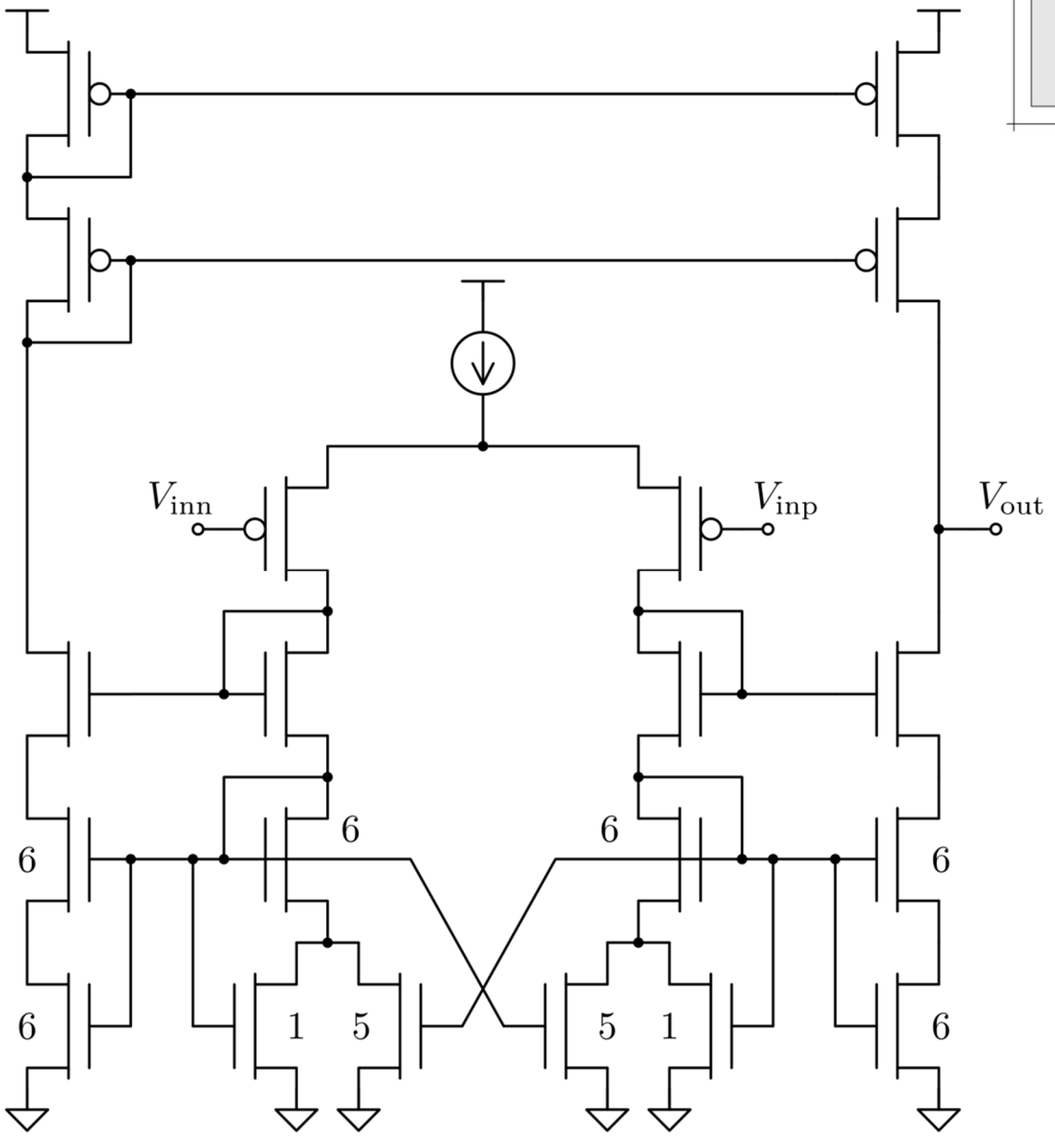


M. Dei, R. Figueras et al., "*Highly Linear Integrate-and-Fire Modulators with Soft Reset for Low-Power High-Speed Imagers*", ISCAS 2017

Low-Power OpAmp

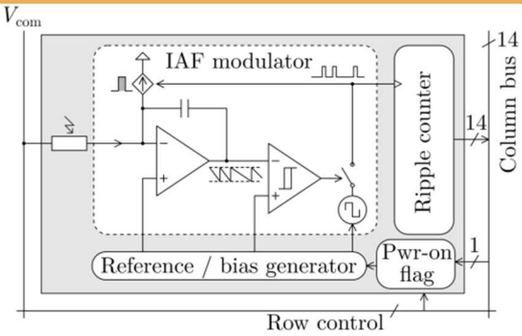
- Class-AB
- Single ended
- VMA



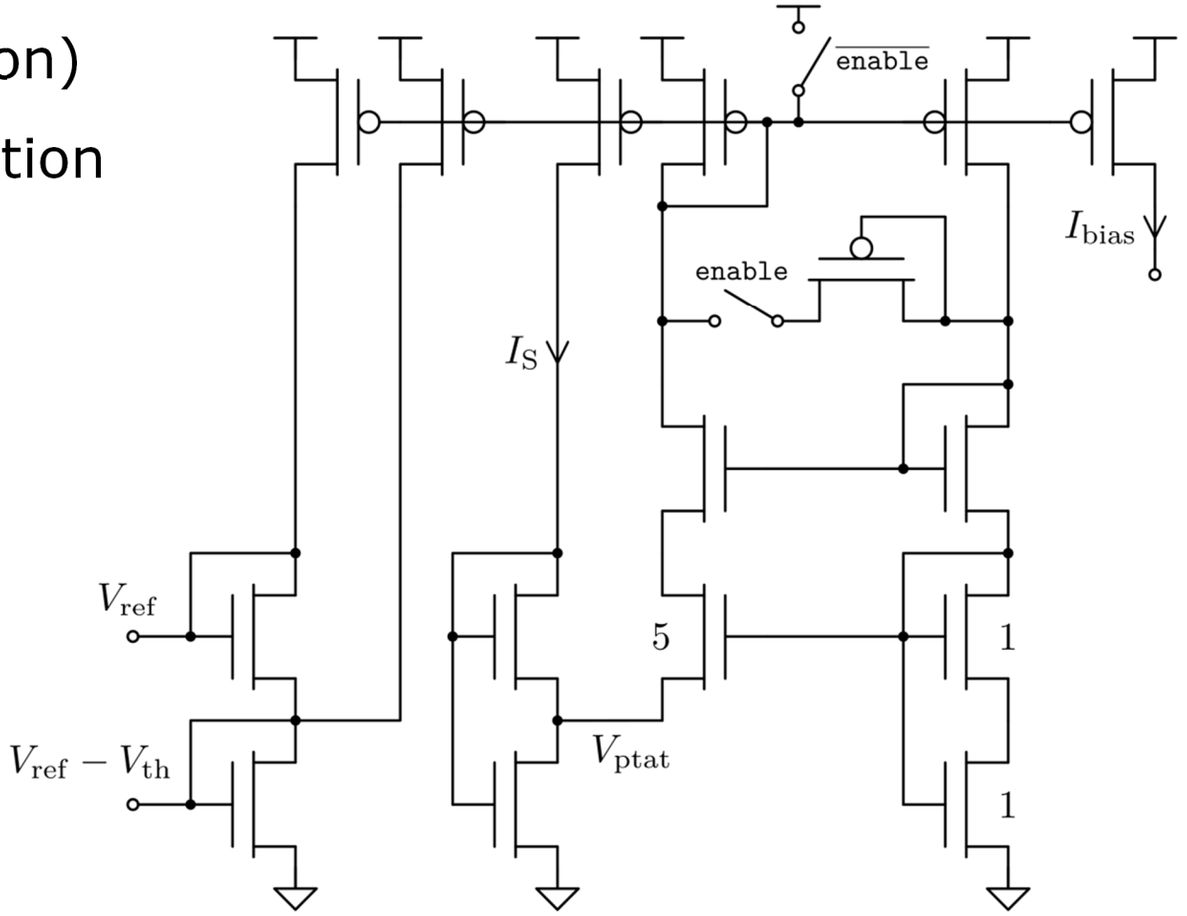


S. Sutula et al., "*Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single Stage OTAs for Low-Power SC Circuits*", ISCAS 2016

Voltage reference & biasing current generator



- Reduced crosstalk
- All-MOS
- Low-power (WI operation)
- Temperature compensation



R. Figueras et al., "*All-MOS Voltage References with Thermal Compensation*", DCIS 2013

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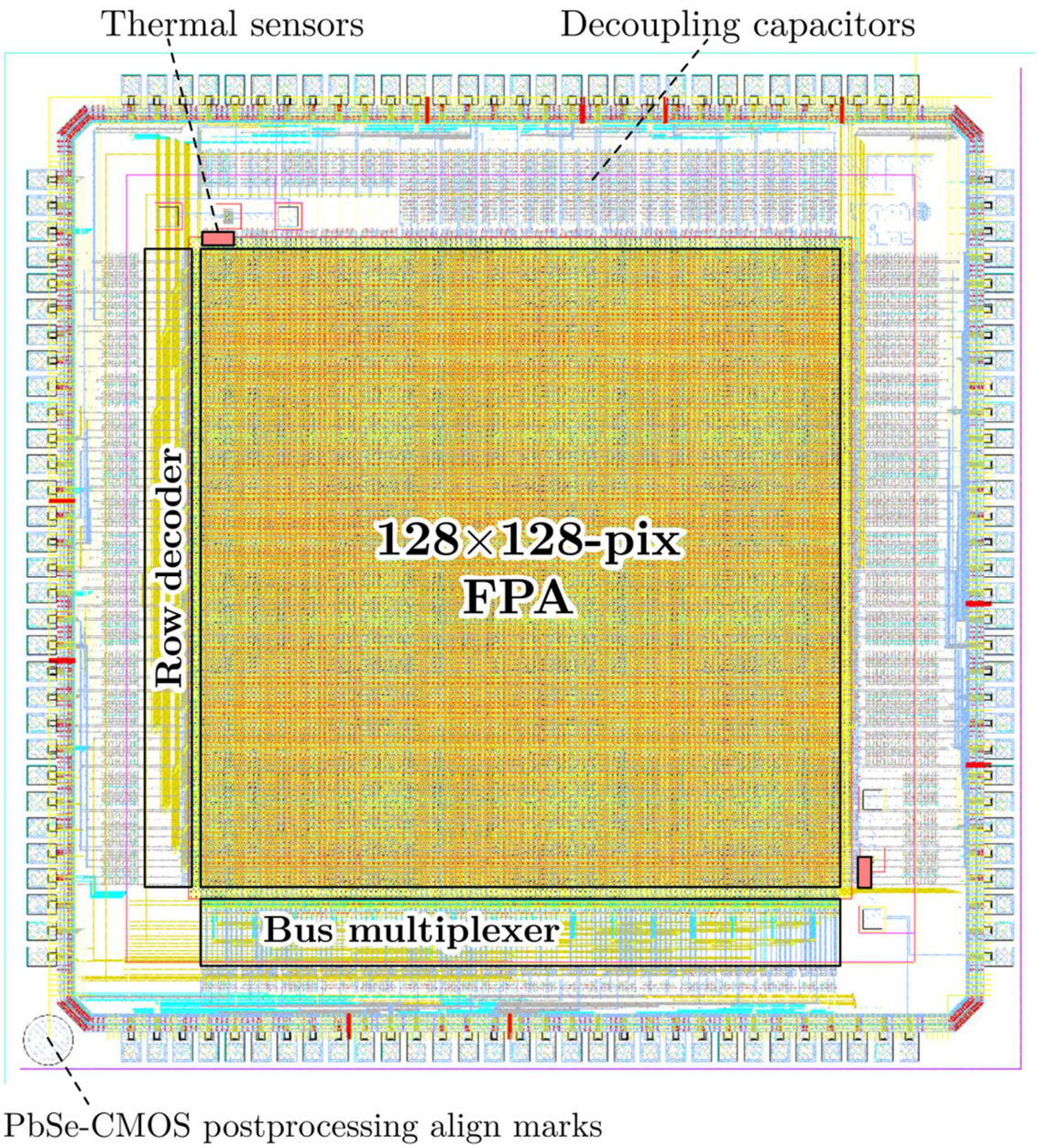
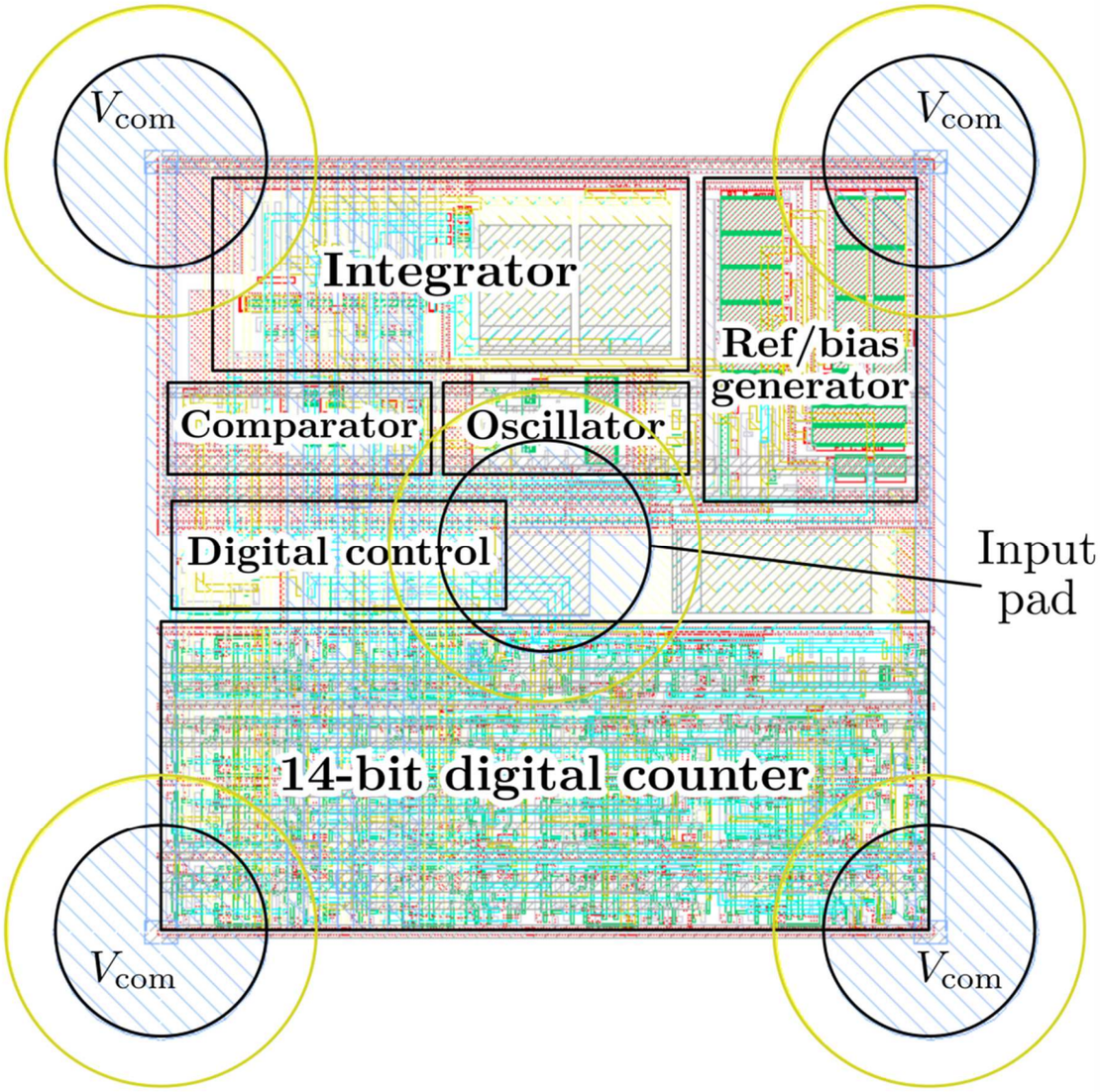
128×128-pix MWIR Imager CMOS layout floorplan

- XFAB 0.18-µm 1P6M CMOS tech.
- 10mm×10mm | 124 pads
- Multi-voltage supply
  - Analog circuits: 1.8V
  - Digital circuits: 1.2V
  - Digital I/O and ESD: 3.3V
- Circuit blocks:
  - FPA
  - Peripheral circuits
  - In-chip decoupling capacitors
- > 10 M transistors
- Global FPA column data buses
- Single/double I/O bus: 14/28-bit
- Clock speed: 50 MHz



DPS Cell CMOS layout floorplan

- 50 µm-pitch
- Separated analog/digital supplies
- 14-bit digital counter
- Low-power IAF modulator
- Overloading and overflow control
- In-pixel voltage references and biasing currents generation
- Individual disabling flag
- Continuous PbSe layer
  - Diamond pattern contacts (20µm)



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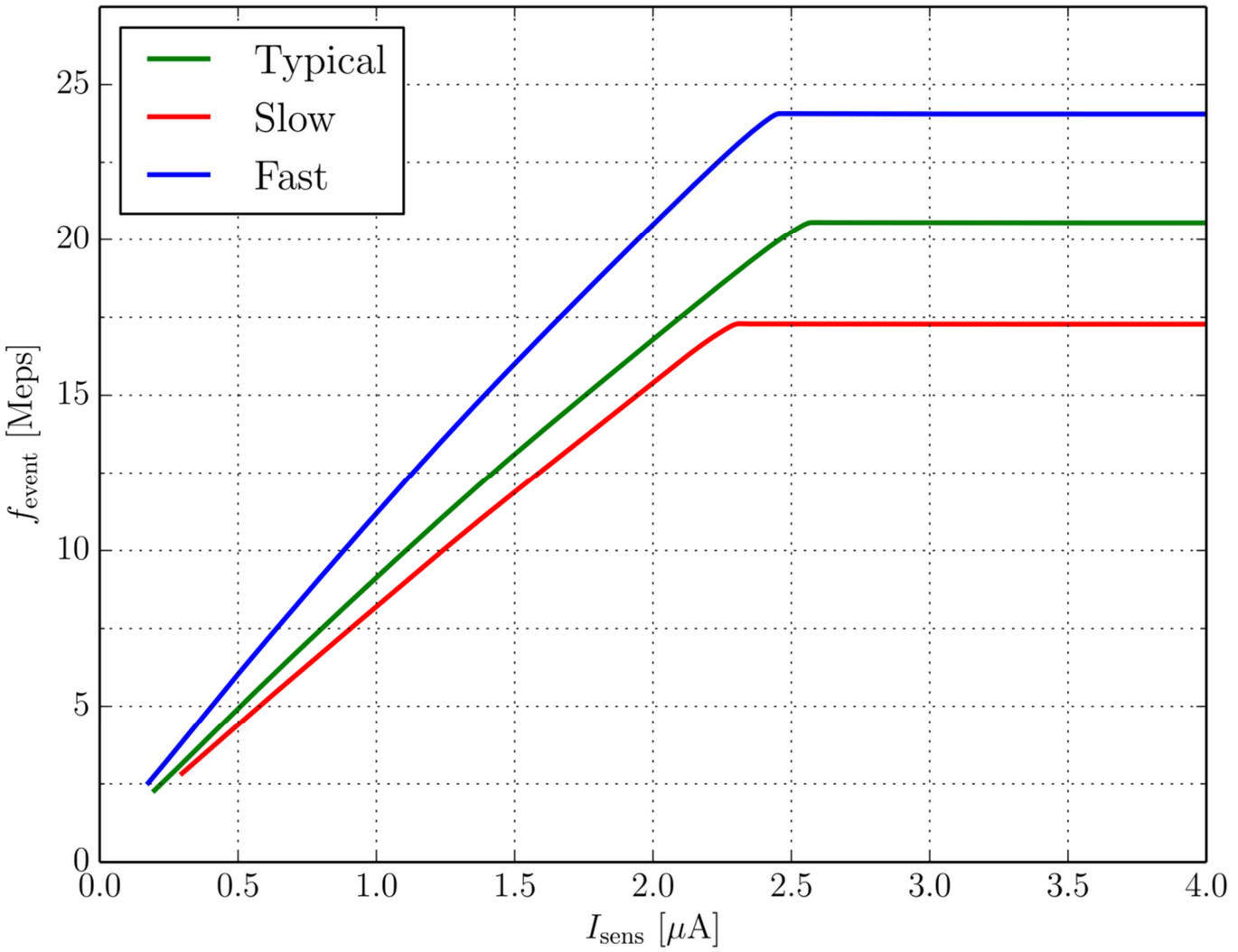
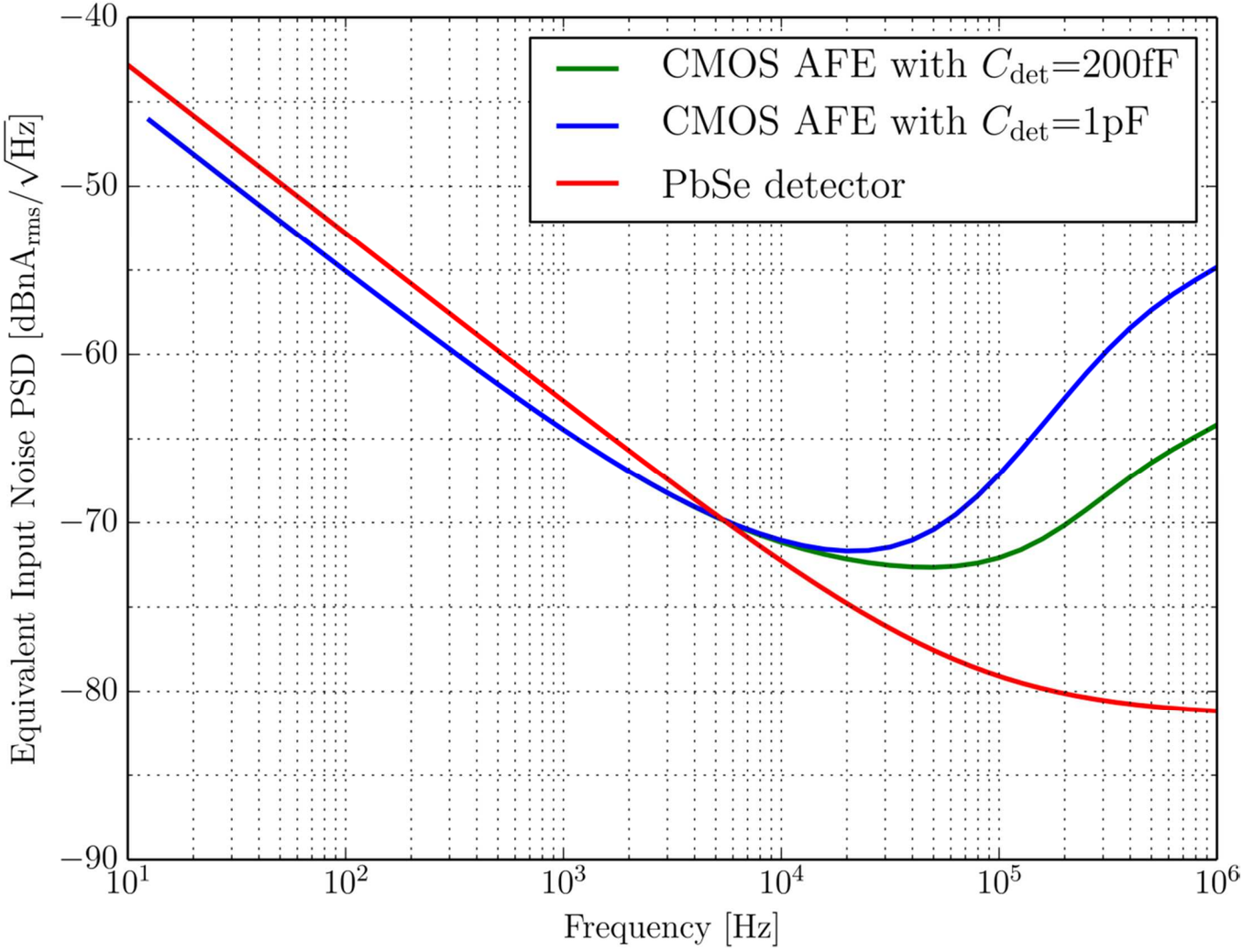
IAF Modulator transfer function

- Moderate technology variation (±15%)
- Linear up to 20 Meps
- Overloading protection



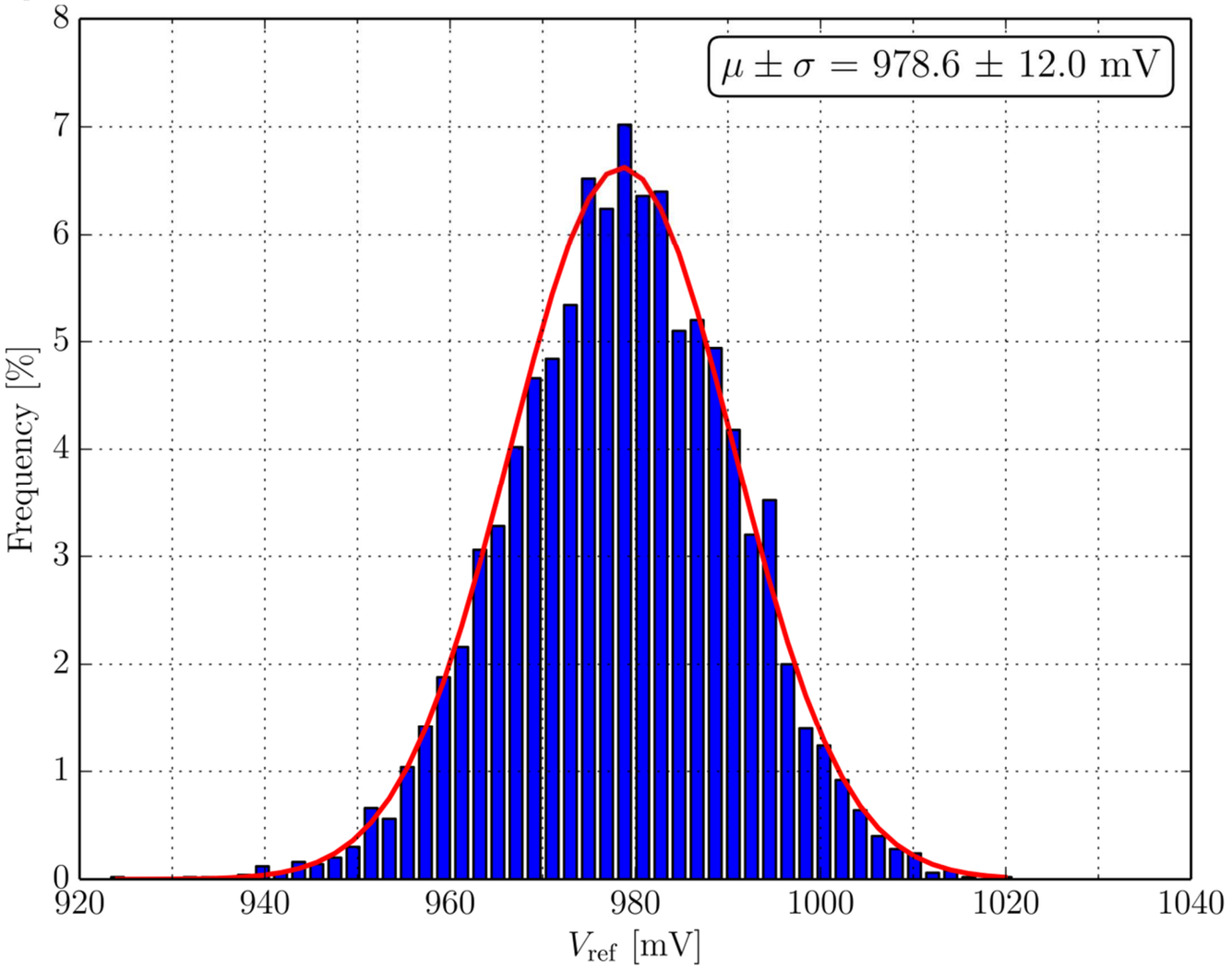
AFE Noise

- Flicker components domination
- CMOS: not the limiting factor



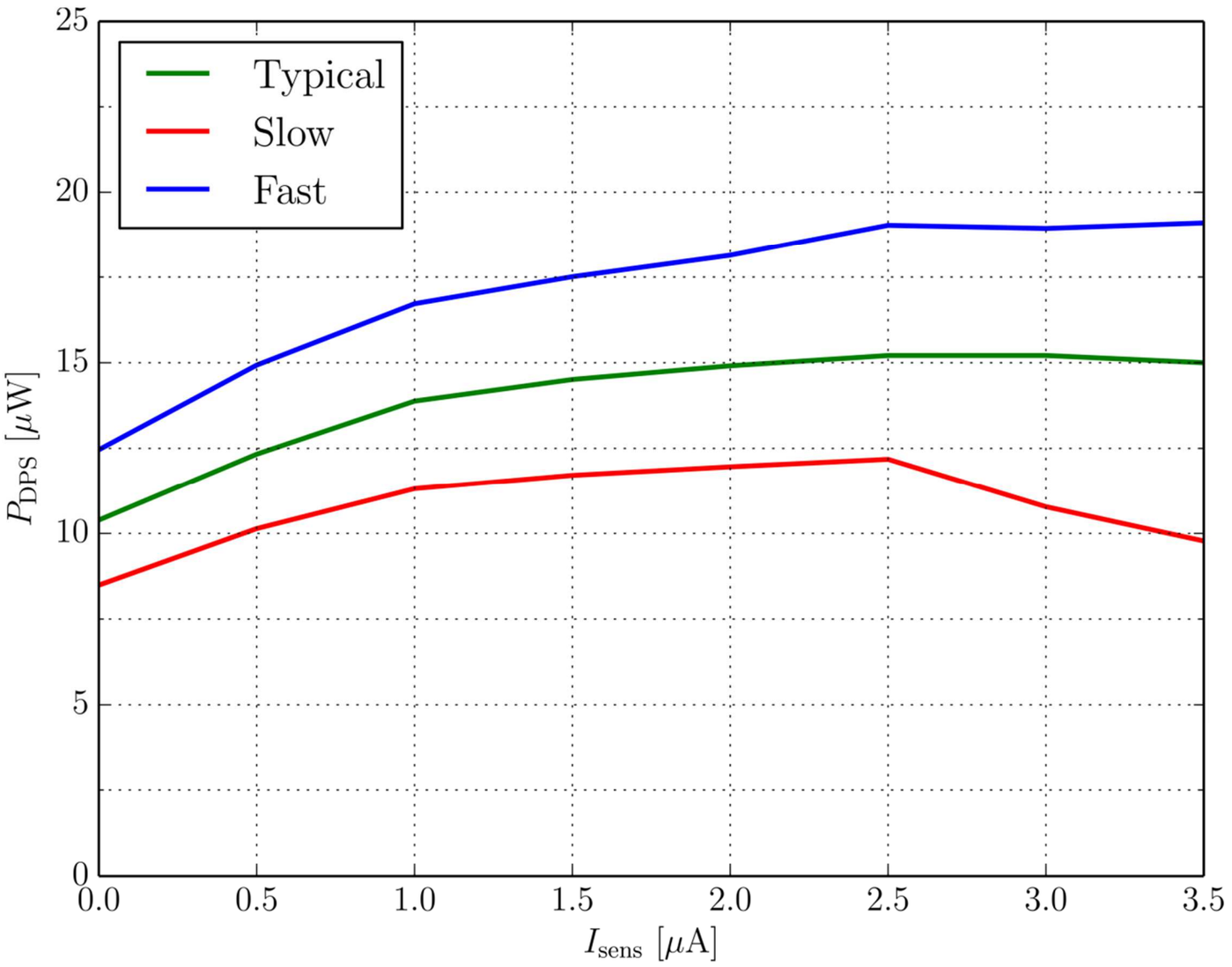
Voltage reference variability

- No inter-pixel crosstalk
- Very low dispersion (±1.2%)
- Reduced FPN



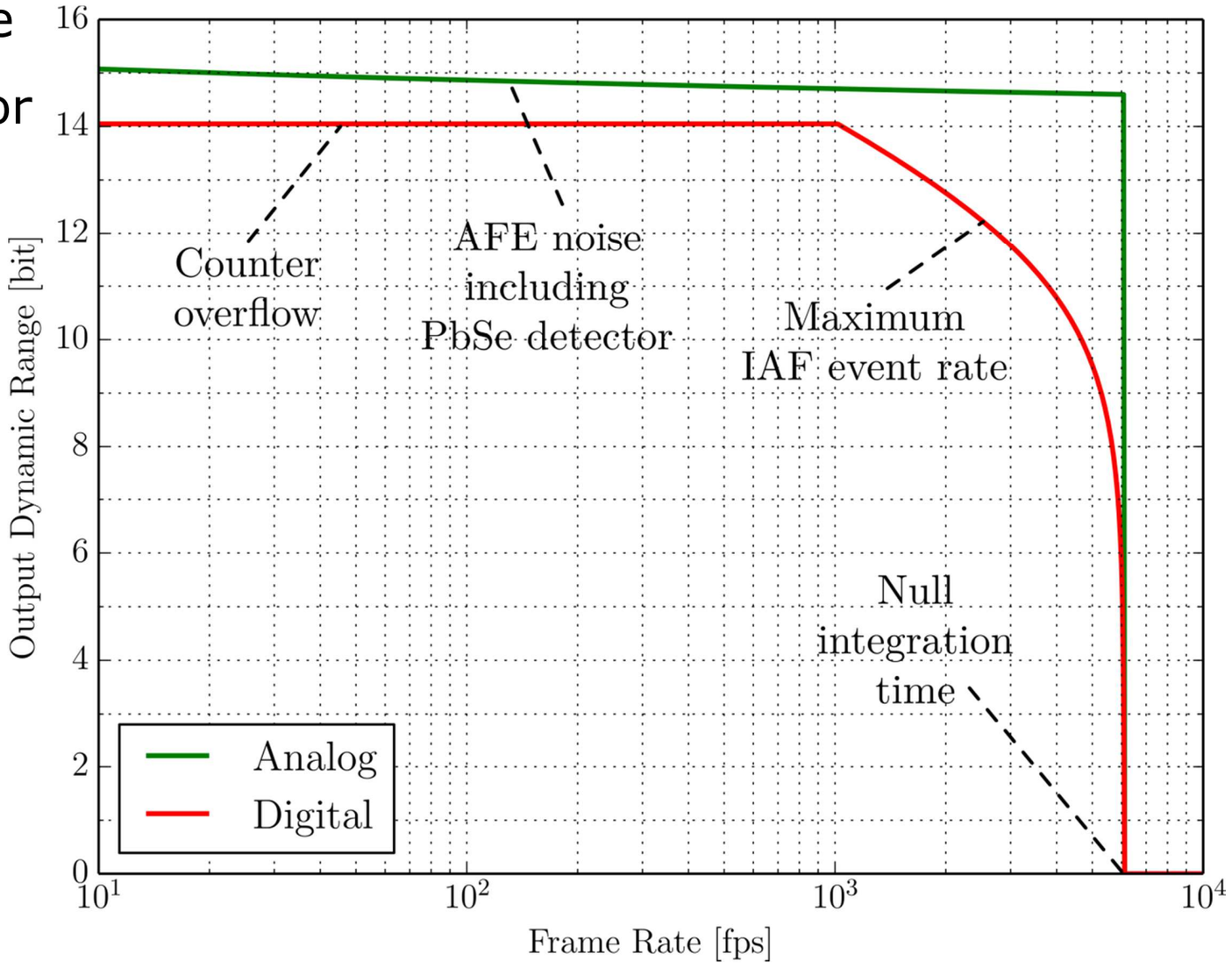
Pixel power consumption

- Dynamic power consumption below 50% of the static value
- Detector optimized
- Noticeable effect of integrator saturation



Dynamic range vs. frame rate

- <1 kfps: nominal 14-bit dynamic range limited by the digital counter
- >1 kfps: dynamic range limited by IAF modulator



State-of-the-Art

	[5]	[6]	[7]	[1]	This work
FPA pitch	640×512	82×80	640×512	80×80	128×128
Pixel pitch	50 µm	35 µm	17 µm	135 µm	50 µm
CMOS tech.	0.35 µm	0.18 µm	0.5 µm	0.35 µm	0.18 µm
IR tech.	InGaAs	µbol.	µbol.	VPD PbSe	VPD PbSe
IR wavelength	SWIR	LWIR	LWIR	MWIR	MWIR
Integration	hybrid	monolithic	monolithic	monolithic	monolithic
Pixel output	digital	analog	analog	digital	digital
Imager output	12 bit	12 bit	14 bit	10 bit	14 bit
Max. frame rate	60 fps	120 fps	60 fps	2000 fps	**4000 fps**
Supply voltage	3.3 V	1.8 V	3.3/5 V	3.3 V	1.2/1.8/3.3 V
Static power	n.a.	50 mW	n.a.	1 µW/pix	10 µW/pix

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Presented Work

- CMOS-ROIC for an uncooled IR Imager using a PbSe Detector.
- Integrated in the XFAB 0.18-µm CMOS technology.
- 128×128-Digital-pixels FPA.
- Industrial prototype ready to be integrated to the camera.

Contributions

- In-pixel A/D conversion: low-power & highly-linear IAF modulator.
  - 20 Meps.
  - Overloading protection.
- CMOS low-noise circuits (not the limiting factor).
- In-pixel references generation.
  - Very low dispersion (1.2%).
  - Global / individual pixel disabling.
- Low-power consumption: static ~ 10µW/pix; dynamic < 50% of static.
  - Efficient class-AB OpAmp.
  - MOS WI operation.
  - IAF modulator with novel soft-reset mechanism.
- High output dynamic range.
  - 14-bit at 1 kfps; 10-bit at 4 kfps.
- Compact design: 50µm-pitch pixel.

...thanks for your attention!

State-of-the-Art

- [5] Y. M. Jo, D. H. Woo, S. G. Kang, and H. C. Lee, "*Very Wide Dynamic Range ROIC With Pixel-Level ADC for SWIR FPAs*", IEEE Sensors J., vol. 16, no. 19, pp. 7227–7233, Oct 2016.
- [6] Y. Park, J. Yun, D. Park, S. Kim, and S. Kim, "*An Uncooled Microbolometer Infrared Imager With a Shutter-Based Successive- Approximation Calibration Loop*", IEEE Trans. VLSI Syst., vol. 26, no. 1, pp. 122–132, Jan 2018.
- [7] D. Liu, W. Lu, Z. Chen, Y. Zhang, S. Lei, and G. Tan, "*A 14- bit Differential-Ramp Single-Slope Column-Level ADC for 640512 Uncooled Infrared Imager*", in Proceedings of the IEEE International Symposium on Circuits and Systems, May 2016, pp. 1922–1925.
- [1] J. M. Margarit, G. Vergara, V. Villamayor, R. Gutierrez-Alvarez, C. Fernandez-Montojo, L. Teres, and F. Serra-Graells, "*A 2 kfps Sub- W/Pix Uncooled-PbSe Digital Imager With 10 Bit DR Adjustment and FPN Correction for High-Speed and Low-Cost MWIR Applications*", IEEE J. Solid-State Circuits, vol. 50, no. 10, pp. 2394–2405, Oct 2015.