Design methodology for Power-Efficient SC Delta-Sigma Modulators Based on Switched-VMAs

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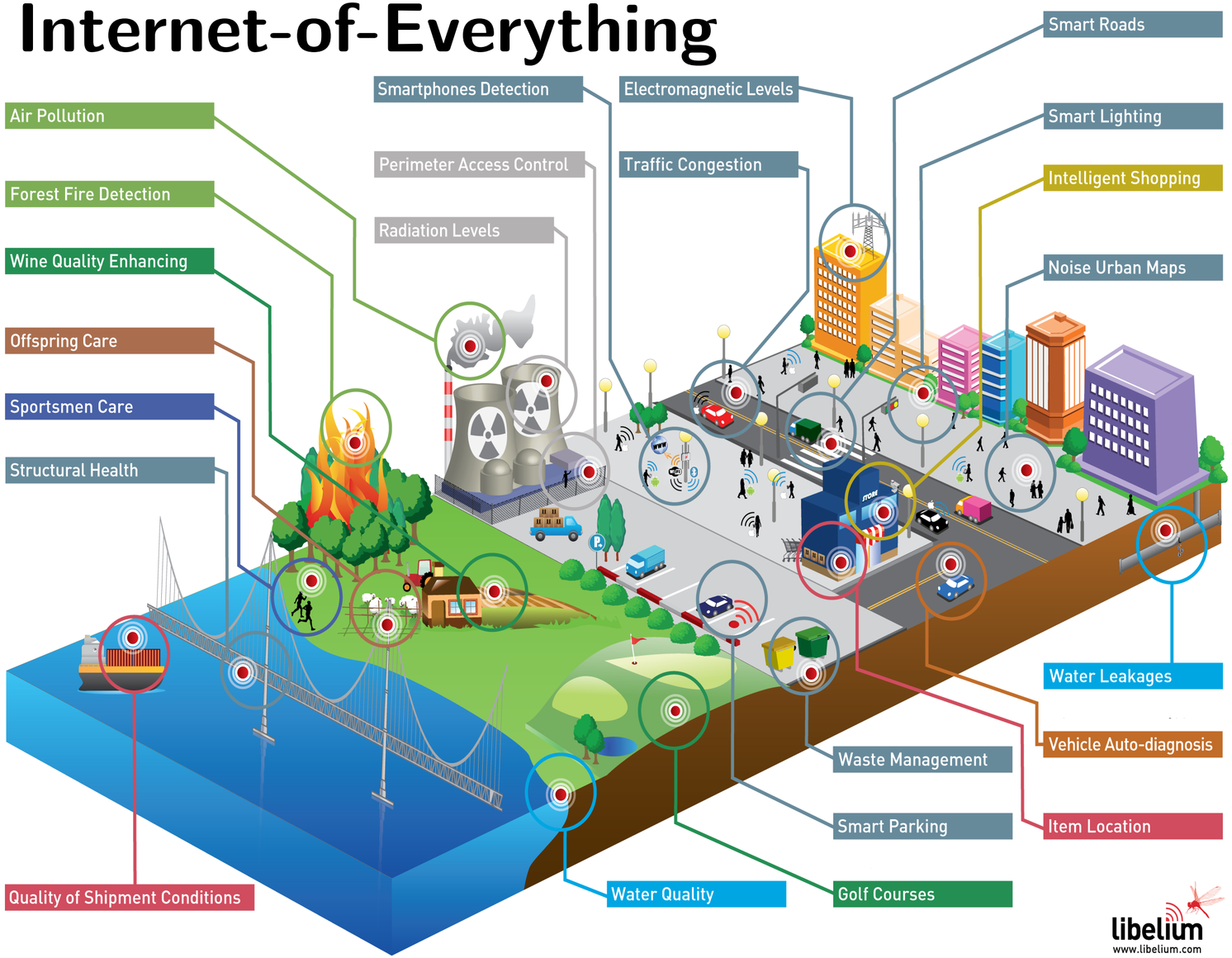
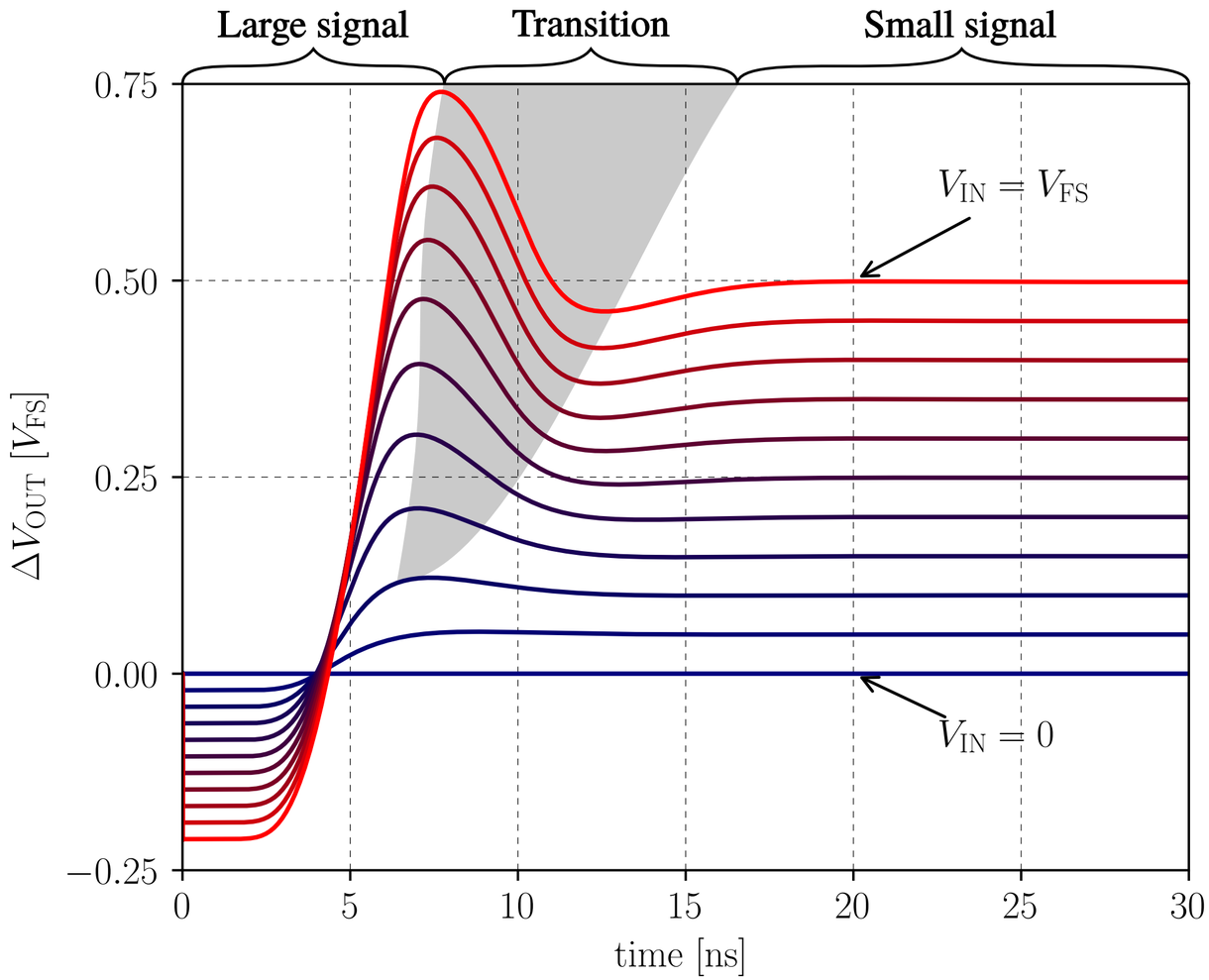
Internet-of-Everything



- IoE market : 10$ trillion revenue, 100 billion conected devices by 2025
- IoE is where the physical world connects to the digital
- Includes sensors, converters, processors and transcievers
- Power efficiency is the keypoint
- Novel techniques and design methodologies are required
- ADC Converters in IoE requirements:
  - Medium-to-low bandwidth signals
  - Medium-to-high resolutions
  - Low power consumption

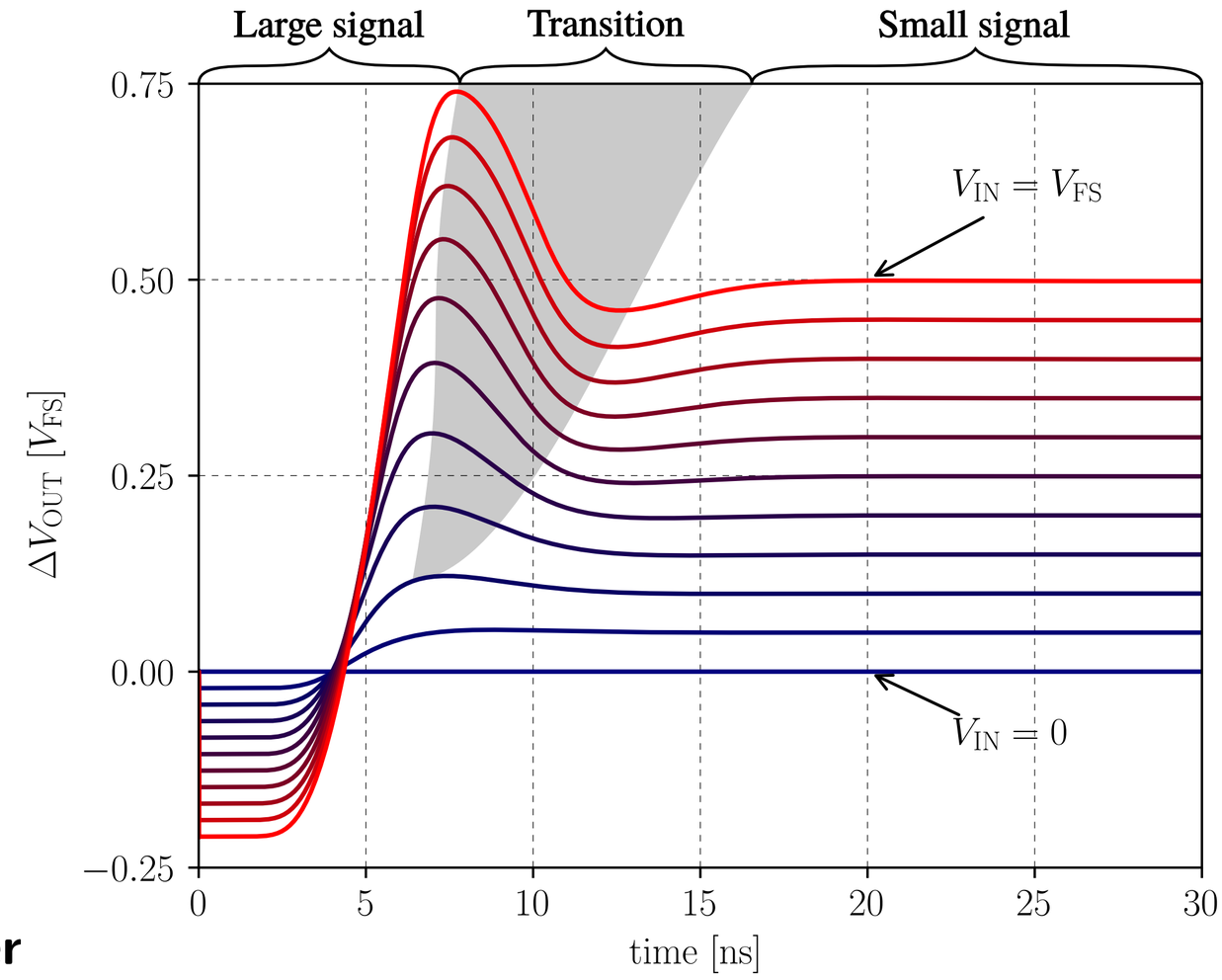
SC-DSM design based on Class-AB OpAmp drawbacks

- Simulation time represents a **bottleneck**
- Simulation time depends on the environment abstraction level
- Class AB operation difficult to model



SC-DSM design based on Class-AB OpAmp drawbacks

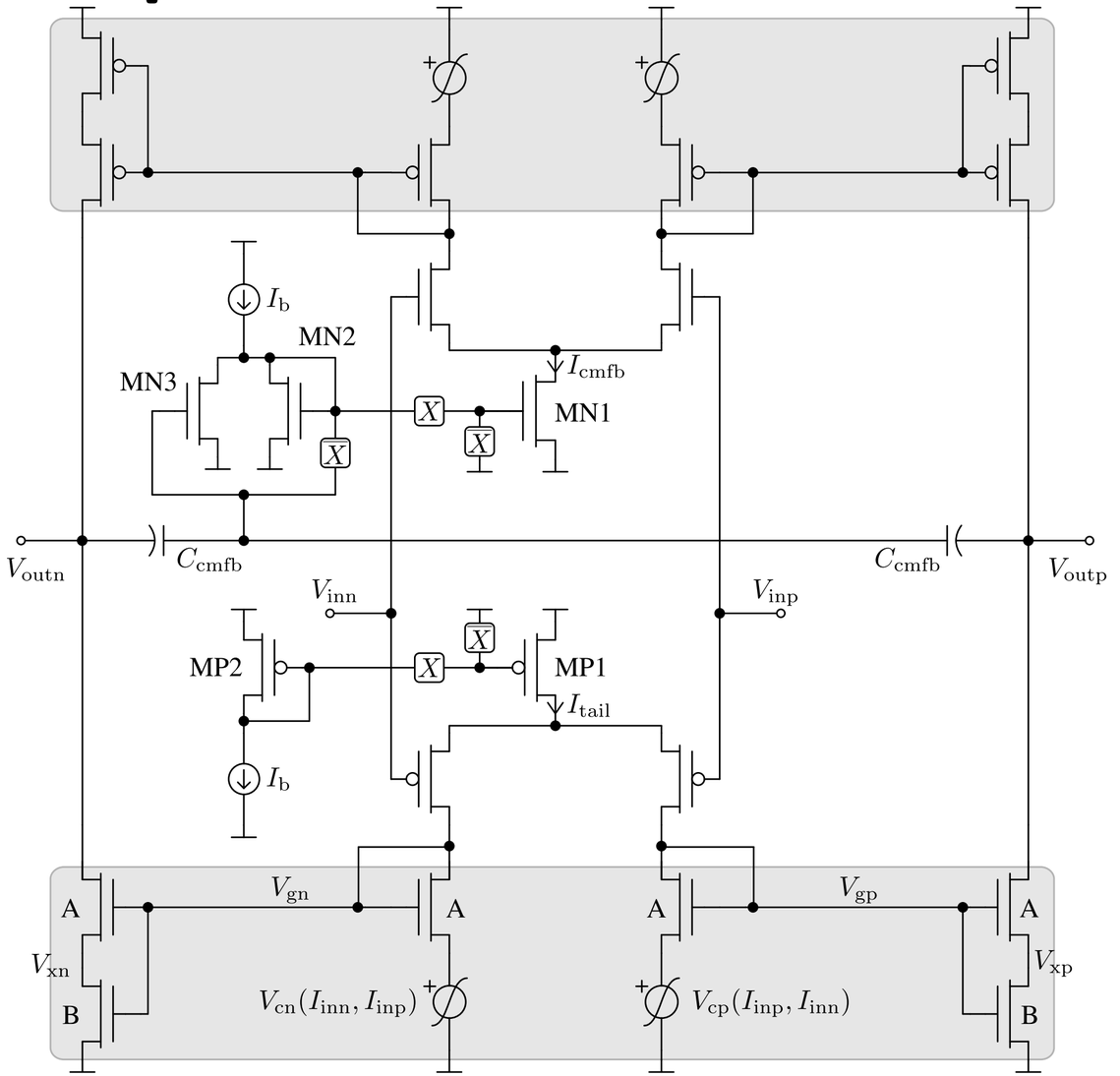
- ▼ Simulation time represents a **bottleneck**
- ▶ Simulation time depends on the environment abstraction level
- ▼ Class AB operation difficult to model
- ▶ Classic methodologies:
  - Top-Down with sub-cells segmentation
  - Prone to errors during the specification translation phase
  - Can generate unrealizable specifications



▲ **Fast** novel **design methodology** allowing for **power optimization** while accounting circuit related effects is needed

Class-AB Switched-Variable Mirror Amplifiers

- Class-AB allows for Low static current consumption
- Fully differential architecture.
- CMFB control through the NMOS pair tail
- 50% power consumption in switched-OpAmp operation
- All Class-AB current generated at the ouput branches
- Two types of non-linear voltage control variable gain current mirrors



Class-AB Switched-Variable Mirror Amplifiers

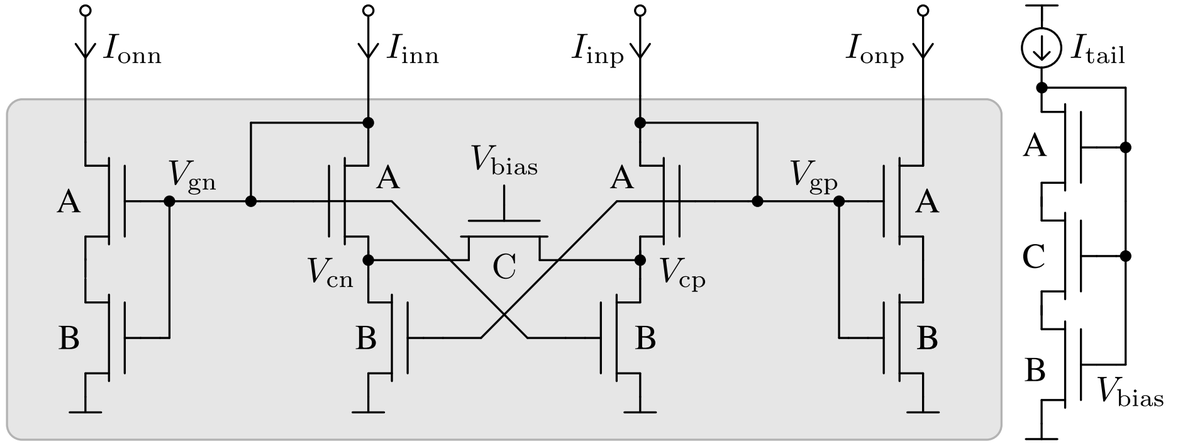
- Fully differential voltage-controlled non-linear current amplifiers
- Two competing Neg/Pos loops
- A, B and C labels represents the multiplicity
- Class-AB coefficient for all regions:

$$K_{\mathrm{AB}} \doteq \frac{I_{\max}}{I_{\mathrm{tail}}} = \begin{cases} 1 + \dfrac{\mathrm{AB}}{\mathrm{C(A+B)}} & \text{Type I} \\ 1 + \dfrac{\mathrm{AB}}{\mathrm{C(A+B+C)}} & \text{Type II} \end{cases}$$

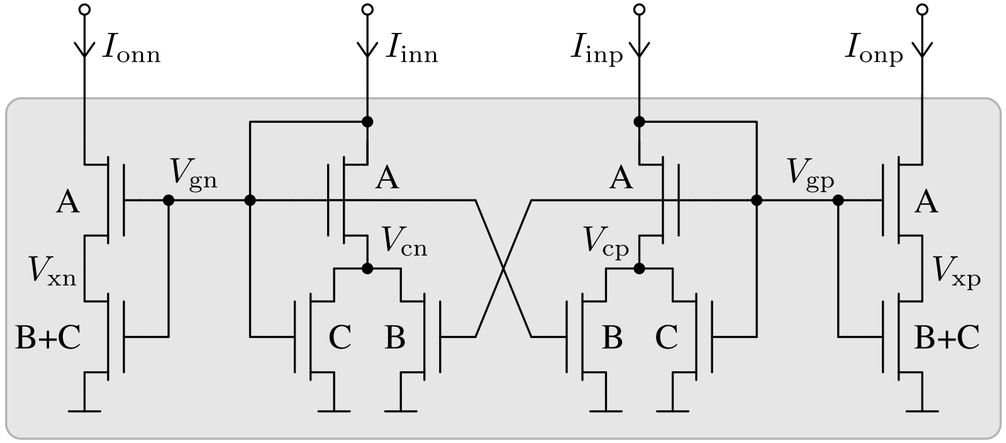
- Good rule of thumb A = B + C

$$K_{\mathrm{AB}} \simeq 1 + \frac{B/C}{2}$$

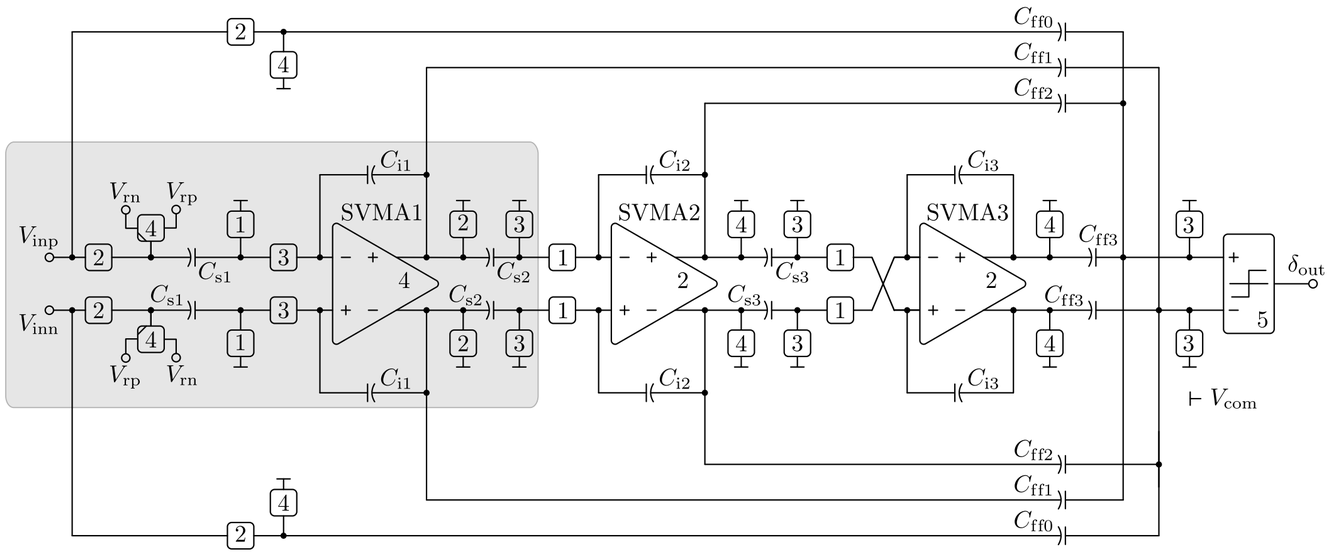
TYPE I

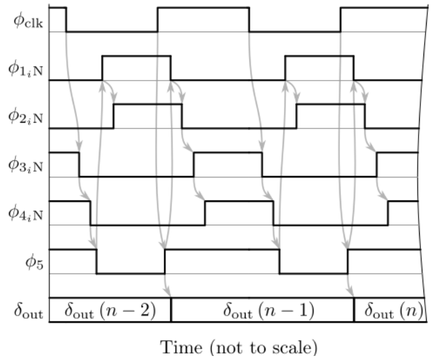


TYPE II



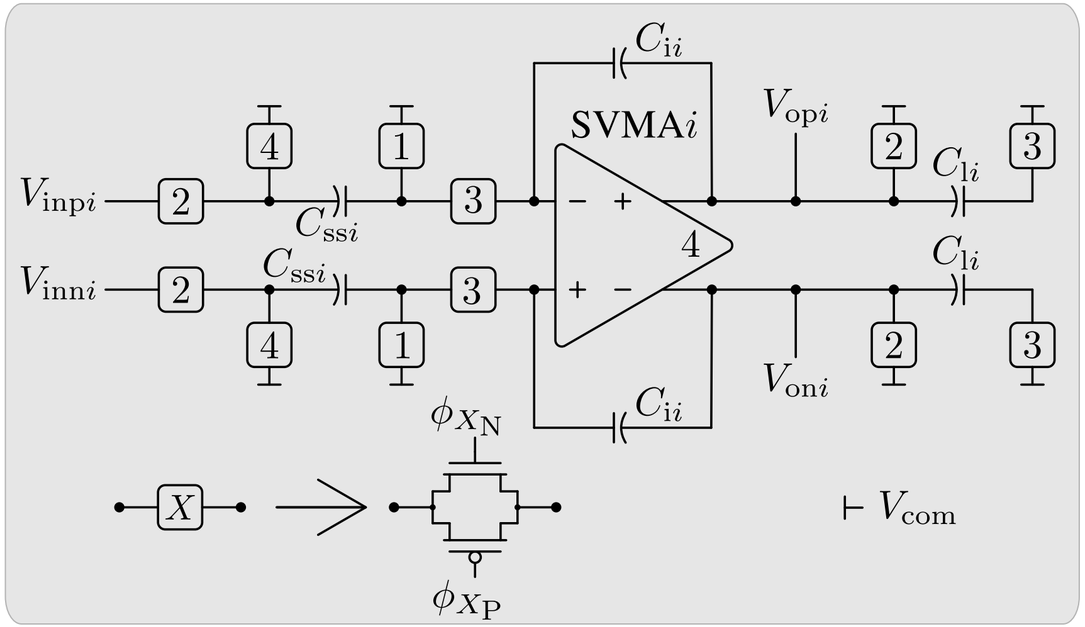
Reduced Switched-VMA Testbench





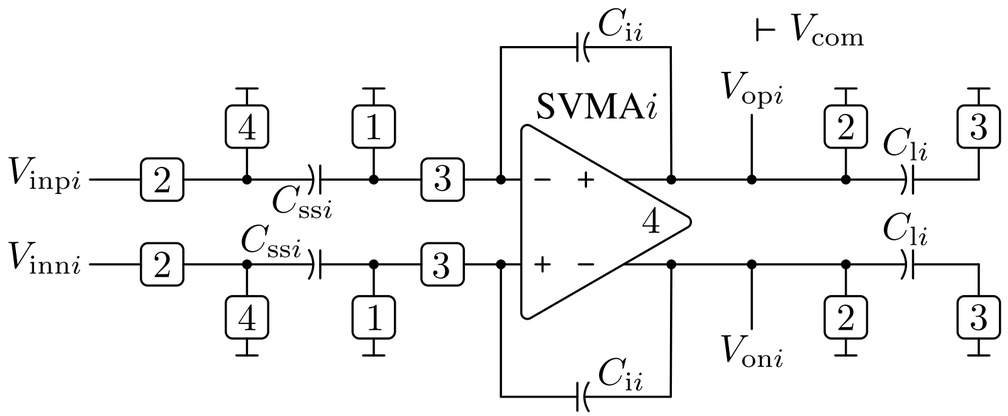
- Same **boundary conditions** and operating points
- **Faster** than a complete DSM electrical simulation

- Reduced electrical Testbench



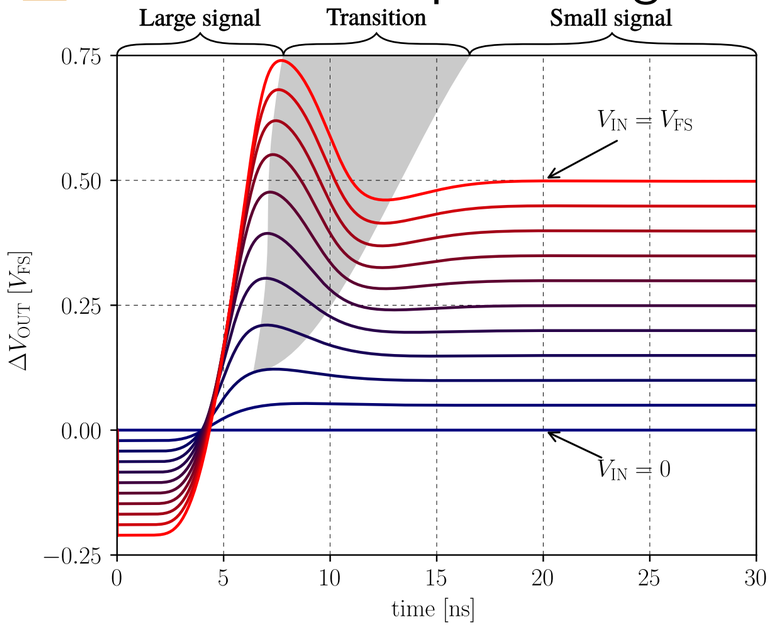
Reduced Switched-VMA Testbench

- Reduced electrical TB



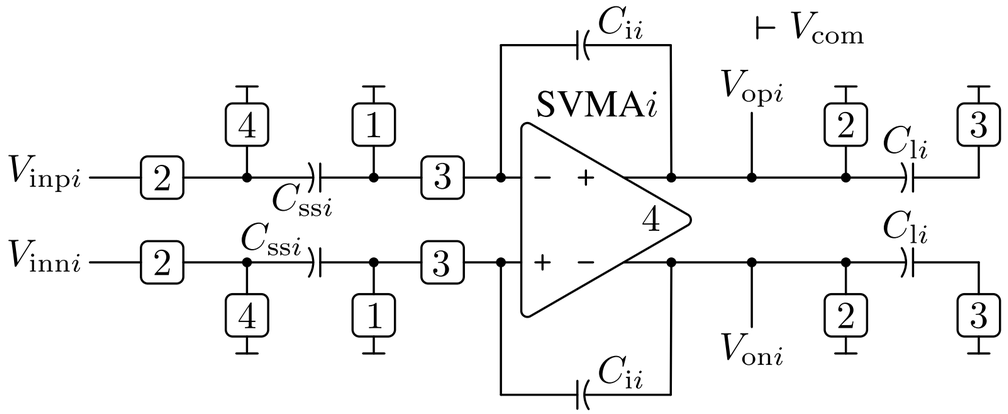
- Differential input is fixed for each charge transfer
- Settling transfer curve generated by sampling at the end of phase 4

- Differential output voltage



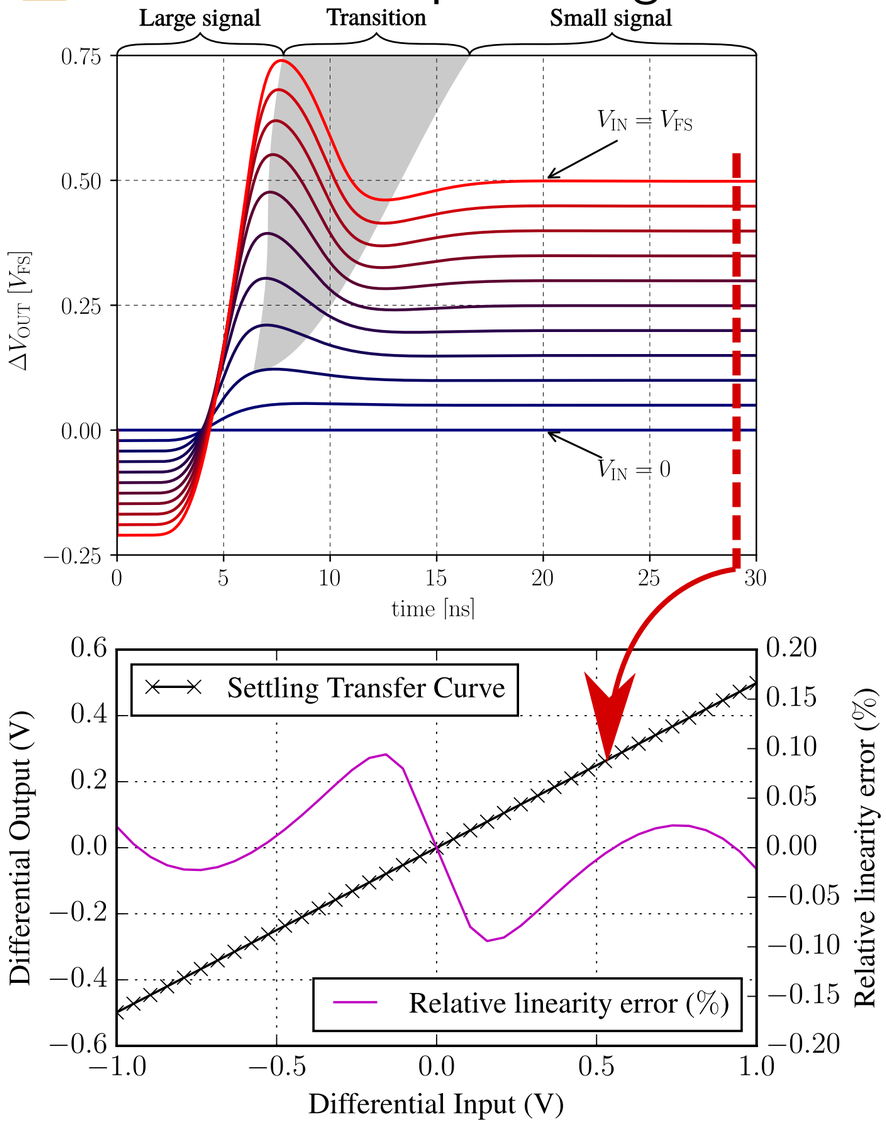
Reduced Switched-VMA Testbench

Reduced electrical TB



- Differential input is fixed for each charge transfer
- Settling transfer curve generated by sampling at the end of phase 4
- The **settling transfer curve** accounts for the OpAmp **non-idealities**
- **Simulation time** is up to ~**15 min** per settling curve

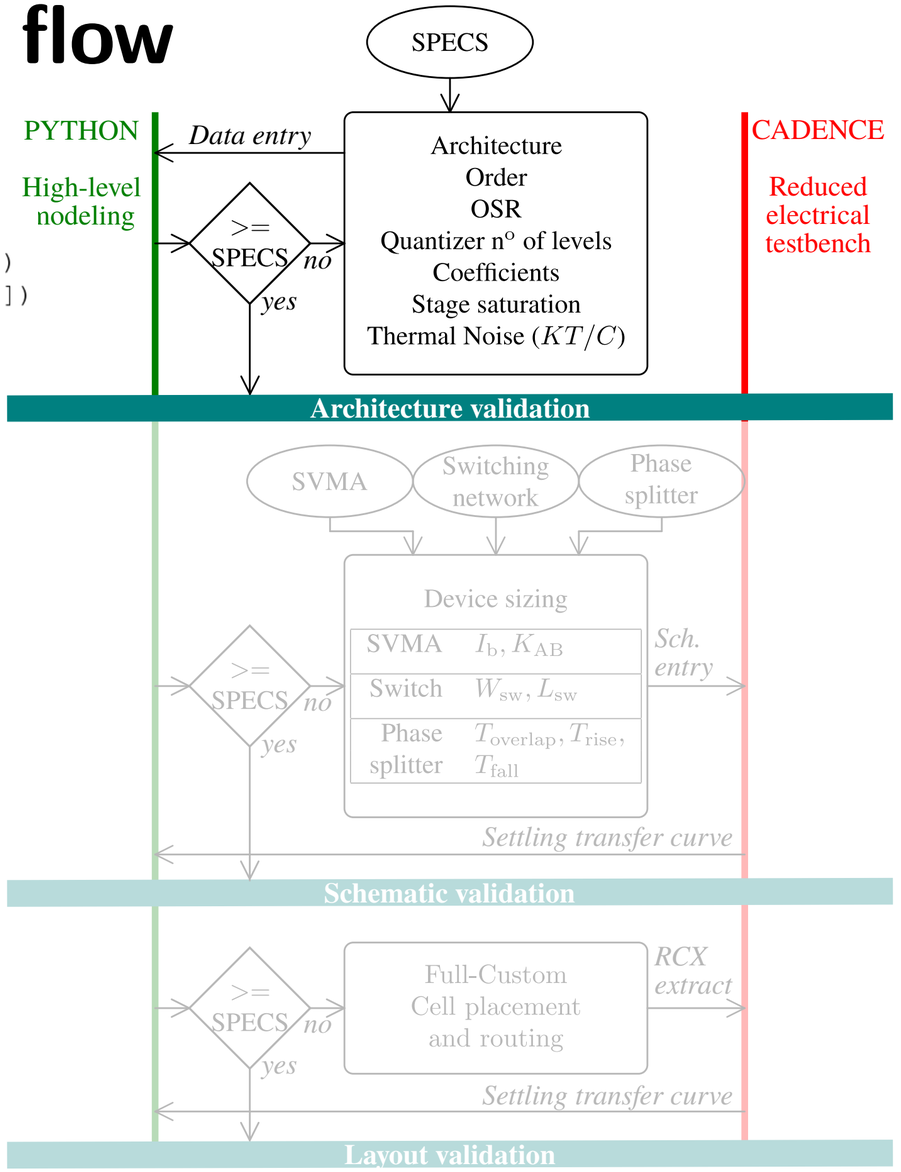
Differential output voltage



Methodology design flow

DSM code

```
for k in range(0, nsamples):
    X1[k] = X1[k - 1] + a1*(X[k - 1] - Y[k - 1])
    X2[k] = X2[k - 1] + a2*(X1[k - 1] - Y[k - 1])
    Y[k] = 1 if X2[k] >= 0 else -1
```



- Fast architecture validation using the high-level environment
- High-level simulation platform developed in Python

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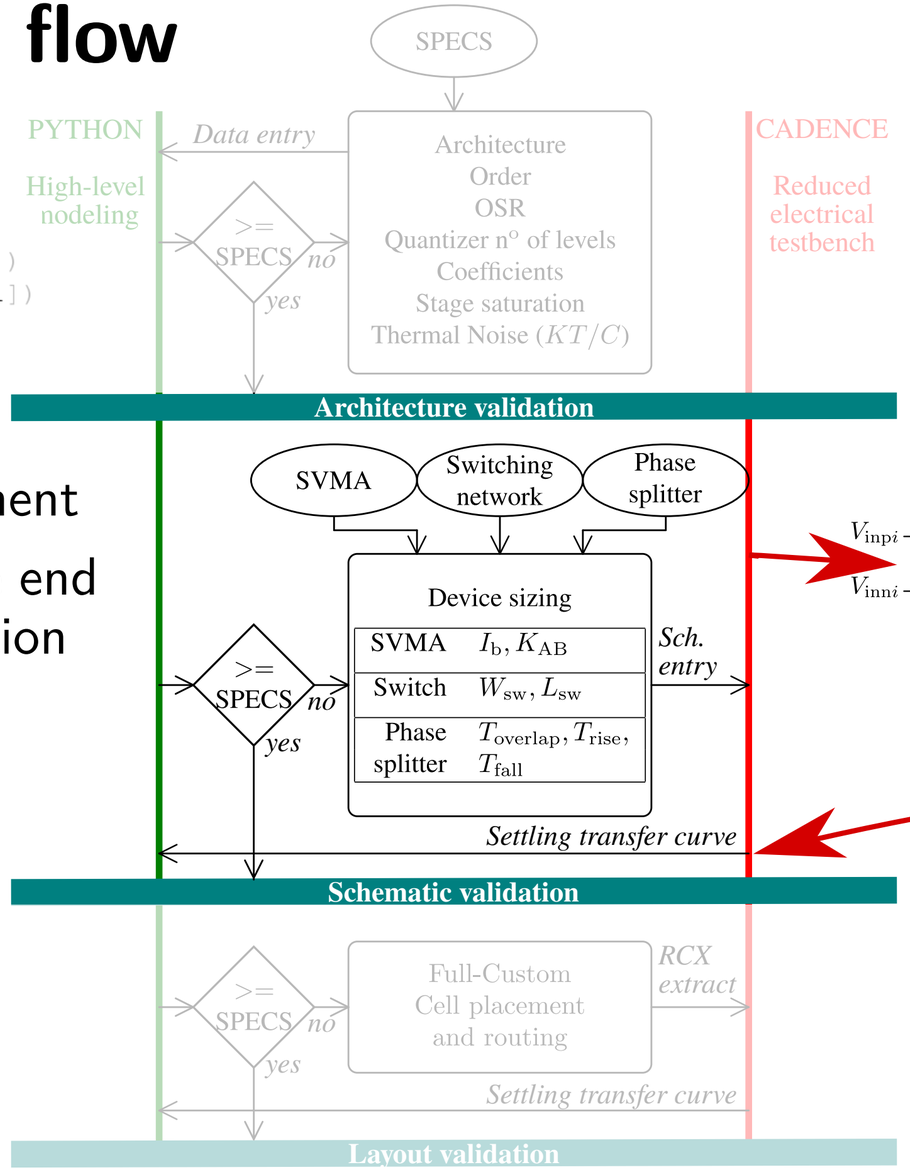
- Extracted settling transfer curve feed into the high-level environment
- DSM electrical simulation at the end of each schematic/layout validation
- Simulation time reduction from ~7days to ~15 min



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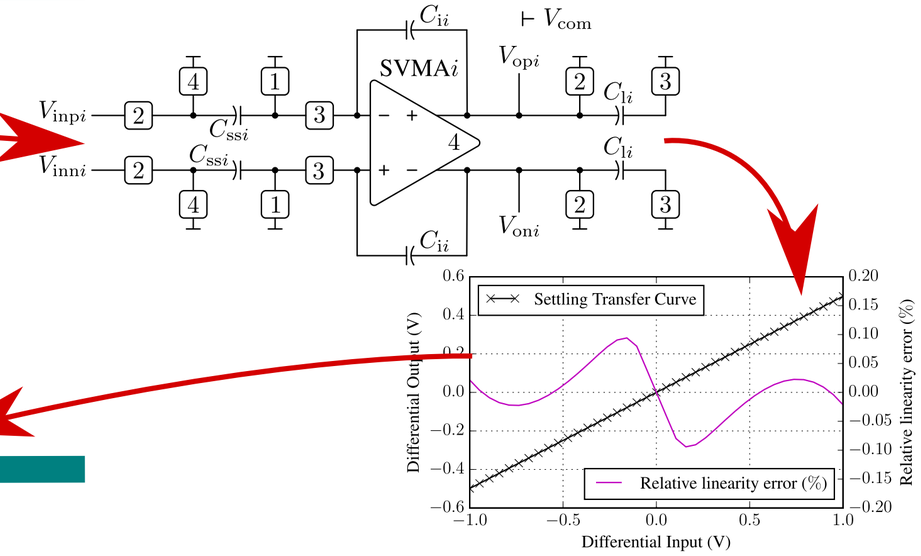

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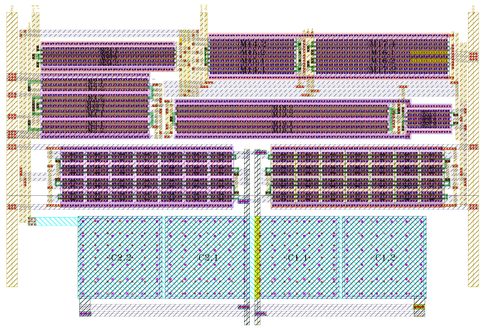

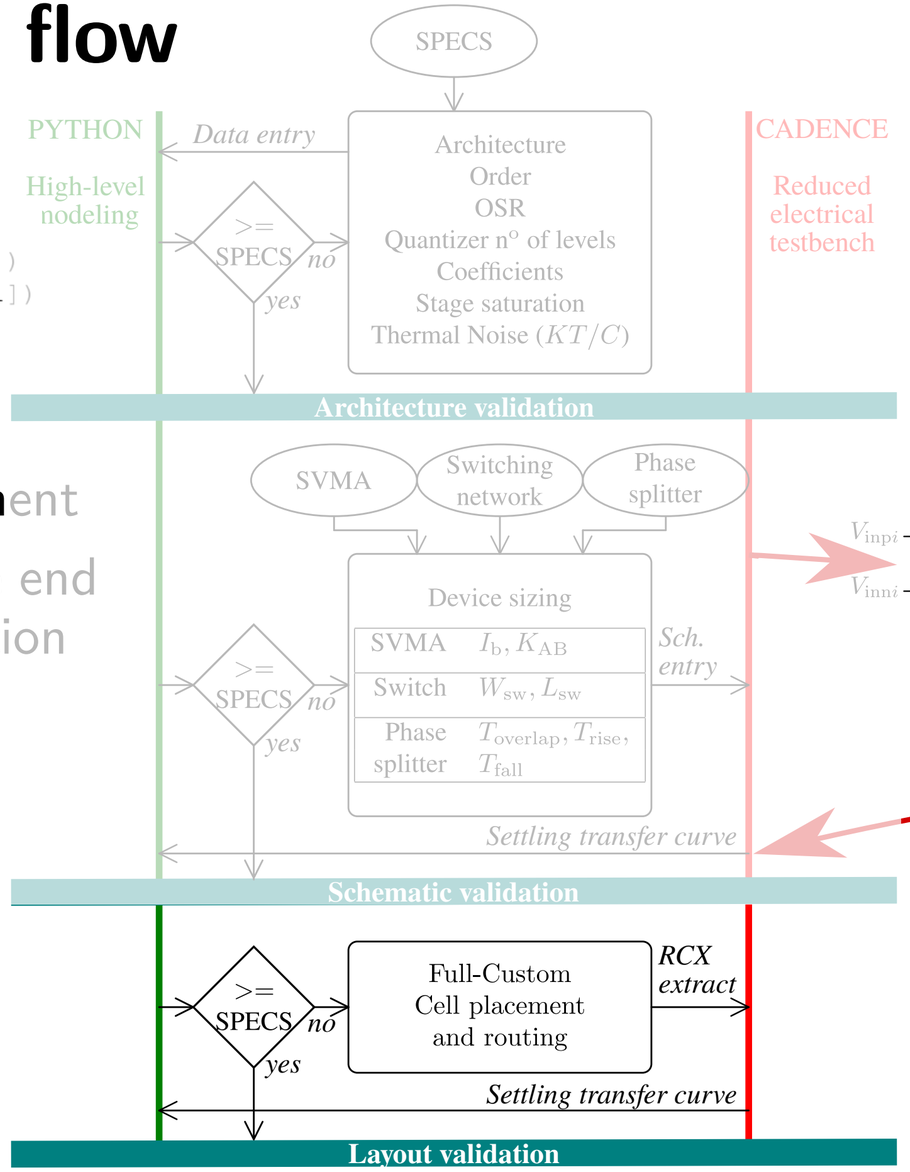

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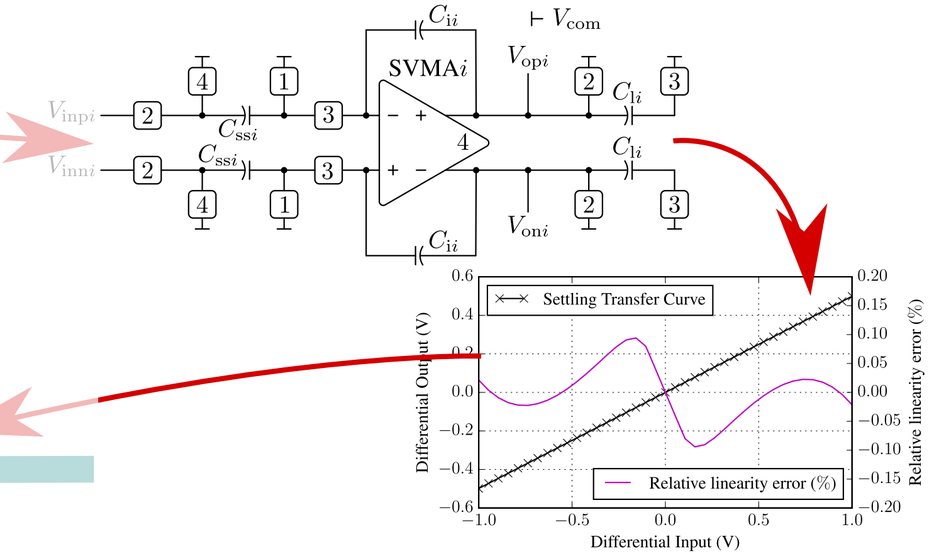
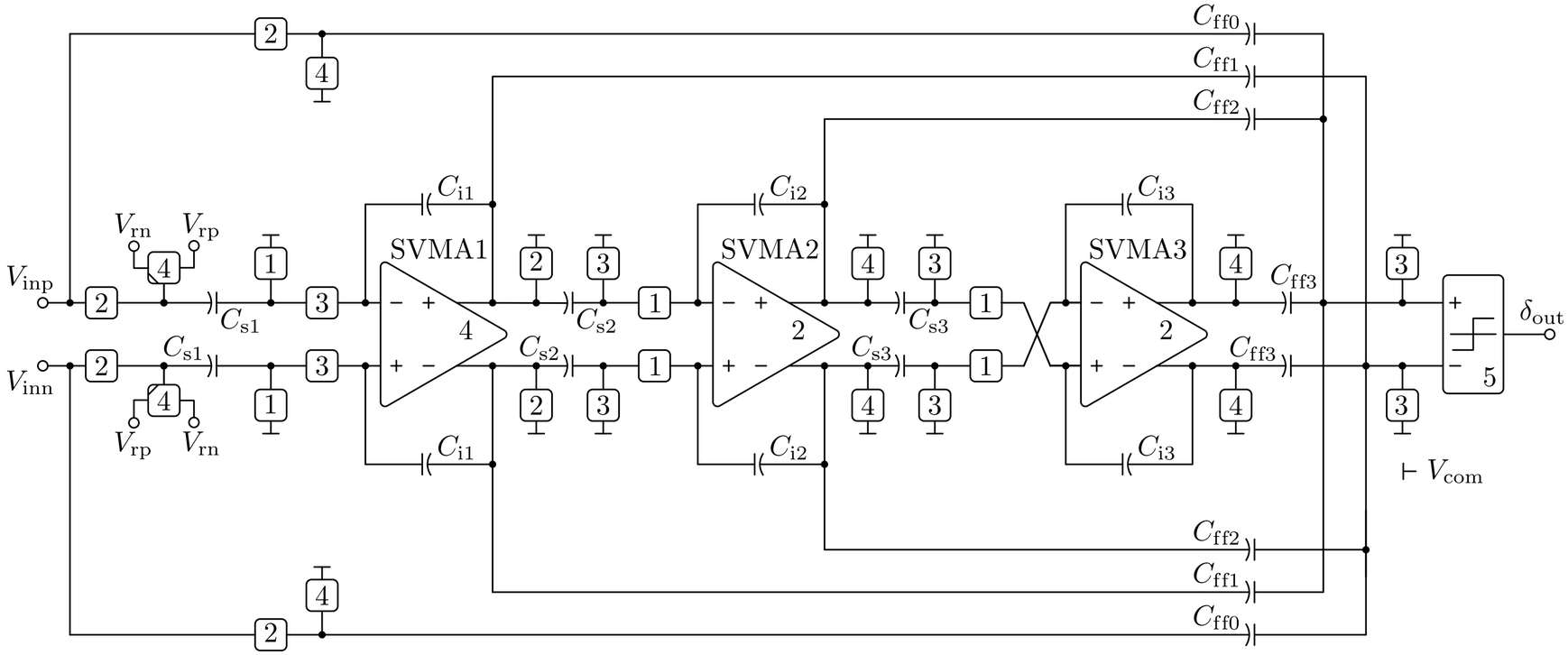
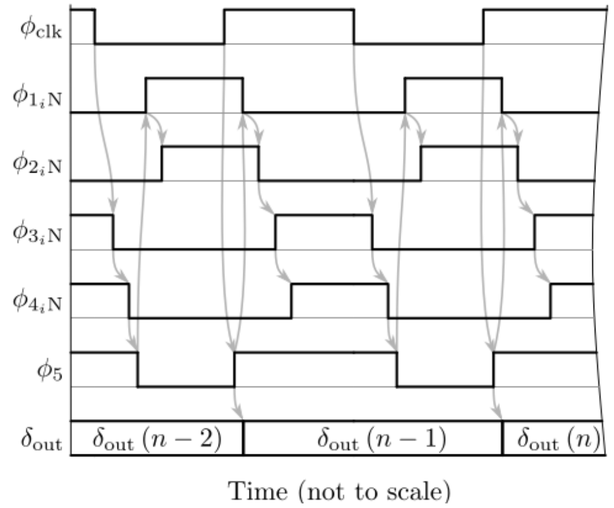


- Layout validation process follows the same iteration flow

Design Case: 16-bits 50-kHz Bandwidth SC-DSM ADC

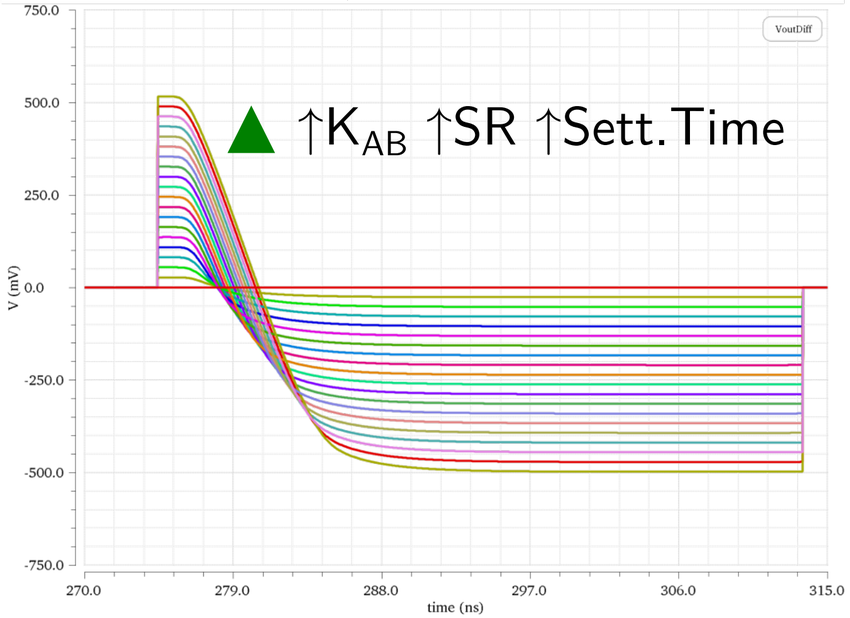




- Architecture validation:
  - 3rd order feedforward single-loop and single-bit architecture
  - OSR = 128
  - Integrator coefficients [0.5,0.2,0.5]
  - Feedforward coefficients [1,1,1]

Design Case: K_{AB} vs Ib trade-off

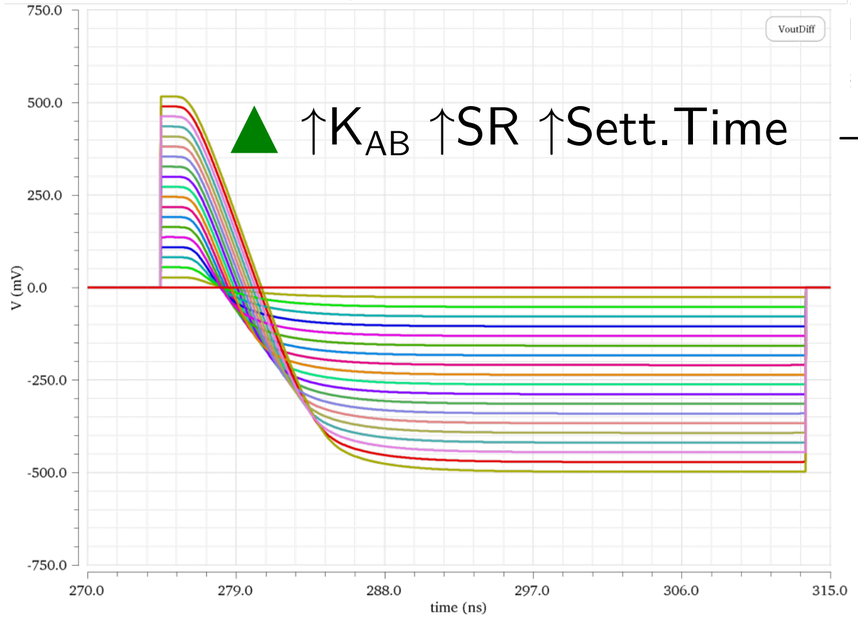
- Goal ↓Ib

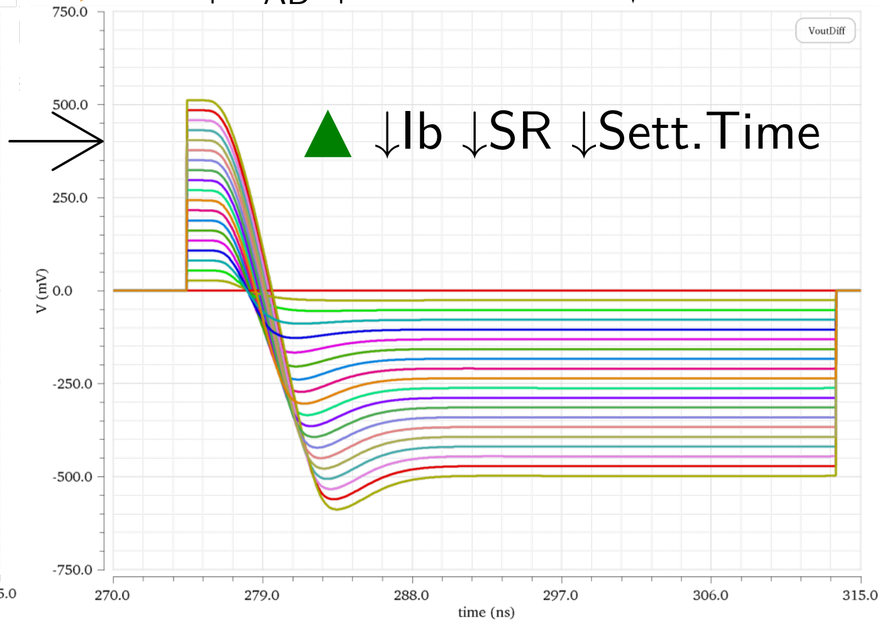


- ↑K_{AB} ↑SR ↑Sett.Time

Design Case: K_{AB} vs Ib trade-off

- Goal ↓Ib
- If ↑K_{AB} ↑Over-shoot ↓Sett. time





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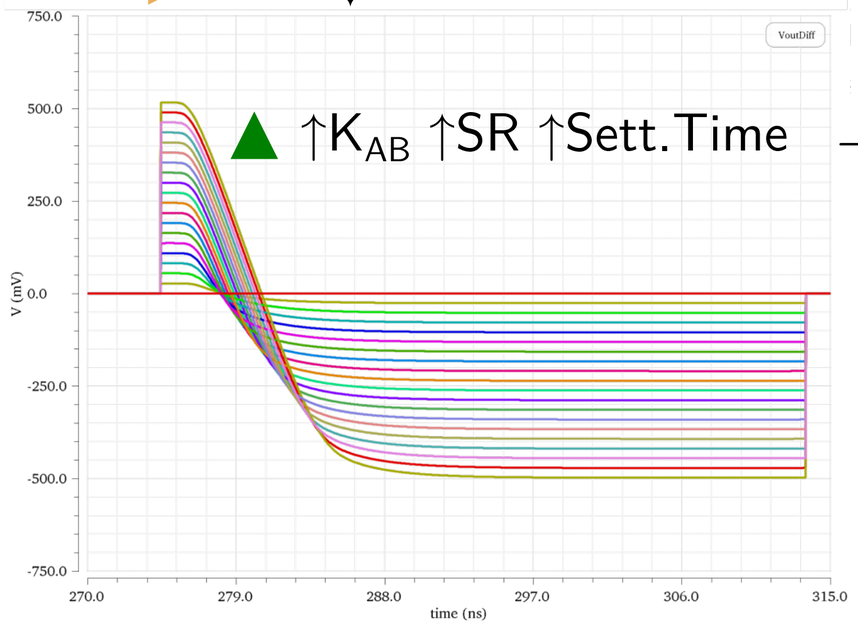

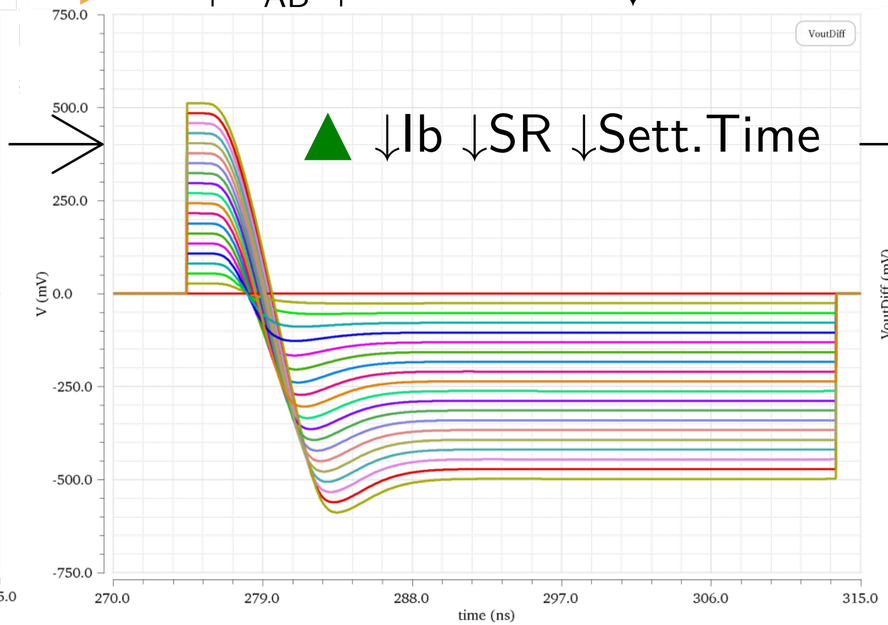

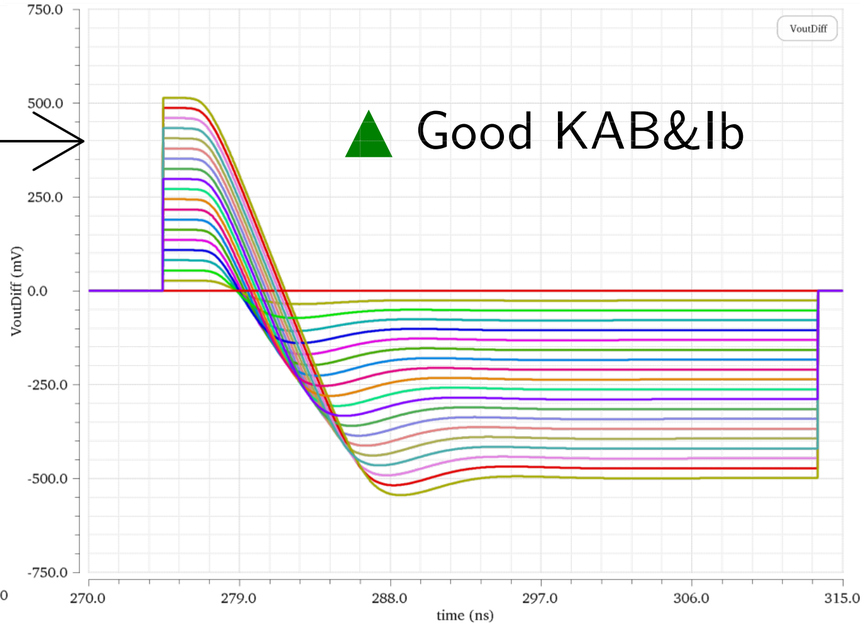

Design Case: K_{AB} vs Ib trade-off

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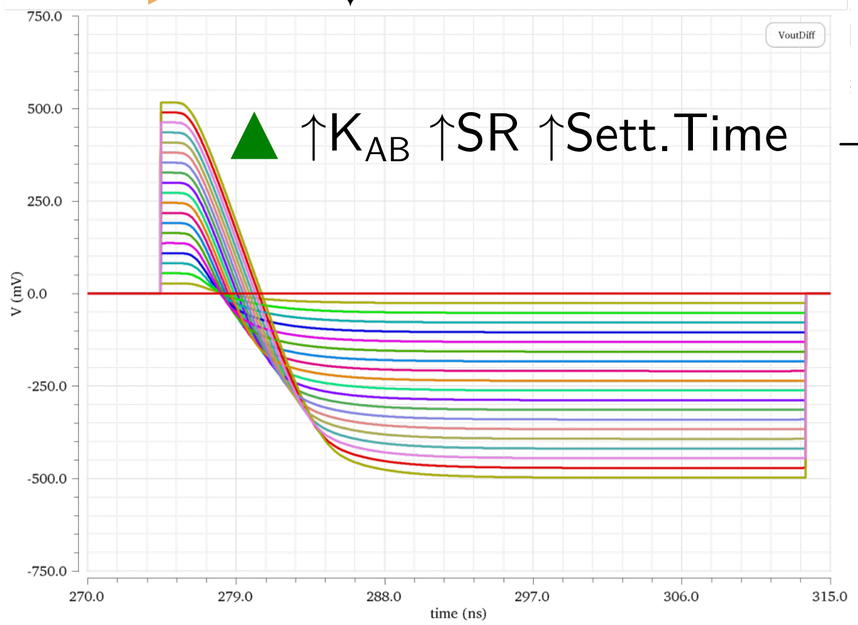
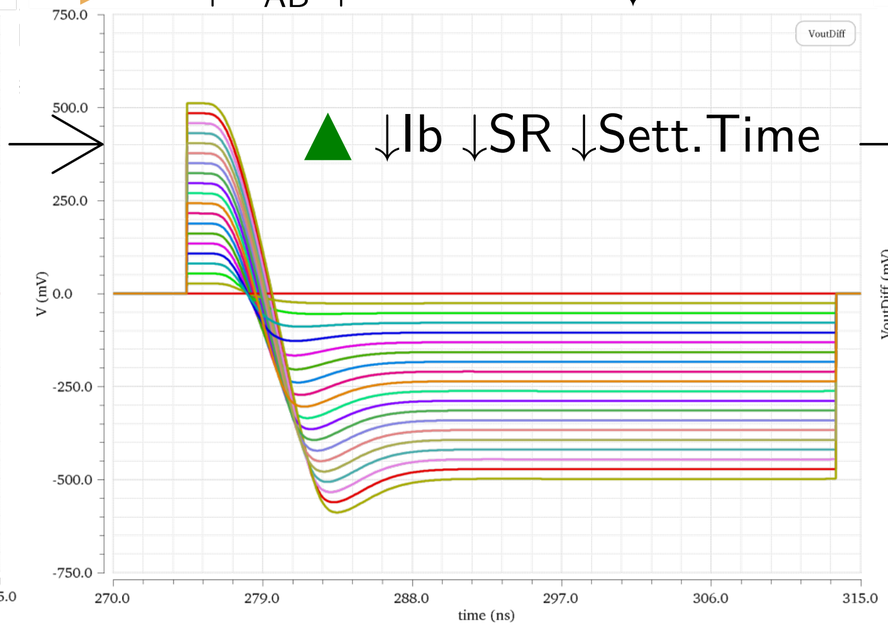
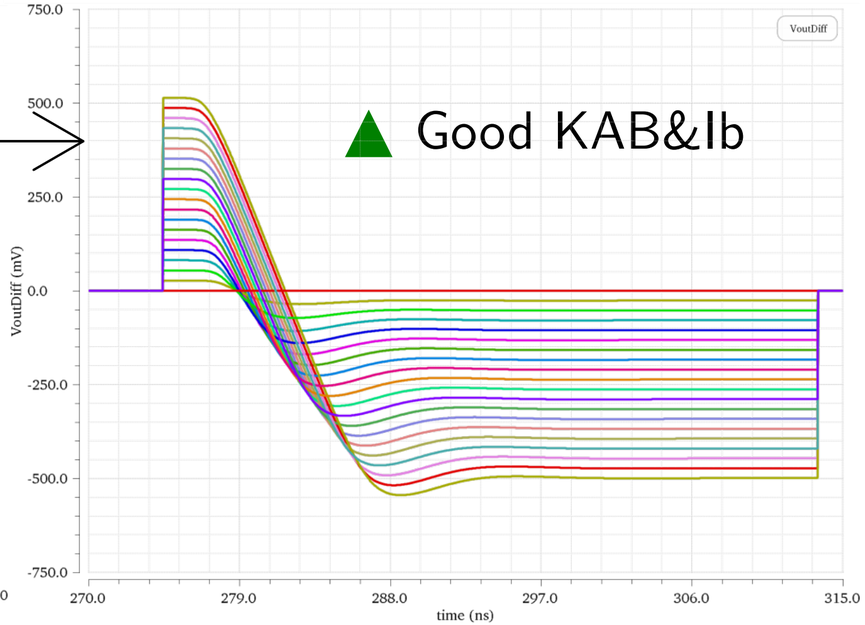




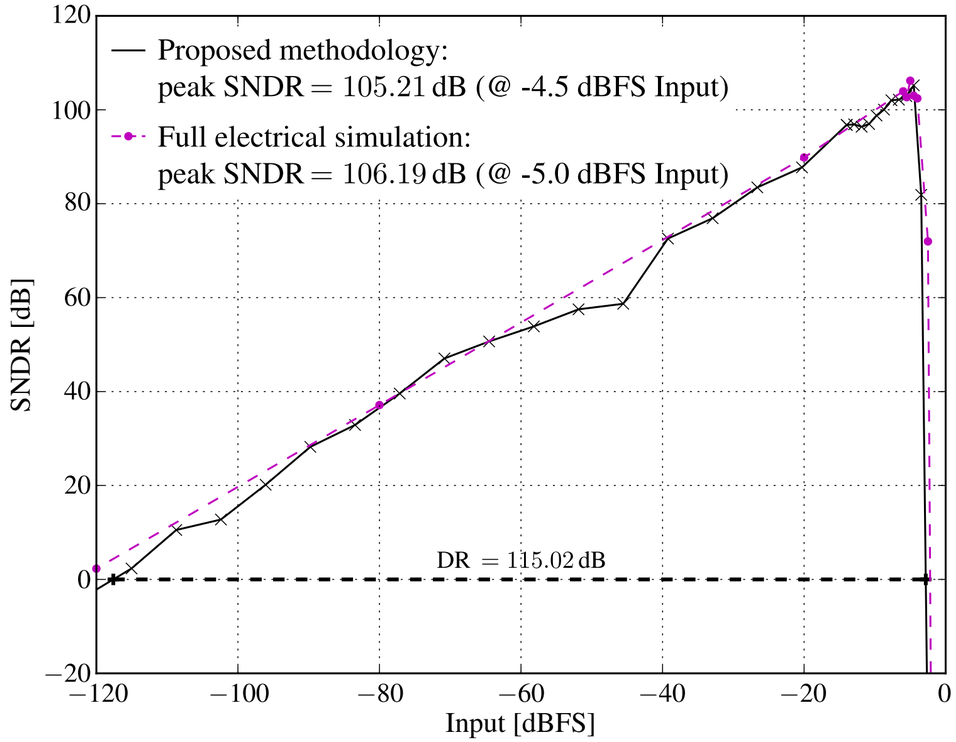


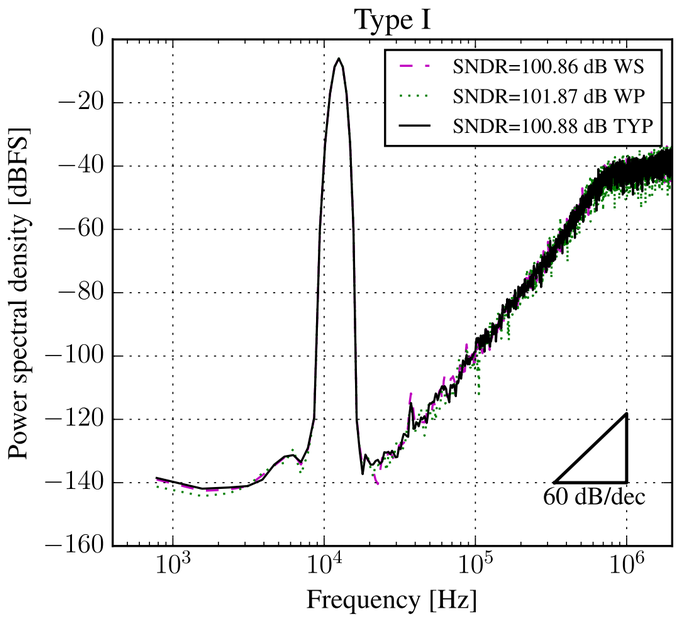
- Schematic validation:

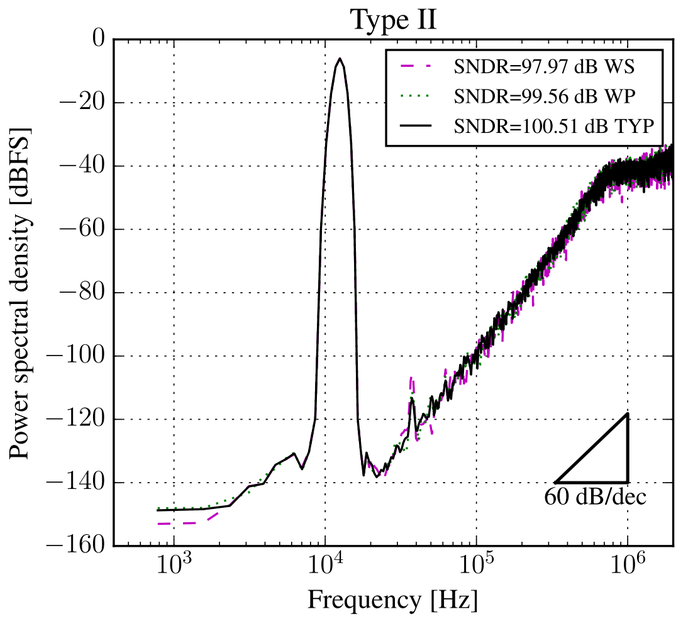
Type I	SVMA1	SVMA2	SVMA3
I_b [µA]	100	50	30
K_{AB}	6	6	6
SNDR [dB]	100.43		

Type II	SVMA1	SVMA2	SVMA3
I_b [µA]	100	50	30
K_{AB}	4	4	4
SNDR [dB]	104.01		

Design Case: Results



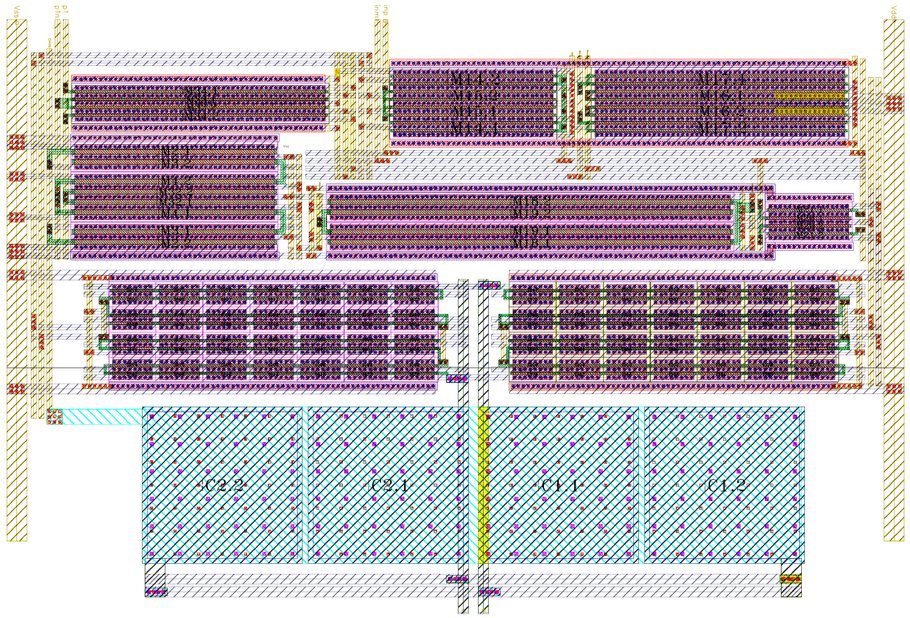




- **Good matching results** between the proposed methodology and Full electrical simulations
- Optimized circuits show **robustness against corners**

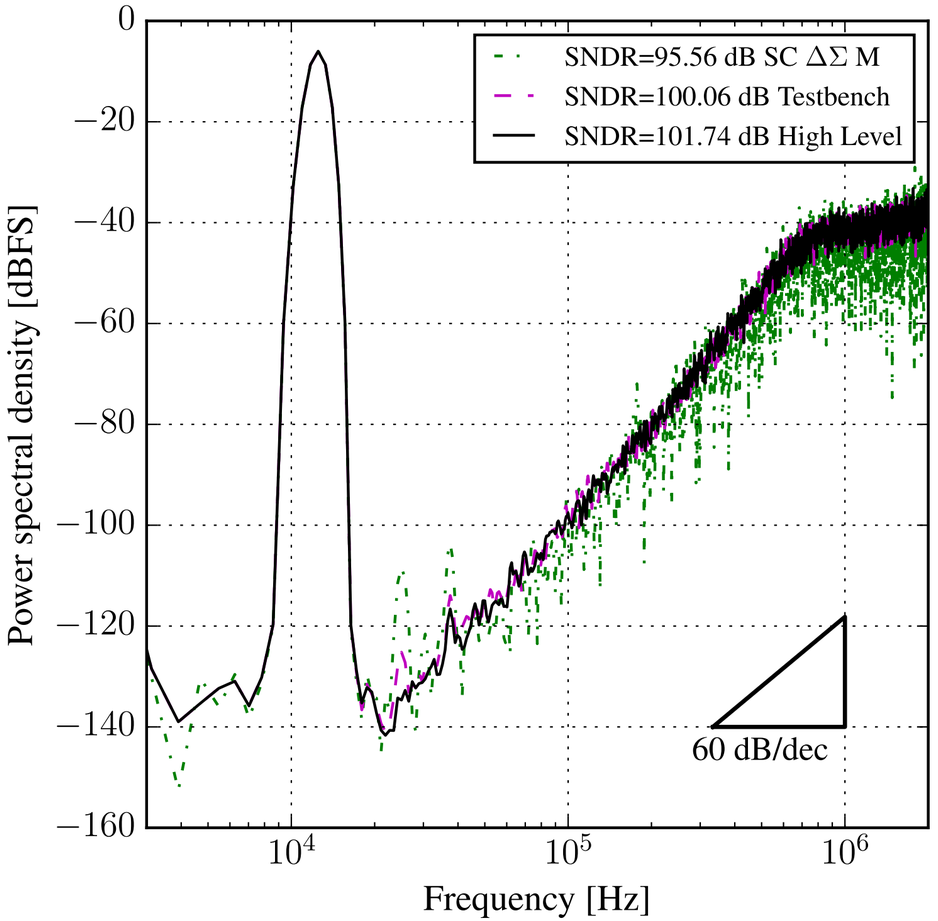
Design Case: Extending the TB method to partial post-layout

- SVMA Type II layout



- ▲ 90 µm x 60 µm
- ▼ 4.5dB SNDR estimation error

- SNDR high-level, TB methodology and Full electrical DSM



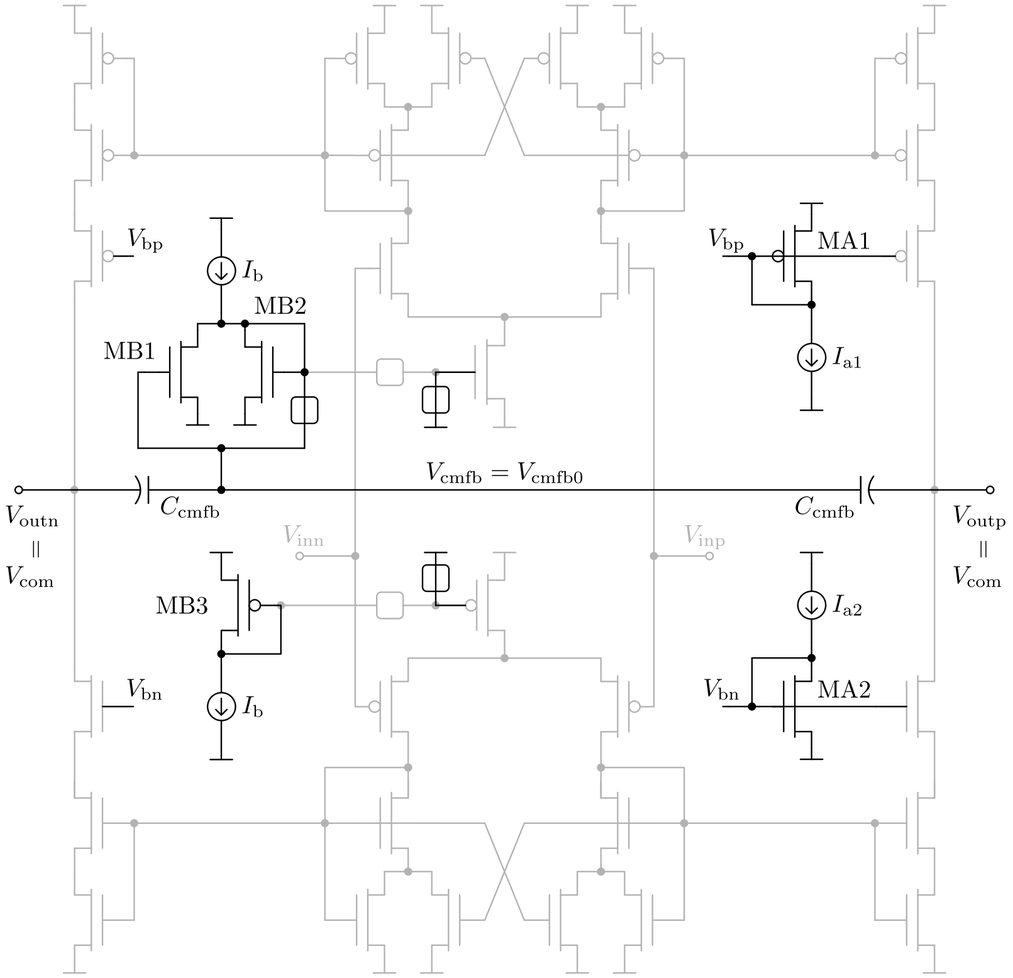
Conclusions

- ▲ New circuit aware design methodology for delta-sigma modulators
- ▲ Time consuming full electrical simulations left for verification purposes
- ▲ Iteration time reduced from ~7 days to ~15 min
- ▲ Reliable design methodology including circuit related non-idealities
- ▲ Can be extended to any other OpAmp circuit topology
- ▼ Specific for discrete-time Delta-Sigma modulators

Thank you!

VMA switched operation

OFF



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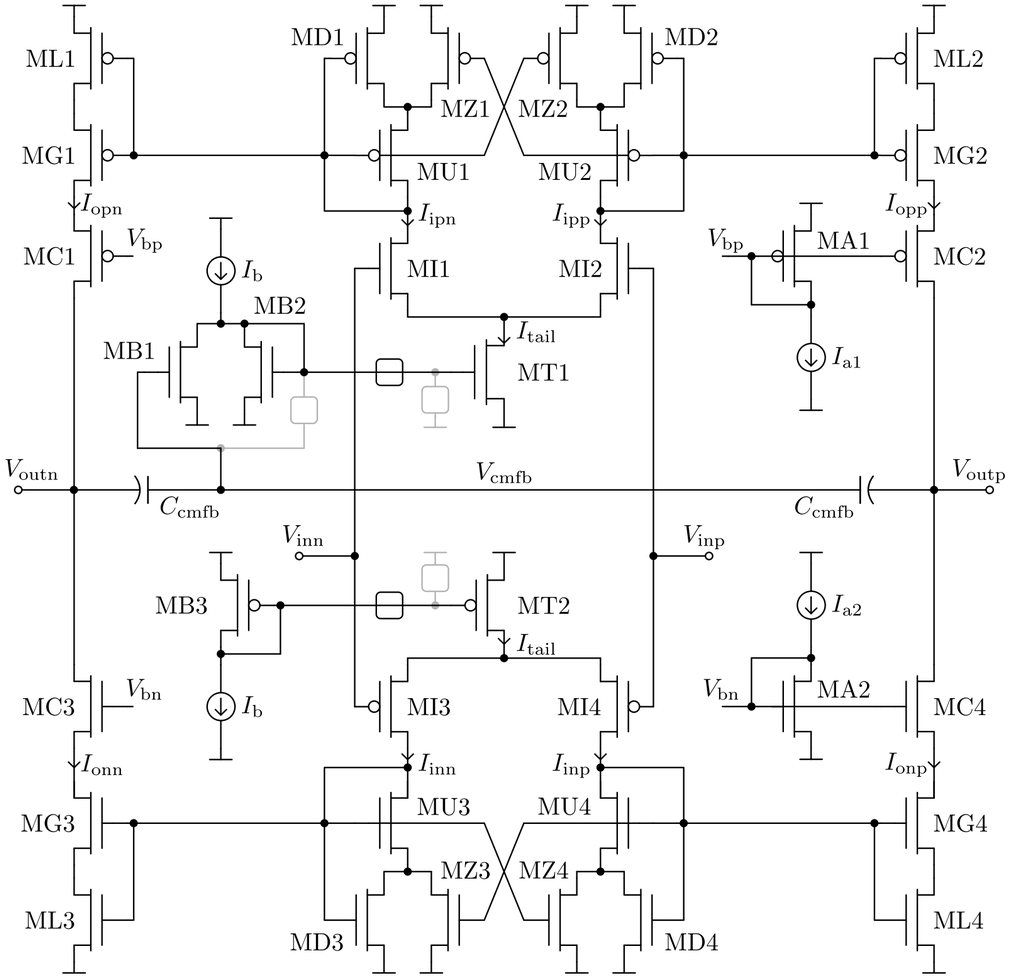


- Classic methodology translation phase

  - Operationg time

$$t_{\mathrm{op}} = \frac{1}{4 \cdot \mathrm{BW} \cdot \mathrm{OSR}} - t_{\mathrm{m}},$$

  - Feedback Factor

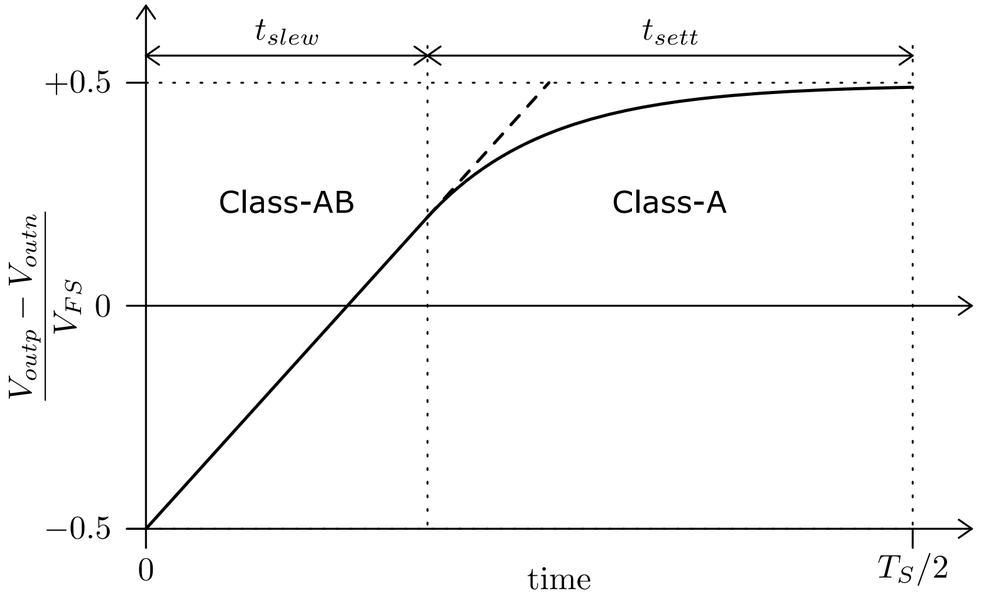
$$\beta_{\mathrm{fb}} = \frac{C_{\mathrm{i}i}}{C_{\mathrm{ss}i} + C_{\mathrm{i}i}}.$$

  - Effective load capacitor

$$C_{\mathrm{leff}i} = C_{\mathrm{l}i} + (1 - \beta_{\mathrm{fb}}) C_{\mathrm{i}i}.$$

  - Open-loop Gain

$$A_{\mathrm{open}} = \frac{1}{\beta_{\mathrm{fb}} \epsilon_{\mathrm{sett}}}.$$



$$\mathrm{SR} = \frac{V_{\mathrm{step}}}{t_{\mathrm{slew}}}.$$

$$t_{\mathrm{op}} = t_{\mathrm{slew}} + t_{\mathrm{sett}},$$

$$I_{\mathrm{max}} = \mathrm{SR} \cdot C_{\mathrm{leff}i}.$$

$$\mathrm{GBW} = \frac{\ln \epsilon_{\mathrm{sett}}^{-1}}{2\pi \beta_{\mathrm{fb}} t_{\mathrm{sett}}}.$$