A 10-bit Linearity Current-Controlled Ring Oscillator with Rolling Regulation for Smart Sensing

M.Dei[1], J.Sacristán[1], E.Marigó[2], M.Soundara[2],L.Terés[1,3] and F.Serra-Graells[1,3]
paco.serra@imb-cnm.csic.es

[1]Instituto de Microelectrónica de Barcelona, IMB-CNM(CSIC), Spain
[2]Silterra Malaysia Sdn. Bhd., Malaysia
[3]Universitat Autònoma de Barcelona, Spain

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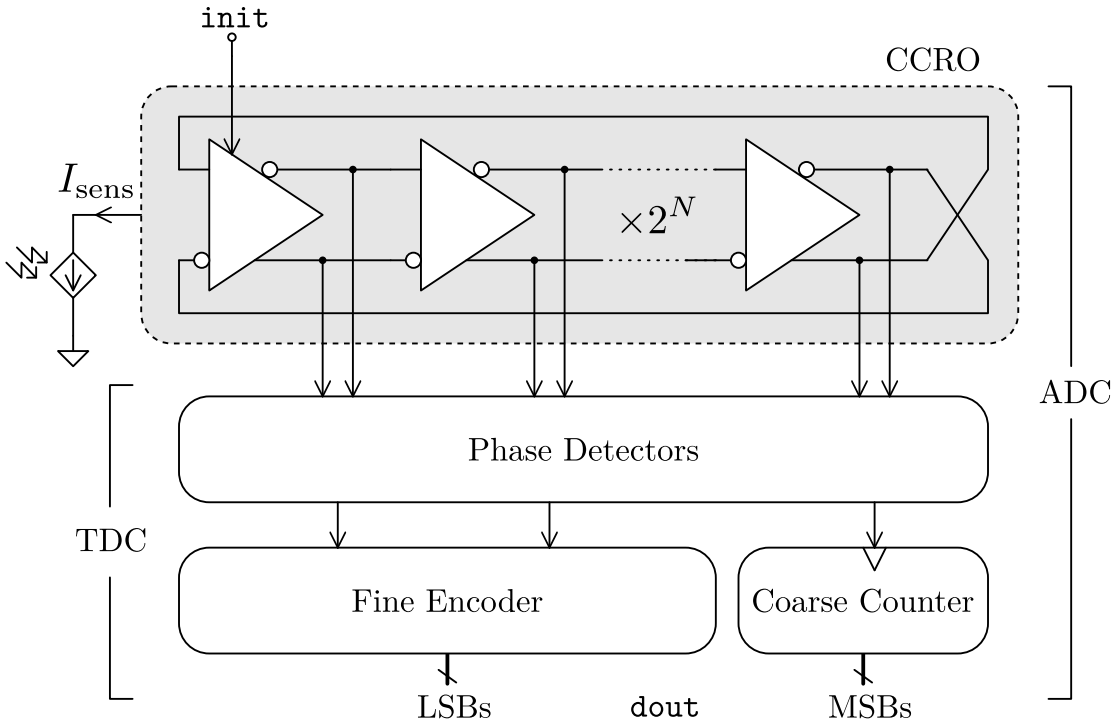
Introduction

- **Time-domain** processing for low-voltage digital-like ADCs
- Current-controlled ring oscillator (**CCRO**) to interface with current-mode sensors (e.g. optical, chemical)
- **Coarse/fine** architectures for low-power operation



Introduction

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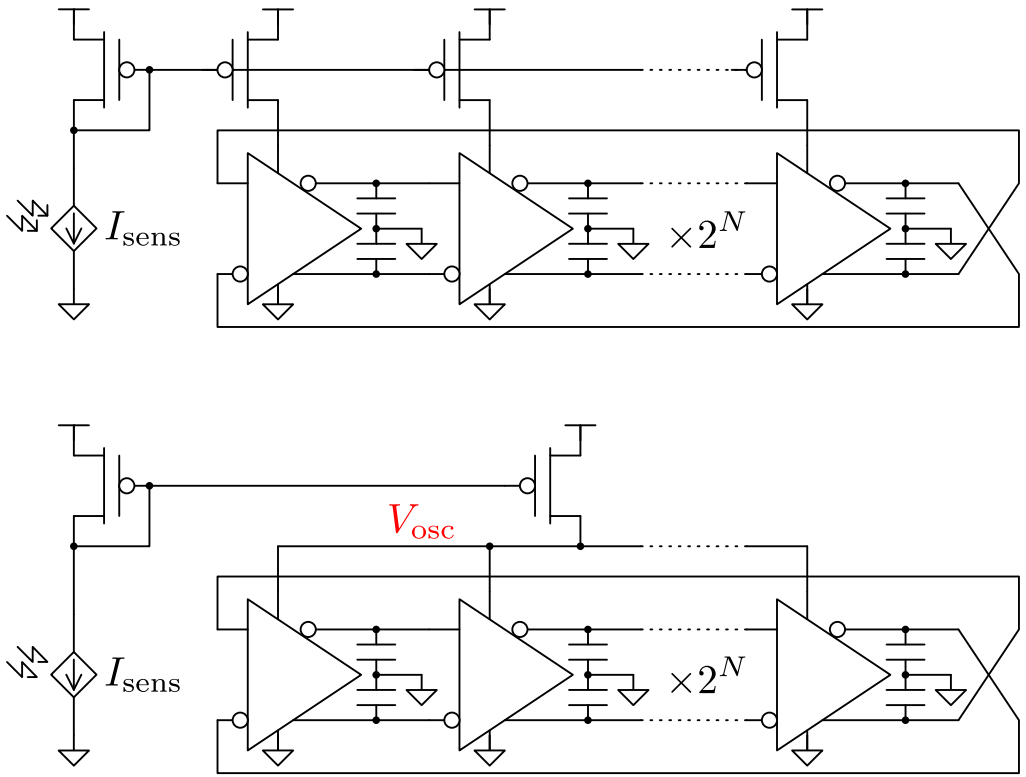
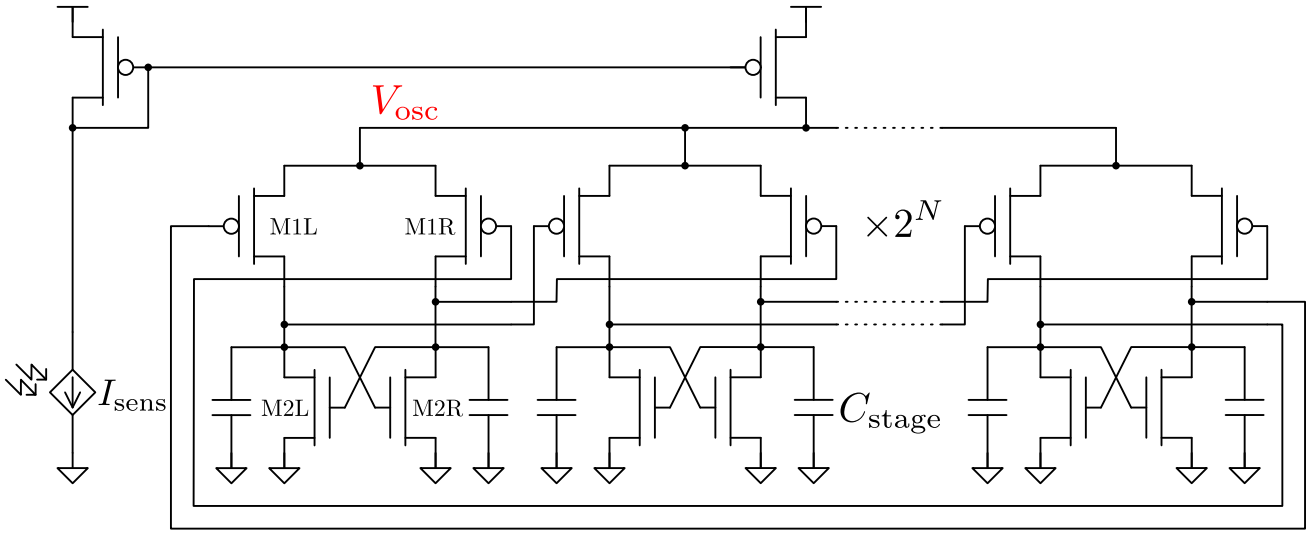
- ▲ Current-controlled ring oscillator (**CCRO**) to interface with current-mode sensors (e.g. optical, chemical)
- ▲ **Coarse/fine** architectures for low-power operation
- ▶ Classic **current-starving** circuit implementation
- ▲ **Current steering** to improve uniformity of fine quantization
- ▼ Signal dependency of CCRO rail voltage (V_{OSC}) causes I-to-F **non-linearity**



CCRO Non-Linearity Issues

- **Differential** latch (M1,2) with symmetrical load capacitance (C_{stage})

$$f_{osc} \propto \frac{I_{sens}}{C_{stage} V_{osc}}$$



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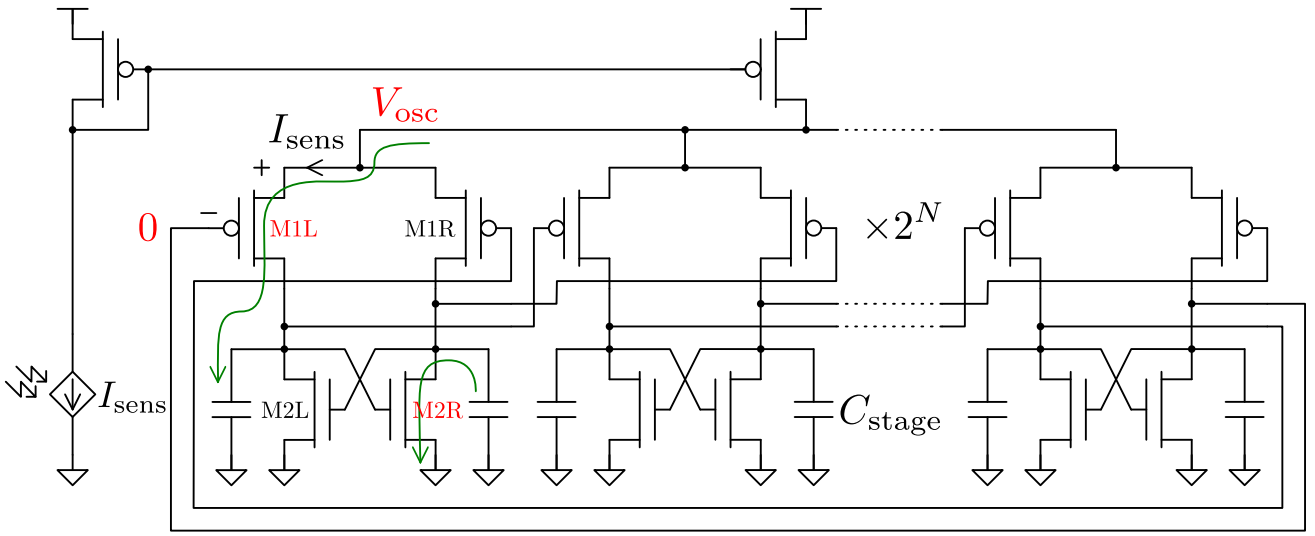

- PMOS transistors define **rail voltage**:

$$V_{osc} = \left(1 - \frac{1}{n}\right) V_{DD} + \frac{V_{TO1}}{n} + \sqrt{\frac{2 I_{sens}}{n \beta_1}}$$

$$f_{osc} \propto \frac{\frac{I_{sens}}{I_{S1}}}{1 + \frac{1}{n}\left(\frac{V_{TO1}}{V_{DD}} - 1\right) + 2\frac{U_t}{V_{DD}}\sqrt{\frac{I_{sens}}{I_{S1}}}}$$

$$\begin{cases} I_D = \dfrac{\beta}{2n} \left(V_{GB} - V_{TO} - n V_{SB}\right)^2 \\ I_S = 2 n \beta U_t^2 \end{cases}$$

EKV model in strong inversion forward saturation

$(V_B \doteq V_{DD})$

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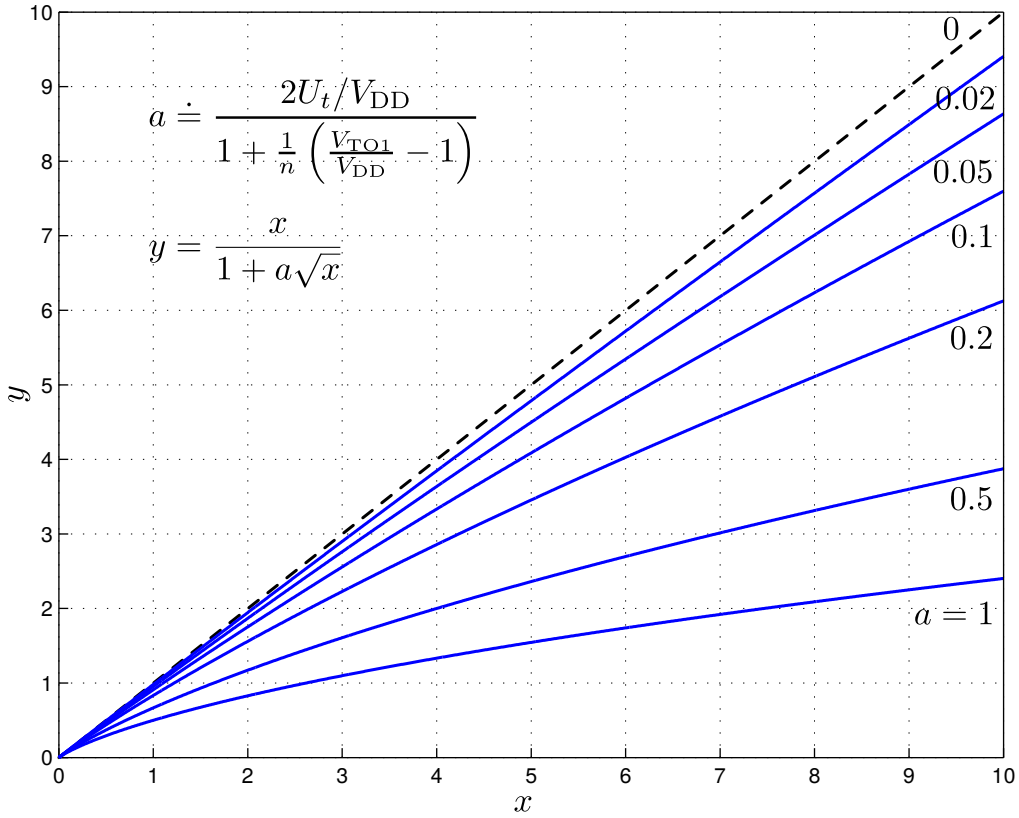
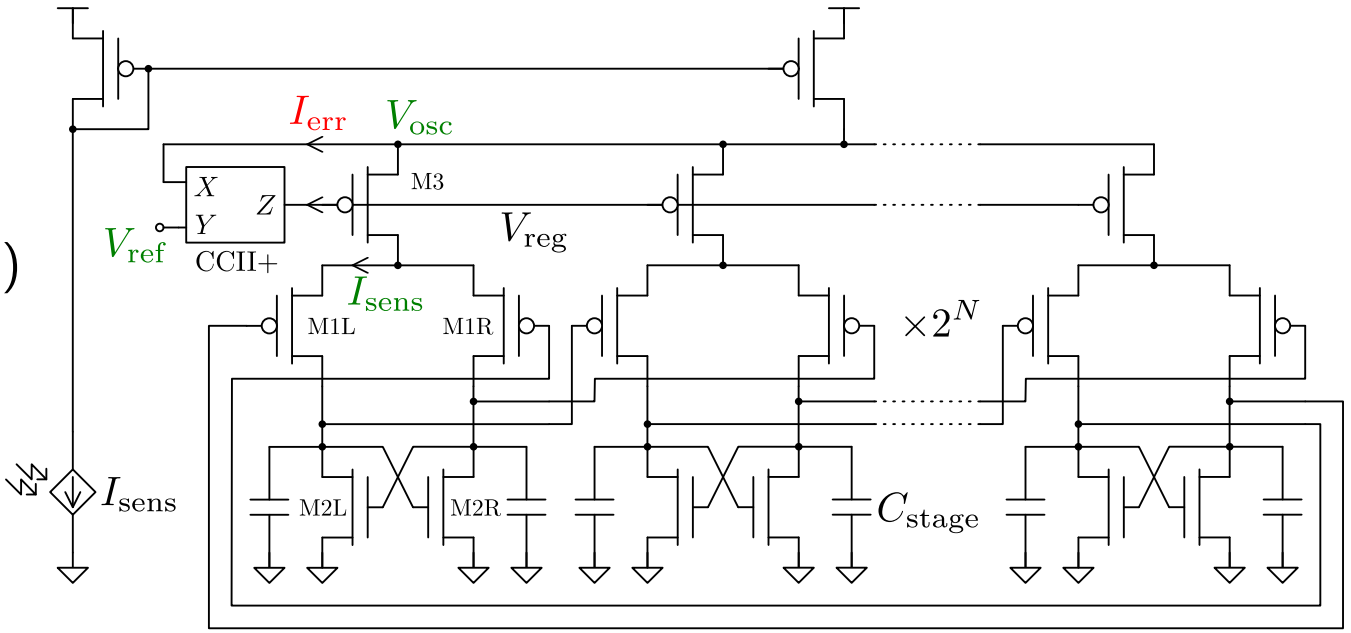


- Strong non-linearities for **high-current** full scale or **low-voltage** operation

CCRO with Rolling Regulation

- Series transistor (**M3**) to regulate rail voltage independently from signal current
- Second generation current conveyor (**CCII+**) as **common** control

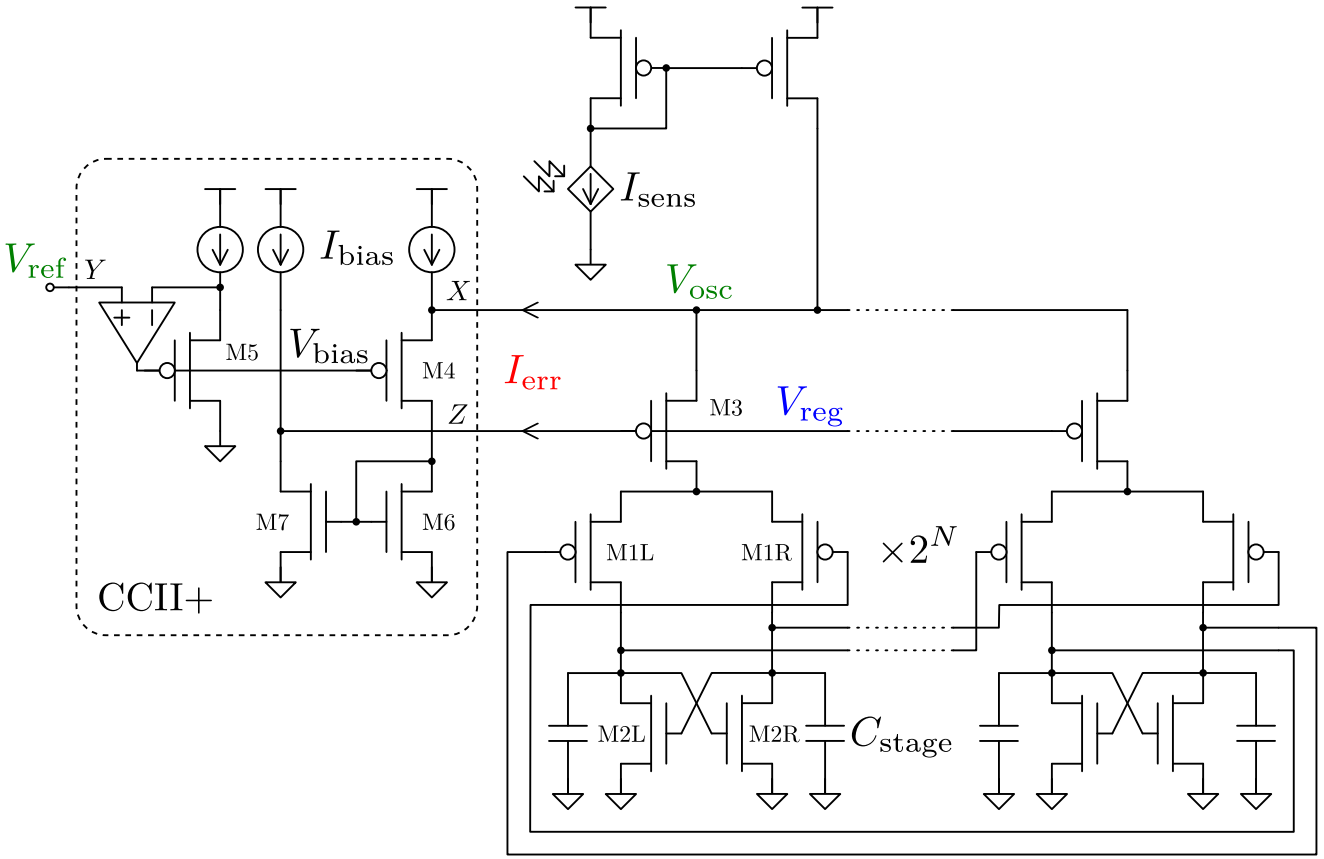


- Rail voltage **regulation** + signal current **steering**
- Control of M3 transistors is **ROLLING** along the ring like I_{sens}

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad \begin{cases} V_{\text{osc}} \leftarrow V_{\text{ref}} \\ I_Z \leftarrow I_{\text{err}} \quad (\rightarrow 0) \end{cases}$$

CMOS Circuit Implementation

- **3-stage** CCII+ circuit:
  - + **X-branch** to supply low input impedance and to sense error current
  - + **Y-branch** to bias M4 for any PVT condition so V_{osc}=V_{ref} when I_{err}=0
  - + **Z-branch** to apply negative-feedback control using error current



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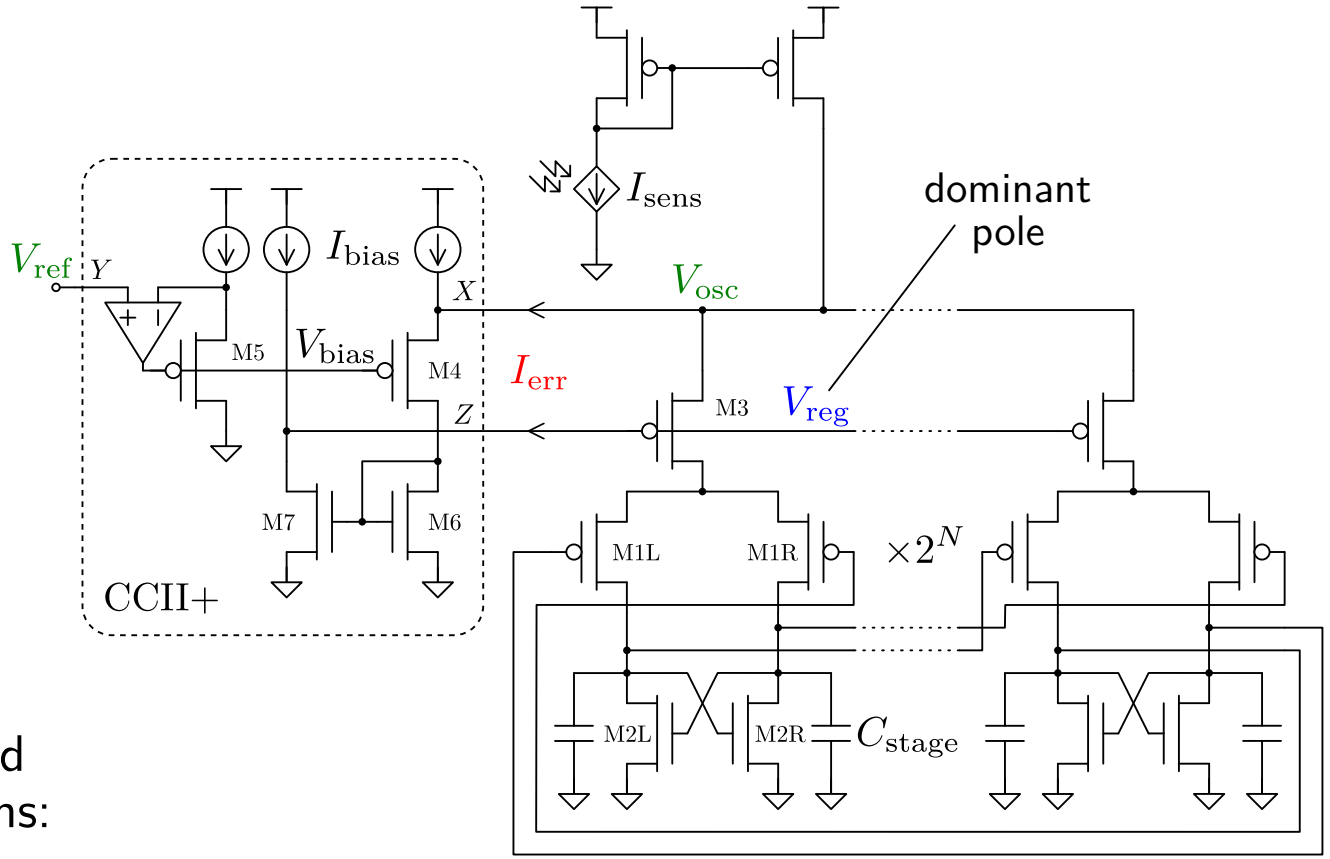


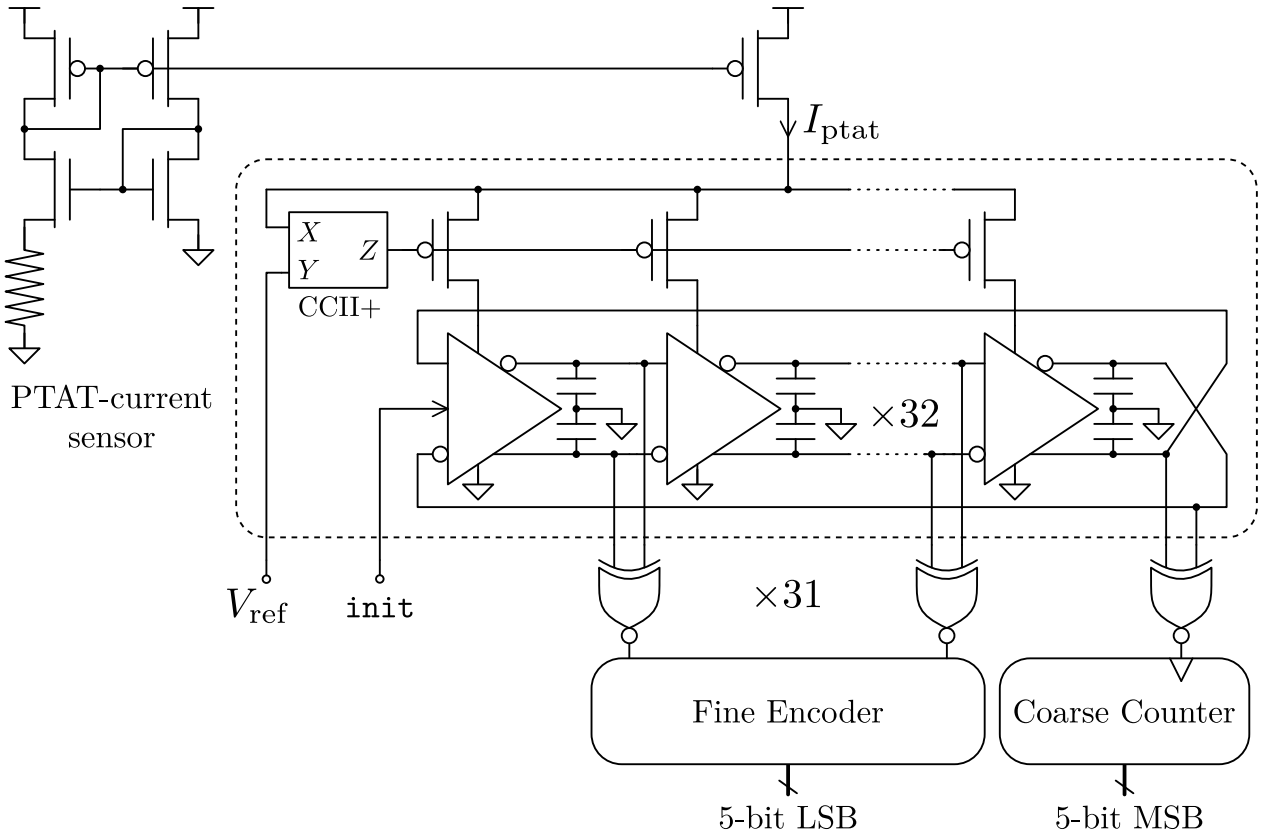
- Better **stability** compared to OpAmp-based solutions:

$$r_{in} \doteq \frac{v_{osc}}{i_{sens}} \simeq \frac{1}{g_{ms3} + \frac{g_{ms4}}{1 + \frac{g_{md4}}{g_{mg6}}}\left(1 + \frac{g_{mg3}}{g_{md7}}\right)} \simeq \left(n\frac{g_{md7}}{g_{ms4}}\right)\frac{1}{g_{ms3}}$$

- Rail-voltage **low sensitivity** respect to signal current

Application Example

- MEMS **temperature** monitoring
- CMOS **PTAT** reference operating in weak inversion as temperature sensor
- **10-bit 100-kS/s** ADC specifications
- Design parameters:
  - + **5-bit**/**5-bit** coarse/fine quantization splitting
  - + $V_{osc} = \mathbf{1.4V}$
    $C_{stage} = \mathbf{20fF}$
    $I_{ptat} = \mathbf{5\mu A}$ at 300K
    $f_{osc} < \mathbf{4MHz}$



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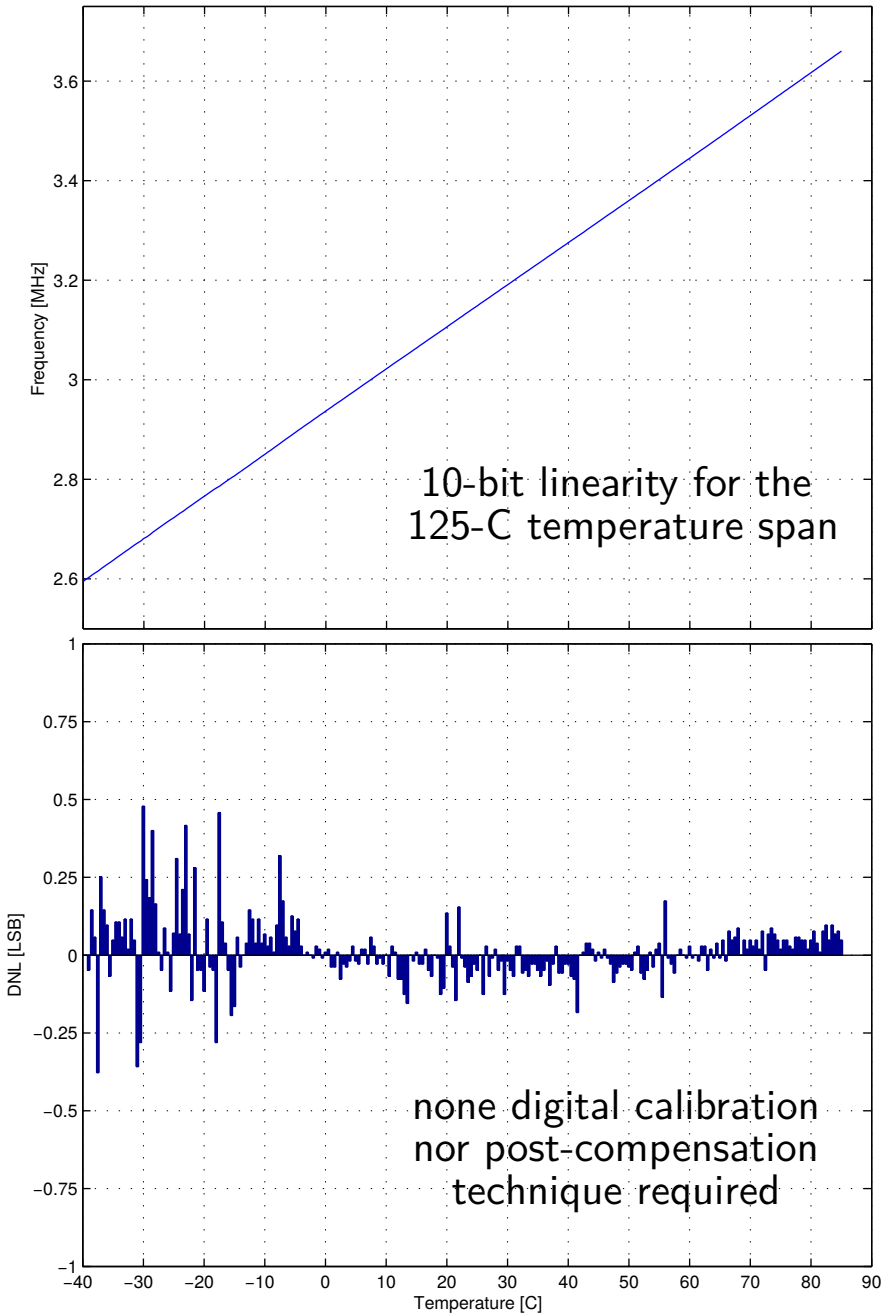

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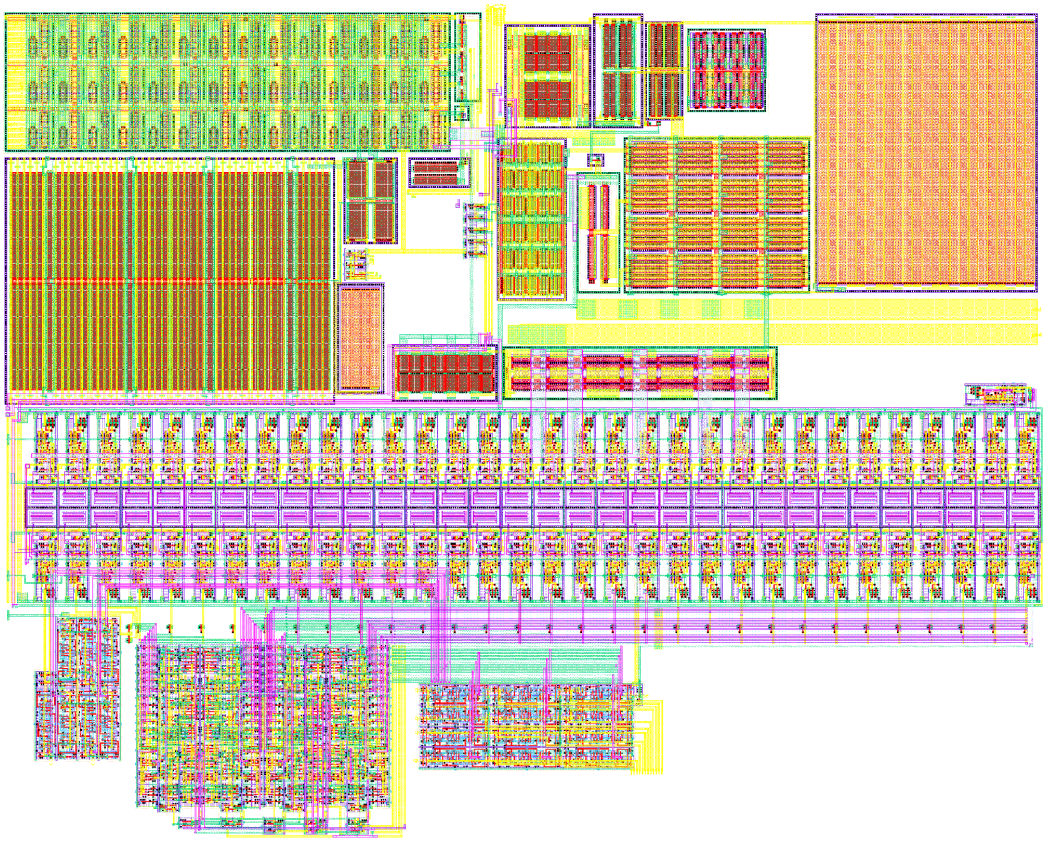
250µm x 200µm (0.05mm^2)



...currently being integrated in 0.18-µm 1P6M CMOS technology.

Conclusions

- A **highly linear** I-to-F current-steering **CCRO** has been presented for ADC
- Based on rail-voltage **distributed regulation** concept
- Usage of **current conveyors** to improve loop **stability**
- **10-bit** 100-kS/s **ADC example** in 0.18-µm 1P6M CMOS technology
- Performance achieved **without** digital calibration nor post-compensation

Thanks for your attention!

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