Class-AB Single-Stage OpAmp for Low-Power Switched-Capacitor Circuits

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2 Class-AB Architecture

3 Process-Independent Circuits

4 Practical Design

5 Experimental Results

6 Conclusions

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Low-Power Switched-Capacitor Design

Low-Voltage Approach

- Bulk-driven OpAmps
- Internal supply multipliers
- Inverter-based OpAmps
- Switched OpAmps

▲ Nominal-voltage downscaling

▼ Moderate power savings

Low-Current Approach

- Telescopic diff. pairs with LCMFB
- Dynamic biasing by RC bias tees
- Hybrid-Class-A/AB
- Adaptive biasing

▲ Higher power savings

▼ Parameter-variation sensitivity

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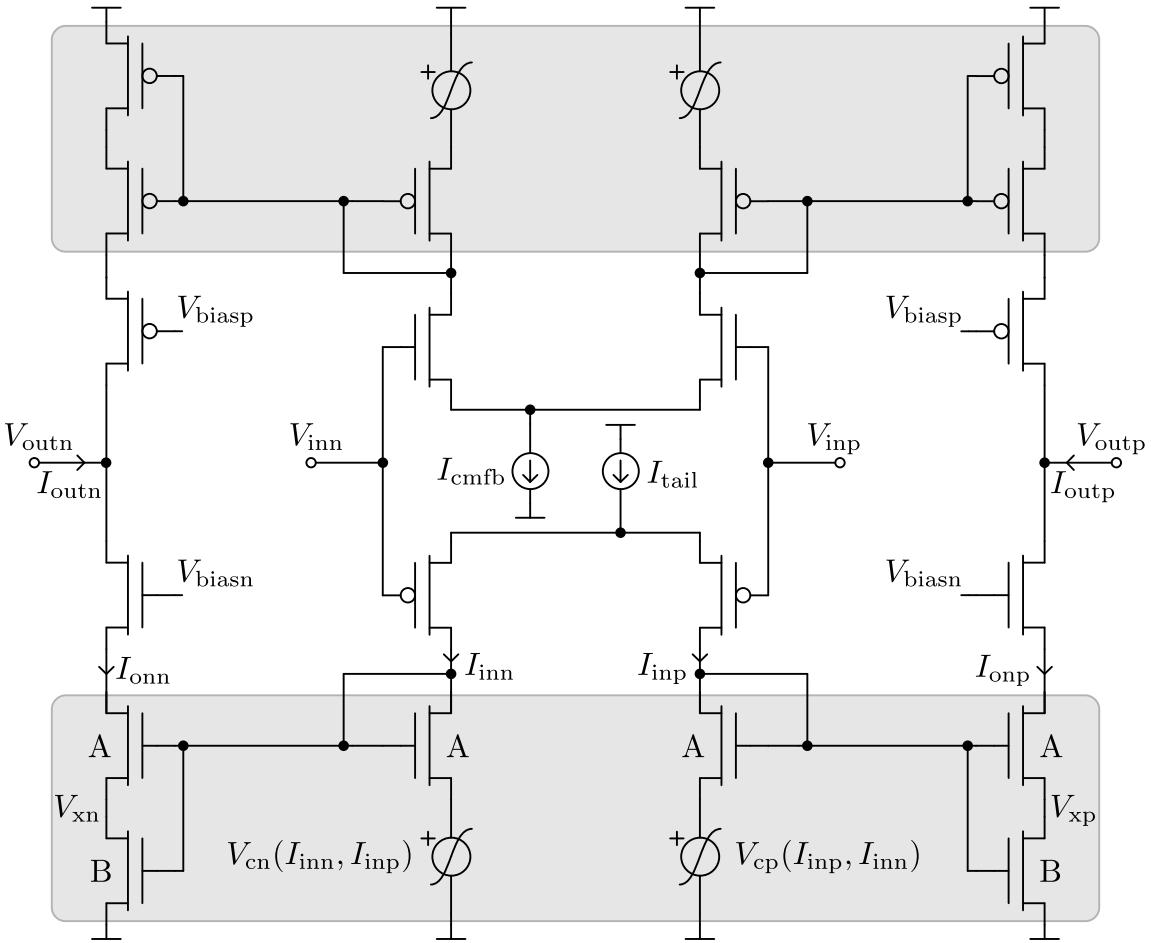
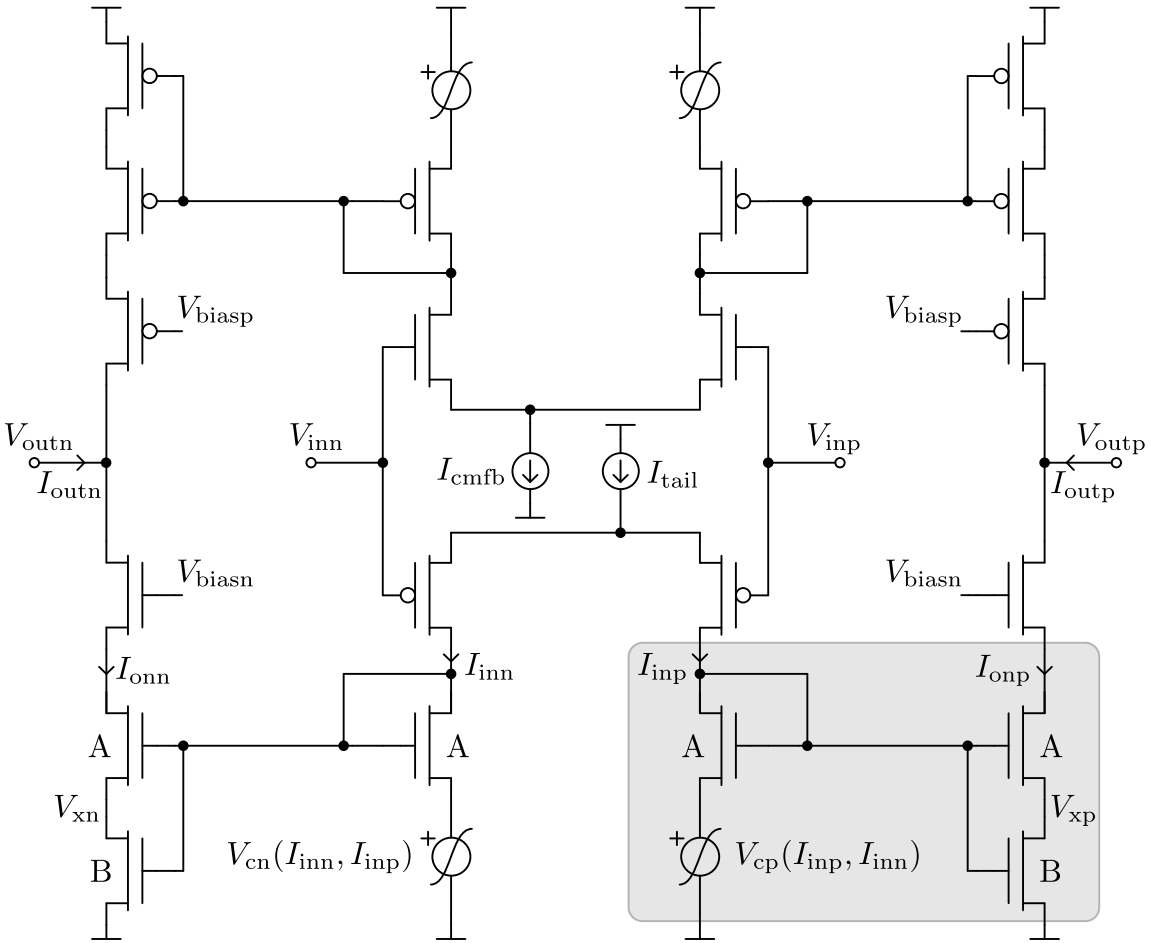
Single-Stage Class-AB OpAmp



- Two **complementary** diff. pairs
- **Dynamic** current mirrors
- **Separate** Class-AB control
- **Partial** positive feedback
- **CMFB** control through the NMOS-pair tail

- Gain improvement by the **output cascode** transistors
- **No** need for the Miller **compensation** capacitors
- **High-peak** Class-AB currents **only in the output** transistors

Single-Stage Class-AB OpAmp



- Supposing all boxed devices operating in strong inversion:

$$\mathrm{D} \doteq \frac{\mathrm{AB}}{\mathrm{A}+\mathrm{B}}$$

$$\sqrt{\frac{I_{\mathrm{onp}}}{\mathrm{D}}} = \sqrt{\frac{I_{\mathrm{inp}}}{\mathrm{A}}} + \sqrt{\frac{n\beta}{2}}\, V_{\mathrm{cp}}$$

- Desired Class-AB behavior:

$$\begin{cases} I_{\mathrm{outp}} \equiv 0 & V_{\mathrm{cp}} \equiv V_{\mathrm{xp}} & I_{\mathrm{onp}} \equiv I_{\mathrm{inp}} \\ I_{\mathrm{outp}} \not\equiv 0 & V_{\mathrm{cp}} \not\equiv V_{\mathrm{xp}} & \begin{cases} I_{\mathrm{onp}} \ll I_{\mathrm{inp}} \\ I_{\mathrm{onp}} \gg I_{\mathrm{inp}} \end{cases} \end{cases}$$

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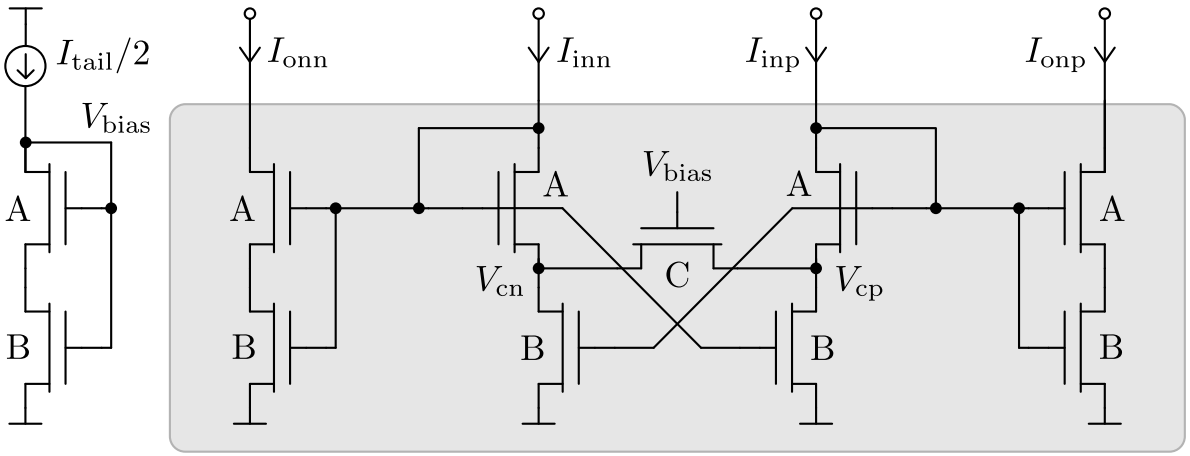
Type I

$$I_{\text{inp}} = \mathrm{B}\left(2\sqrt{\frac{I_{\text{onn}}}{\mathrm{D}}} - \sqrt{\frac{I_{\text{onp}}}{\mathrm{D}}} + \sqrt{\frac{I_{\text{inp}}}{\mathrm{A}}}\right)\left(\sqrt{\frac{I_{\text{onp}}}{\mathrm{D}}} - \sqrt{\frac{I_{\text{inp}}}{\mathrm{A}}}\right) + \mathrm{C}\left(\sqrt{\frac{2I_{\text{tail}}}{\mathrm{D}}} - \sqrt{\frac{I_{\text{onp}}}{\mathrm{D}}} - \sqrt{\frac{I_{\text{onn}}}{\mathrm{D}}} + \sqrt{\frac{I_{\text{inp}}}{\mathrm{A}}} + \sqrt{\frac{I_{\text{inn}}}{\mathrm{A}}}\right)\left(\sqrt{\frac{I_{\text{onp}}}{\mathrm{D}}} - \sqrt{\frac{I_{\text{onn}}}{\mathrm{D}}} - \sqrt{\frac{I_{\text{inp}}}{\mathrm{A}}} + \sqrt{\frac{I_{\text{inn}}}{\mathrm{A}}}\right)$$

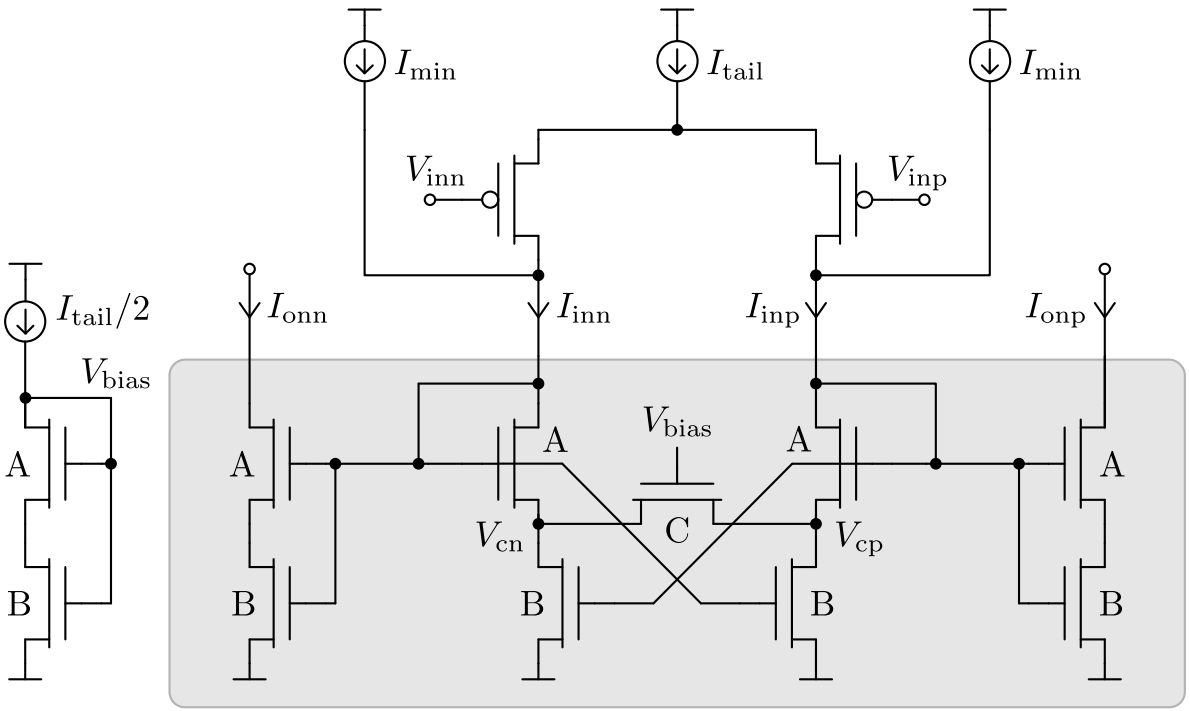


- **Cross-coupled** pair for the Class-AB operation
- **Crossing** transistor as a Class-AB **limiter**

▲ **Independence** from the technology parameters

▼ Need for an **extra bias** reference

Type I with Class-AB Smoother

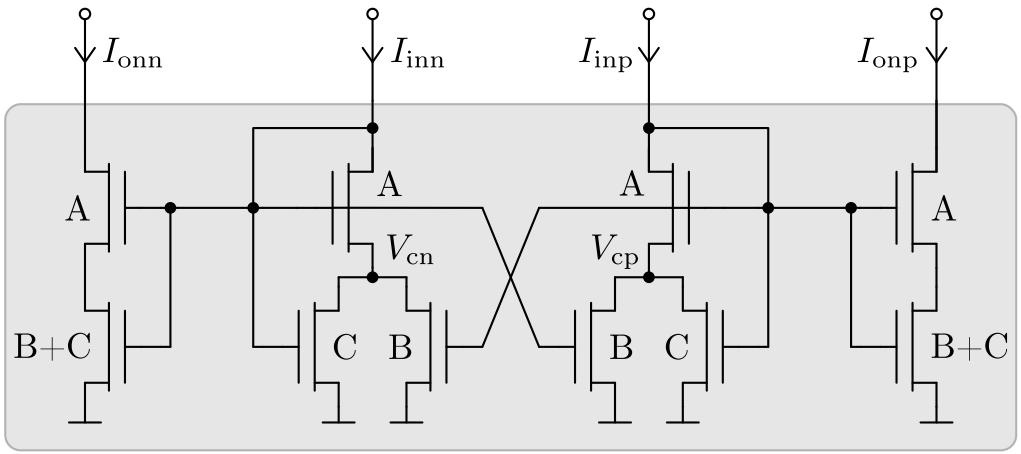


- Low-level common-mode current **injection**
- Instability **prevention** under a high Class-AB modulation
- Need for **extra current** sources

Type II

$$I_{\text{inp}} = \left[2\left(\text{B}\sqrt{\frac{I_{\text{onn}}}{\text{D}}} + \text{C}\sqrt{\frac{I_{\text{onp}}}{\text{D}}} \right) - (\text{B}+\text{C})\left(\sqrt{\frac{I_{\text{onp}}}{\text{D}}} - \sqrt{\frac{I_{\text{inp}}}{\text{A}}} \right) \right] \left(\sqrt{\frac{I_{\text{onp}}}{\text{D}}} - \sqrt{\frac{I_{\text{inp}}}{\text{A}}} \right)$$

$$\text{D} \doteq \frac{\text{A}(\text{B}+\text{C})}{\text{A}+\text{B}+\text{C}} \qquad I_{\text{max}} \simeq \frac{1+\frac{\text{A}}{\text{C}}}{1+\frac{\text{A}}{\text{B}+\text{C}}} I_{\text{tail}} > I_{\text{tail}}$$



- **Independence** from the technology parameters
- **Auto-biased** Class-AB limiter
- Self-latch **prevention**
- **Simple sizing** procedure

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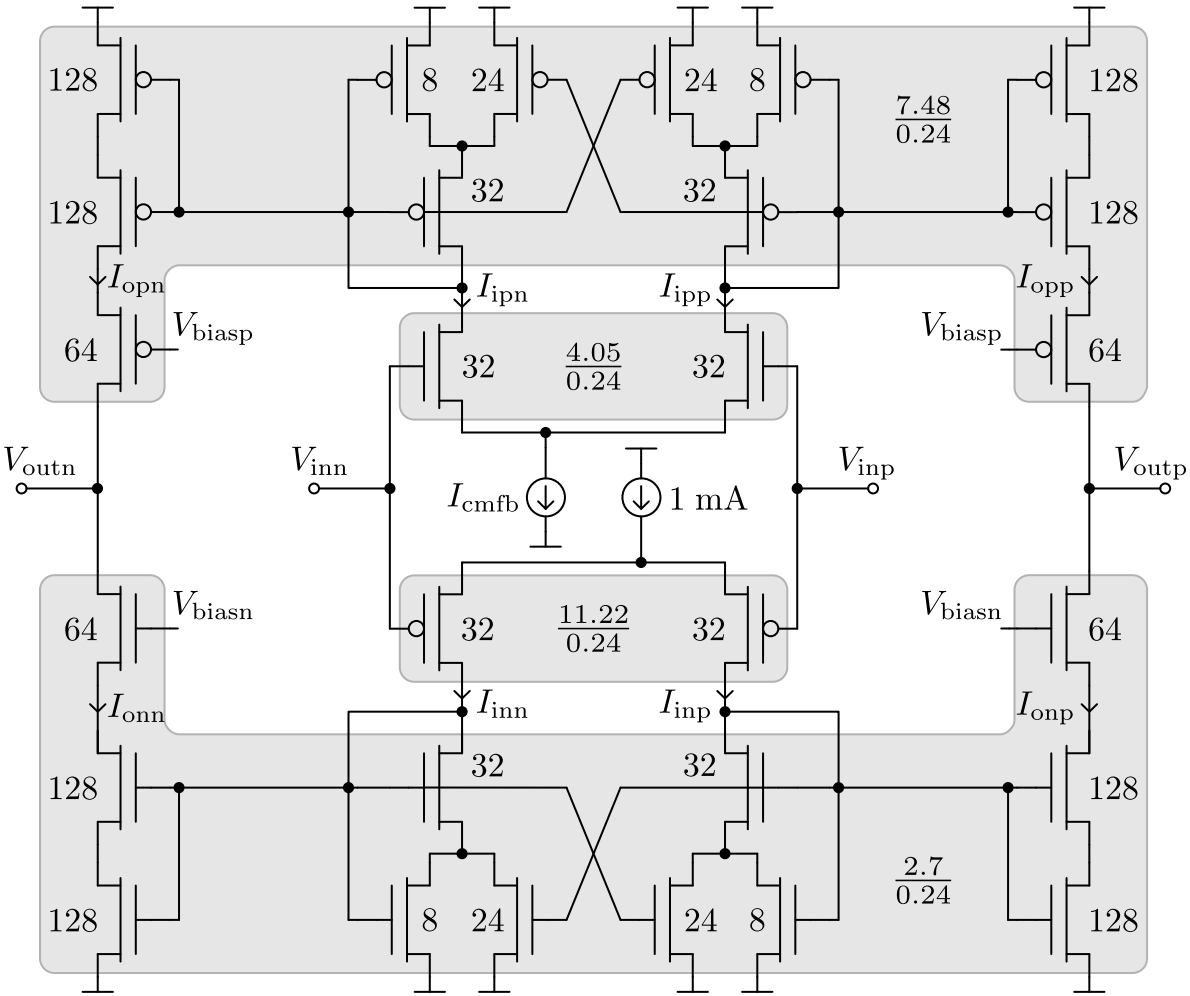
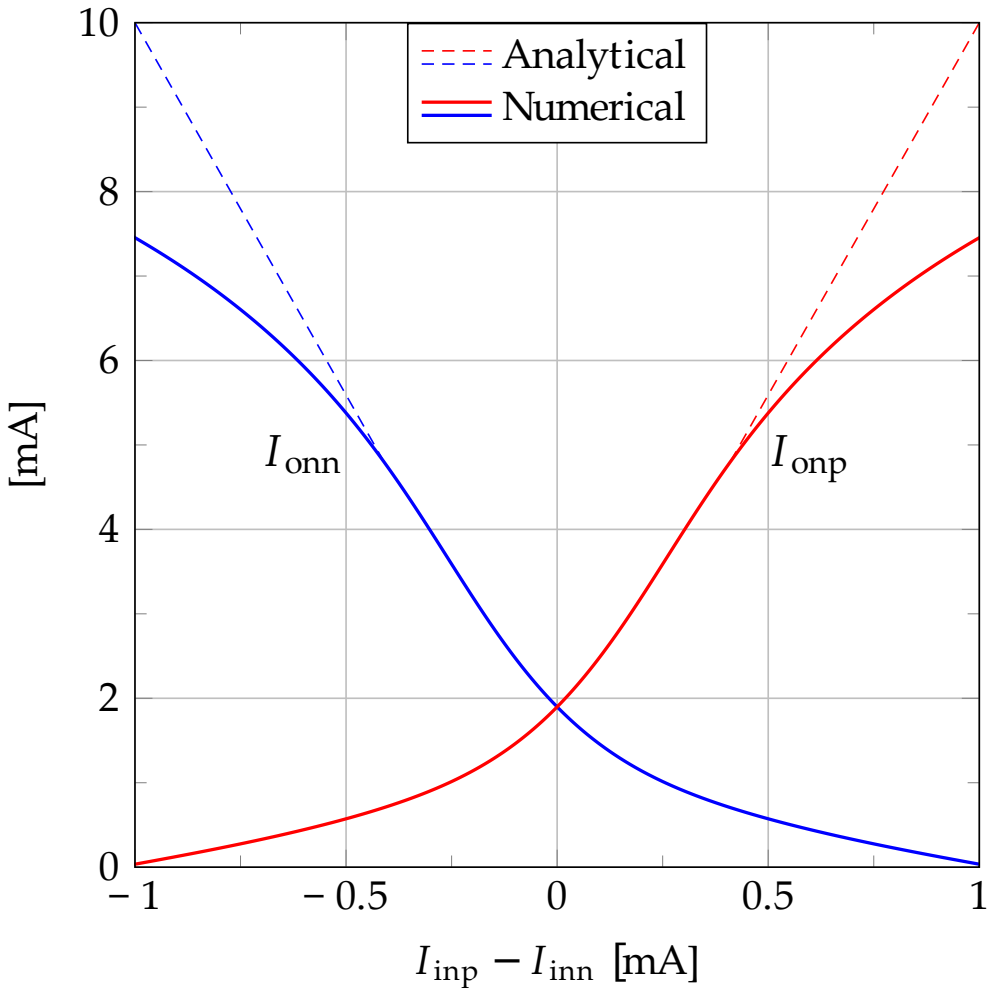
Type-II OpAmp Using a 0.18-µm CMOS Technology

- Circuit design based on the **inversion-coefficient**
- **Reduced set** of transistor matching groups
- **Minimum-channel-length** devices can be used
- Bias for cascode transistors **optimized** for maximum output full scale
- 1.8-V **nominal** voltage supply of the CMOS technology



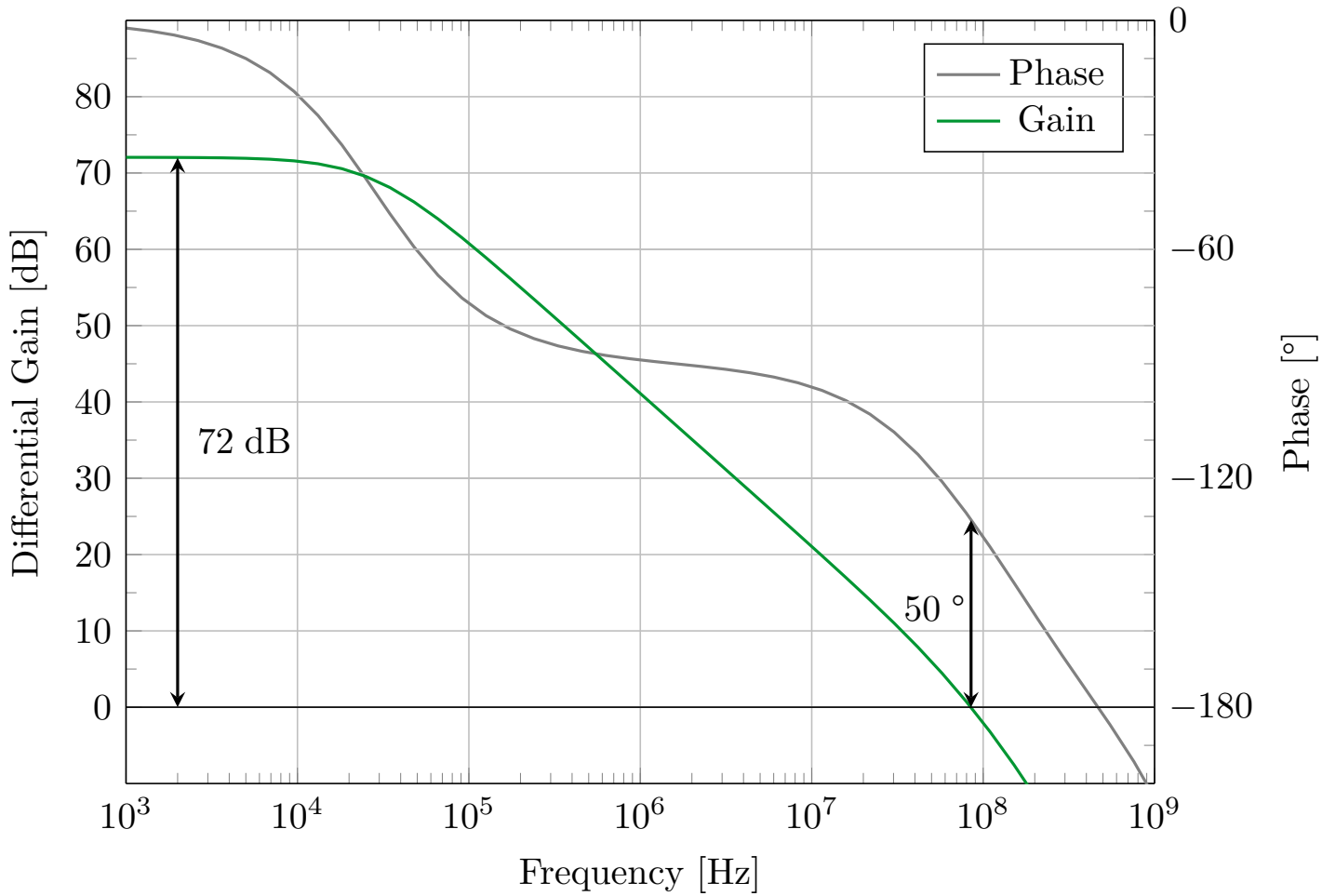
Simulation Results

- DC transfer curve
- Analytical versus numerical behavior
- Class-AB achieves about $\times 4$ bias current



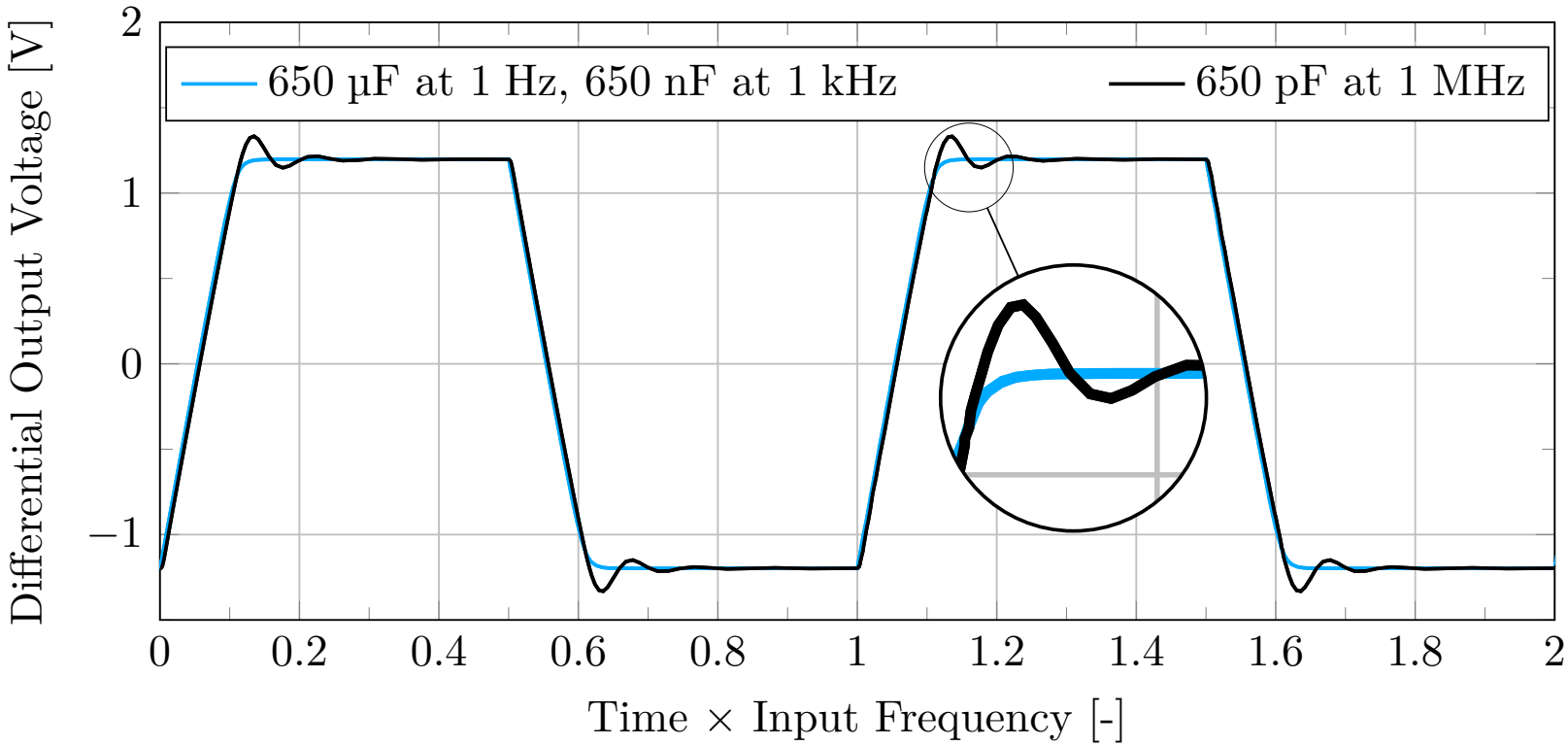
Simulation Results

- Frequency response
- 200-pF load capacitance



Simulation Results

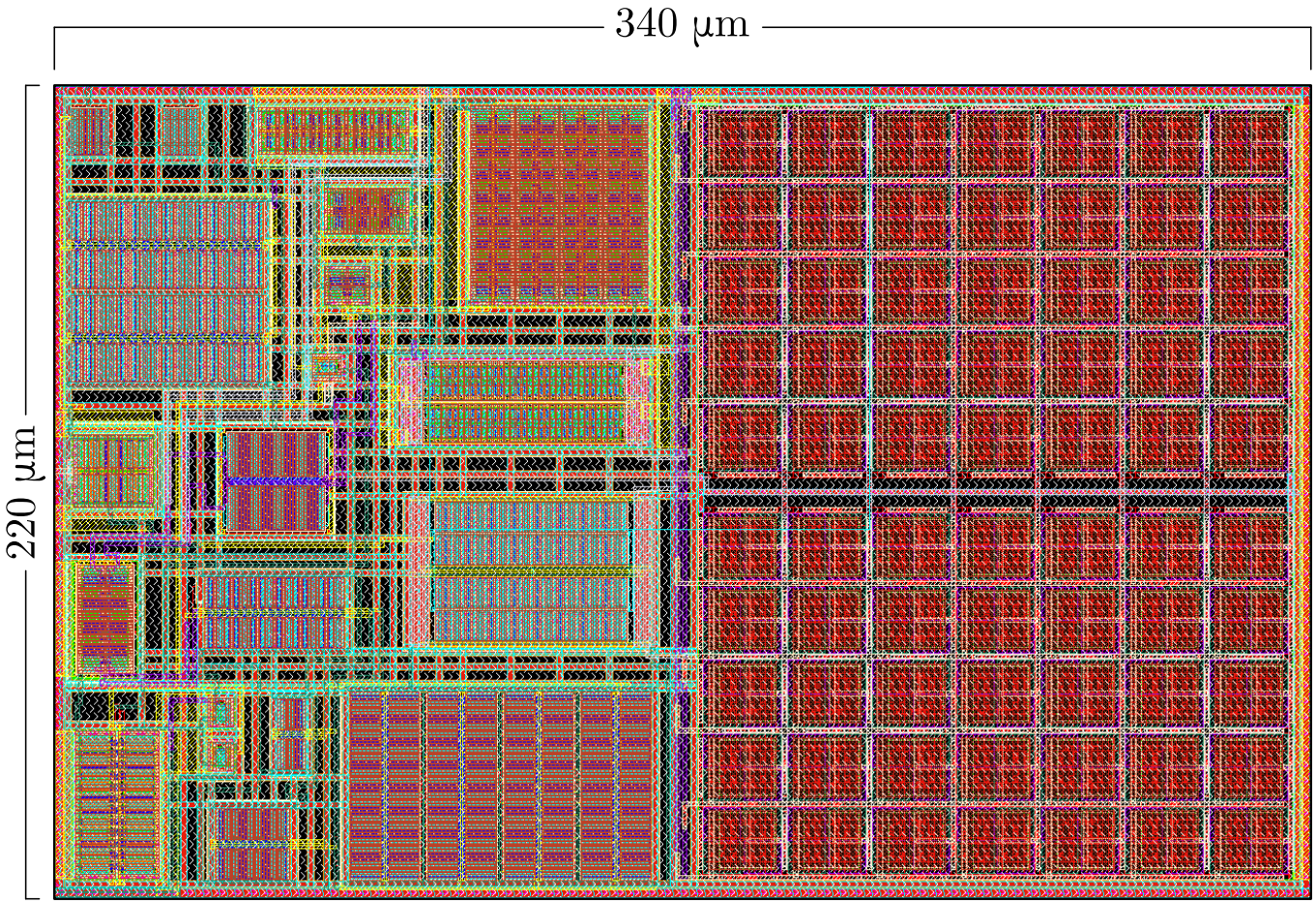
- Step response for several load conditions



- Stability robustness

Integration

- **Standard** 0.18-µm 1P6M CMOS technology
- **0.07-mm^2** area
- Additional **CMFB** averaging capacitors for SC applications



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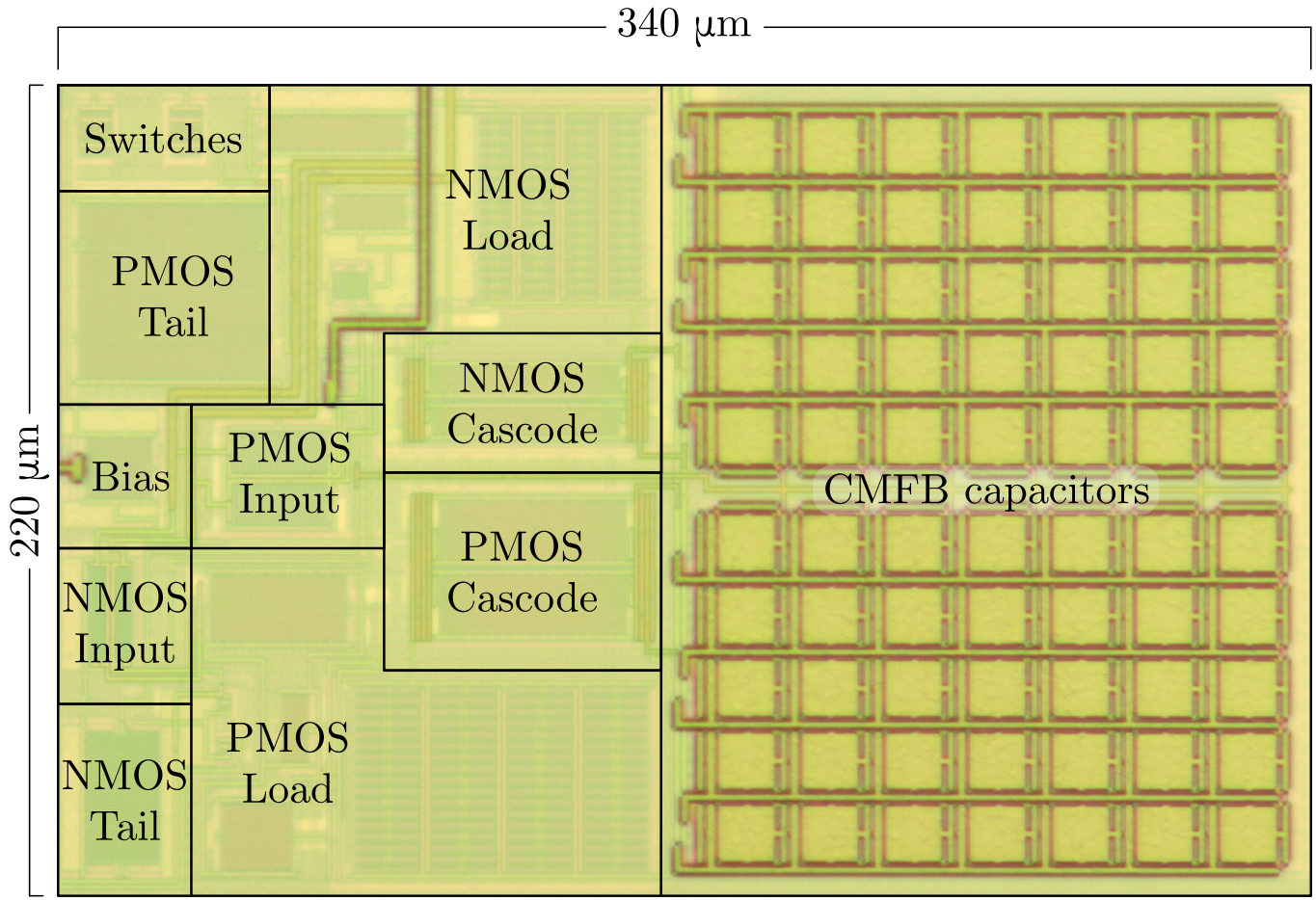

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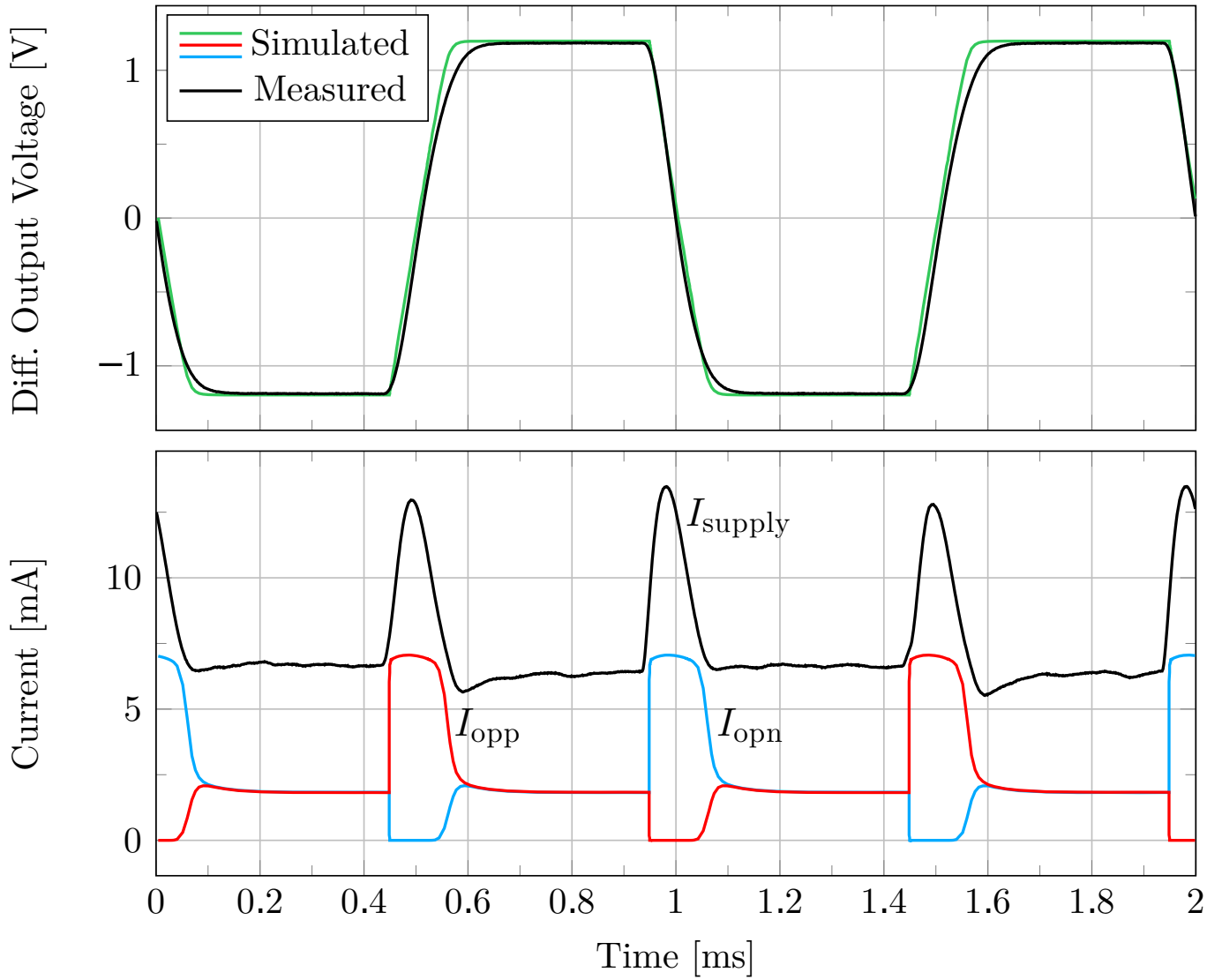
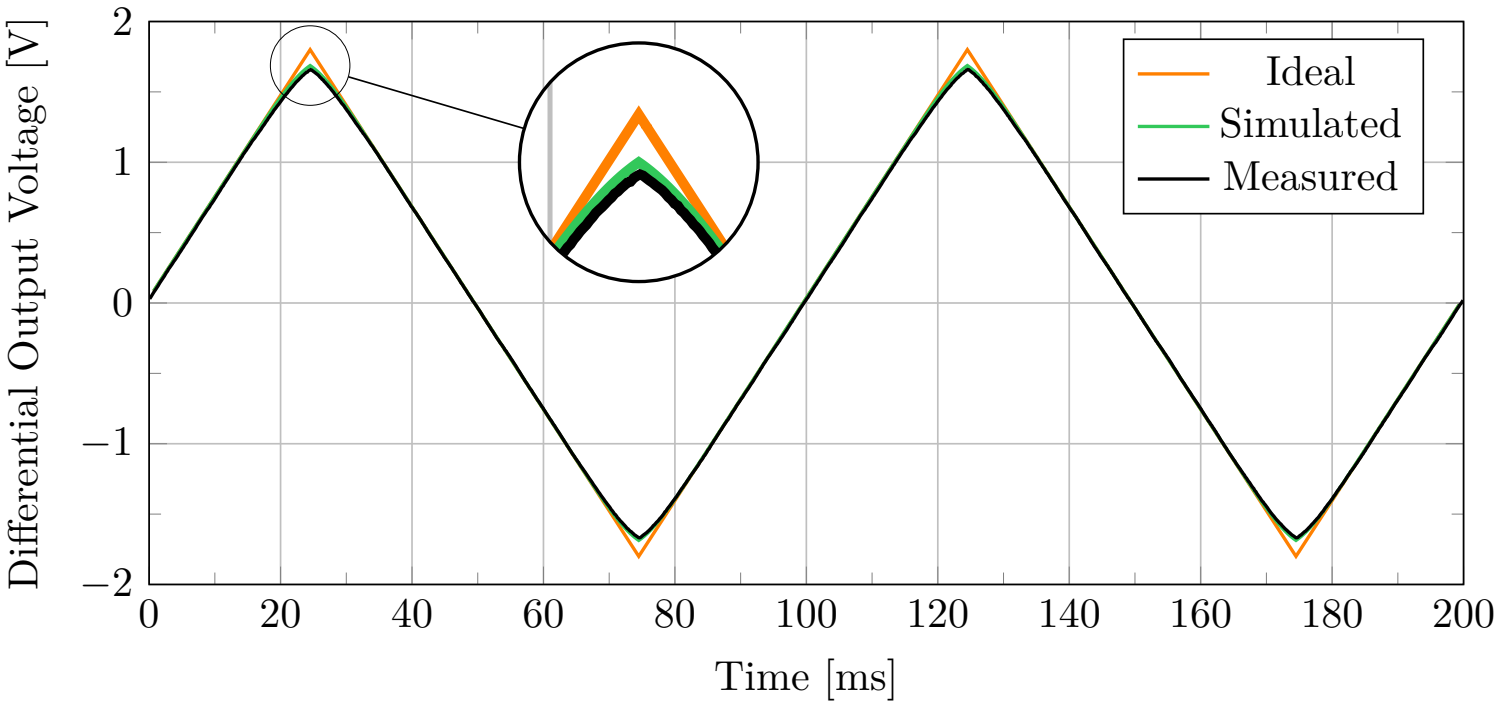
Step Response



Full-Scale Evaluation



- **3.3-V_{pp}** differential full scale at 1.8-V voltage supply

Figure-of-Merit Comparison

Parameter	[1]	[2]	[3]	[4]	[5]	This work	Units
Technology	0.5	0.5	0.25	0.13	0.18	0.18	µm
Supply	2	2	1.2	1.2	0.8	1.8	V
DC gain	43	45	69	70	51	72	dB
C_{load}	80	25	4	5.5	8	200	pF
GBW	0.725	11	165	35	0.057	86.5	MHz
Phase margin	89.5	N/A	65	45	60	50	°
Slew rate, SR	89	20	329	19.5	0.14	74.1	V/µs
Static power, P	0.12	0.04	5.8	0.11	0.0012	11.9	mW
Area	0.024	0.012	N/A	0.012	0.057	0.07	mm^2
FOM	59.33	12.50	0.28	0.98	0.93	**1.25**	$\frac{\text{V}}{\text{µs}}\frac{\text{pF}}{\text{µW}}$

$$\text{FOM} = \frac{\text{SR}\cdot C_{\text{load}}}{P} \qquad \left[\frac{\text{V}}{\text{µs}}\frac{\text{pF}}{\text{µW}}\right]$$

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Conclusions

- New family of **Class-AB OpAmps**
- **Single-stage** topology
- **No** need for an internal frequency **compensation**
- Class-AB current **peaks in the output transistors only**
- **Low sensitivity** to the technology parameter variations
- **Simple** analytical design flow
- **Successfully used** in a 16-bit 100-kS/s $\Delta\Sigma$ ADC

Thank you!

References

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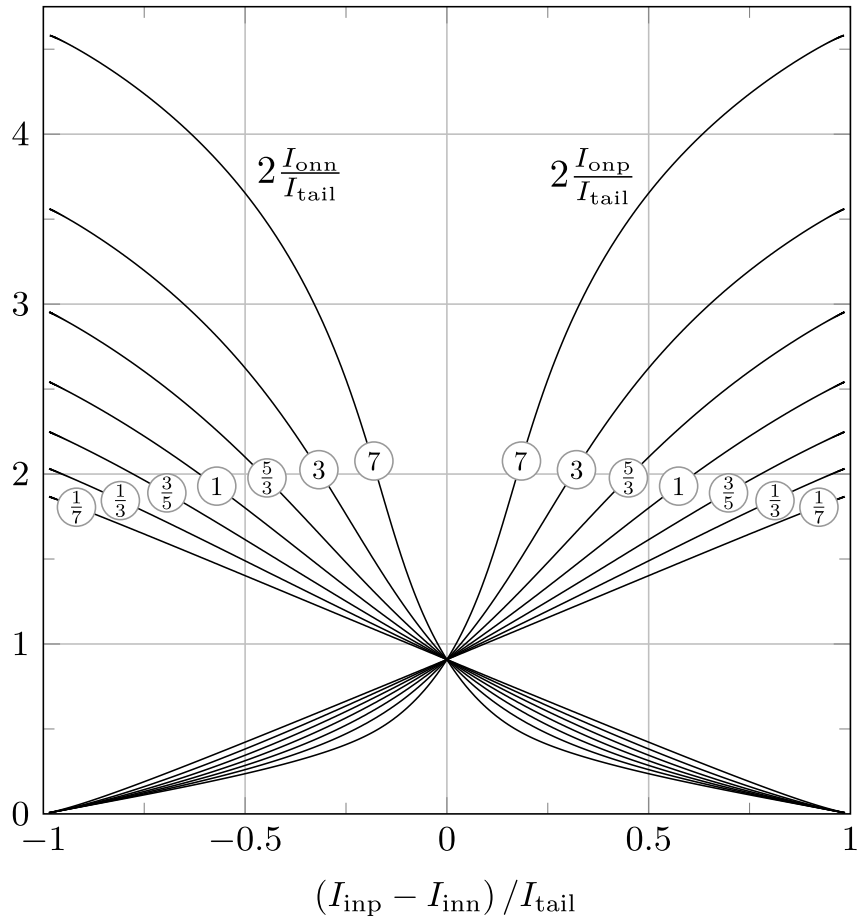
Normalized Current Transfer Curve for Different B/C Ratios



Normalized Current Transfer Curve Under Corners for B/C=3