Class-AB Single-Stage OpAmp for Low-Power Switched-Capacitor Circuits

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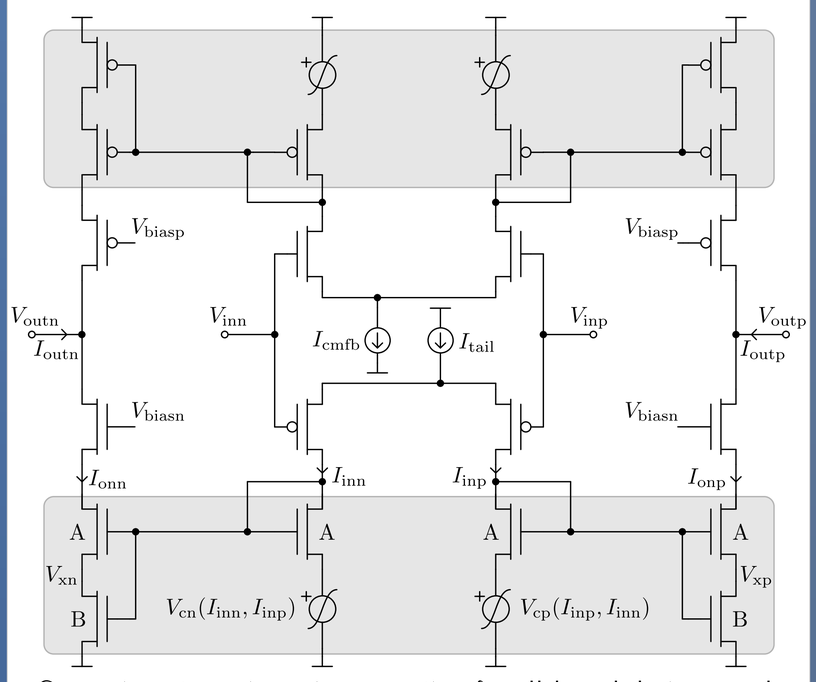
Abstract

A new family of Class-AB OpAmp circuits based on single-stage topologies with non-linear current amplifiers is presented. The proposed architecture is characterized by generating all Class-AB current in the output transistors only. It exhibits low sensitivity to technology parameter variations and avoids the need for internal frequency compensation. It is suitable for low-power switched-capacitor circuits and optimized for a fast on-off operation and multi-decade load-capacitance specifications. A complete OpAmp design example is integrated in a standard 0.18-µm 1P6M CMOS technology. Compared to the MOS-only state-of-the-art Class-AB OpAmps, the presented architecture obtains the highest figure of merit.

Architecture

A single-stage-OpAmp architecture is proposed with two complementary Class-AB control paths for the NMOS and PMOS output transistors.



Supposing strong inversion operation for all boxed devices, each non-linear current amplifier behaves as

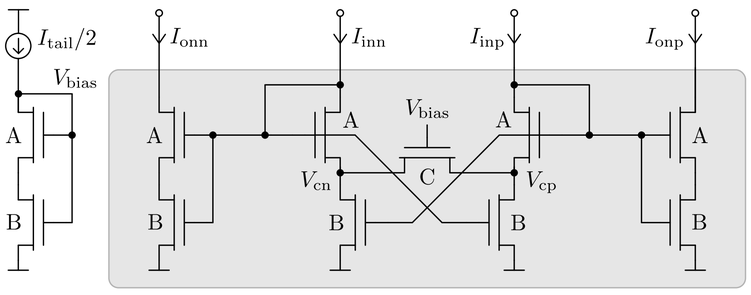
$$\sqrt{\frac{I_{onp}}{D}} = \sqrt{\frac{I_{inp}}{A}} + \sqrt{\frac{n\beta}{2}} V_{cp} \qquad D \doteq \frac{AB}{A+B}$$

From the Class-AB viewpoint, the wanted functionality for these voltage-controlled current mirrors is:

$$\begin{cases} I_{outp} \equiv 0 \quad V_{cp} \equiv V_{xp} \quad I_{onp} \equiv I_{inp} \equiv \frac{I_{tail}}{2} & \text{Bias point} \\ I_{outp} \not\equiv 0 \quad V_{cp} \not\equiv V_{xp} \quad \begin{cases} I_{onp} \ll I_{inp} \\ I_{onp} \gg I_{inp} \end{cases} & \text{Class-AB operation} \end{cases}$$

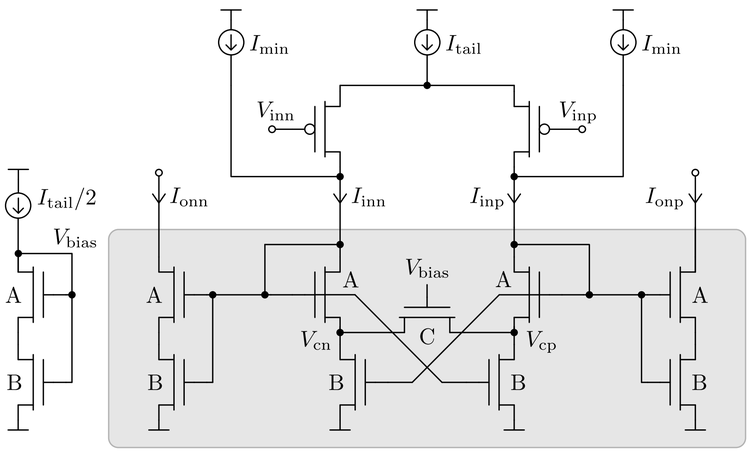
Type-I Circuit

A cross-coupled pair (B-B) is introduced to provide the positive feedback for the Class-AB operation, while a crossing transistor (C) play the role of a feedback limiter.



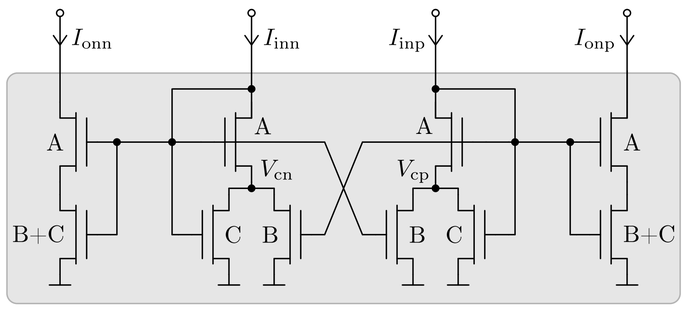
$$I_{inp} = B\left(2\sqrt{\frac{I_{onn}}{D}} - \sqrt{\frac{I_{onp}}{D}} + \sqrt{\frac{I_{inp}}{A}}\right)\left(\sqrt{\frac{I_{onp}}{D}} - \sqrt{\frac{I_{inp}}{A}}\right) + C\left(\sqrt{\frac{2I_{tail}}{D}} - \sqrt{\frac{I_{onp}}{D}} - \sqrt{\frac{I_{onn}}{D}} + \sqrt{\frac{I_{inp}}{A}} + \sqrt{\frac{I_{inn}}{A}}\right)\left(\sqrt{\frac{I_{onp}}{D}} - \sqrt{\frac{I_{onn}}{D}} - \sqrt{\frac{I_{inp}}{A}} + \sqrt{\frac{I_{inn}}{A}}\right)$$

The process parameters β and n disappear from the current-amplifier equation. Hence, independence from technology is achieved. Under Class-AB high modulation, common-mode currents can be injected to prevent a possible self-latch.



Type-II Circuit

Here, the crossing transistor (C) of the Type-I circuit is replaced by two split counterparts (C-C), which are auto-biased. Thus, extra reference circuits are not needed and power consumption is reduced.



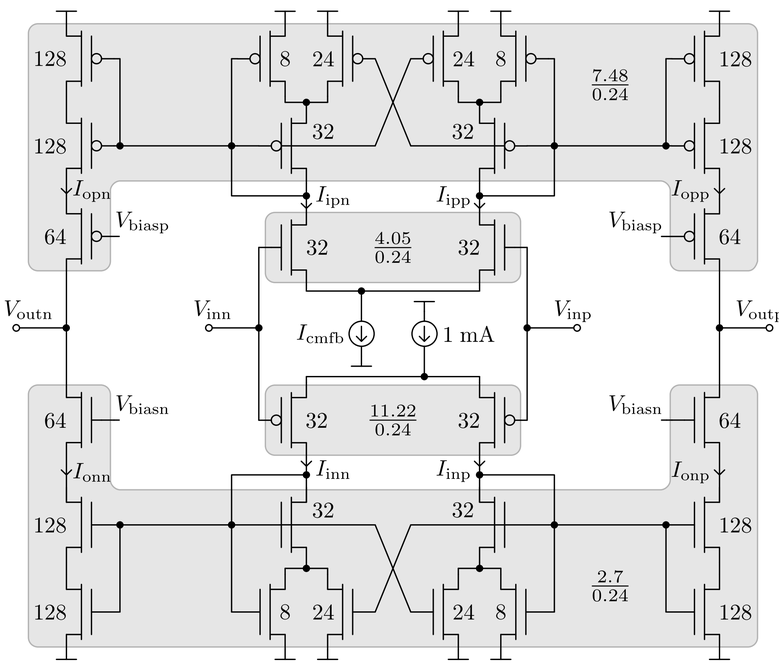
$$I_{inp} = \left[2\left(B\sqrt{\frac{I_{onn}}{D}} + C\sqrt{\frac{I_{onp}}{D}}\right) - (B+C)\left(\sqrt{\frac{I_{onp}}{D}} - \sqrt{\frac{I_{inp}}{A}}\right)\right]\left(\sqrt{\frac{I_{onp}}{D}} - \sqrt{\frac{I_{inp}}{A}}\right)$$

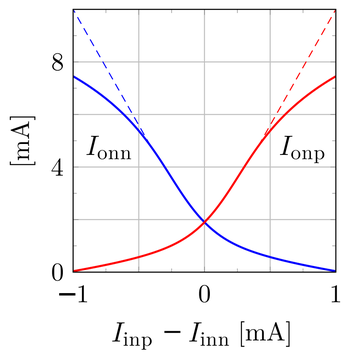
$$D \doteq \frac{A(B+C)}{A+B+C} \qquad I_{max} \simeq \frac{1+\frac{A}{C}}{1+\frac{A}{B+C}} I_{tail} > I_{tail}$$

Independence from the technology parameters is also preserved.

Practical Design

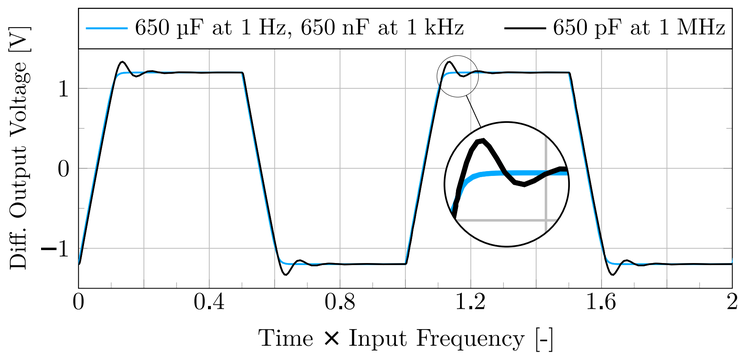
Type-II architecture is chosen for the design example in a 0.18-µm CMOS technology node.



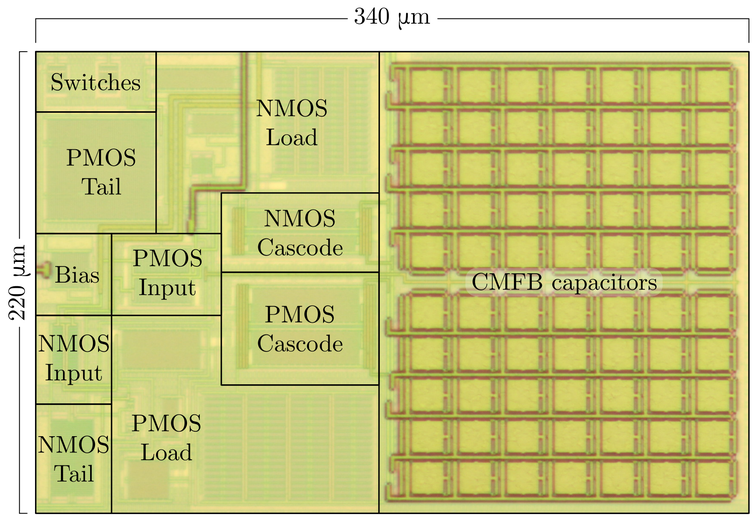


As shown, the number of transistor groups is minimized and minimum device lengths can be used. In this particular case, optimization finds the best performance for A=4, B=3 and C=1. The Class-AB behavior is demonstrated for the NMOS outputs.

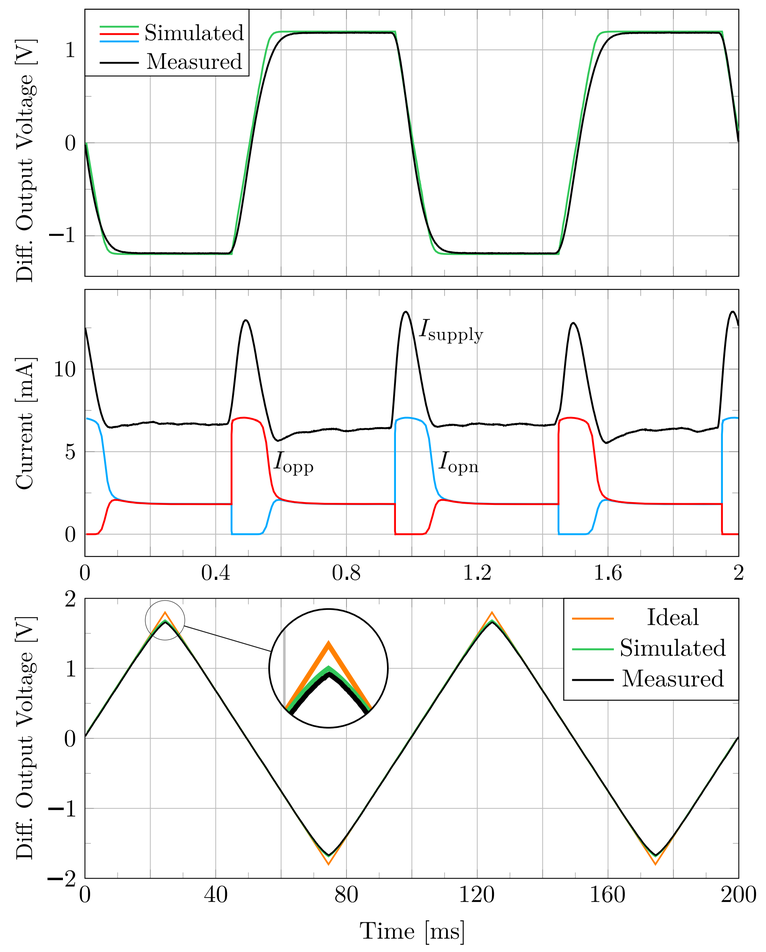
The OpAmp is stable for a wide range of load capacitance values.



The OpAmp is integrated using a standard 0.18-µm 1P6M CMOS technology, achieving an overall area of 0.07-mm^2. The circuit layout includes additional common-mode feedback (CMFB) averaging capacitors for switched-capacitor applications.



Experimental Results



Operating at a 1.8-V power supply, a remarkable differential full scale of 3.3 V_{pp} is measured. The performance of the proposed OpAmp is compared with others from published Class-AB amplifiers [1]–[5] by using the figure of merit (FOM) from [5]

$$\text{FOM} = \frac{\text{SR} \cdot C_{load}}{P} \quad \left[\frac{\text{V}}{\mu\text{s}} \frac{\text{pF}}{\mu\text{W}}\right].$$

Parameter	[1]	[2]	[3]	[4]	[5]	This work	Units
Technology	0.5	0.5	0.25	0.13	0.18	0.18	µm
Supply	2	2	1.2	1.2	0.8	1.8	V
DC gain	43	45	69	70	51	72	dB
C_{load}	80	25	4	5.5	8	200	pF
GBW	0.725	11	165	35	0.057	86.5	MHz
Phase margin	89.5	N/A	65	45	60	50	°
Slew rate, SR	89	20	329	19.5	0.14	74.1	V/µs
Static power, P	0.12	0.04	5.8	0.11	0.0012	11.9	mW
Area	0.024	0.012	N/A	0.012	0.057	0.07	mm^2
FOM	59.33	12.50	0.28	0.98	0.93	**1.25**	$\frac{\text{V}}{\mu\text{s}} \frac{\text{pF}}{\mu\text{W}}$

The works [1], [2] report higher FOM, but at the cost of requiring integrated resistors, which makes them more sensitive to technology parameter variations, and of a considerable lowering of their DC gain, which may be incompatible with high-precision applications. The works using MOS-only devices [3]–[5] present lower FOM and DC gain. Therefore, a contribution to the improvement of MOS-only Class-AB OpAmps is demonstrated.

Conclusions

- A new family of **Class-AB OpAmps** has been presented.
- The architecture is based on a **single-stage** topology.
- The circuits do **not need** any internal frequency **compensation**.
- The Class-AB current peaks are produced in the output transistors only.
- The resulting OpAmps exhibit **low sensitivity** to the technology parameter variations.
- Good performance is achieved using a **simple** design flow.
- The Type II has been **successfully used** in a 16-bit 100-kS/s $\Delta\Sigma$ ADC.

References

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