A 10kfps 32x32 Integrated Test Platform for Electrical Characterization of Imagers

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1 Introduction

2 ITP Architecture

3 ITP Pixel Cell

4 Low-Cost CMOS Integration

5 Experimental Results

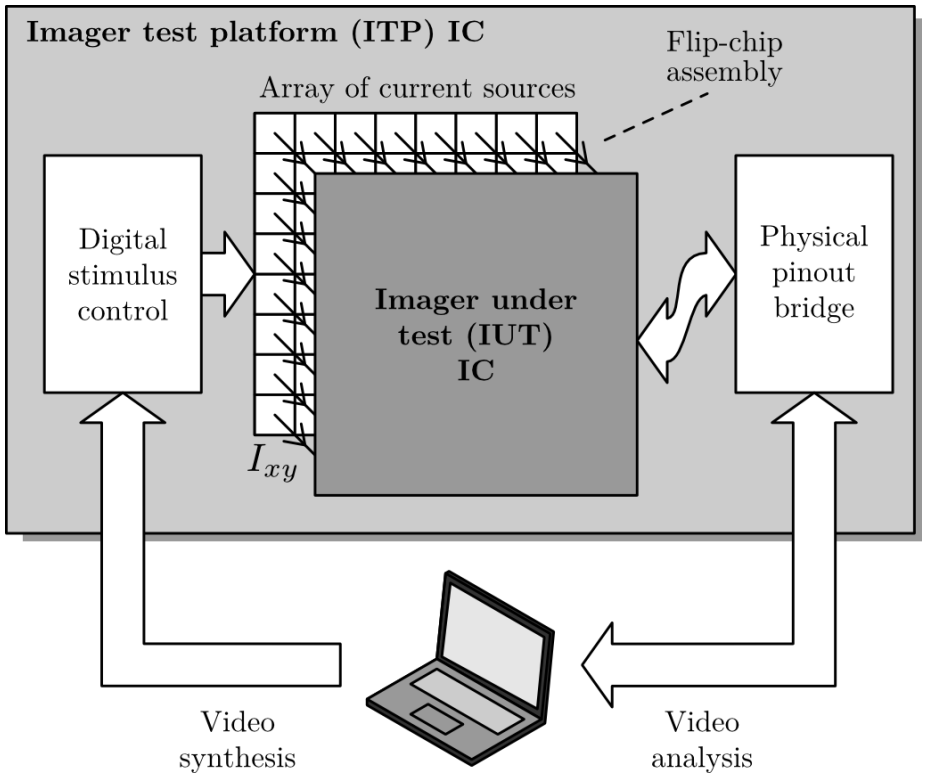
6 Conclusions

Introduction

- How to **characterize** imager response to **image patterns** and **motion sequences**?

1. **Standard approach: Optical** stimulation (LED arrays, TFT displays, mechanical choppers...)
   - ▼ **Bulky** + optical chain **uncertainty**
   - ▼ Requires detector: **Not** suitable for **electrical direct tests**

2. **Our proposal: Electrical Imager test platform (ITP)** custom IC + **Imager under test (IUT)** attached pixel-by-pixel to ITP by flip-chip packaging
   - ▲ **Compact** setup



- ▲ ITP **digital current sources** (I_{xy}) allow direct stimulation of each **individual** IUT **pixel**
- ▲ **Hybrid imager** prototypes can be tested before sensor integration at wafer level (e.g. IR and X-ray imagers)

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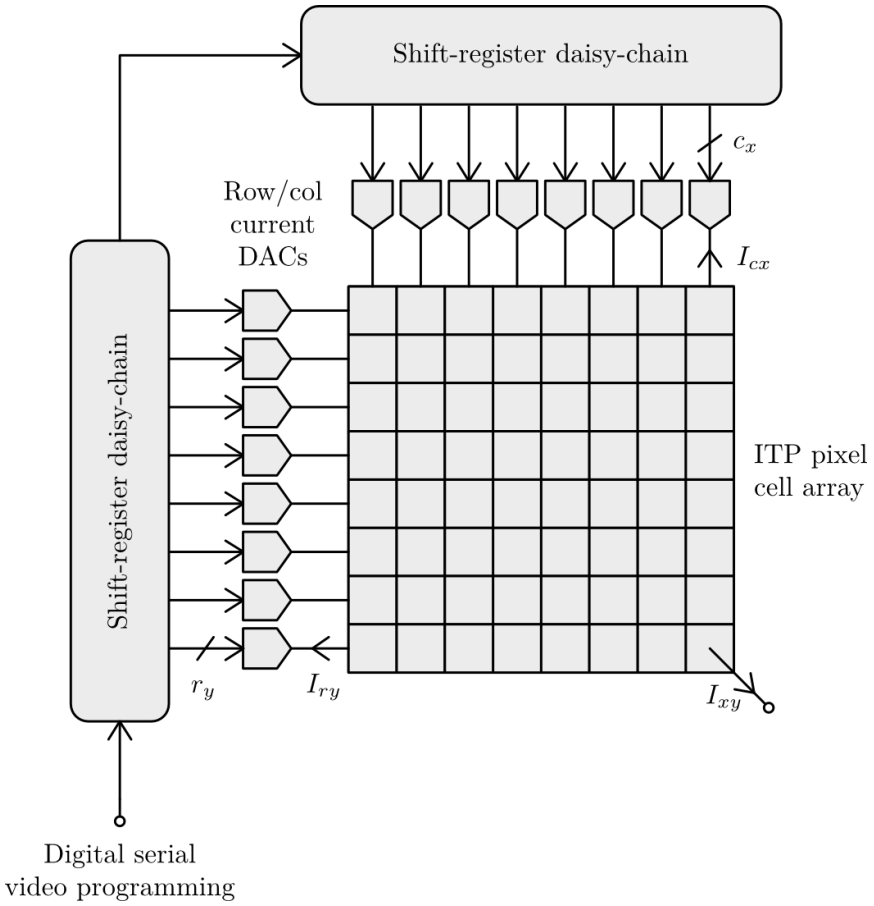
ITP Architecture

- 2D array of **digitally controlled** current sources (I_{xy})
- I_{xy} individual value obtained as a combination of **row** (I_{ry}) and **column** (I_{cx}) **currents**
- Programmed at **each frame** through ry and cy digital codes and **peripheral current DACs**
- **Compact** pixel pitch
- Square root **scalability** with image size
- Reduced programming data size enables **high frame rates**



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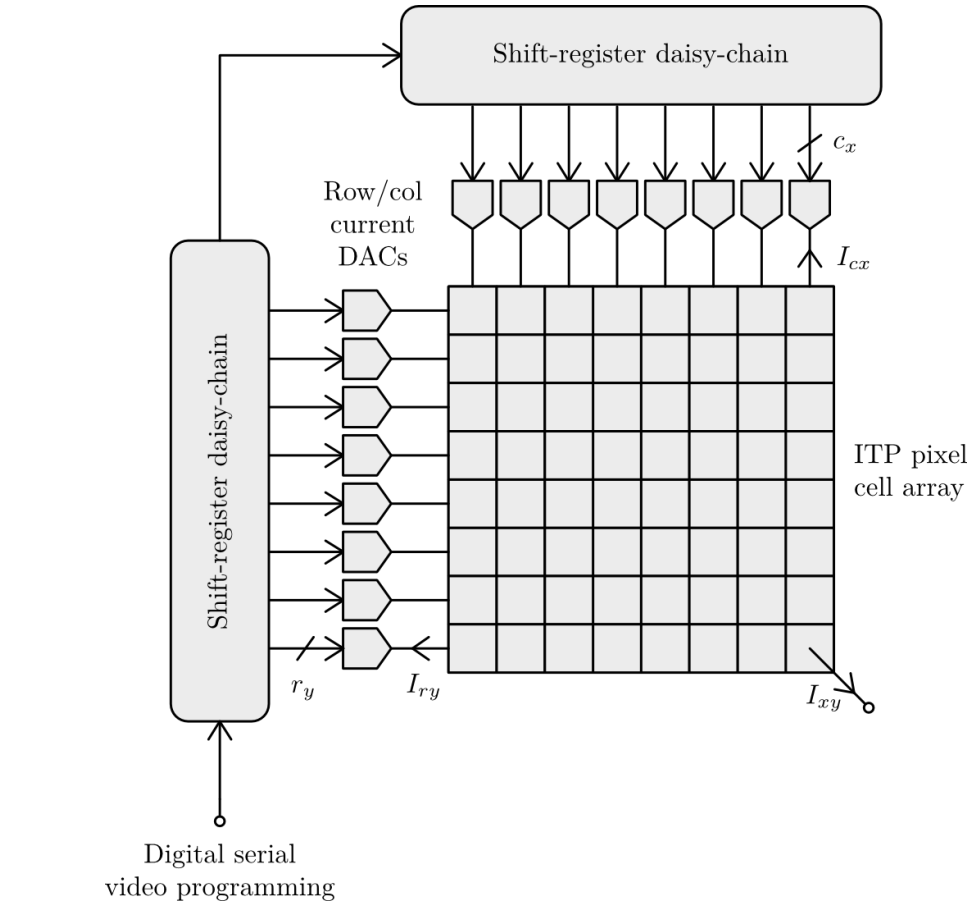
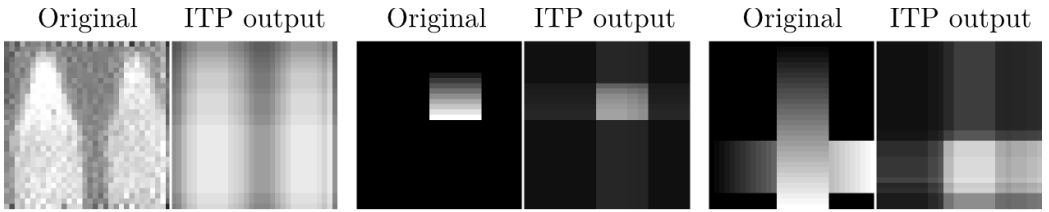
- Synthesizable images are reduced to practical **moving test patterns** (e.g. rectangles, lines, gradients)





1 Introduction

2 ITP Architecture

3 ITP Pixel Cell

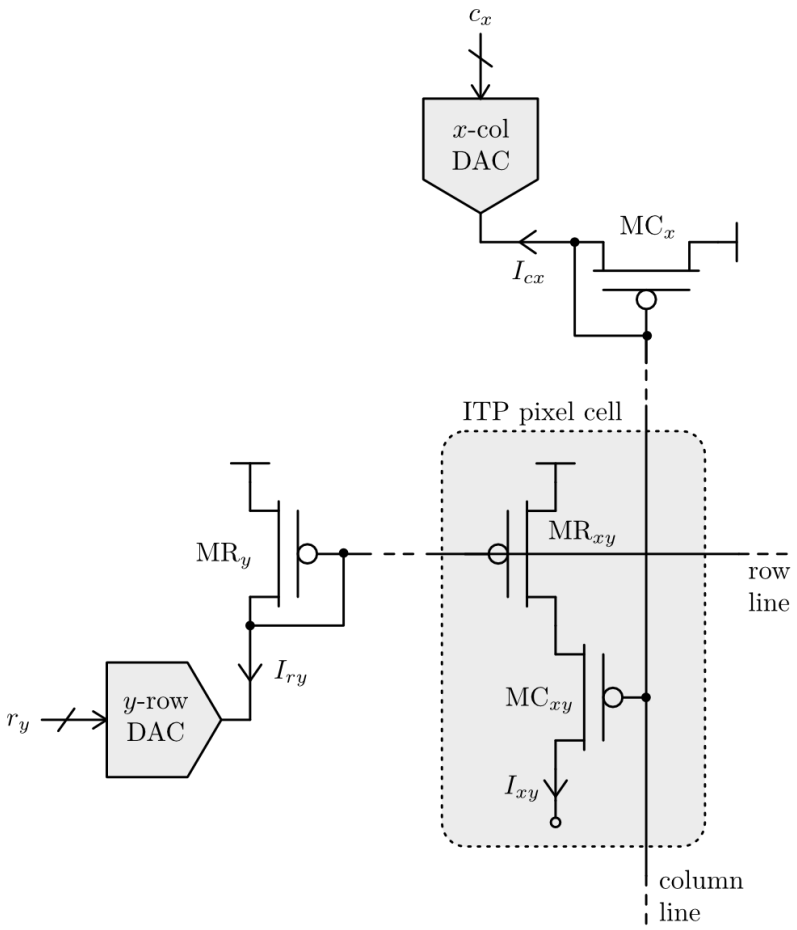
4 Low-Cost CMOS Integration

5 Experimental Results

6 Conclusions

ITP Pixel Cell

- **2-transistor** only pixel
- **Matching** at row (MR_{xy}-MR_y) and column (MC_{xy}–MC_x) levels
- **Strong inversion** operation for all devices and forward saturation for MC_{xy}, MR_y and MC_x:
- **Independence** from technology improves fixed pattern noise (FPN) and integration yield
- **Non-linear** behavior



$$I_{xy} = \frac{1}{4}\left(\sqrt{I_{cx}} - \sqrt{I_{ry}} + \sqrt{I_{ry} - I_{cx} + 2\sqrt{I_{ry}I_{cx}}}\right)^2$$

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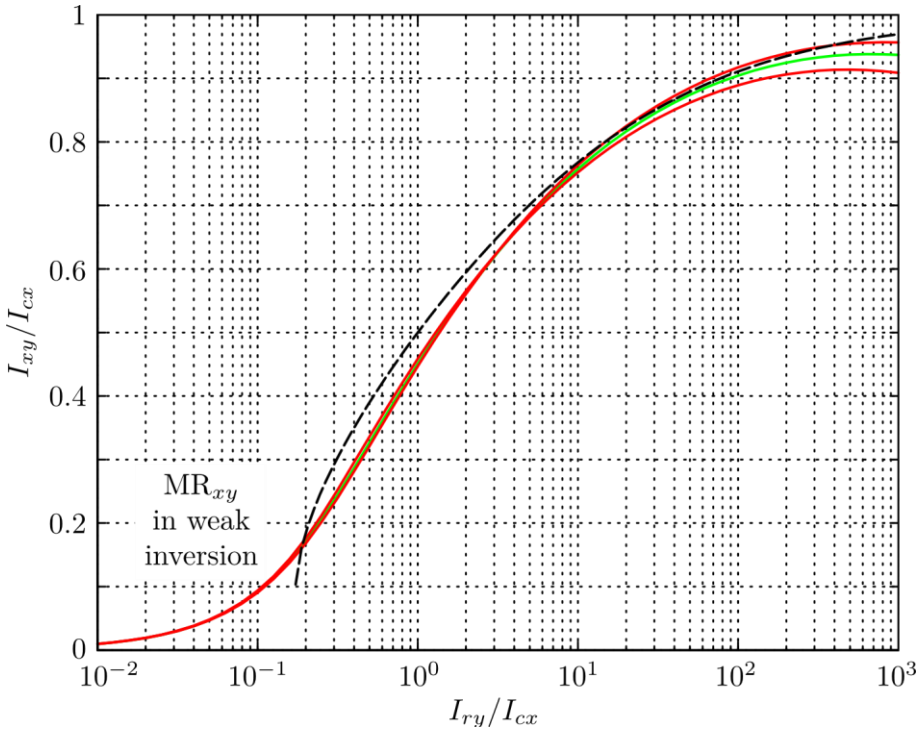
- ▲ Good agreement between **analytical-simulated** results. Linearization through digital **pre-emphasis**
- ▲ **Low sensitivity** against CMOS process corners

- **Row** control only:



$$\frac{I_{xy}}{I_{cx}} = \frac{1}{4}\left(1 - \sqrt{\frac{I_{ry}}{I_{cx}}} + \sqrt{\frac{I_{ry}}{I_{cx}} - 1 + 2\sqrt{\frac{I_{ry}}{I_{cx}}}}\right)^2$$

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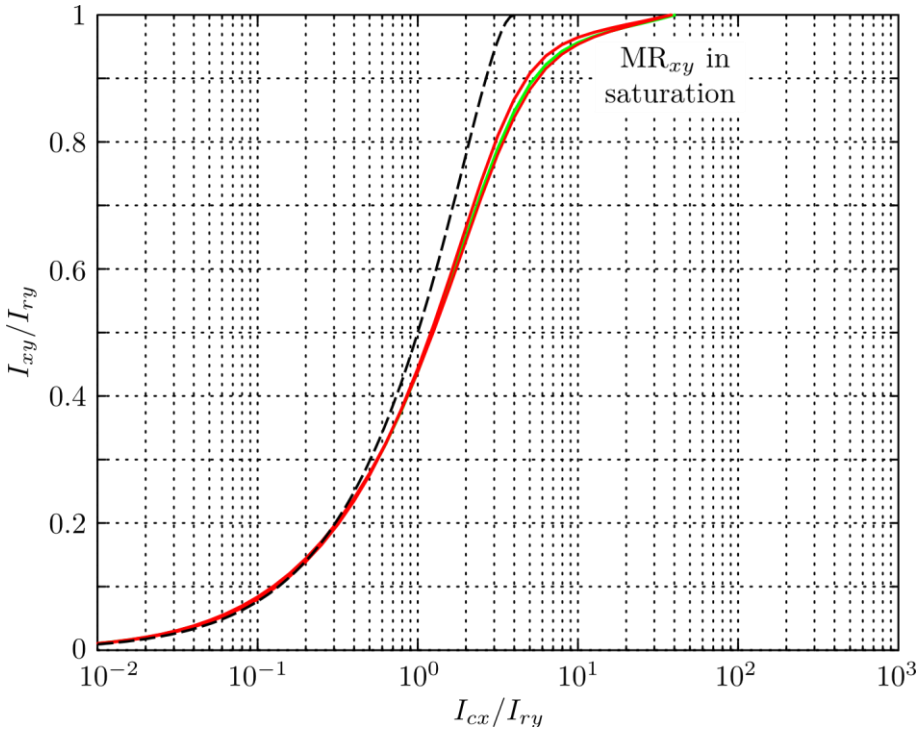
- **Column** control only:



$$\frac{I_{xy}}{I_{ry}} = \frac{1}{4}\left(\sqrt{\frac{I_{cx}}{I_{ry}}} - 1 + \sqrt{1 - \frac{I_{cx}}{I_{ry}} + 2\sqrt{\frac{I_{cx}}{I_{ry}}}}\right)^2$$

1 Introduction

2 ITP Architecture

3 ITP Pixel Cell

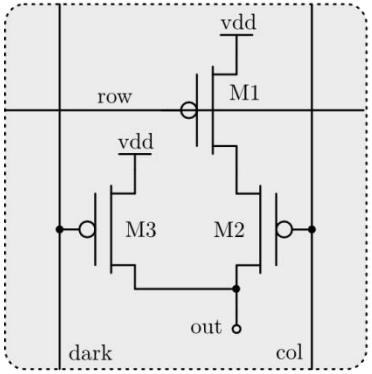
4 Low-Cost CMOS Integration

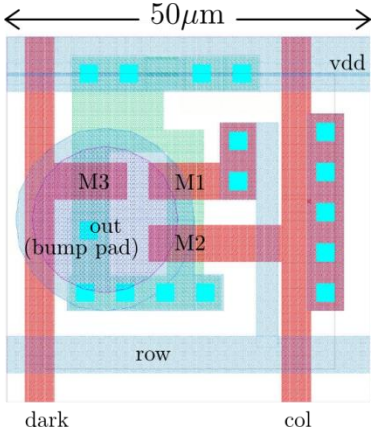
5 Experimental Results

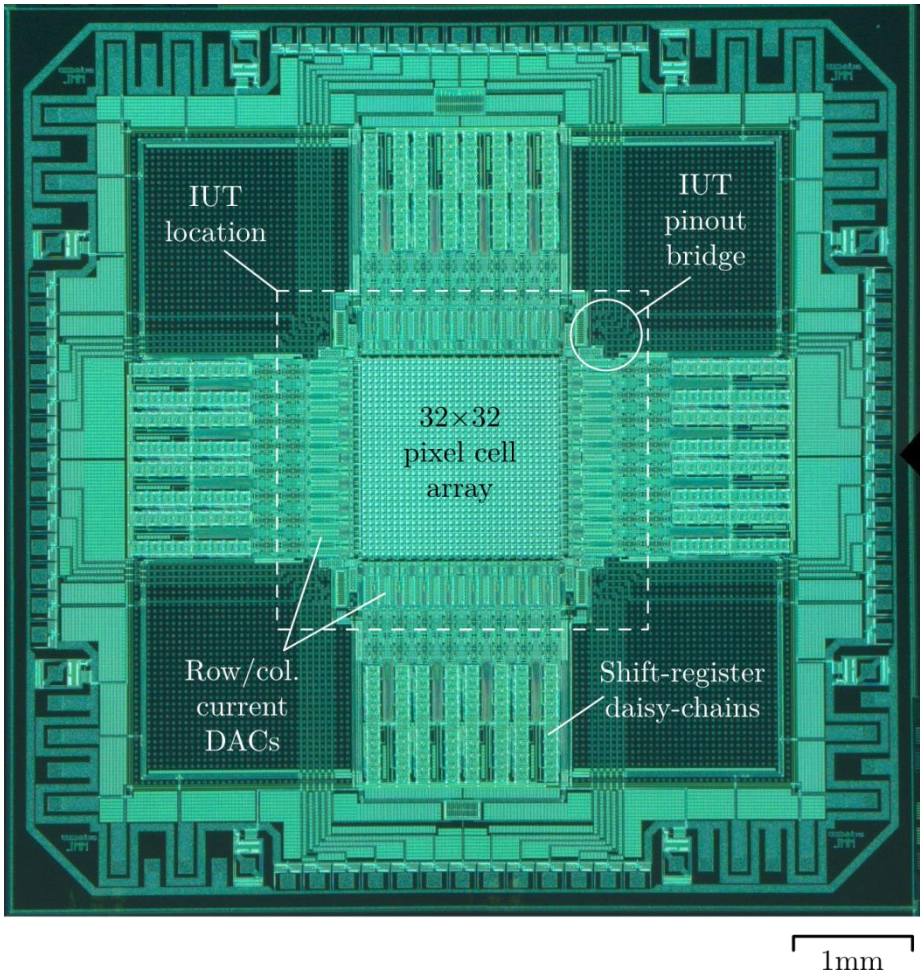
6 Conclusions

CMOS Integration

- **32x32-pix 50µm-pitch** ITP
- **Low-cost** 2.5µm 1M CMOS tech. suitable for full-wafer flip-chip
- Global **dark current** added to pixel cell (M3)
- **4-bit** (16-level) row and column current DAC programmability







$$I_{xy} = I_{bkgd} + \frac{1}{4}\frac{I_{fs}}{16}\left(\sqrt{c_x} - \sqrt{r_y} + \sqrt{r_y - c_x + 2\sqrt{r_y c_x}}\right)^2$$

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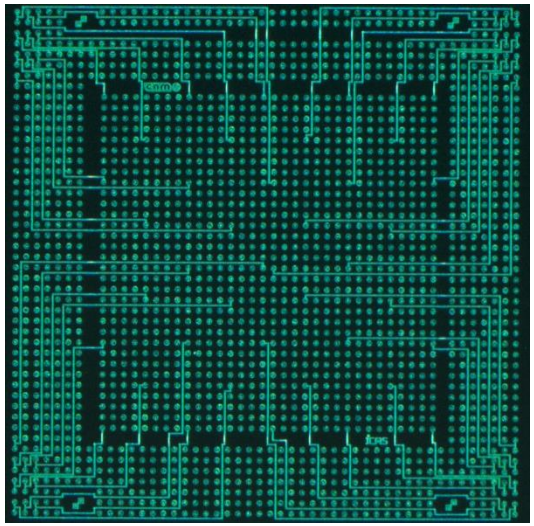
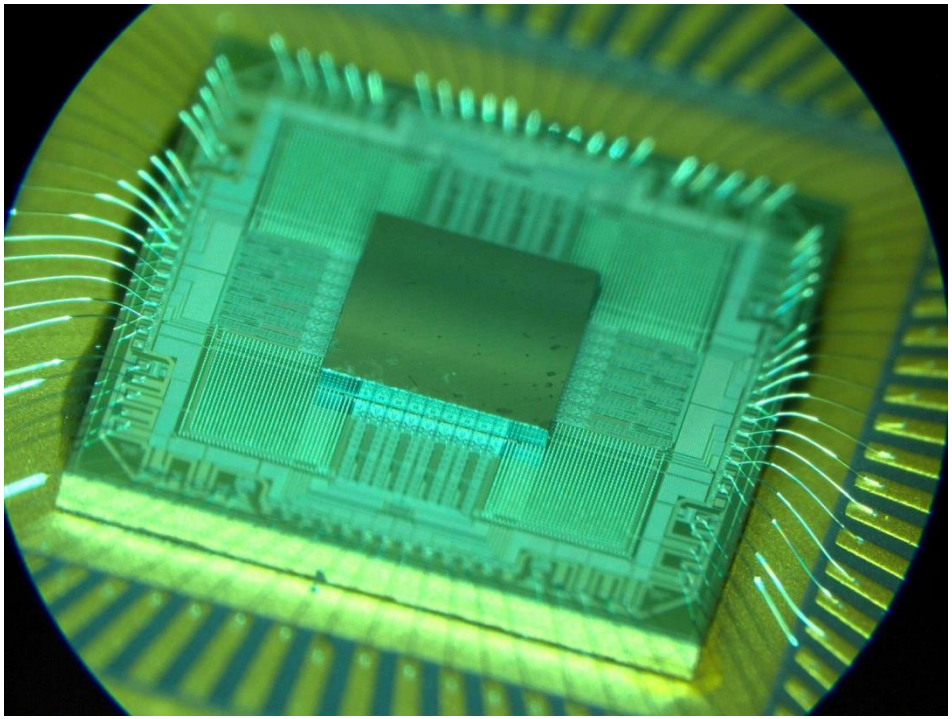


- **Phantom IUT** chip (3x3mm^2) with **routing map** for the direct measurement of selected ITP pixel cells



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2 ITP Architecture

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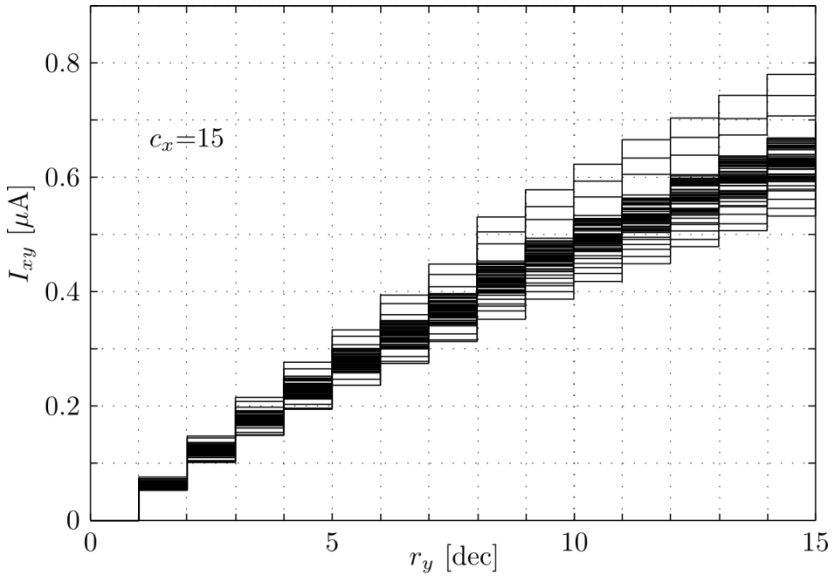
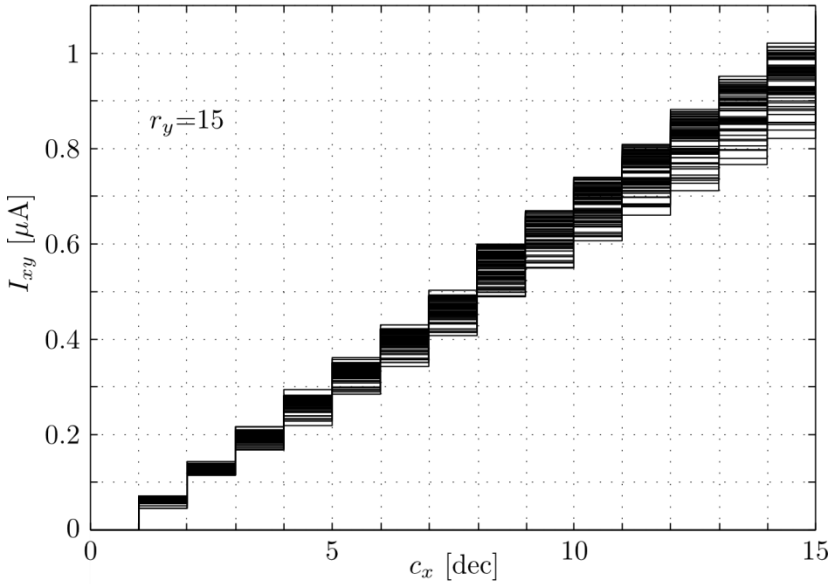
Experimental Results

- Individual pixel current **programmability** can cover practical levels of sensor **background** and **full-scale**
- **5%$_{rms}$ FPN** from 50 pixel readings of 3 ITP dies





Experimental Results

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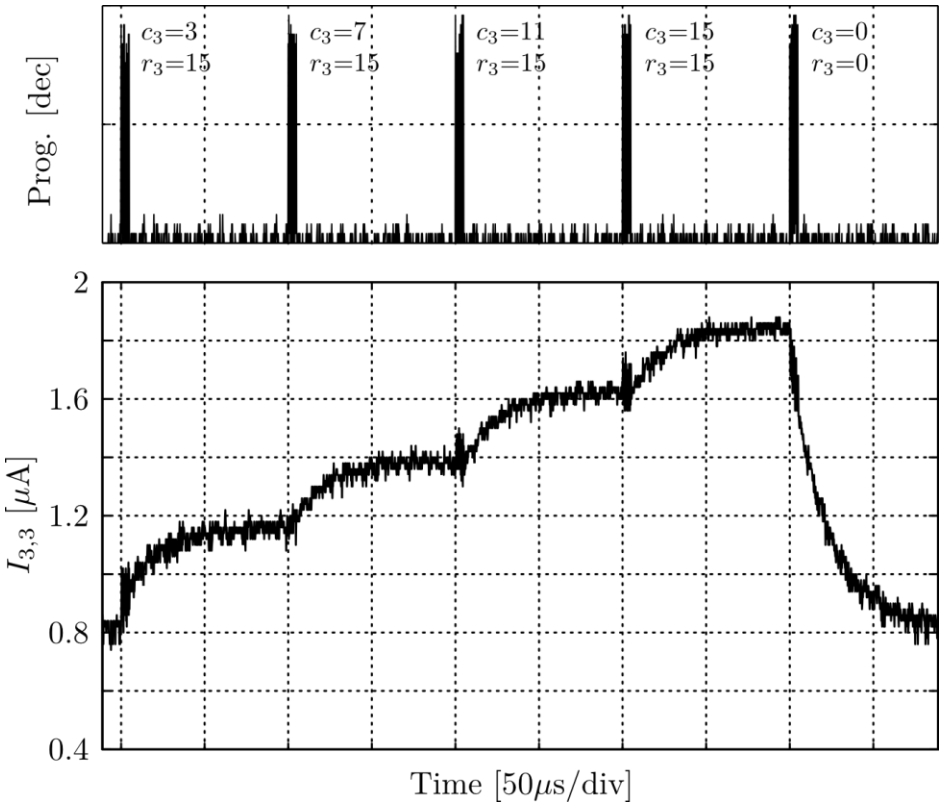
- **5%$_{rms}$ FPN** from 50 pixel readings of 3 ITP dies
- **10kfps** rate achievable with smooth transitions

Parameter	Value	Units
Array size	32×32	pix
Pixel pitch	50	μm
Digital row/col control	4	bit
Full-scale current range	0 to 4	μA
Background current range	0 to 10	μA
Fixed pattern noise	< 5	$\%_{rms}$
Max. prog. rate	20	Mbps
Max. image rate	10	kfps
Supply voltage	5	V
Die area	7.2×7.2	mm^2



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3 ITP Pixel Cell

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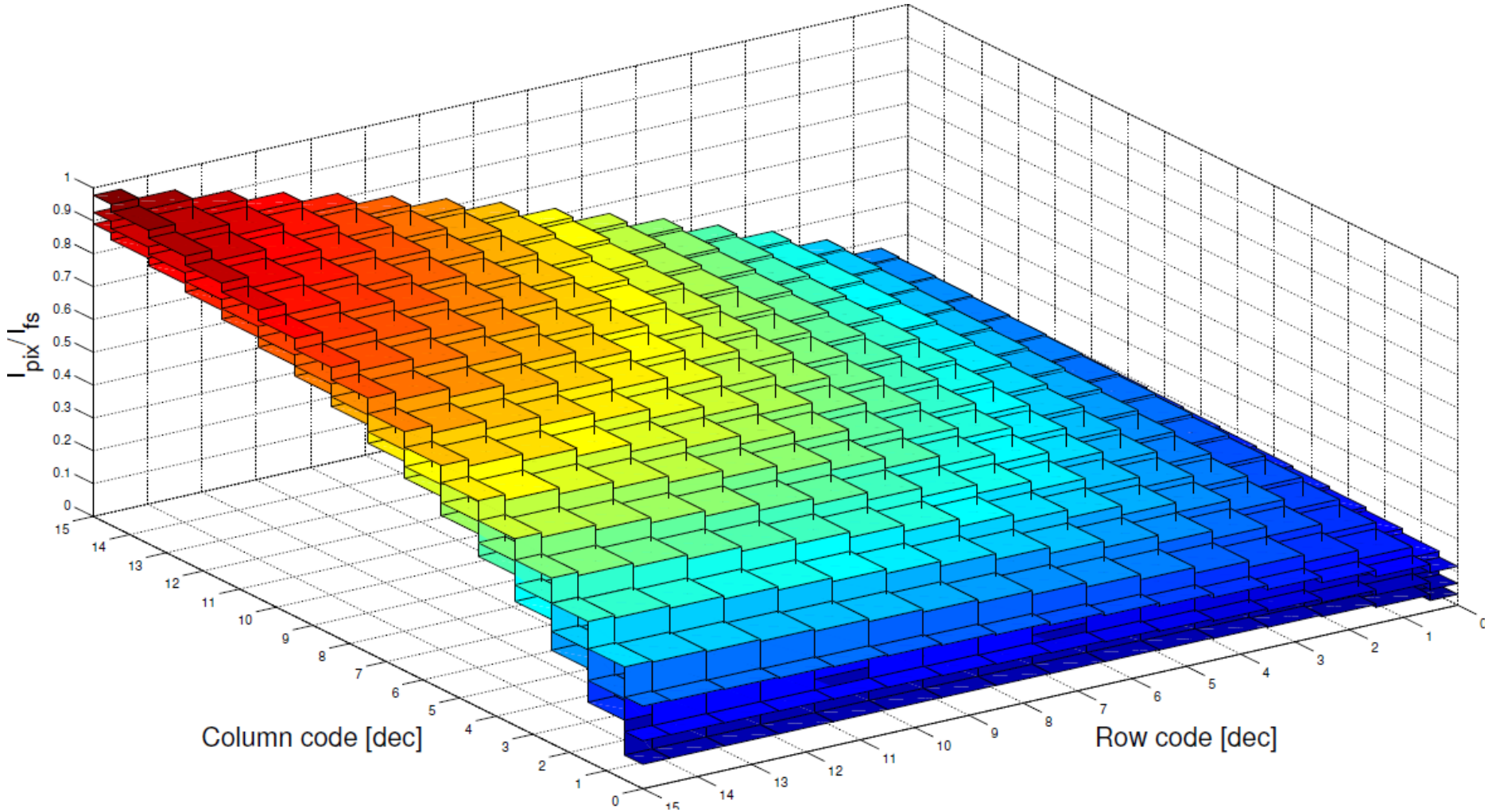
Conclusions

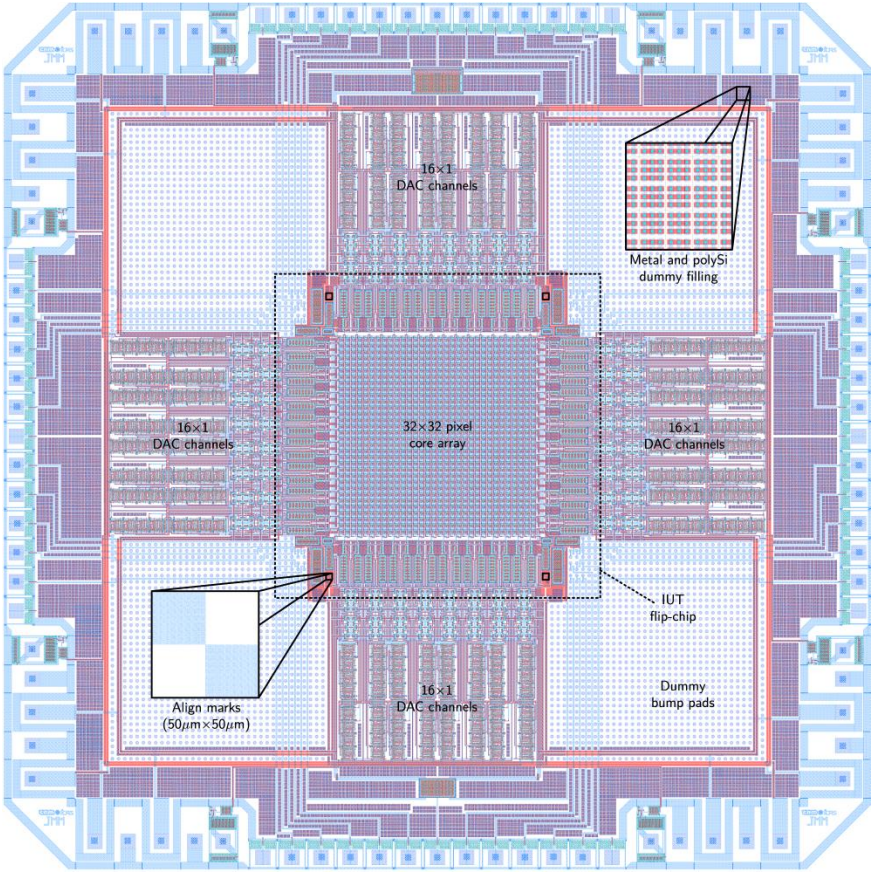
- Novel **integrated test platform** (ITP) proposal for imagers
- Direct **electrical test** of each individual imager **pixel**
- Combined row/column **digital** programmability with **low technology** sensitivity
- Synthesis of practical image **test patterns** and high-speed **motion** sequences
- **32x32-pix** 4x4-bit ITP example in **low-cost** 2.5µm 1M CMOS technology
- **Experimental results** return µA-range 5%$_{rms}$-FPN 10kfps performance suitable for imager testing

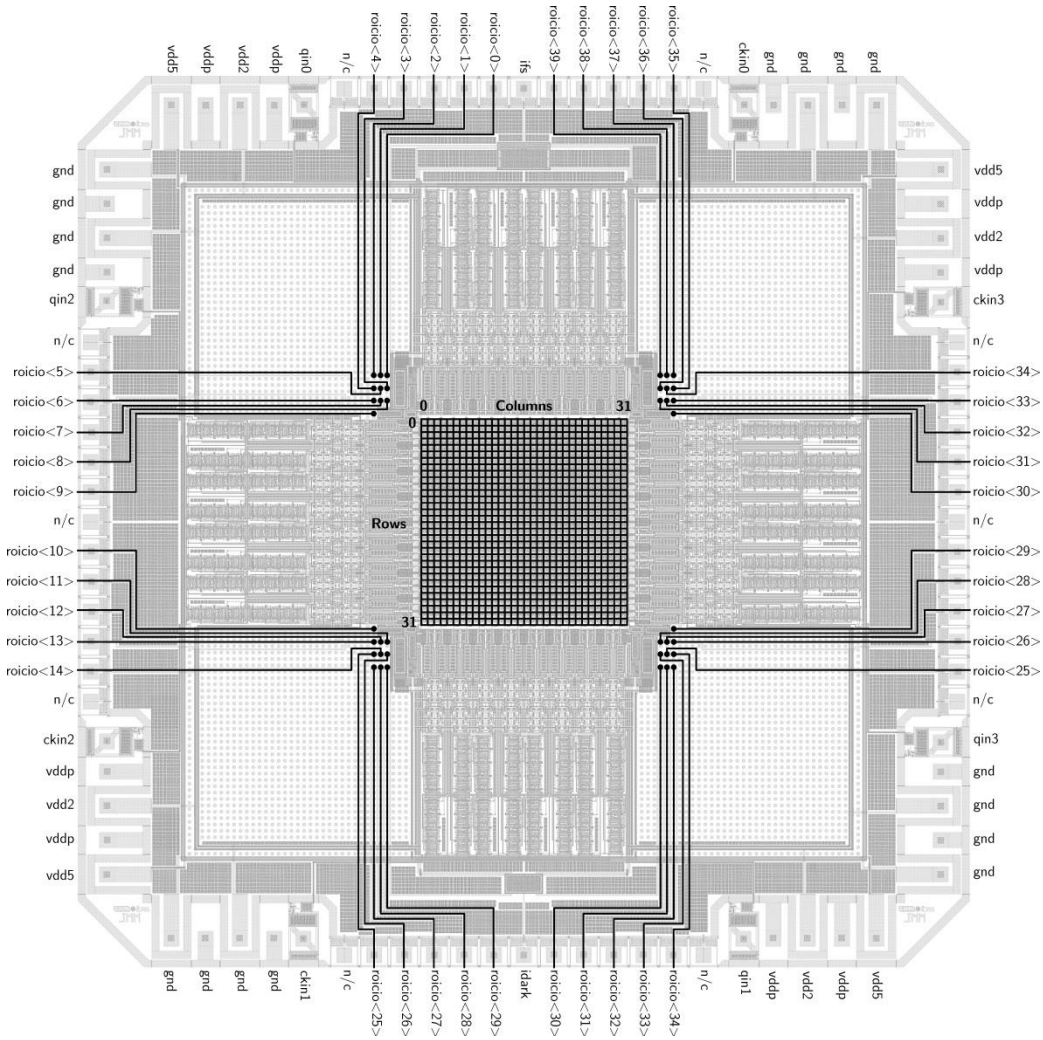
Thanks for your attention!!!

I_{pix} Programmability

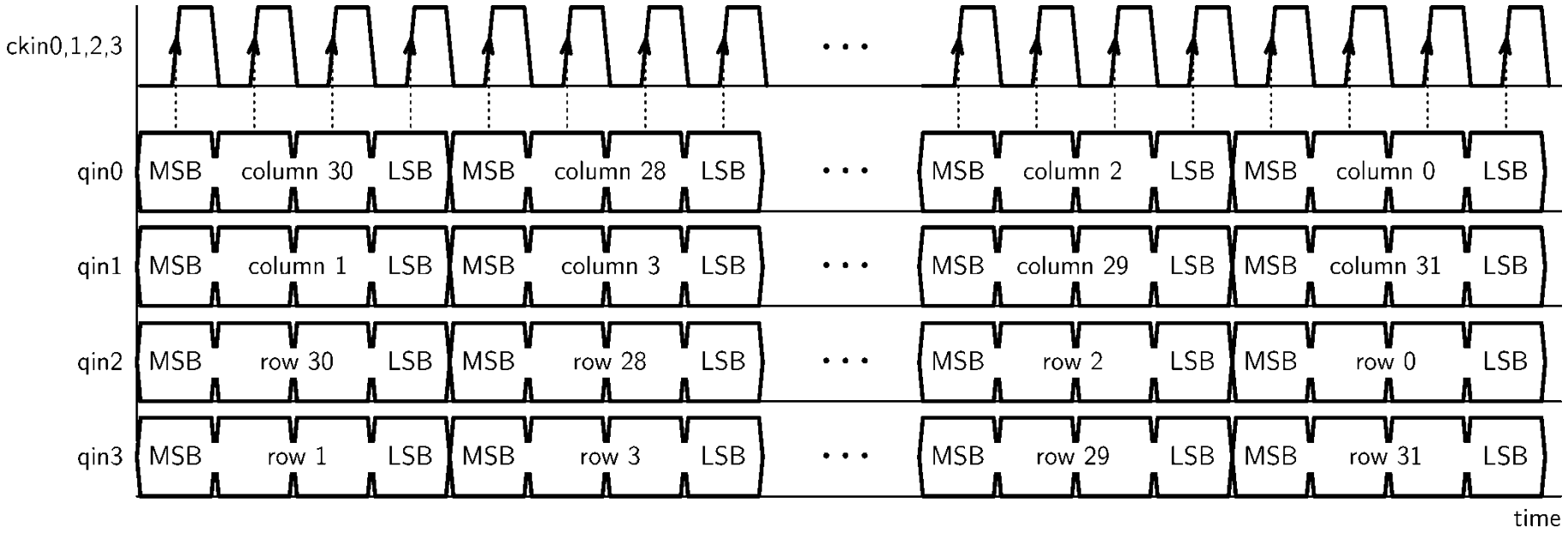


ITP Layout

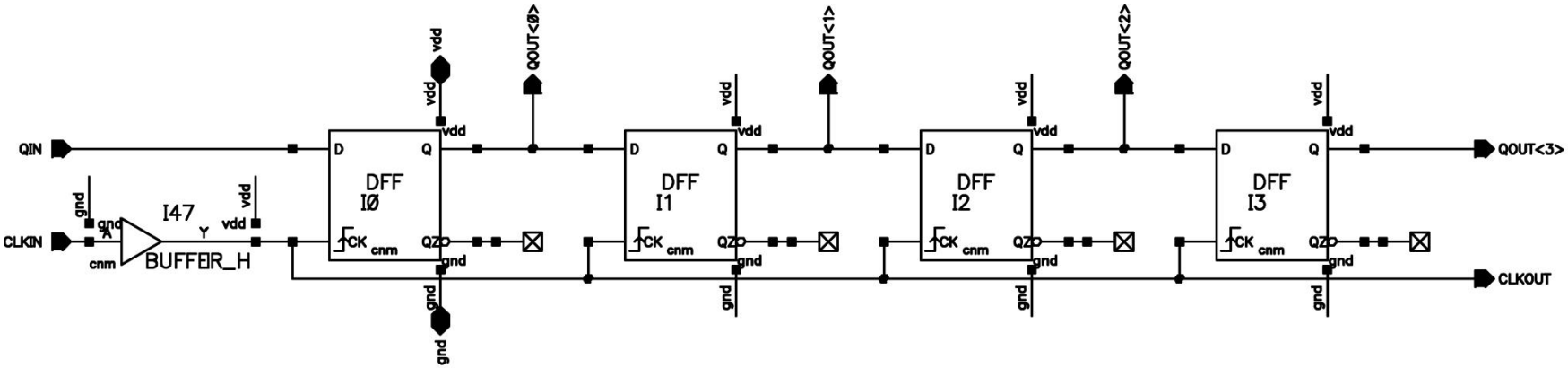

16×1
DAC channels
Metal and polySi
dummy filling
16×1
DAC channels
32×32 pixel
core array
16×1
DAC channels
IUT
flip-chip
Align marks
(50μm×50μm)
16×1
DAC channels
Dummy
bump pads

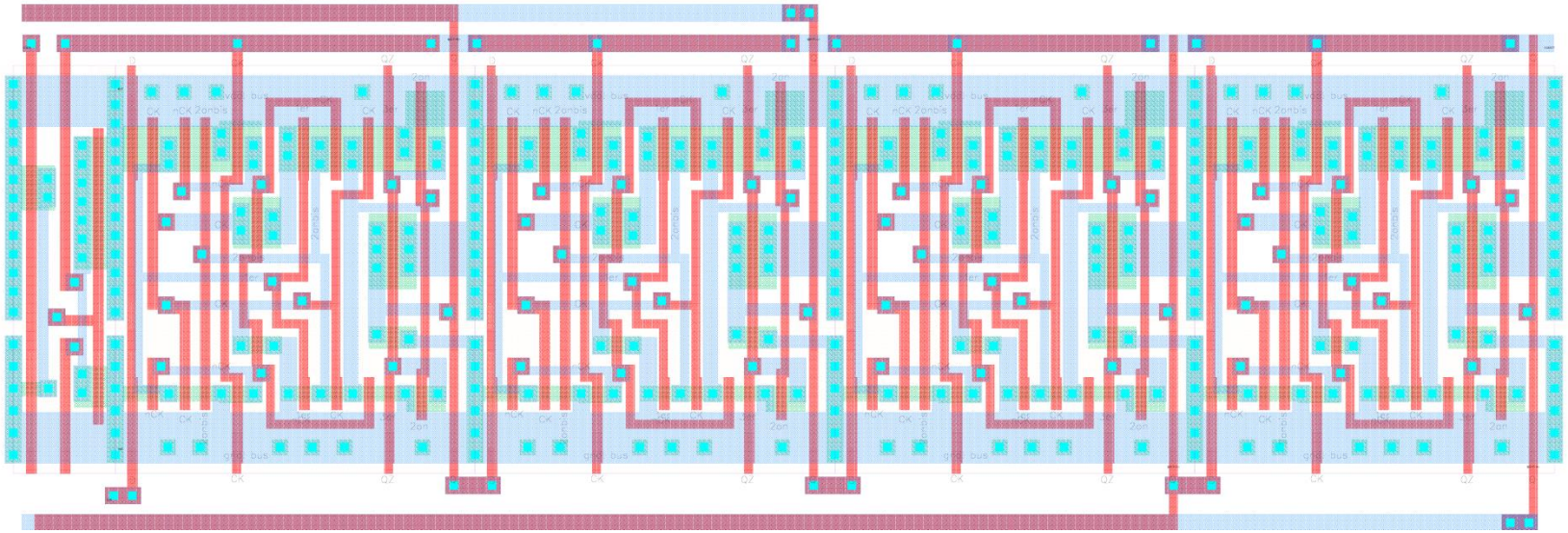

vdd5 vddp vdd2 vddp qin0 n/c roicio<4> roicio<3> roicio<2> roicio<1> roicio<0> ifs roicio<39> roicio<38> roicio<37> roicio<36> roicio<35> n/c ckin0 gnd gnd gnd gnd
gnd gnd gnd gnd qin2 n/c roicio<5> roicio<6> roicio<7> roicio<8> roicio<9> n/c roicio<10> roicio<11> roicio<12> roicio<13> roicio<14> n/c ckin2 vddp vdd2 vddp vdd5
vdd5 vddp vdd2 vddp ckin3 n/c roicio<34> roicio<33> roicio<32> roicio<31> roicio<30> n/c roicio<29> roicio<28> roicio<27> roicio<26> roicio<25> n/c qin3 gnd gnd gnd gnd
0 Columns 31
0
Rows
31
gnd gnd gnd gnd ckin1 n/c roicio<25> roicio<26> roicio<27> roicio<28> roicio<29> idark roicio<30> roicio<31> roicio<32> roicio<33> roicio<34> n/c qin1 vddp vdd2 vddp vdd5

ITP Configuration Chronogram

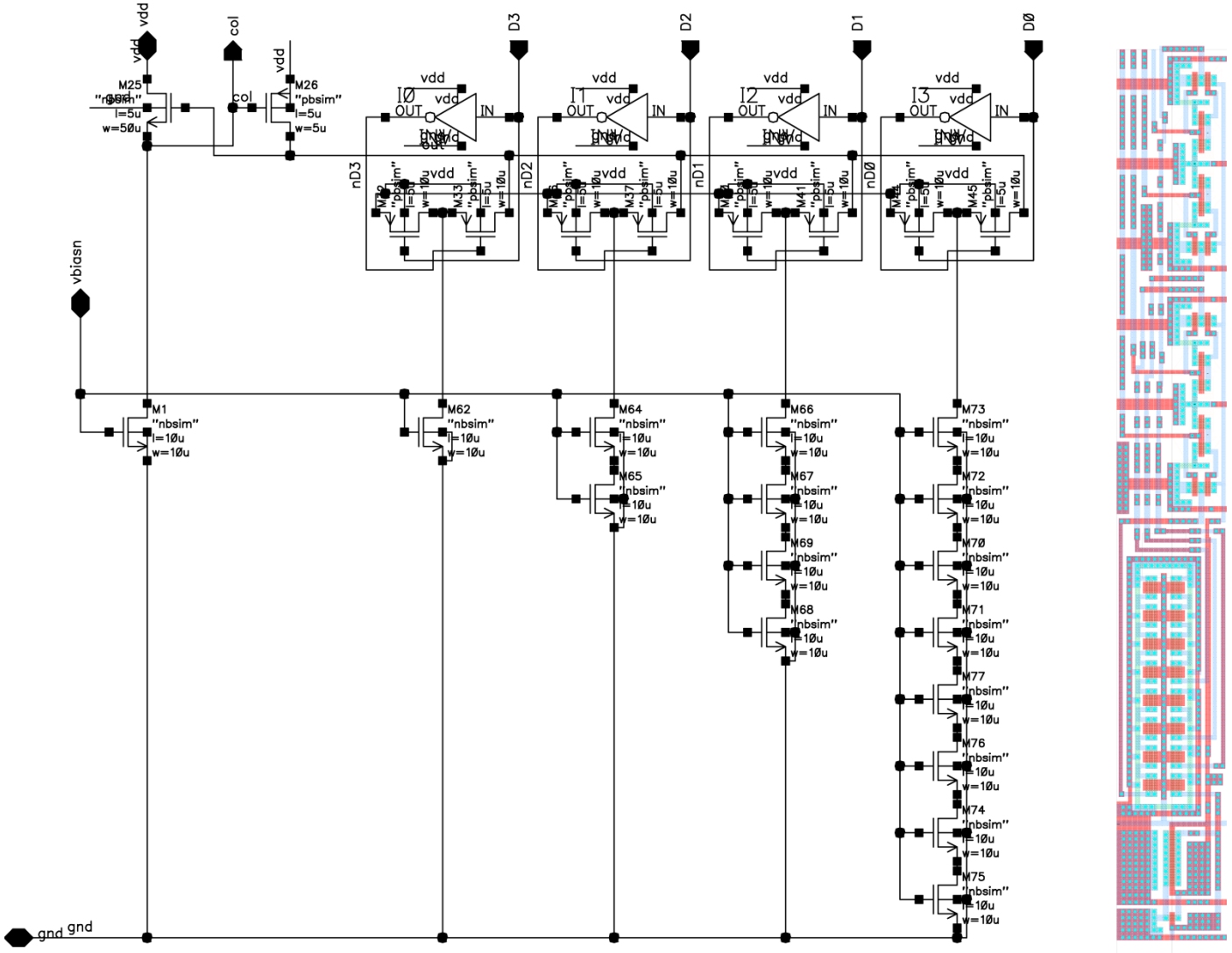
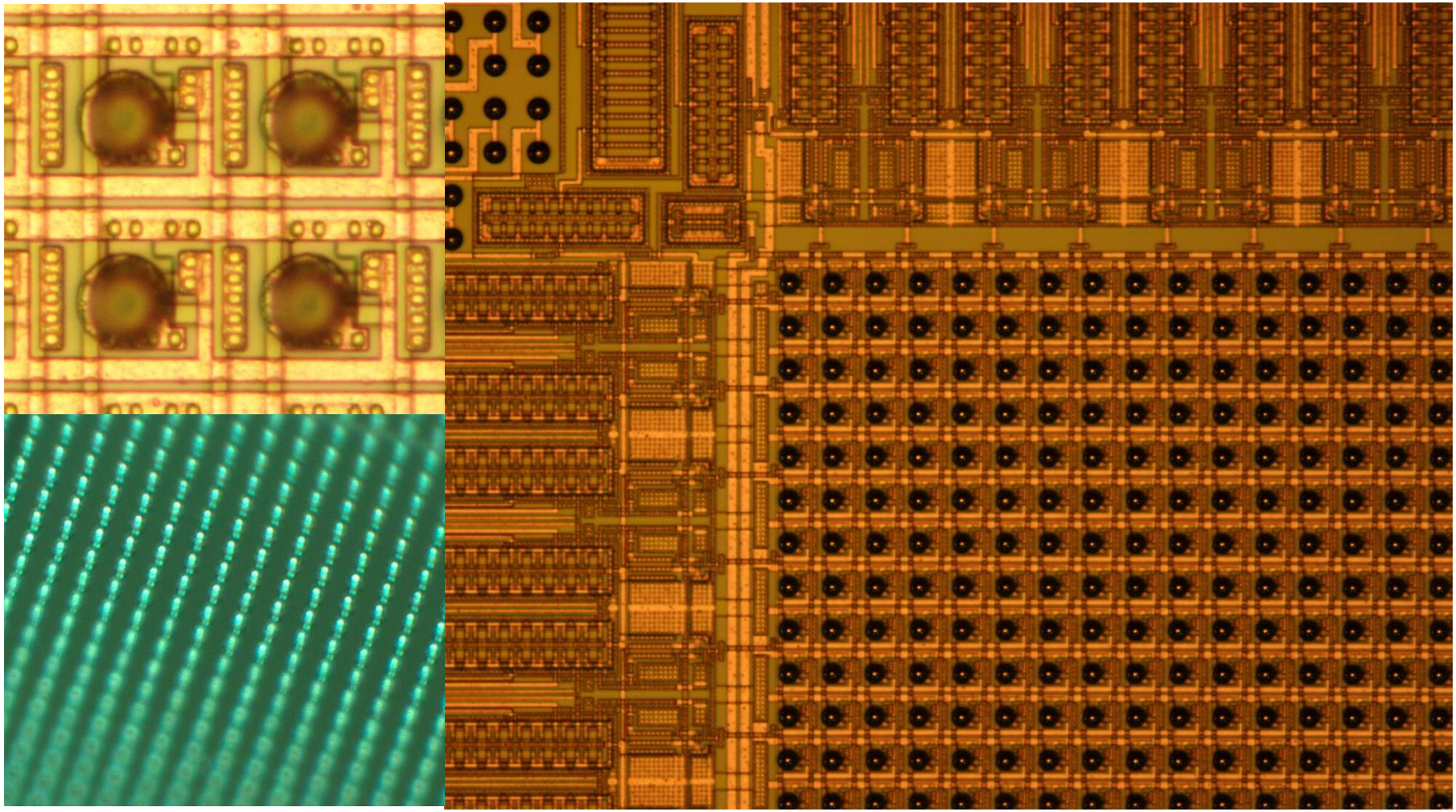


ITP Digital Control





ITP D/A Converter



ITP-IUT Bump Bonding (In, SnPb)