Compact and Low-Power All-MOS Voltage References with Thermal Compensation

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Conference on Design of Circuits and Integrated Systems

Introduction:

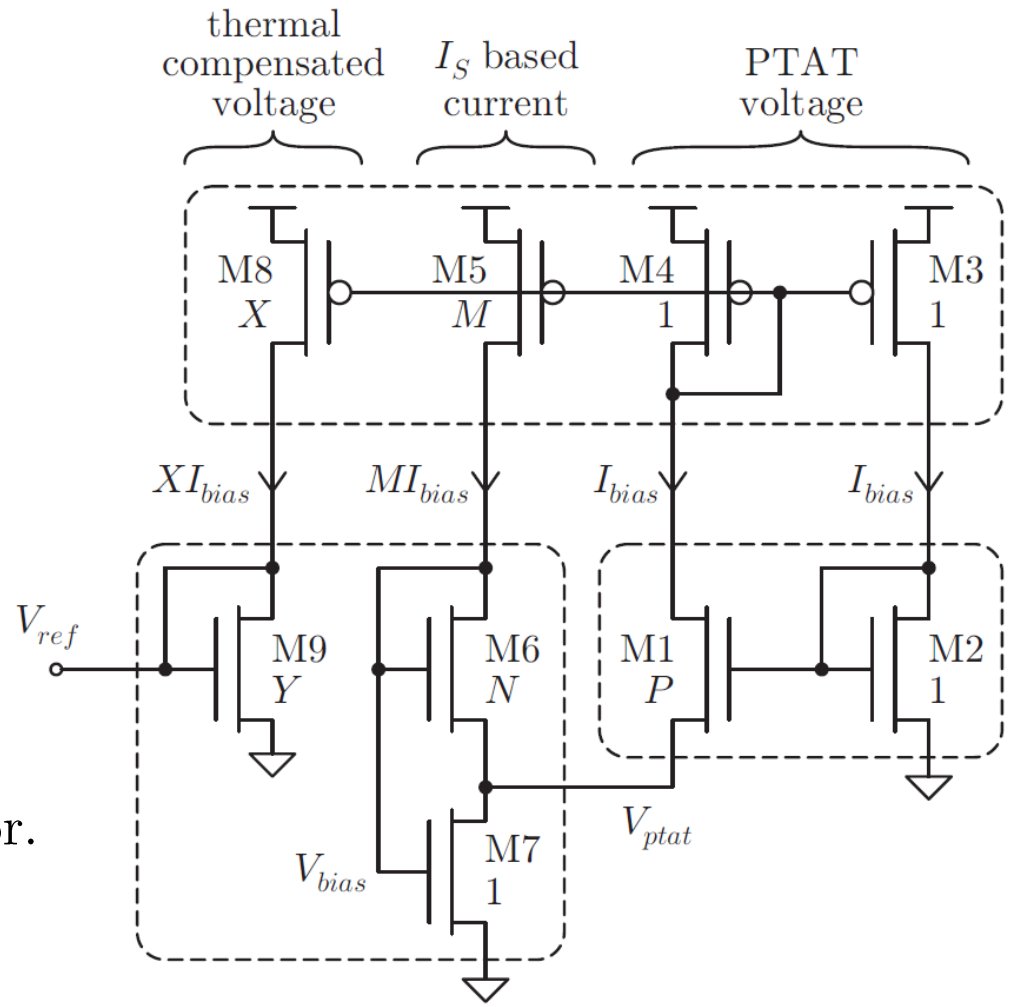
- Current and voltage references are essential components of analog and mixed-signal circuits for biasing, tuning or trimming.

- Common requirements for voltage reference generator circuits:
  - Low-power and area.
  - Low-voltage operation.
  - Compatibility with standard CMOS technologies.
  - Independent of PVT variations.

- State of the art: designs based on complex circuits or on the use of parasitic BJT, diodes, resistors or multi-threshold process options.

Circuit Proposal:

- Specifications:
  - All-MOS.
  - Low-power and area.
  - Low-voltage operation.
  - Thermally compensated.
- Three cascaded sections:
  - PTAT voltage core.
  - Specific current generator.
  - Thermally compensated output voltage reference.



Circuit Operation:

- **M1-M2**: weak inversion saturation;

  M3-M4 current mirror:

$$I_{D1} \equiv I_{D2} \quad \rightarrow \quad V_{ptat} = U_t lnP$$

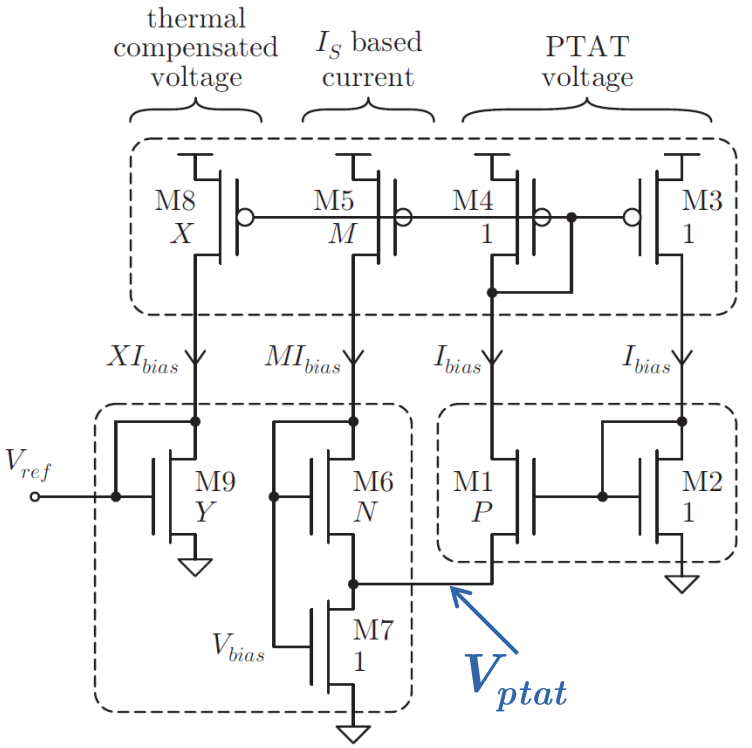
- **M5**: current mirror M scaled;
- N ratio between:

  M6 (strong inversion saturation)

  and **M7** (strong inversion conduction)

$$\begin{cases} MI_{bias} = \dfrac{N\beta_7}{2n}\left(V_{bias} - V_{T0} - nV_{ptat}\right)^2 \\ (M+1)I_{bias} = \beta_7\left(V_{bias} - V_{T0} - \dfrac{n}{2}V_{ptat}\right)V_{ptat} \end{cases}$$

$$I_{bias} \doteq QI_{S7} \qquad Q = \left[\frac{lnP}{2(M+1)}\left(\sqrt{\frac{M}{N}} + \sqrt{\frac{M}{N} + M + 1}\right)\right]^2$$



weak inversion saturation:

$$I_D = I_S e^{\frac{V_{GB}-V_{T0}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad I_S = 2n\beta U_t^2$$

strong inversion saturation:

$$I_D = \frac{\beta}{2n}(V_{GB} - V_{T0} - nV_{SB})^2$$

strong inversion conduction:

$$I_D = \beta\left[V_{GB} - V_{T0} - \frac{n}{2}(V_{DB} - V_{SB})\right](V_{DB} - V_{SB})$$

Circuit Operation:

- **M8**: current mirror X scaled;
- Y ratio between **M9** and **M7;**
- **M9:** strong inversion saturation

$$V_{ref} = 2n\sqrt{\frac{QX}{Y}}U_t(T) + V_{T0}(T)$$

$$V_{T0}(T) = V_{T0}(T_0) - \alpha\left(\frac{T}{T_0} - 1\right)$$

Design constraint for thermal compensation:

$$\sqrt{\frac{QX}{Y}} = \frac{1}{2n}\frac{\alpha}{U_t(T_0)}$$

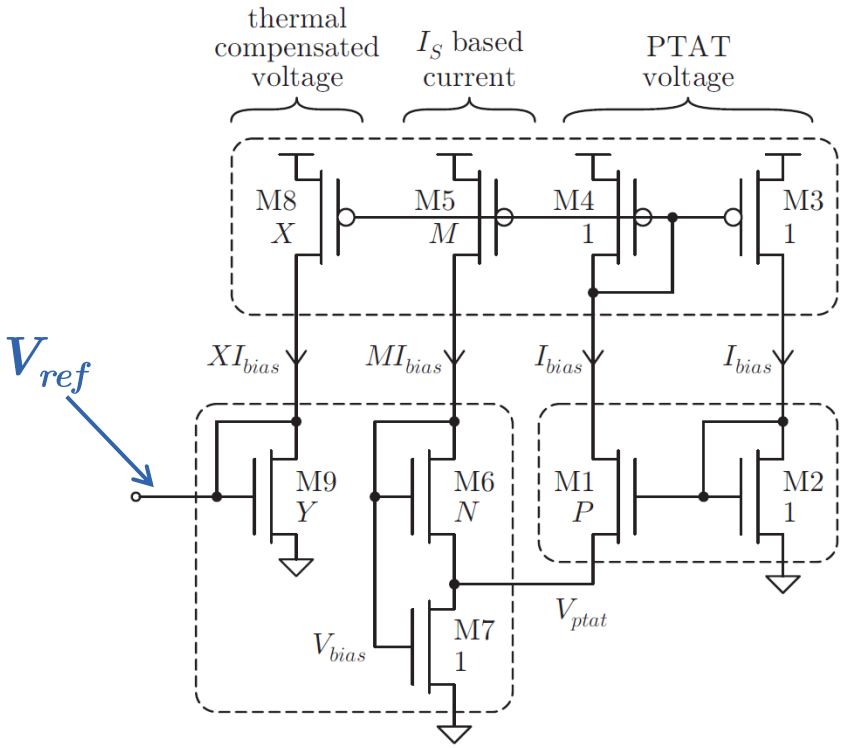
$$V_{ref} \equiv \alpha + V_{T0}(T_0)$$

Design parameters restrictions:

P>>1 for M1-M2 matching.

QM>>N for M6-M7 operating in strong inversion

QX>>Y for M9 operating in strong inversion



weak inversion saturation:

$$I_D = I_S e^{\frac{V_{GB}-V_{T0}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad I_S = 2n\beta U_t^2$$

strong inversion saturation:

$$I_D = \frac{\beta}{2n}(V_{GB} - V_{T0} - nV_{SB})^2$$

strong inversion conduction:

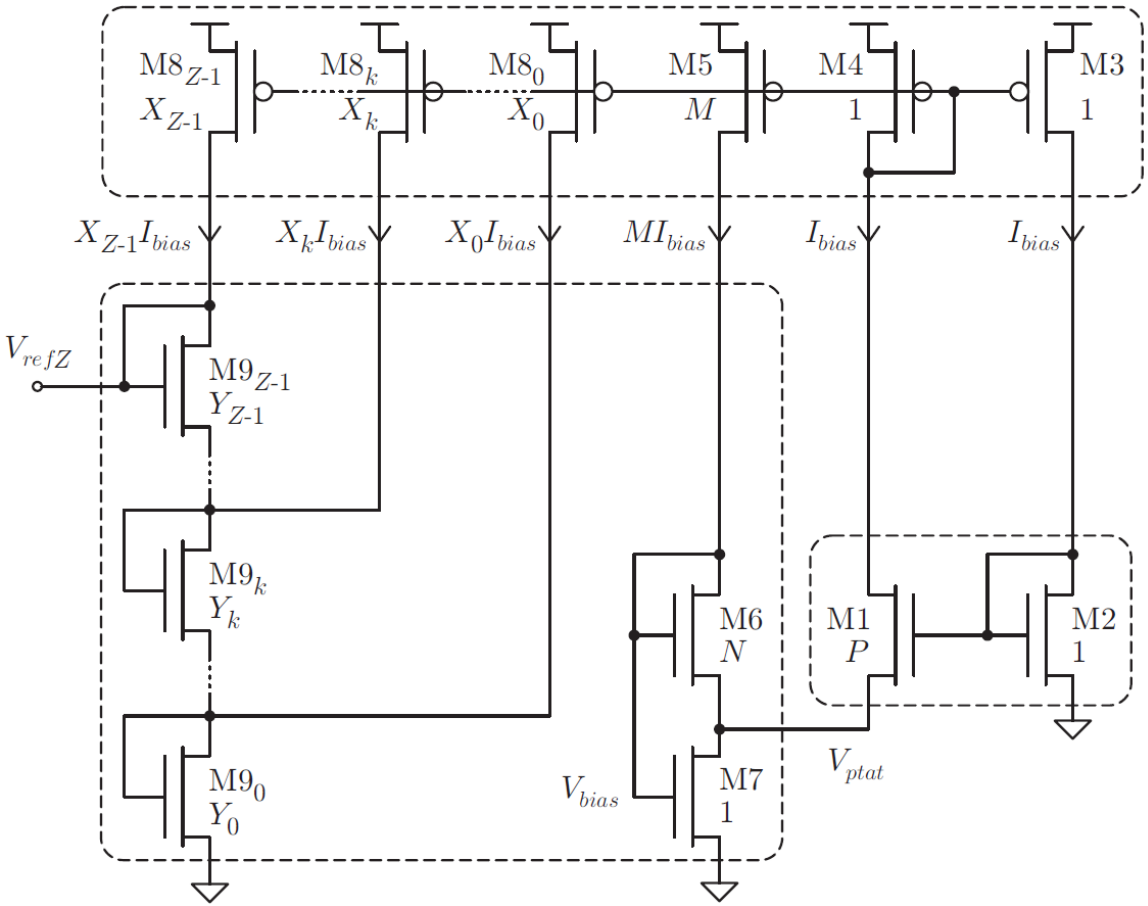
$$I_D = \beta\left[V_{GB} - V_{T0} - \frac{n}{2}(V_{DB} - V_{SB})\right](V_{DB} - V_{SB})$$

Generalization for high voltage references:

$$\sum_{k=0}^{Z-1} n^k \sqrt{\frac{Q}{Y_k}\sum_{i=k}^{Z-1} X_i} = \frac{1}{2n}\frac{\alpha}{U_t(T_0)}\sum_{k=0}^{Z-1} n^k$$

$$V_{refZ} = V_{ref}\sum_{k=0}^{Z-1} n^k = V_{ref}\frac{n^Z - 1}{n-1}$$

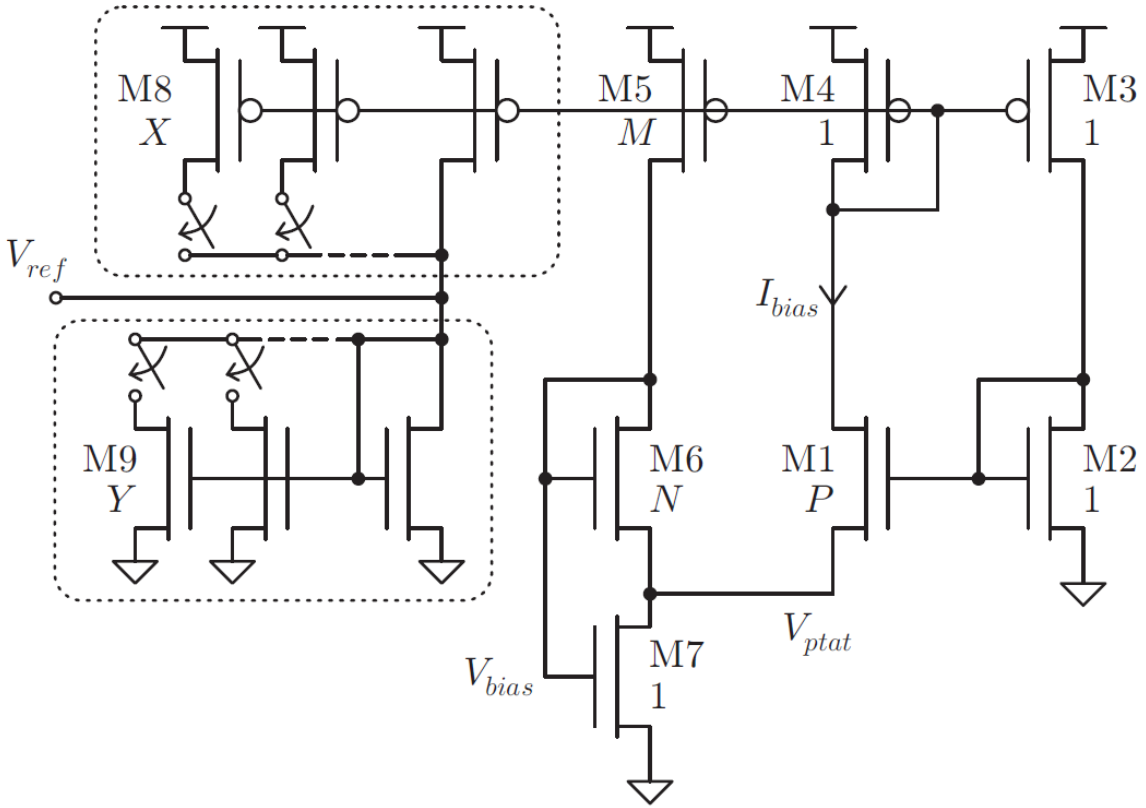
$$1 < n < 2$$



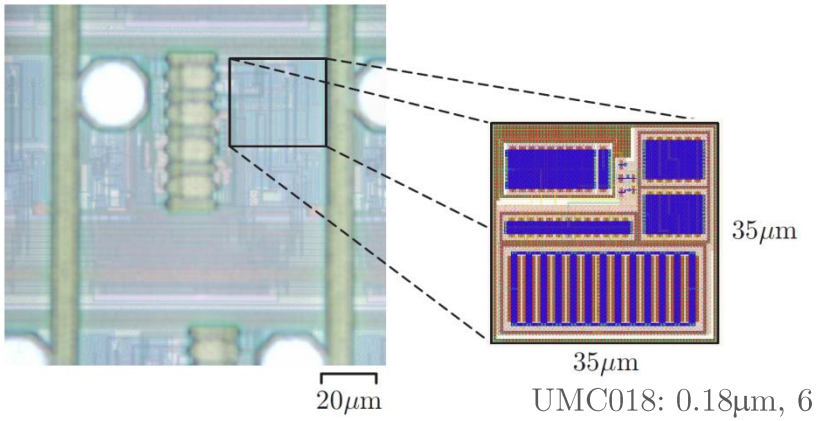
Digital trimming:

- Process deviations compensation:

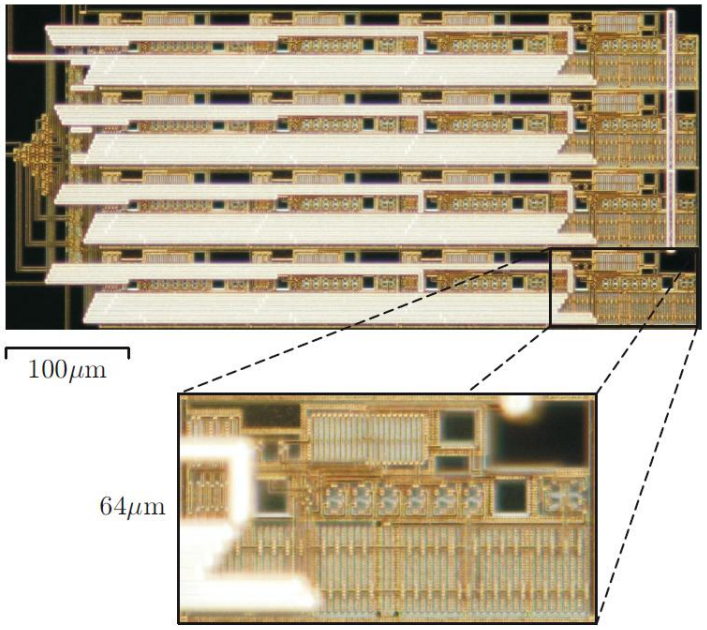
$$\sqrt{\frac{QX}{Y}} = \frac{1}{2n}\frac{\alpha}{U_t(T_0)}$$



Circuit integration:



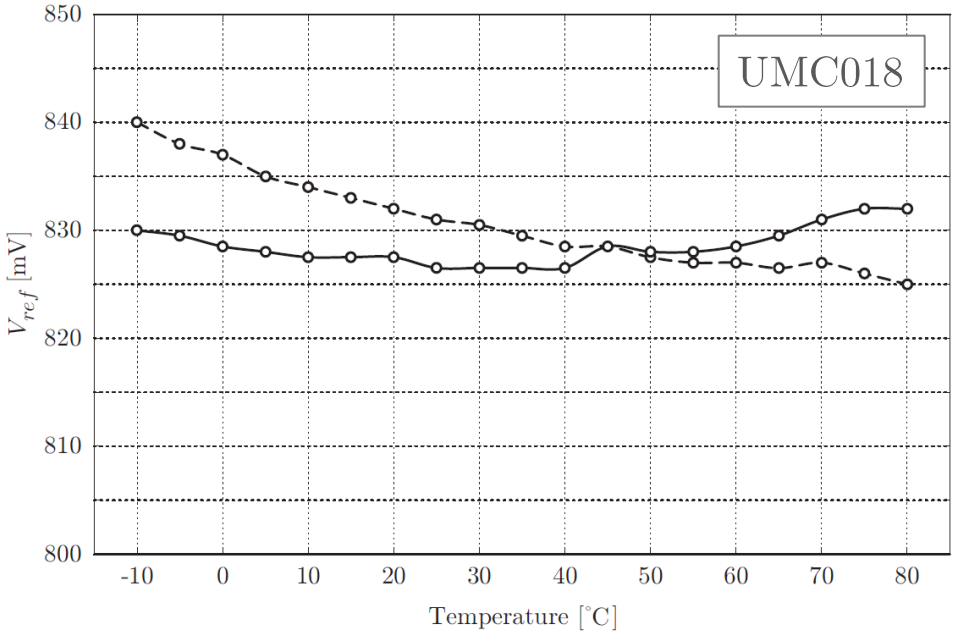
UMC018: 0.18μm, 6 metals.



AMS035: 0.35μm, 4 metals.

Parameter	UMC	AMS	units
Technology	0.18	0.35	μm
$V_{TO}(27^{\circ}\mathrm{C})$	600	525	mV
α	225	330	mV
n	1.12	1.28	
$I_S(27^{\circ}\mathrm{C})$	390	220	(W/L)nA
P	10	24	
M	1	3	
N	1/2	1	
$(W/L)_7$	1/6	3/3	μm/μm
$V_{ptat}(27^{\circ}\mathrm{C})$	58	80	mV
Q	3.86	3	
$I_{bias}(27^{\circ}\mathrm{C})$	250	660	nA
X	1	35/2	
Y	1/4	2	
V_{ref}	825	855	mV

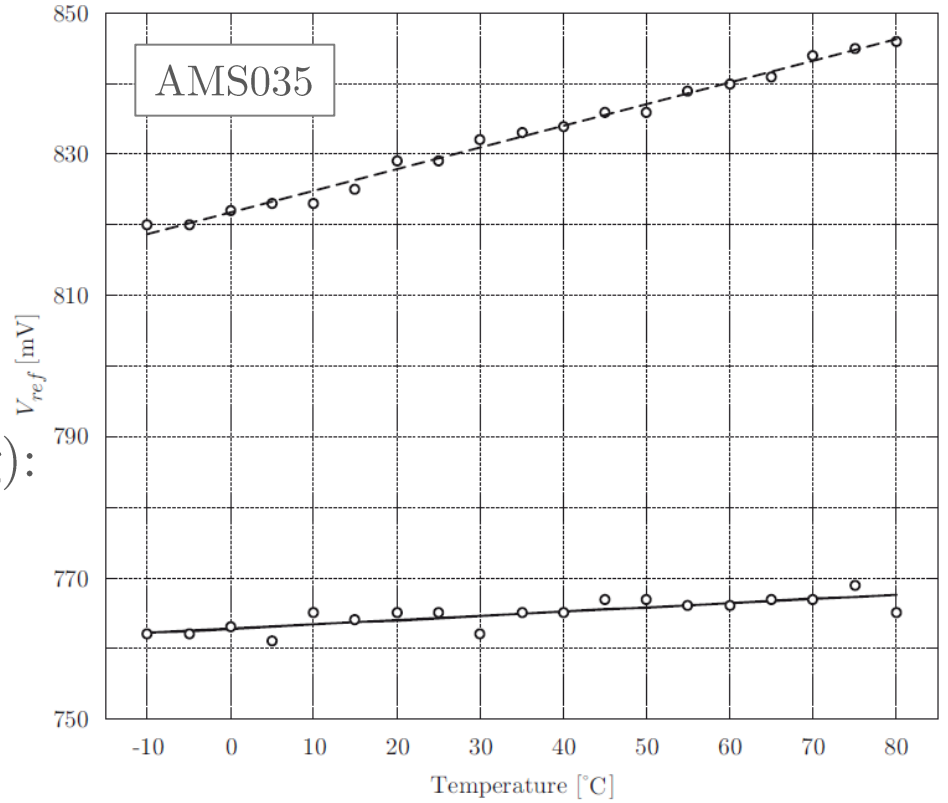
Results: power consumption and sensitivity



UMC018 design:

power consumption: $< 2\ \mu W$.

sensitivity: $< 120 ppm/^oC$



AMS035 design (with digital trimming):

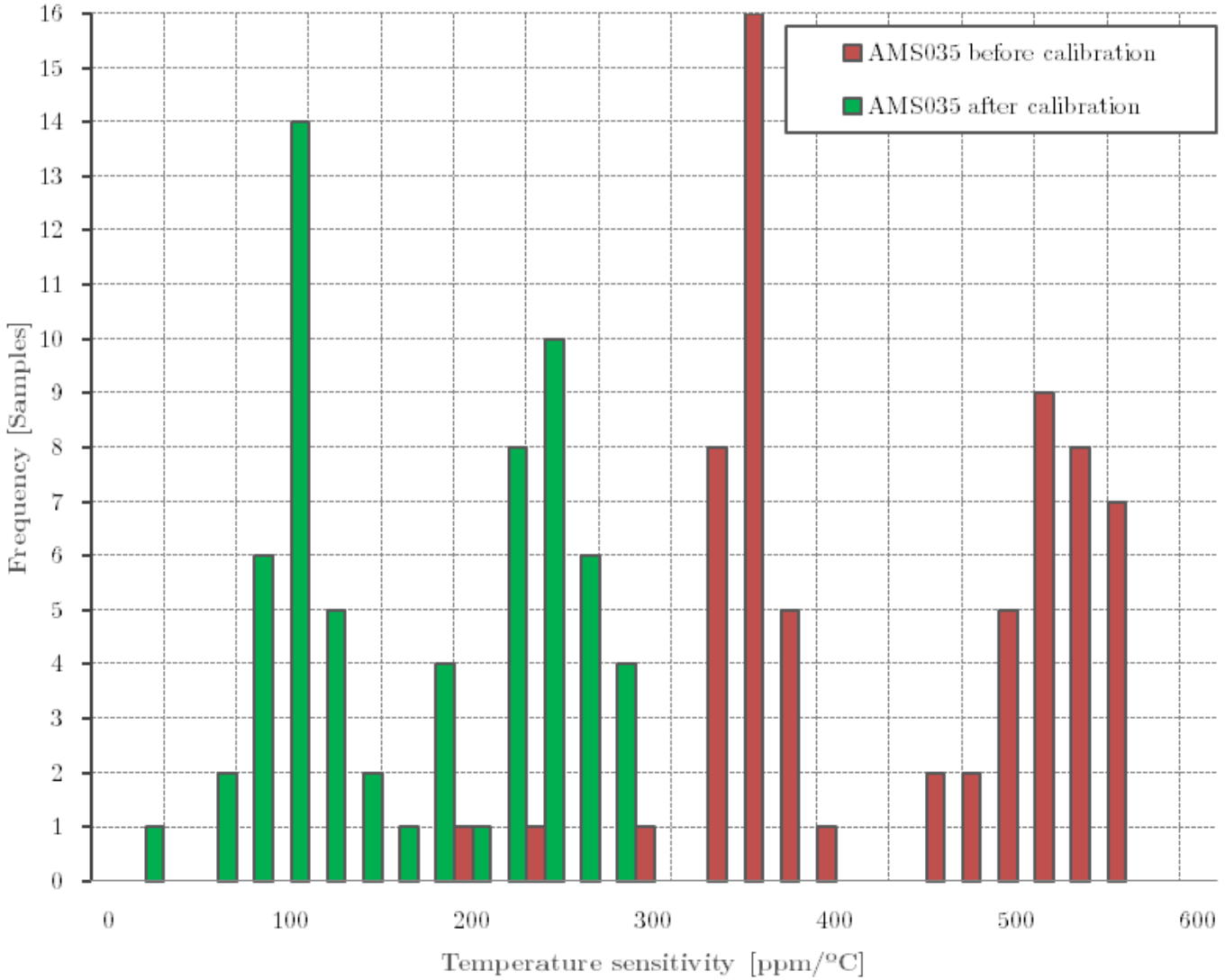
power consumption: $< 50\ \mu W$.

sensitivity:

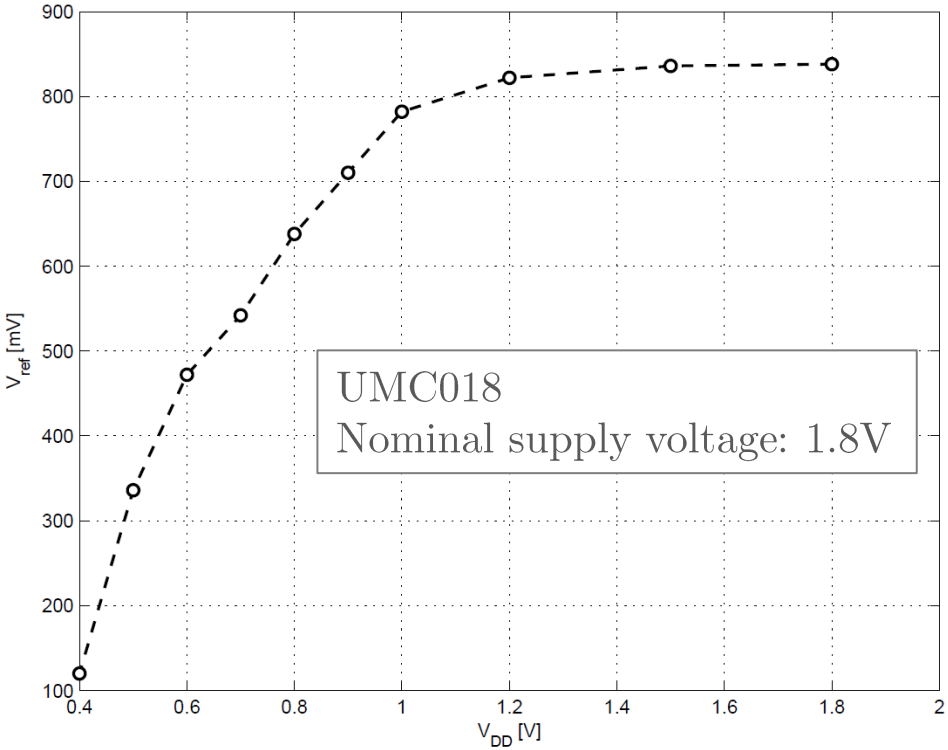
uncalibrated: 370 $ppm/^oC$

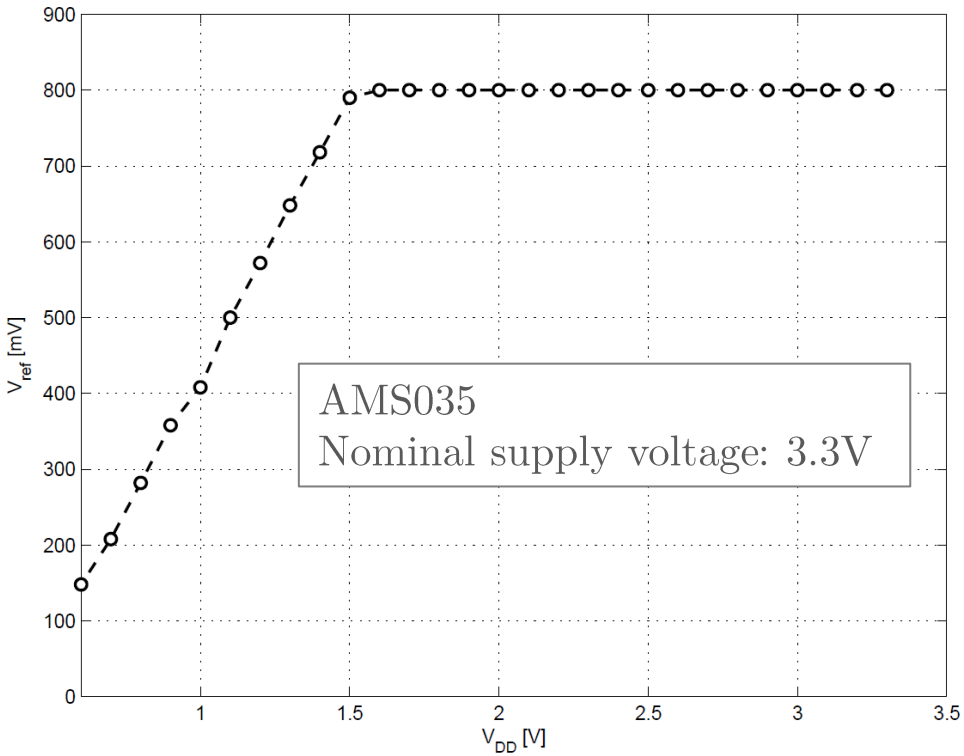
calibrated: 80 $ppm/^oC$

Results: trimming calibration

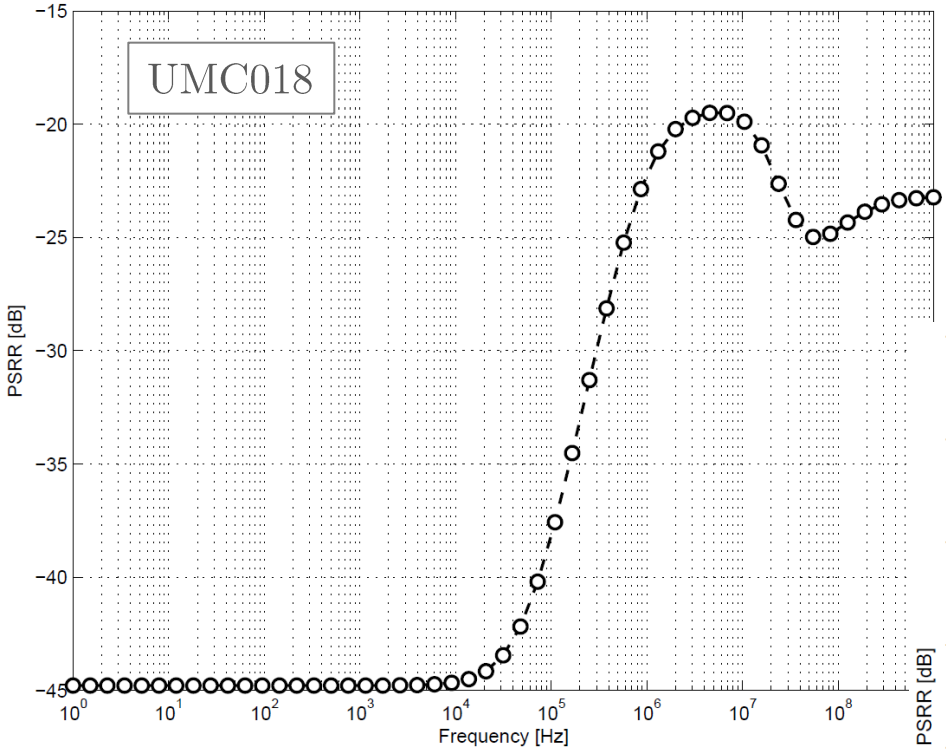


Results: low voltage operation

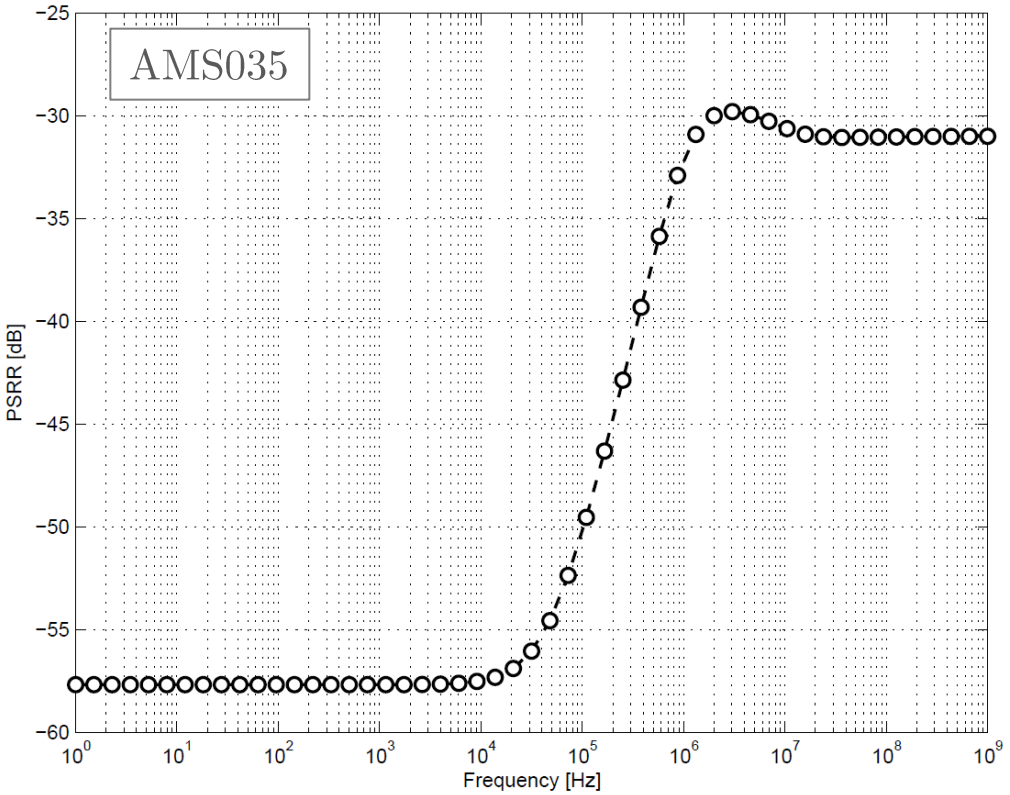




Results: PSRR



UMC018 design:
PSRR (100Hz) = 44.8 dB
PSRR (10MHz) = 19.9 dB



AMS035 design:
PSRR (100Hz) = 57.7 dB
PSRR (10MHz) = 30.6 dB

Results:

Parameter		Value		Units
		UMC	AMS	
Technology		0.18	0.35	µm
Supply voltage		1.8	3.3	V
V_{ref}		825 (±10%)	855 (±10%)	mV
I_{bias}		250 (±10%)	660 (±10%)	nA
Power consumption		<2	<50	µW
Temperature sensitivity		100	100	ppm/ºC
Silicon area		0.0004	0.006	mm^2
Low voltage operation		1	1.4	V
PSRR	100Hz	45	58	dB
	10MHz	20	30	

Conclusions:

Voltage reference circuit:

- All-MOS.
- Low-area and simplicity.
- Low-power consumption.
- Low-voltage operation.
- Thermal compensation.

Generalization for high voltage references.

Digital trimming to improve accuracy avoiding PVT variations.

Integration in two different CMOS technologies to proof the validity of the proposed design techniques.

Experimental results showing good performance.

Questions?