A Self-Biased PLL-Tuned AER Pixel for High-Speed Infrared Imagers

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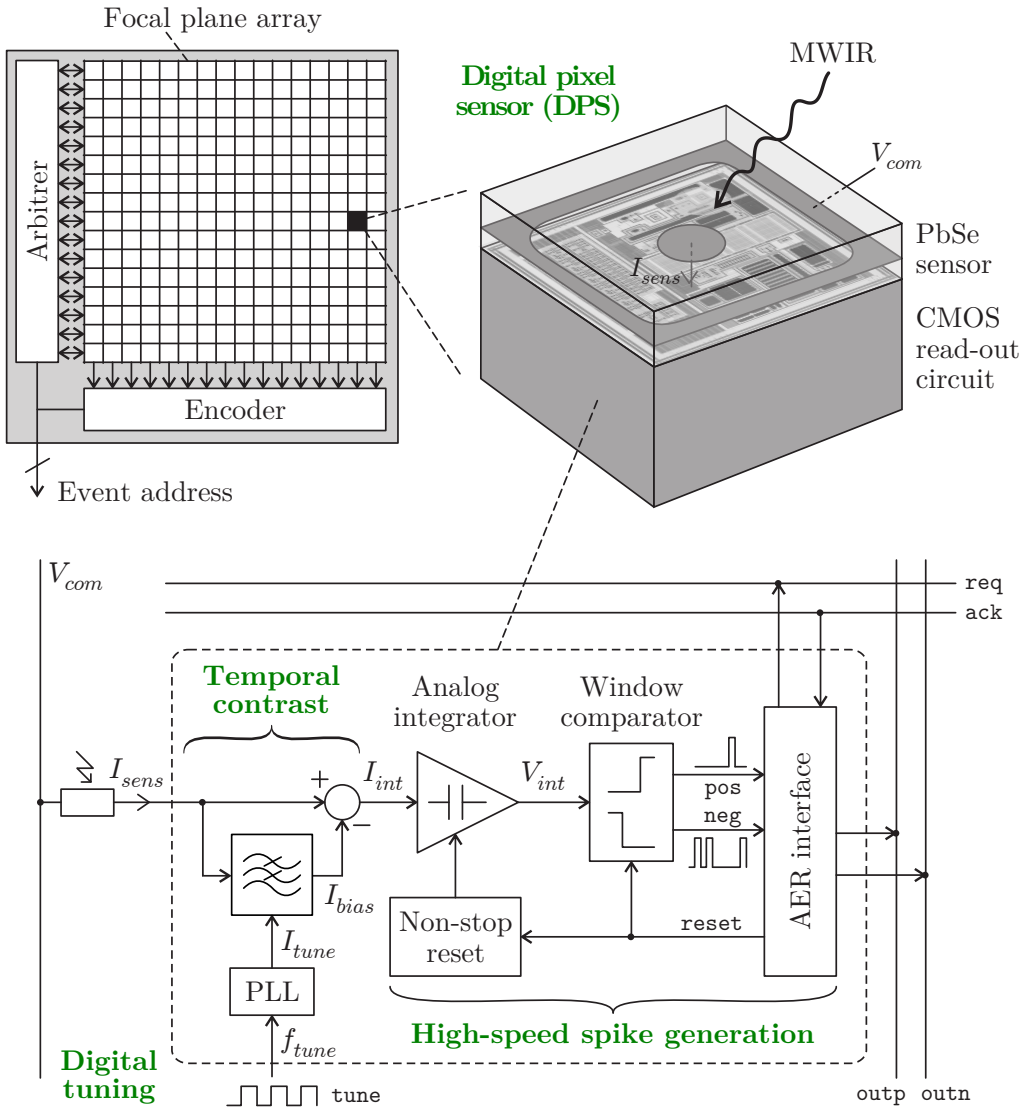
DPS Introduction

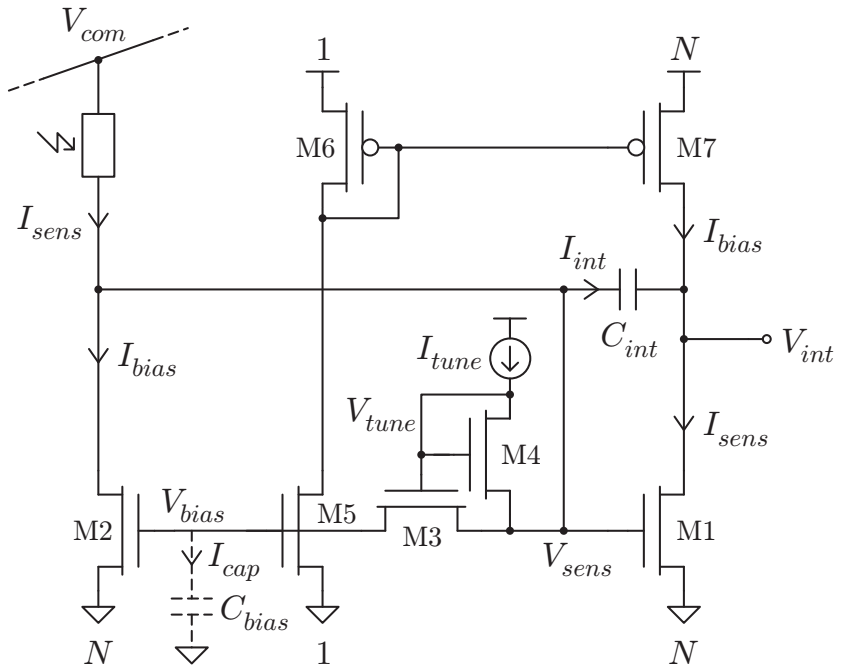
- **Uncooled MWIR** PbSe VPD technology
- **High-speed** (>1Kfps) vision for automotive, process control...

- **Compact** and **low-power** CMOS circuits
- **High dark-to-signal** current ratios
- **Tunable** temporal contrast to match applications
- High-speed spiking **insensitive** to AER delay



Log-Domain Temporal Contrast

- **Dark current** cancellation
- Emphasis on **high-freq.** contents
- **Self-biasing** capability



- I-domain **low-pass** linear ODE

$$\frac{dI_{bias}}{dt} = 2\pi f_c \left(I_{sens} - I_{bias}\right)$$

- **Subthreshold** companding (M1-M2)

$$I_D = \underbrace{2n\beta U_t^2}_{I_S} e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}}$$

- V-domain **non-linear** ODE (M3-M4)

$$\underbrace{C_{bias}\frac{dV_{bias}}{dt}}_{I_{cap}} = \underbrace{2\pi f_c n U_t C_{bias}}_{I_{tune}} \left(e^{\frac{V_{sens}-V_{bias}}{nU_t}} - 1\right)$$

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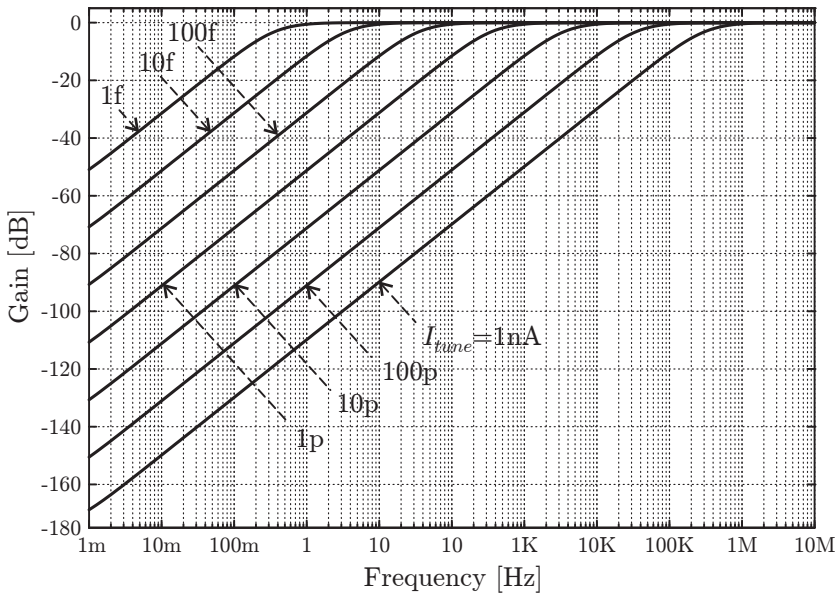
- Corner frequency **tuning**

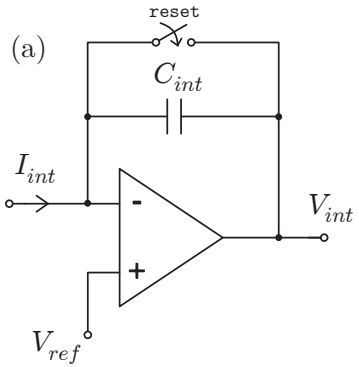


- I_{tune} **programmability**?

Reset-Insensitive High-Speed AER

- **CTIA**-based integration for high-speed imaging ($C_{int} \downarrow$)
- Spiking frequency non-linearity at high-rate due to **AER delay**:

$$f'_{req} = \frac{f_{req}}{1 + t_{res} f_{req}} \qquad f_{req} = \frac{|I_{int}|}{C_{int}\, V_{th}}$$



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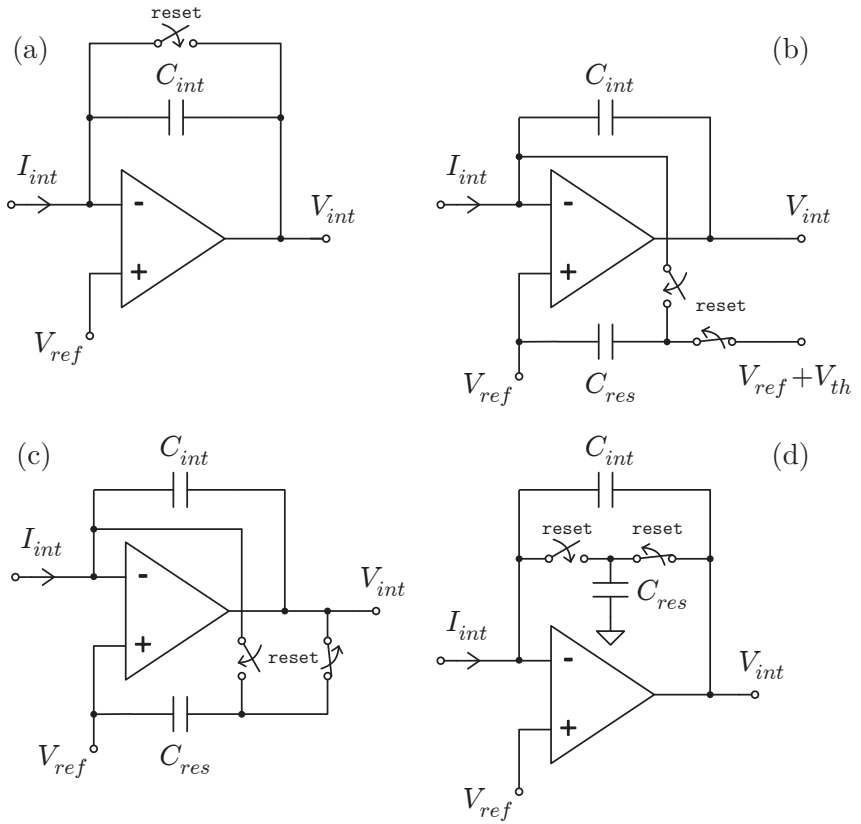
- Novel **reset-insensitive** schemes based on **charge injection**:
  - Inherent **CDS**?
  - **Extra** capacitors?
  - **Low-impedance** sources?



	Dead time	CDS	Voltage sources	Cap area
(a)	×	×	✓	✓
(b)	✓	×	××	×
(c)	✓	✓	×	×
(d)	✓	✓	✓	×

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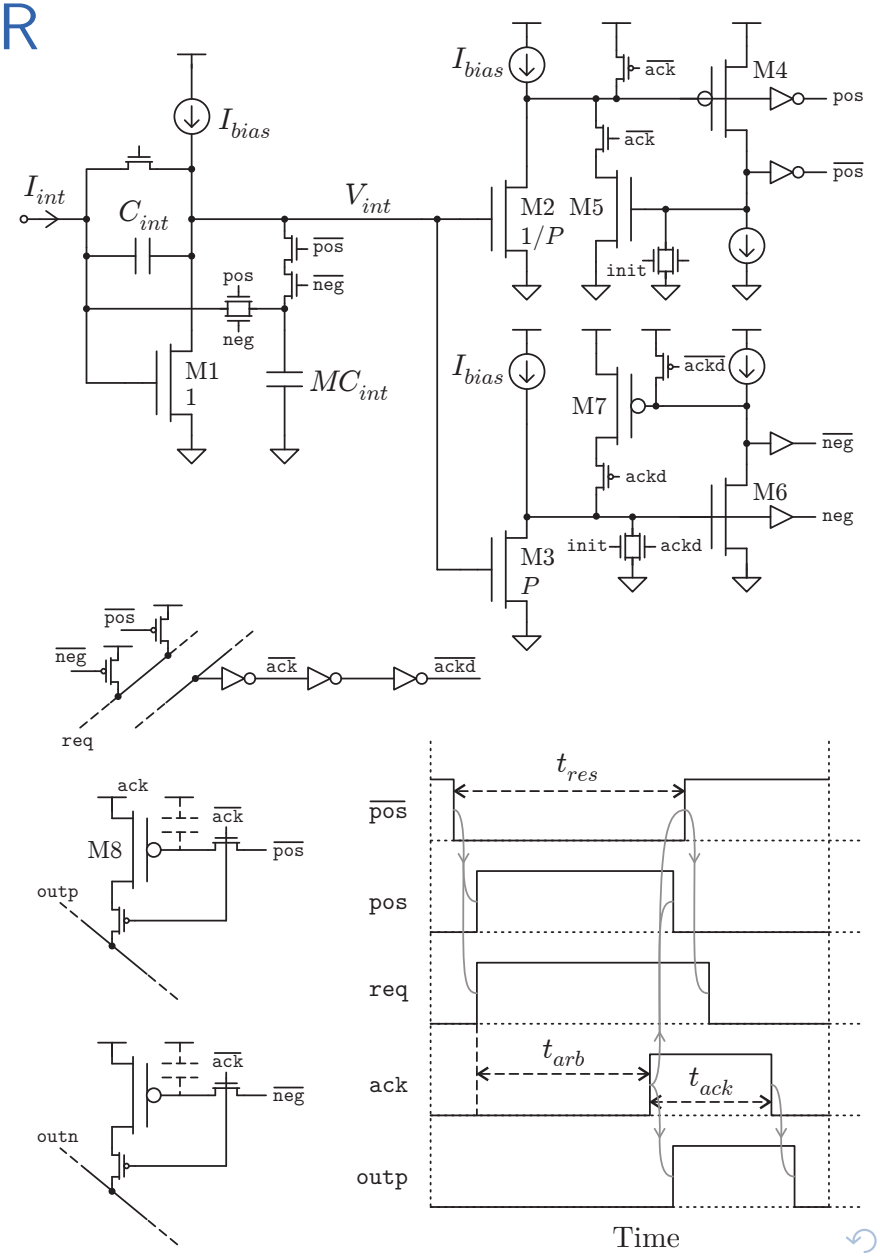
- Novel **reset-insensitive** schemes based on **charge injection** with inherent **CDS**
- **Compact** and **low-power** CMOS circuit realization

$$V_{th} = \pm n U_t M \ln(P)$$



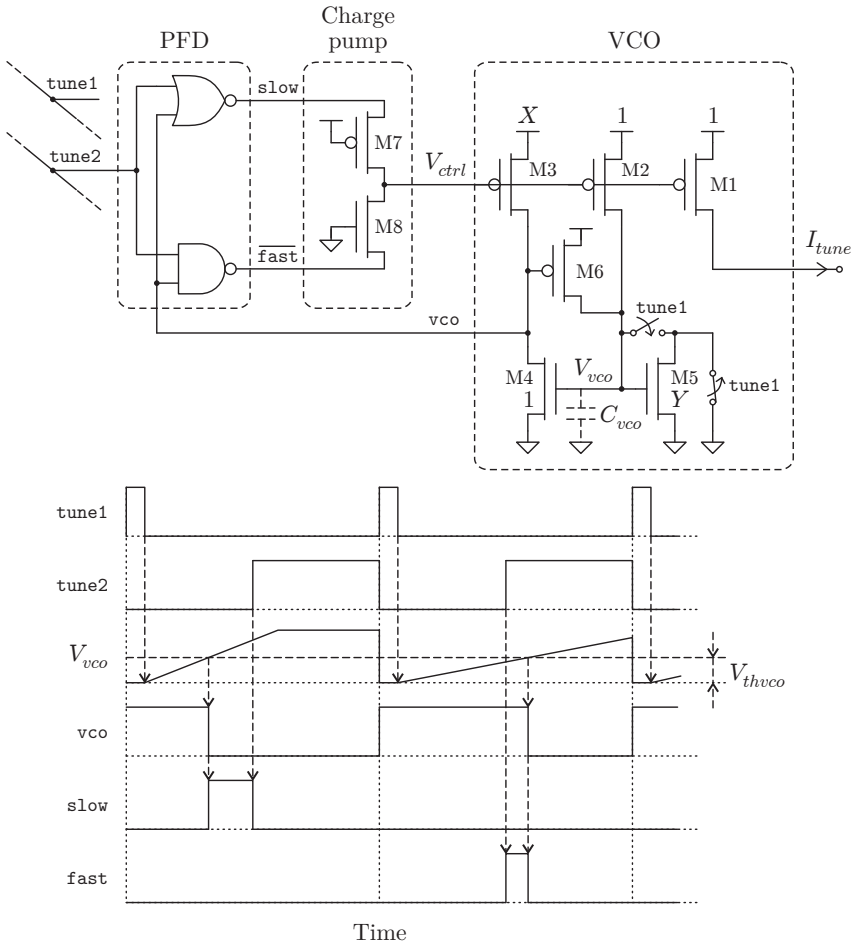
PLL-Based Tuning

- Temporal contrast f_c
- **Weak integrity** pA-range I_{tune}
- **Digital frequency** tuning based on in-pixel **PLL**:

$$f_{tune} = \frac{I_{tune}}{2\,V_{thvco}\,C_{vco}}$$

$$V_{thvco} = nU_t \ln\left(\frac{1+Y}{1+1/X}\right)$$

- **Robust** KHz-range clocking
- **Process** and **thermal** compensation for I_{tune}
- **Dynamic** and adaptive contrast?

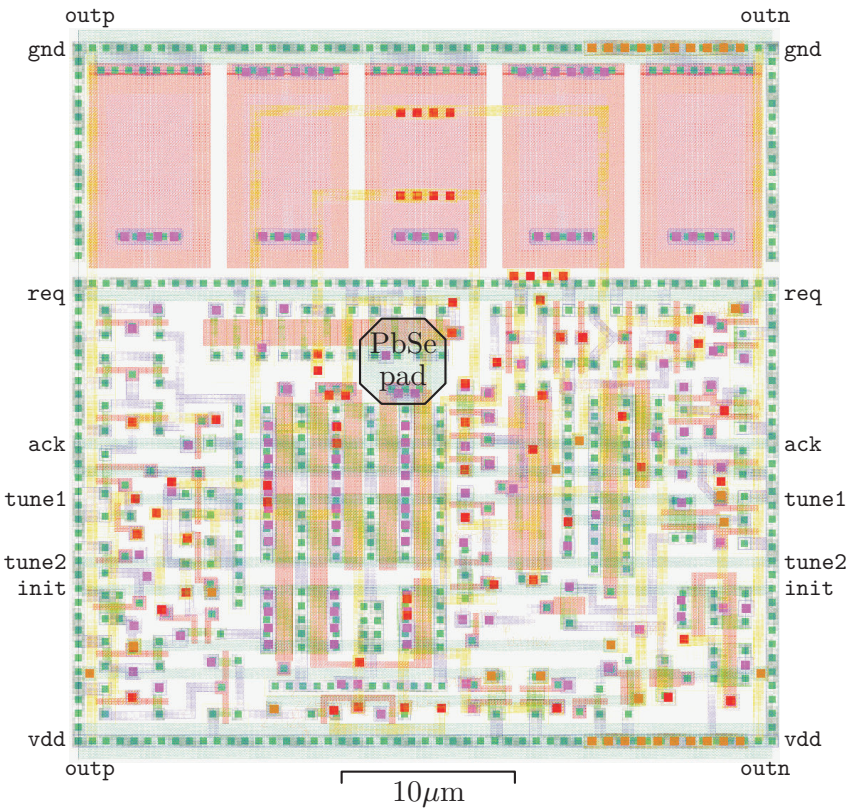


$$f_c = \frac{1}{\pi}\frac{C_{vco}}{C_{bias}} \ln\left(\frac{1+Y}{1+1/X}\right) f_{tune}$$

CMOS Design Example

- 0.35μm 2P4M CMOS technology
- Design parameters: $I_{dark} \simeq 1\mu$A, $N=4$, $C_{int}=80$fF, $M=3/2$, $P=4$, $X=1$, $Y=2$ and $C_{vco}/C_{bias}=15$

- 40μm-**pitch** DPS



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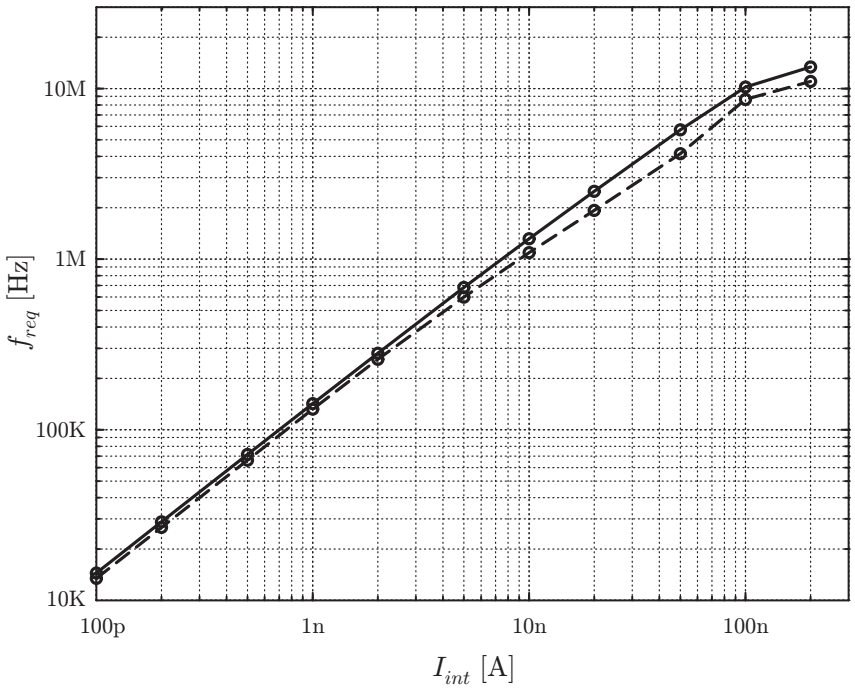
- Good 0.12MHz/nA **linearity** up to the spiking rate hard limit $\frac{1}{t_{arb}+t_{ack}} \simeq$27MHz



CMOS Design Example

- 0.35μm 2P4M CMOS technology
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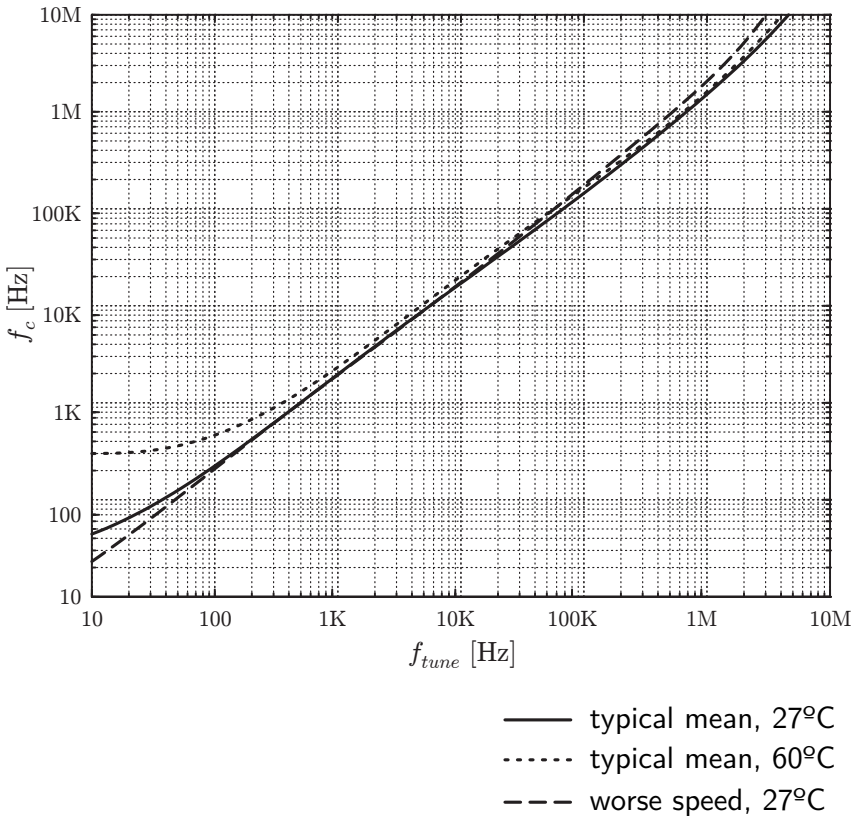
- 40μm-**pitch** DPS
- Good 0.12MHz/nA **linearity** up to the spiking rate hard limit $\frac{1}{t_{arb}+t_{ack}}\simeq$27MHz
- **Process** and **temperature** compensation for the temporal contrast f_c
- **Power** consumption $\propto 2I_{dark}$



Conclusions

- Novel DPS circuit for **uncooled MWIR PbSe** sensors
- **Log-domain** filtering for **temporal contrast** and **self-biasing**
- **AER insensitive** spike generation with inherent **CDS**
- **Digital PLL-based** temporal contrast tuning with **process** and **thermal** compensation
- A 40μm-pitch DPS **design example** in 0.35μm 2P4M CMOS technology

- Currently, a **128×128** imager is under development in **0.15μm** 1P6M CMOS technology...

Thanks for your attention!