A 55µm×55µm Charge-Integration Digital Pixel Sensor for Digital Direct Mammography in 0.18µm CMOS Technology

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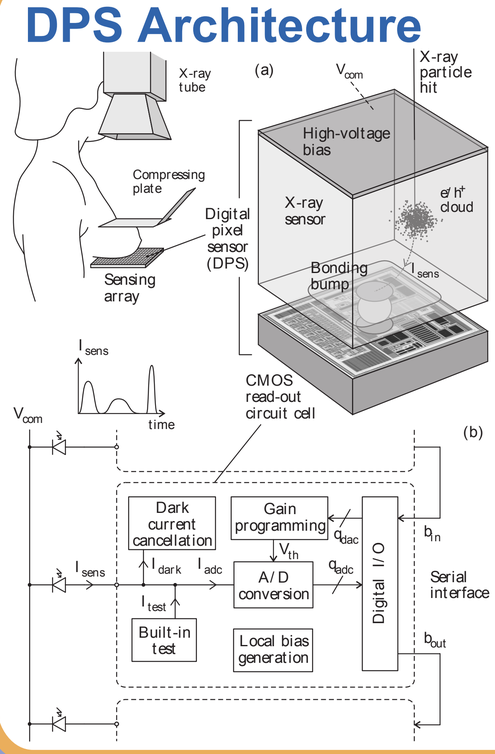
Motivation

Mammography has become a key tool for the diagnosis of breast cancer in women, and it is currently one of the recommended screening methods for its early detection, with practical pitch requirements in the range of 50µm to 100µm. In this sense, high resolution CMOS X-ray imagers based on photon counting digital pixel sensors (DPS) are reported in literature, which can meet the pitch requested by direct digital mammography applications. However, active pixels based on photon counting A/D conversion tend to suffer from signal losses due to pile-up and charge-sharing between neighboring pixels. This work presents a compact and low-power CMOS DPS circuit based on charge-integration for direct X-ray mammography applications, which has been integrated in 0.18µm 1P6M CMOS technology.

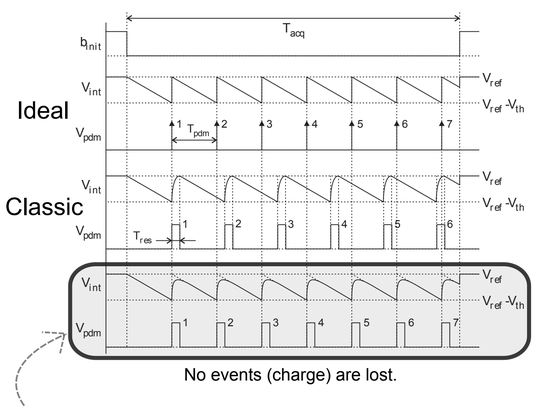
Pixel Key Features

- 12-bit charge-integration lossless A/D conversion.
- Local D/A converter to program individually the gain of each pixel for FPN supression.
- Selectable electrons/holes collection.
- Built-in test mechanism.
- Local analog reference and bias generation to avoid crosstalk.
- 100Mbps digital only I/O serial interface.
- Dark current self-calibration-cancellation.

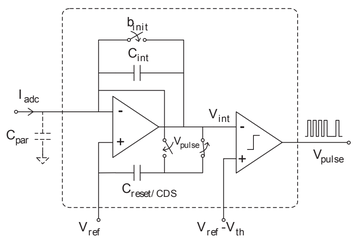
DPS Architecture

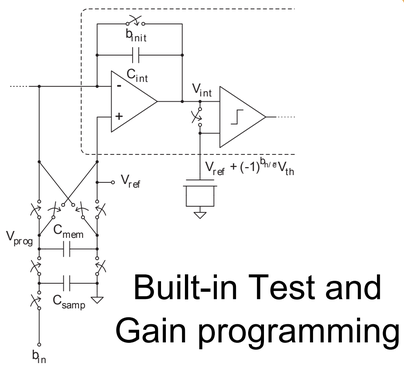


A/D Conversion

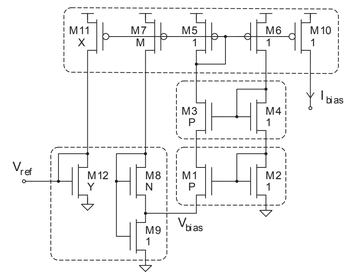


Lossless charge-integrator





Built-in Test and Gain programming

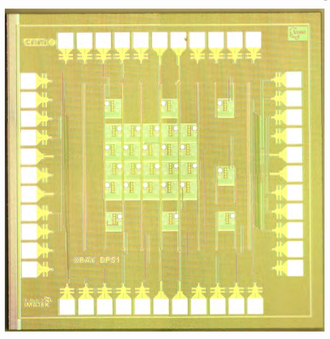


Temperature compensated local bias generation

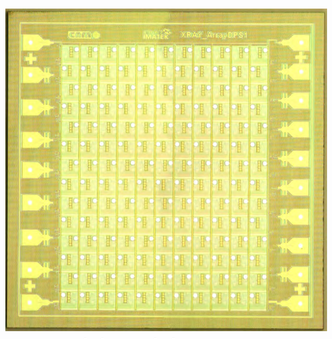
CMOS Integration: 3 DPS generations.

Die size 1.5mm × 1.5mm

100µm pitch

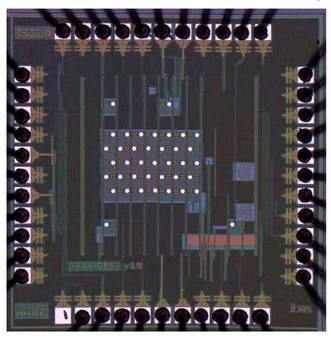


electrical test vehicle

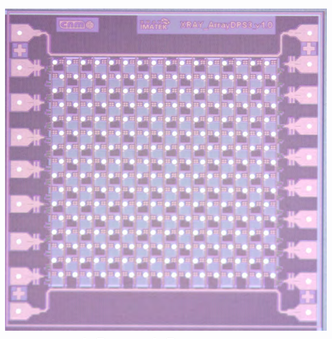


11 × 14 array
for x-ray experiments

70µm pitch

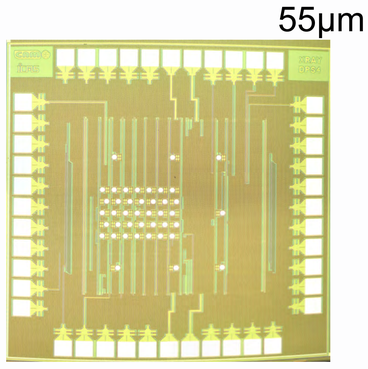


electrical test vehicle

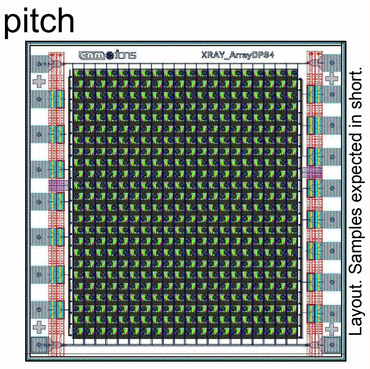


16 × 16 array
for x-ray experiments

55µm pitch



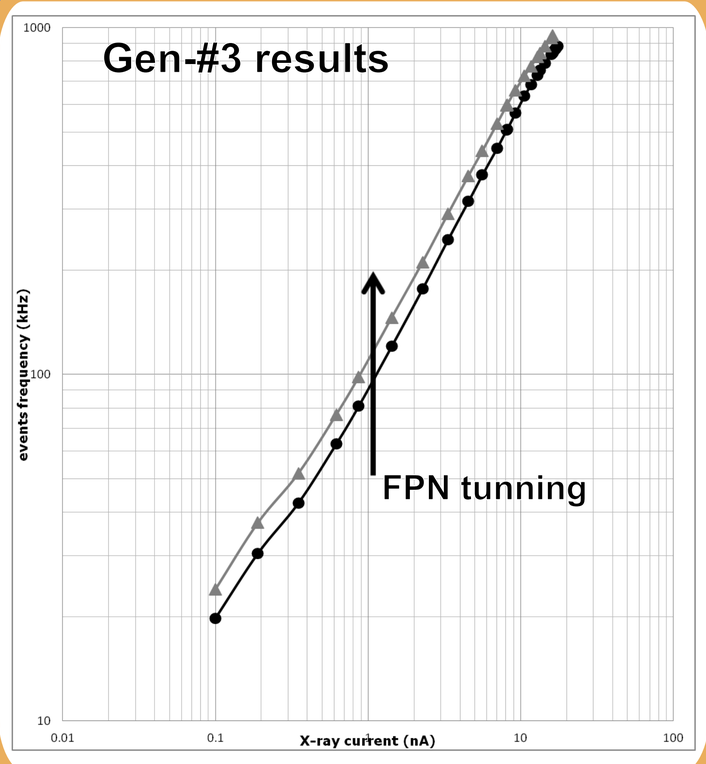
electrical test vehicle

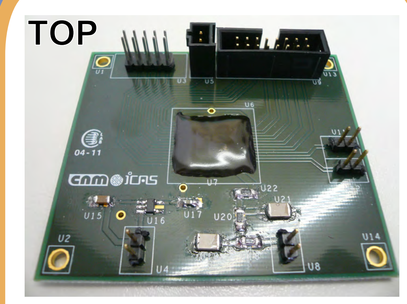


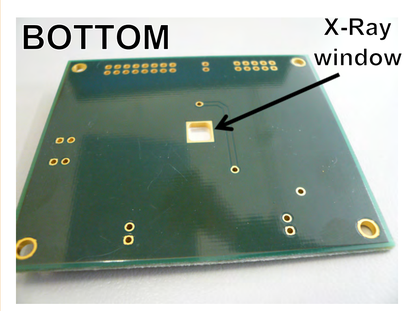
Layout. Samples expected in short.

20 × 24 array
for x-ray experiments

Parameter	Gen-#1	Gen-#2	Gen-#3
Supply Voltage	1.8 V	1.8 V	1.8 V
Reference Voltage	650 mV	815.21 mV	700±30 mV
Bias Current	270 nA	553.46 nA	300±50 nA
Dark Current Range	0.01 to 20 nA	0.01 to 20 nA	NA
Typical Transfer Gain	1/50 LSB/kq	1/50 LSB/kq	1/50 LSB/kq
Integration Time	10 to 1000 ms	10 to 1000 ms	10 to 1000 ms
Output Dynamic Range	10 bit	10 bit	12 bit
Digital I/O Speed	>50 Mbps	>60 Mbps	100 Mbps
Static Power Consumption	5 µW	8 µW	6 µW
Silicon Area	100µm x 100µm	70µm x 70µm	55µm x 55µm
Compensated Dark Current	95%	95 %	NA
Events Frequency	up to 560 kHz	up to 560 kHz	up to 800 kHz
Crosstalk	no observed	no observed	no observed
Equivalent Noise Charge	1.5 to 18 kq	NA	1.88 kq
Bias Mismatching	<10 %	<10 %	<15 %
Full Scale	>10 nA	>10 nA	>10 nA
Integrating Capacitor	150 fF	150 fF	150 fF







Custom setup
for X-Ray test

Conclusions and Status

- 3 generations of pixels have been developed with 100, 70 and 55µm pitch.
- All of them have been electrically tested obtaining satisfactory results.
- Test under real radiation is currently undergoing with preliminary satisfactory results.
- The migration of the designs to a 0.15µm CMOS technology is currently undergoing.
- The design of a novel dual pixel, which can work either in charge-integration or photon-counting methods, is also currently undergoing.

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