

Design and Modeling of a 0.4mW/Ch Multi-Channel Integrated Circuit for Infrared Gas Recognition

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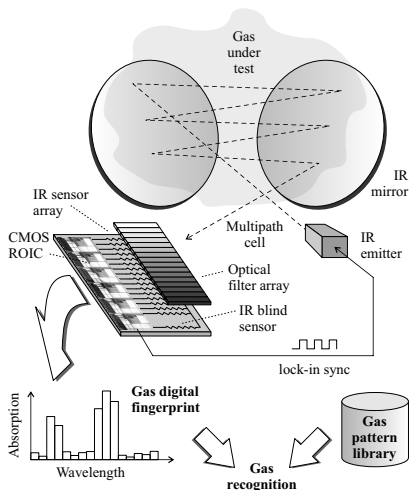
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- 1 Introduction
- 2 ROIC Channel Architecture
- 3 Pre-Amplification and Filtering
- 4 Blind Cancellation and Lock-in Demodulation
- 5 Integrating A/D Conversion
- 6 Post Layout High Level Modeling
- 7 CMOS Integration and Experimental Results
- 8 Conclusions

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Introduction

- ▶ Real-time **gas recognition** for environmental monitoring, toxic gas detection...
- ▶ **IR spectroscopic** absorption digital fingerprint
- ▶ Thermal μ bolometer LWIR **sensing array**
- ▲ **Multi-channel ROIC** for fast acquisition and low-noise
- ▲ Channel **lock-in** demodulation for high-accuracy
- ▲ **Low-power** operation to avoid thermal drifts of IR sensors
- ▲ **Compact pitch** for direct sensors-ROIC bonding



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Blind Cancellation and Lock-in Demodulation

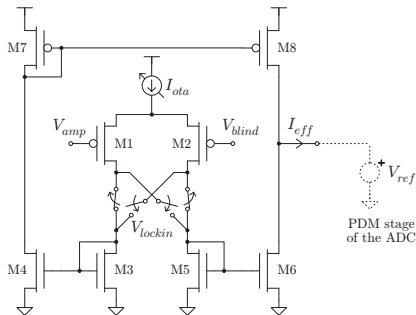
- ▶ Differential to **single ended**
- ▶ Voltage-to-**current** conversion
- ▶ **Lock-in** demodulation

- ▲ Low-power subthreshold **OTA**:

$$G_m = \frac{I_{eff}}{\Delta V_{amp}} = \frac{I_{ota}}{2nU_t} \propto U_t$$

$$I_{ota} \propto I_S = 2n\beta U_t^2$$

- ▲ **Current-domain** lock-in demodulation by cross-coupling
- ▲ Voltage log compression allows **fast switching** at low-power

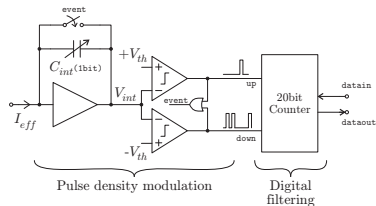


(cascode topology not shown)

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Integrating A/D Conversion

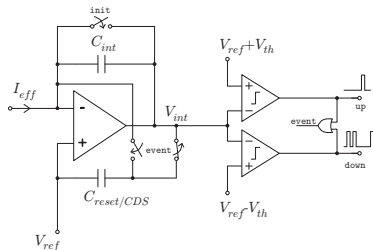
- ▶ **PDM** noise shaping
- ▶ Digital **counter** as low-pass filter
- ▲ **Asynchronous** operation for very low-power and low-crosstalk



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- ▲ **Loss-less** analog integrator with **CDS** for high-linearity and noise reduction:

$$f_{PDM} = \frac{I_{eff}}{C_{int} V_{th}}$$



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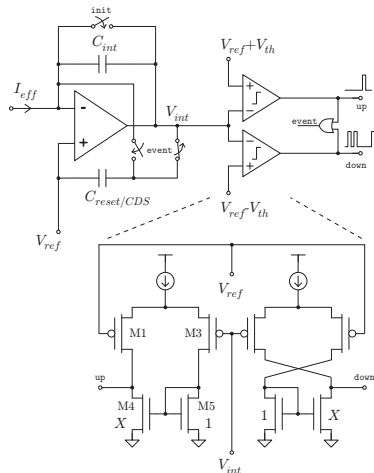
$$f_{PDM} = \frac{I_{eff}}{C_{int} V_{th}}$$

- ▲ **Built-in** threshold comparator:

$$V_{th} = nU_t \ln X$$

- ▲ **Thermal compensation** of G_m :

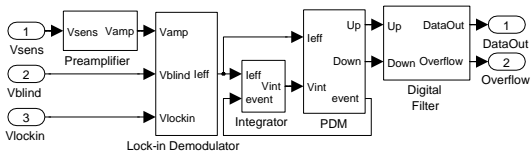
$$q_{adc} = \lfloor n_{adc} \rfloor \quad n_{adc} = T_{samp} f_{PDM} = \frac{C_A}{C_B} \frac{G_m}{V_{th}} \frac{T_{samp}}{C_{int}} \Delta R_{sens}$$



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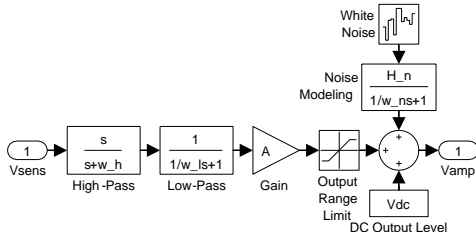
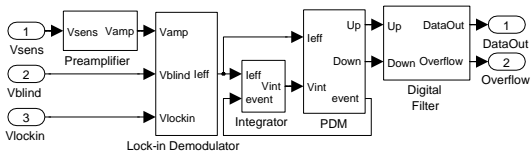
Post Layout High Level Modeling

- ▲ Simulation **time reduction**
- ▲ Complete **read-out channel model**
- ▲ Entire set of **channel configurations**



Post Layout High Level Modeling

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- ▲ Complete **read-out channel model**
- ▲ Entire set of **channel configurations**
- ▲ Wide range of **nonidealities modeling**
- ▶ **Technology process and temperature**
- ▶ **Flicker and thermal noise options**
- ▶ **External sensor modeling**



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CMOS Integration and Experimental Results

- ▶ 0.35 μm 2P4M CMOS channel module **test chip**
- ▶ Main **design parameters**:

$$C_A = 20\text{pF}$$

$$C_B = \{0.1, 0.2, 0.4, 1\}\text{pF}$$

$$K = 10$$

$$N = \{1, 11\}$$

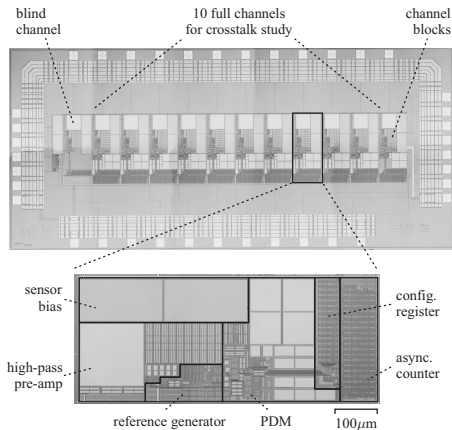
$$M = 3$$

$$I_{tun} = 100\text{nA}$$

$$I_{ota} = \{1, 2, 5, 10\}\mu\text{A}$$

$$V_{th} = 120\text{mV}$$

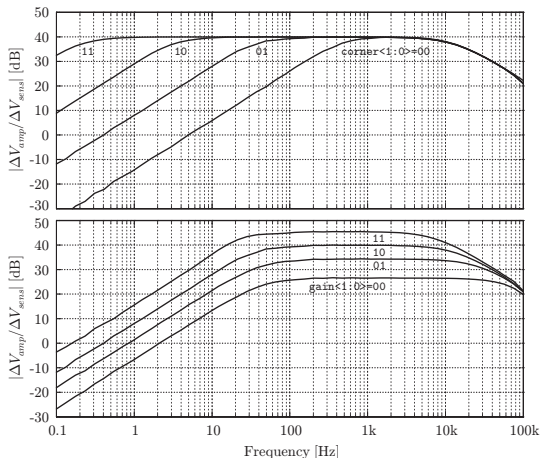
$$T_{pulse} = 500\text{ns}$$



▲ Access to **intermediate stages**

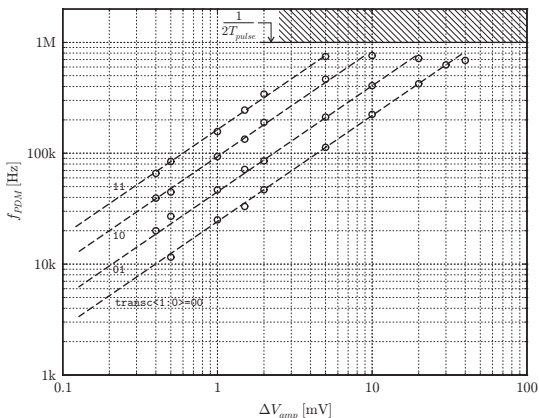
CMOS Integration and Experimental Results

- ▲ Sub-Hz pre-amplifier independent tuning (16 configurations)



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- ▲ Highly linear PDM up to pulse width hard limit



for $cint<0>=0$

CMOS Integration and Experimental Results

- ▲ Sub-Hz **pre-amplifier**
independent tuning
(16 configurations)
- ▲ Highly linear **PDM**
up to pulse width
hard limit
- ▲ 9bit digital
programmability per
channel
- ▲ **No crosstalk**
observed between
channels

experimental (vs simulated)
results per channel

Parameter	Value	Units
I_{bias} bias<1:0>=00	01	0.97 (1)
	10	1.9 (2)
	11	4.6 (5)
	11	9.1 (10)
f_c corner<1:0>=00	01	0.3 (0.25)
	10	3.9 (4.1)
	10	50 (60)
	11	625 (825)
G gain<1:0>=00	01	27 (26)
	10	34 (34)
	10	40 (40)
	11	46 (45)
G_m transc<1:0>=00	01	(15)
	10	(30)
	10	(70)
	11	(130)
C_{int} cint<0>=0	1	(5)
	1	(10)
Total Harmonic Distortion	<0.25	%
Crosstalk	<0.5	LSB
V_{nieq} for $R_{sens}=300k\Omega$	(100)	nV _{rms} /√Hz
Supply voltage	3.3	V
Supply current	100	μA
Silicon area	300 × 715	μm ²

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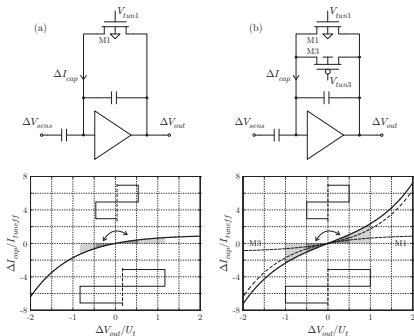
Conclusions

- ▶ **Digital read-out** channel for IR spectroscopic gas recognition
- ▶ **Fully integrable** sub-Hz high-pass pre-amplification
- ▶ **Blind** cancellation and **lock-in** demodulation
- ▶ **Highly linear** integrating A/D conversion
- ▶ **High-programmability** (9bit) per channel
- ▶ **Low-current** ($100\mu\text{A}$) and **compact** (0.2mm^2) channel module in $0.35\mu\text{m}$ 2P4M CMOS technology
- ▶ Experimental results **agree** with simulated performance
- ▶ Post layout **high level modeling**
- ▶ **No-crosstalk** reported between channels

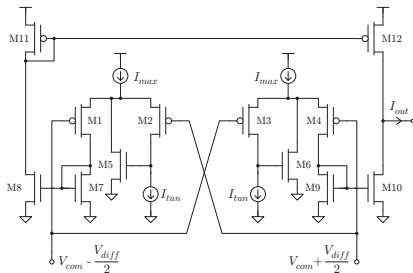
... thanks for your attention!

Improvements?

▼ Pre-amplifier dynamic offset



▼ OTA linear range



▲ A 32-channel ROIC is under development!