

A fA-Range Low-Power Multi-Channel Digital Read-Out Integrated Circuit for Differential Mobility Analyzers

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- 2 ROIC Channel Architecture
- 3 Reset times
- 4 Switch Leakage
- 5 CMOS Integration and Simulation Results
- 6 Test Environment
- 7 Conclusions

1 Introduction

2 ROIC Channel Architecture

3 Dead times

4 Switch Leakage

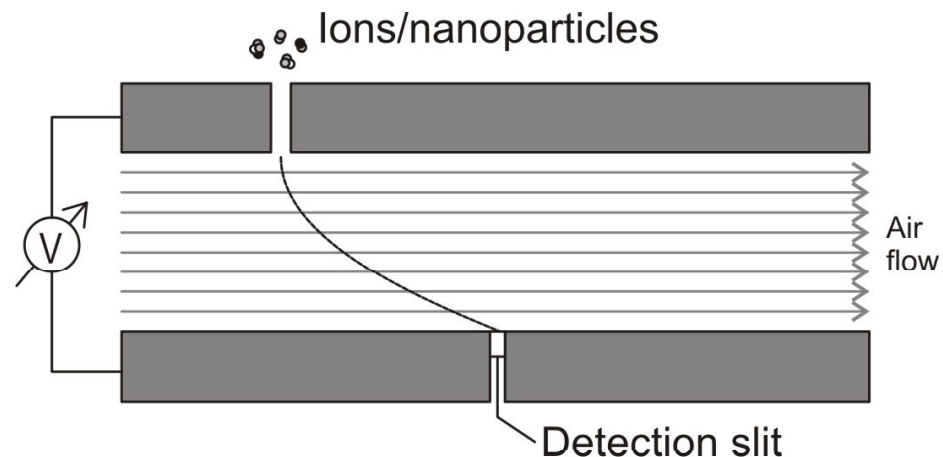
5 CMOS Integration and Simulation Results

6 Test Environment

7 Conclusions

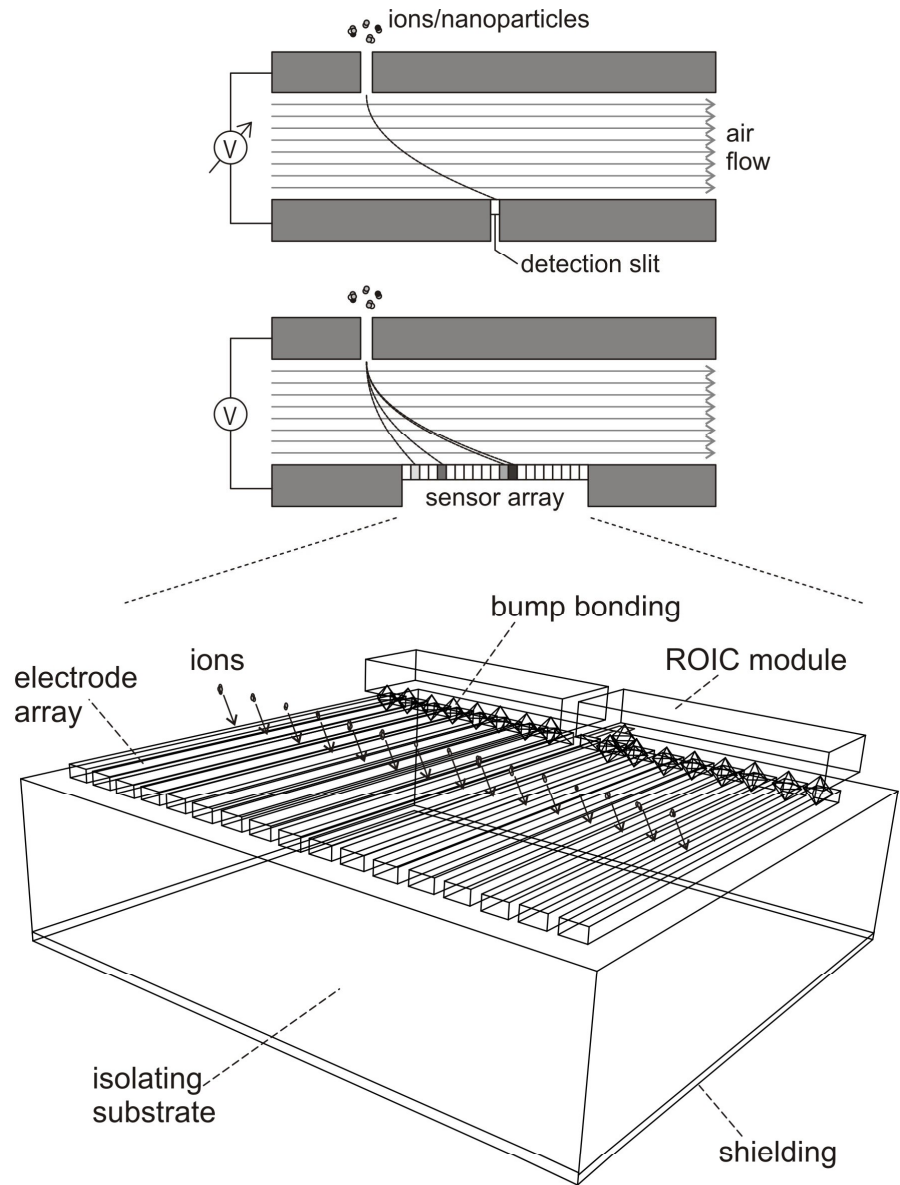
Introduction

- ▶ Aerosol identification for medicine, biology, environment monitoring, security...
- ▶ Differential Mobility Analyzer (DMA): ion/particle classification according to mass and charge
- ▼ Long acquisition time (several seconds)



Introduction

- ▶ Aerosol identification for medicine, biology, environment monitoring, security...
- ▶ Differential Mobility Analyzer (DMA): ion/particle classification according to mass and charge
- ▼ Long acquisition time (several seconds)
- ▶ Array of independent and separated microelectrodes
- ▶ Parallel signal processing
- ▶ Fast acquisition time (ms) for the same noise bandwidth



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6 Test Environment

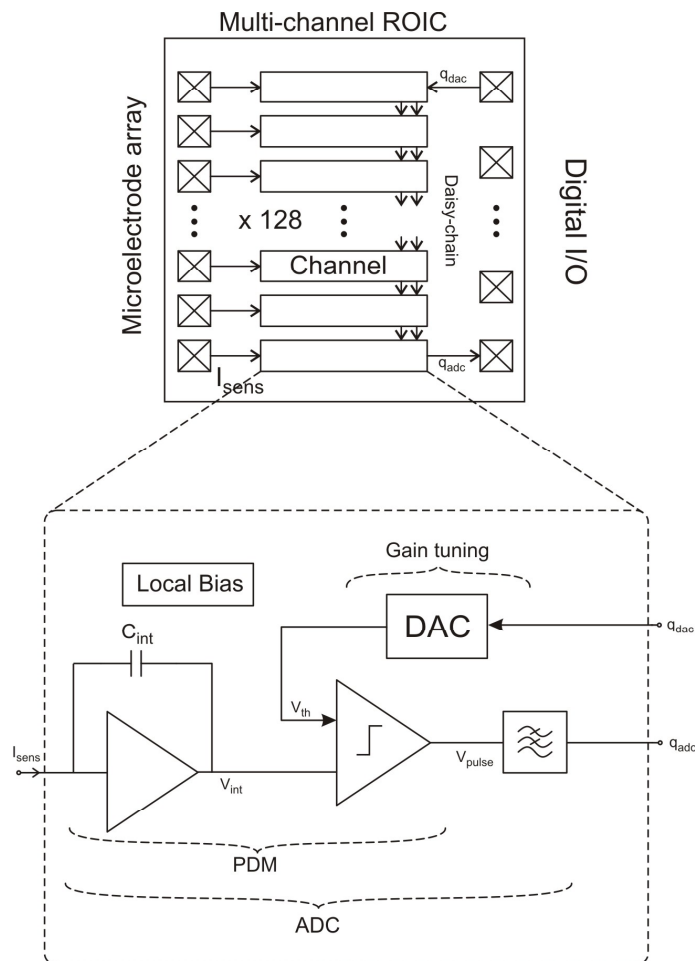
7 Conclusions

ROIC Channel Architecture

Parameter	Value	Units
<i>Channel pitch</i>	50	μm
<i>Micro-electrode resistance</i>	≤ 50	Ω
<i>Micro-electrode capacitance</i>	≤ 2	pF
<i>Acquisition time</i>	1 : 100	ms
<i>Input resolution (@100ms)</i>	± 1	fA
<i>Input dynamic range</i>	80	dB
<i>Supply voltage</i>	3.3	V
<i>Power consumption</i>	< 0.5	mW/Ch
<i>Temperature (@100ms)</i>	-20:0:30	$^{\circ}\text{C}$

- ▶ Main specifications of the ROIC
- ▶ Compact channel area
- ▶ Short acquisition time
- ▶ High current sensitivity
- ▶ Wide dynamic range
- ▶ Low-power operation

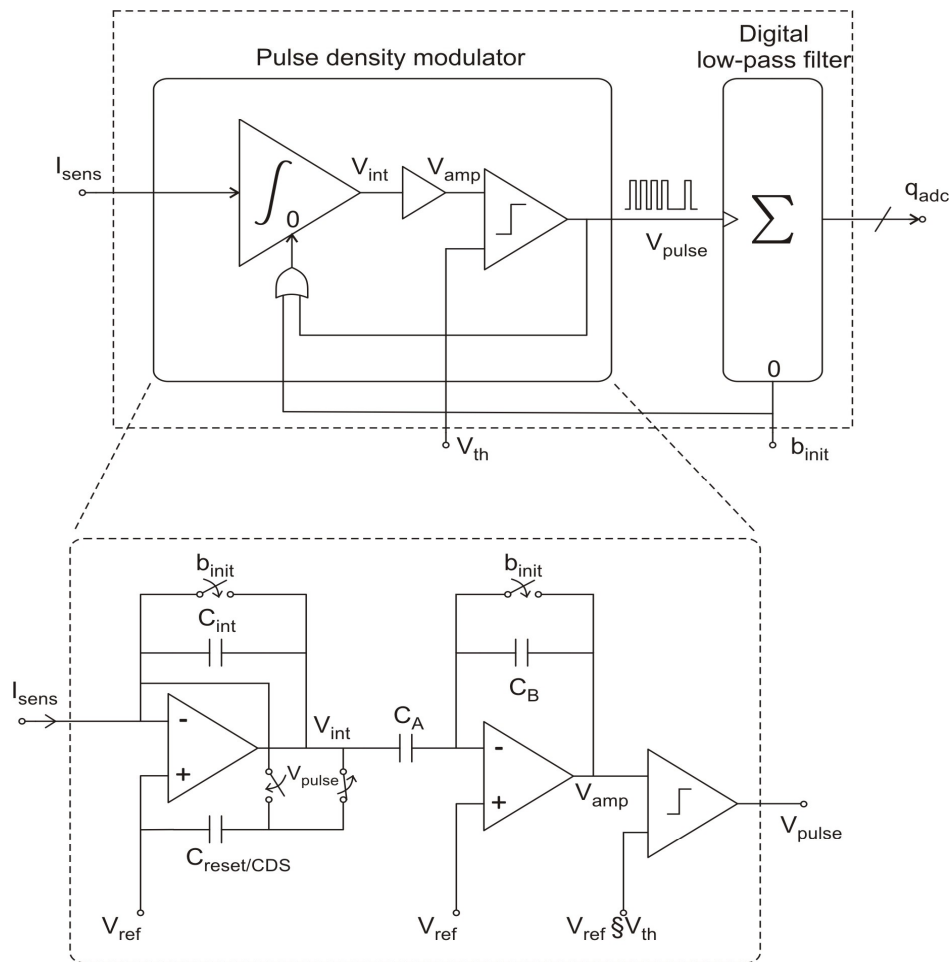
ROIC Channel Architecture



- ▶ Integrating A/D Conversion
- ▲ Full-parallel signal processing.
- ▲ No input signal multiplexing is required.
- ▲ Narrow noise bandwidth.
- ▲ Minimum crosstalk.
- ▲ Fixed pattern noise compensation.
- ▼ Low power CMOS and compact circuits required.

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Reset Times



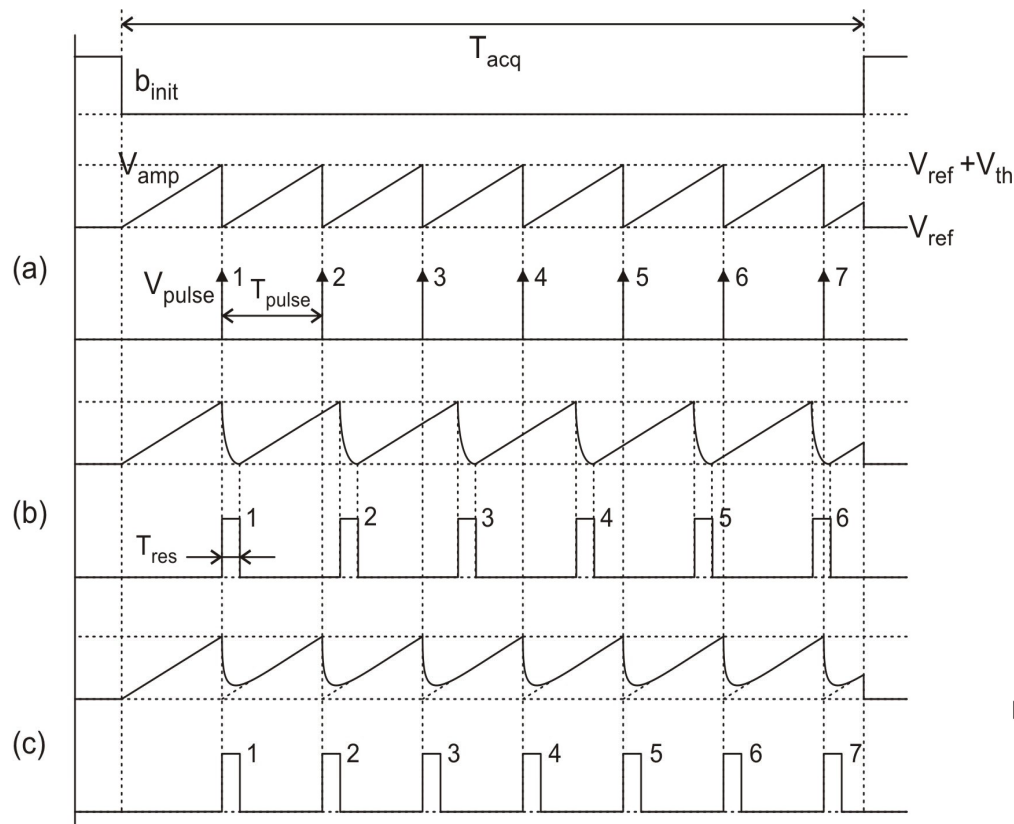
► Novel integration scheme for in-channel ADC conversion.

▲ High linearity.

▲ Correlated Double Sampling (CDS).

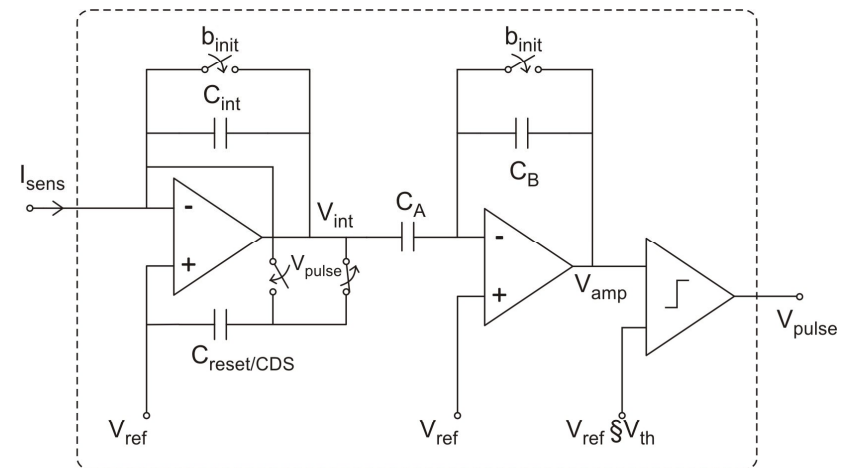
▲ Compact CMOS circuits.

Reset Times



► Novel PDM scheme for minimum reset time during integration:

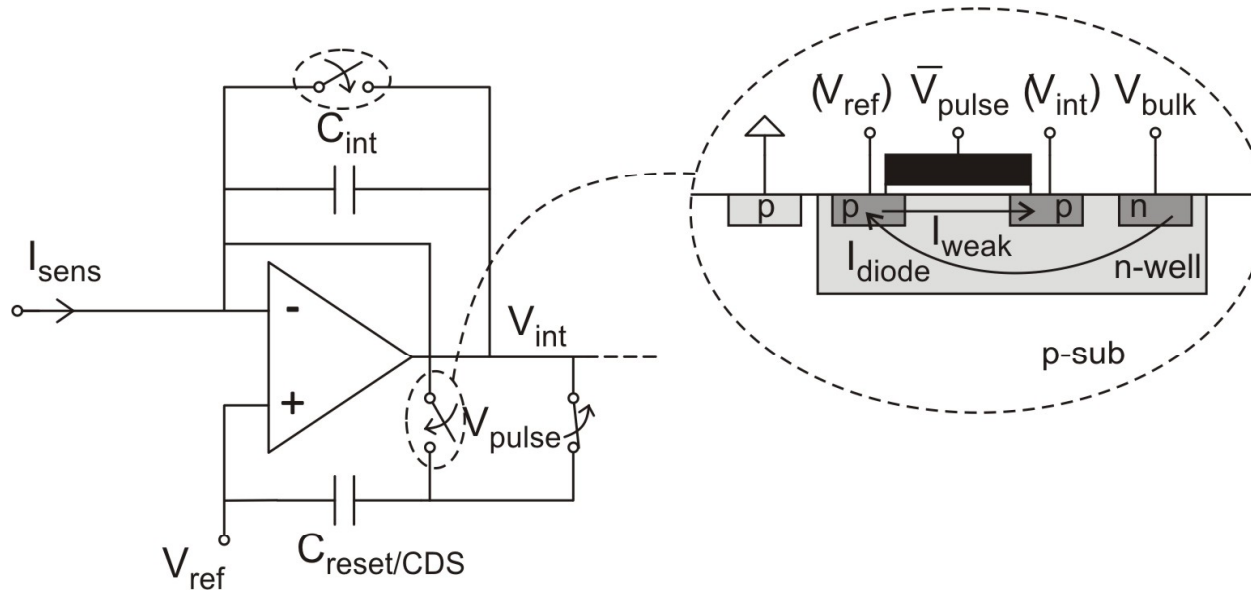
- ▲ High linearity.
- ▲ Correlated double sampling (CDS).
- ▲ Robust.
- ▲ Compact CMOS circuits.



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Switch Leakage

► MOSFET switch non-idealities:



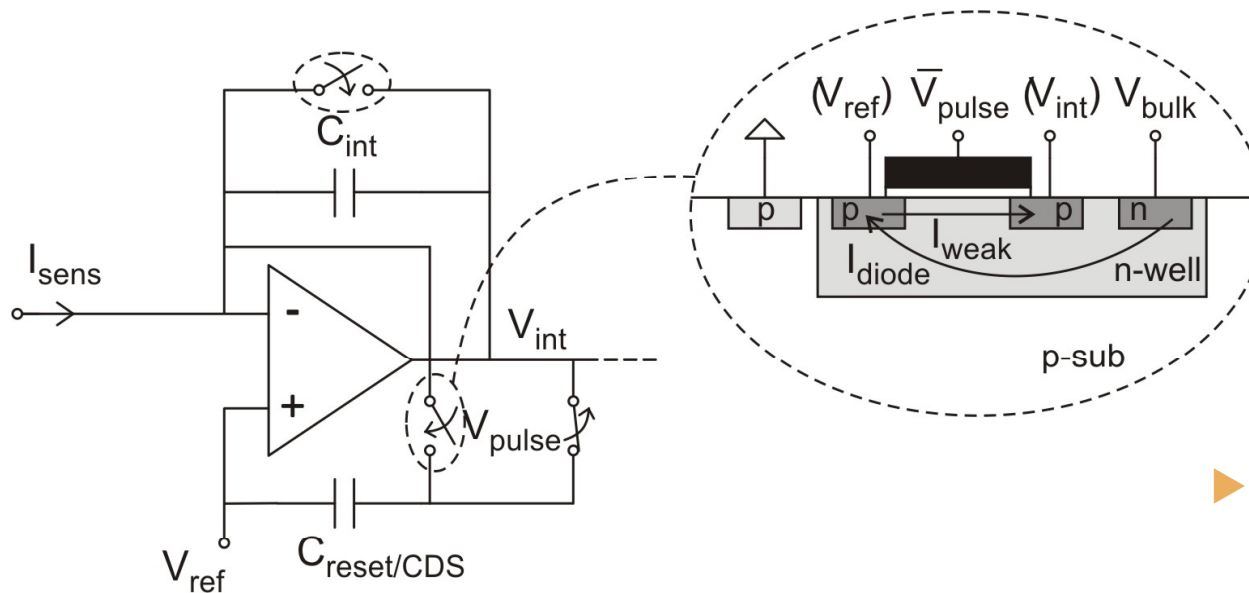
- ▼ Subthreshold conduction
- ▼ D/S diffusion diodes leakage

$$I_{leak} = I_{weak} - I_{diode}$$

$$I_{weak} = I_{SM} e^{\frac{V_{bulk} - V_{DD} + V_{TO}}{nV_t}} e^{\frac{V_{ref} - V_{bulk}}{V_t}} \quad I_{diode} = I_{SD} \left(1 - e^{-\frac{V_{bulk} - V_{ref}}{V_t}} \right)$$

Switch Leakage

- MOSFET switch non-idealities:



- Proper n-well biasing (V_{bulk})

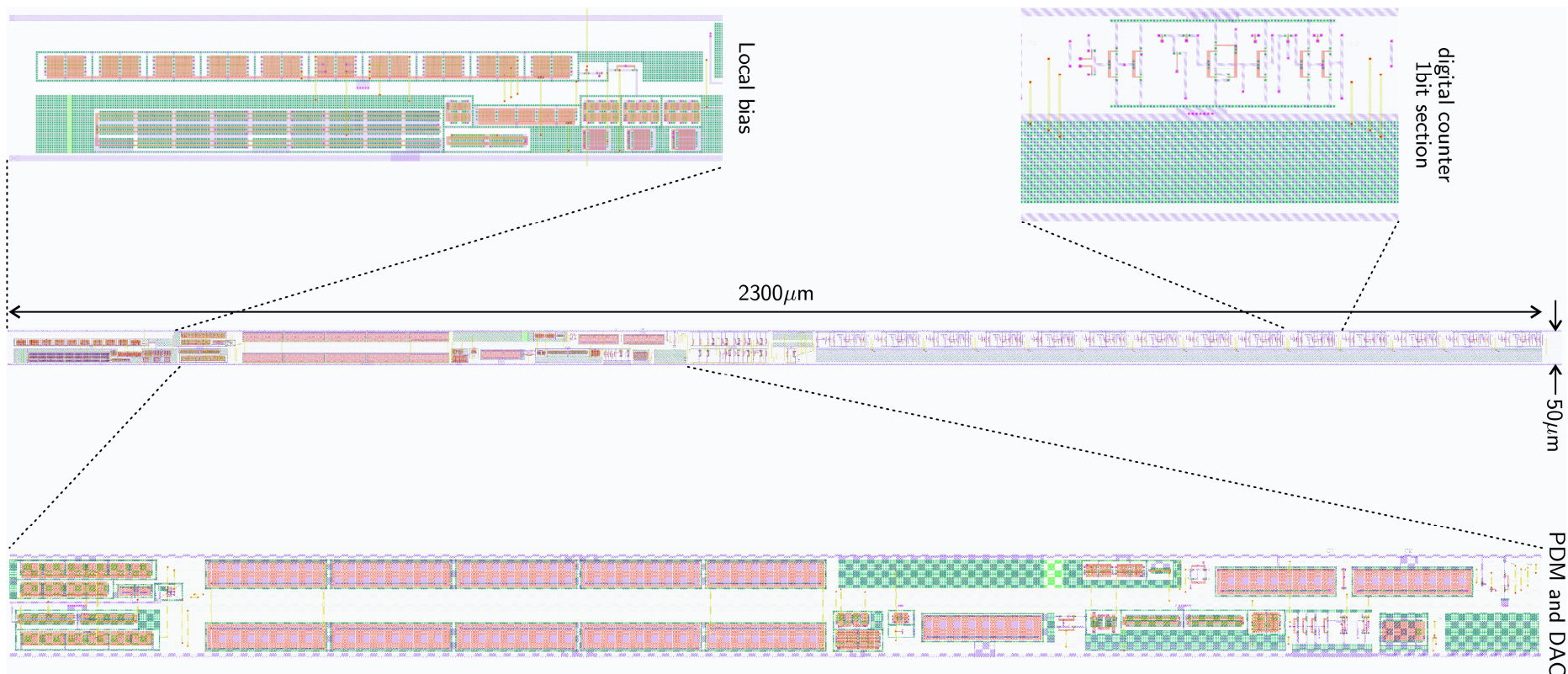
- $I_{leak} \leq 0.5 \text{ fA}$

$$I_{leak} < I_{SM} e^{\frac{V_{ref} - V_{DD} + V_{TO}}{nU_t}} \quad \text{for } V_{bulk} \equiv V_{ref}$$

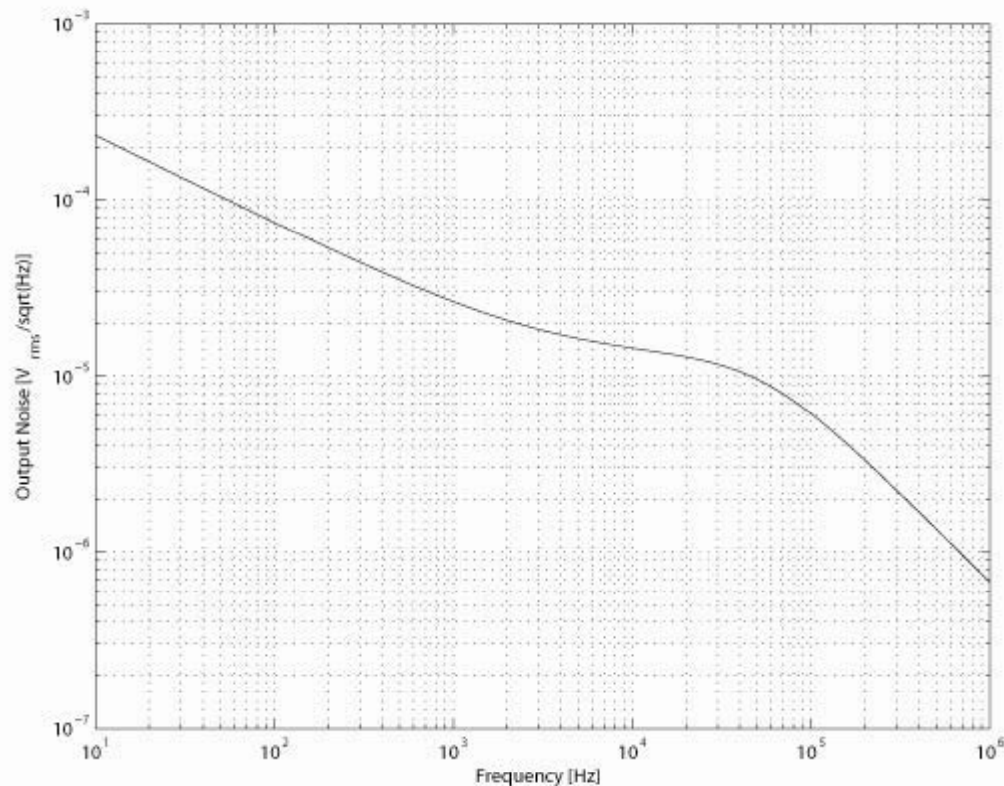
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CMOS Integration and Simulation Results

- ▶ Full channel layout in 0.35 μm 2P4M CMOS technology:



CMOS Integration and Simulation Results



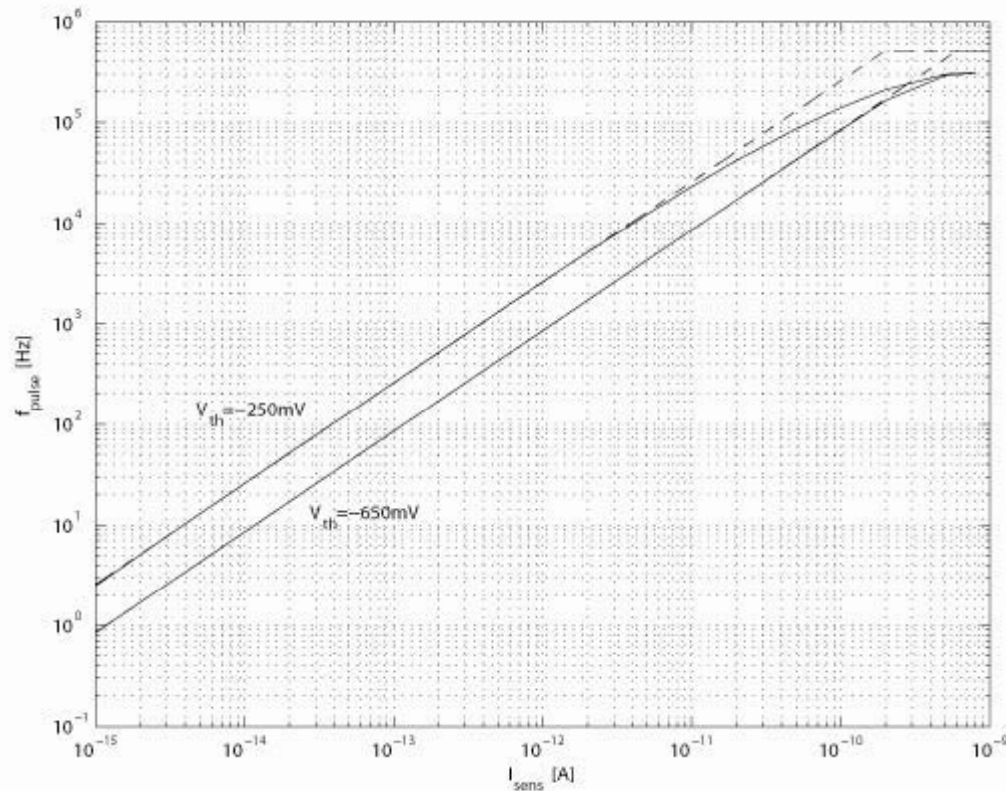
- ▶ CMOS noise dominate over electrode noise
- ▶ 65% thermal and 35% flicker

$$ENC = C_{int}V_{intn} \simeq 10\text{fF} \times 4\text{mV}_{\text{rms}} = 40\text{aC}_{\text{rms}} = 250e_{\text{rms}}^-$$

$$I_{sensn} = \frac{ENC}{T_{acq}} = \frac{40\text{aC}_{\text{rms}}}{100\text{ms}} = 0.4\text{fA}_{\text{rms}}$$

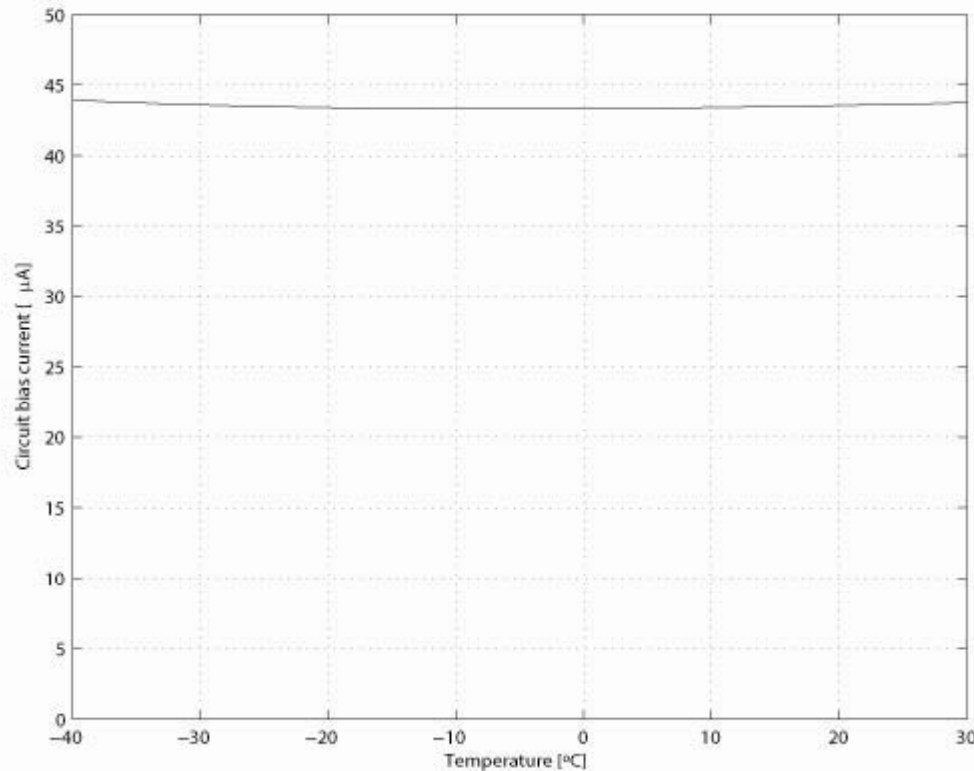
- ▶ Adequate LSB for 1 fA resolution

CMOS Integration and Simulation Results



- ▶ PDM transfer function
- ▼ Poor linearity at full-scale

CMOS Integration and Simulation Results



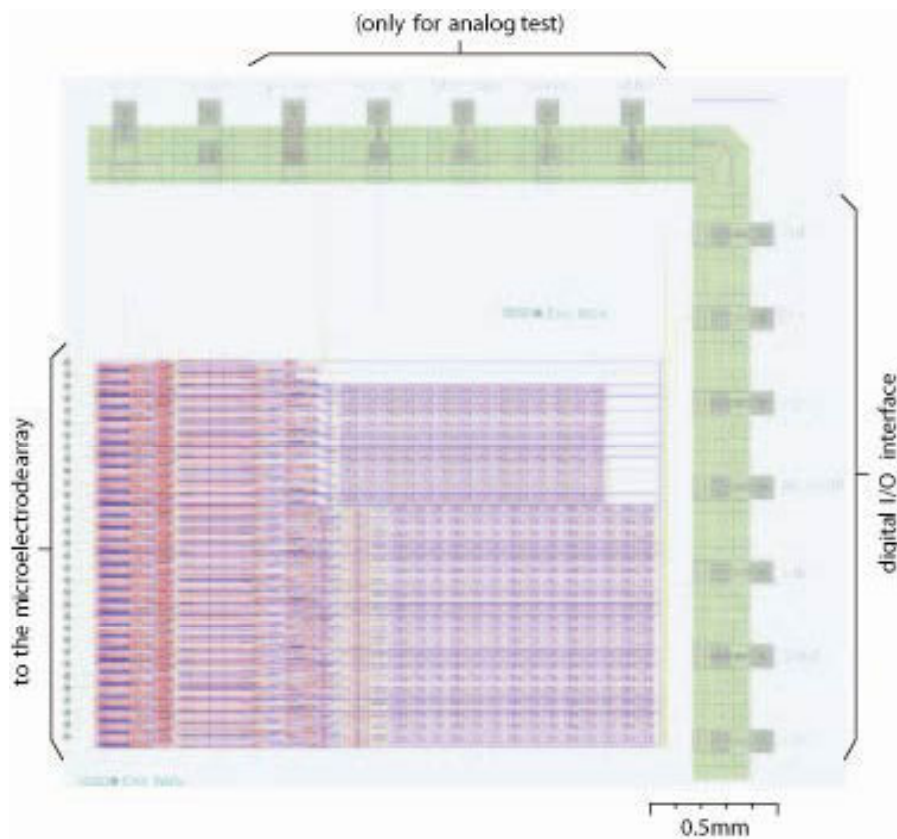
- ▶ Local bias generator
- ▲ Flat temperature sensitivity

CMOS Integration and Simulation Results

Parameter	Value	Units
<i>Channel pitch</i>	50	μm
<i>Silicon area</i>	0.12	mm^2
<i>Acquisition time</i>	1 : 100	ms
<i>Equivalent input noise (@100ms)</i>	0.4	fA_{rms}
<i>Instantaneous dynamic range</i>	84	dB
<i>Overall dynamic range</i>	100	dB
<i>Threshold range (V_{th})</i>	$\pm 250 : \pm 650$	mV
<i>Threshold step (ΔV_{th})</i>	± 10	mV
<i>Supply voltage</i>	3.3	V
<i>Current consumption</i>	110	μA

► Main performance parameters of the ROIC channel module

CMOS Integration and Simulation Results

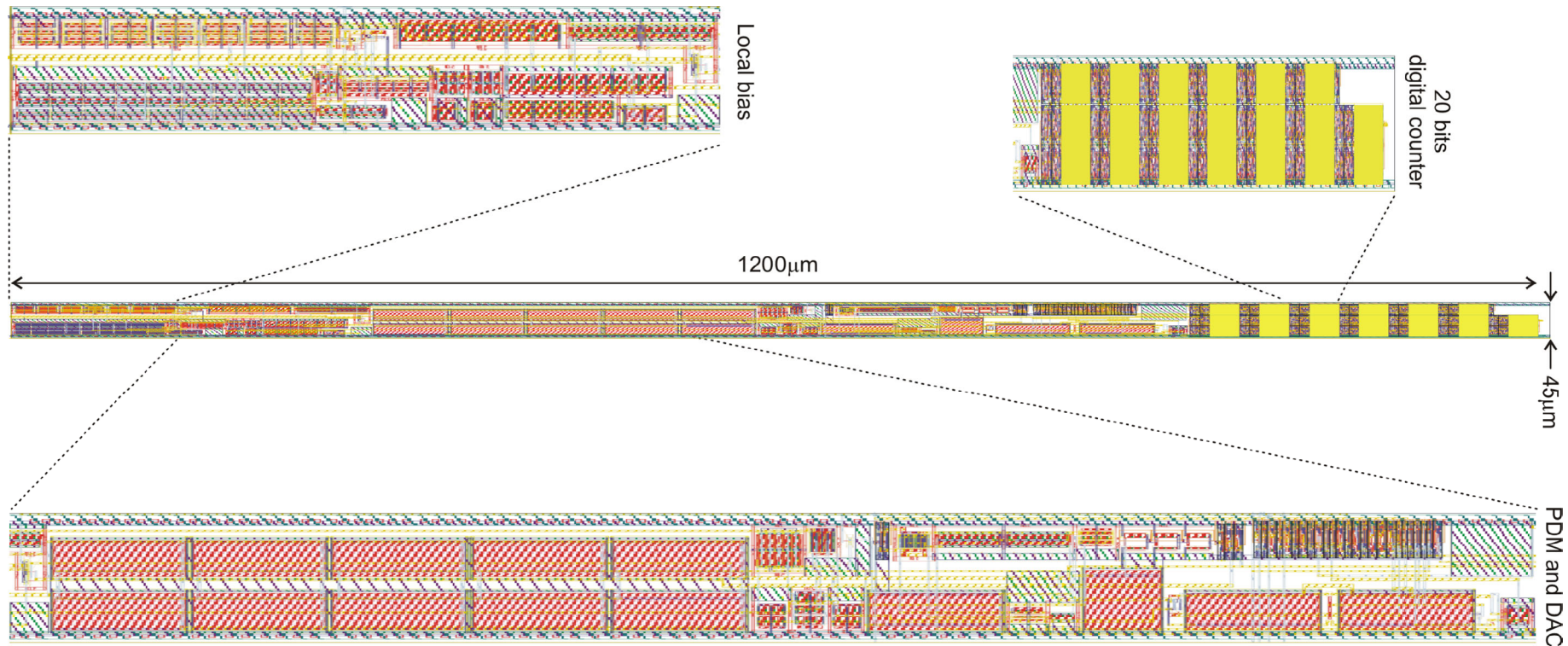


$$2950\mu\text{m} \times 2850\mu\text{m} = 8.4\text{mm}^2$$

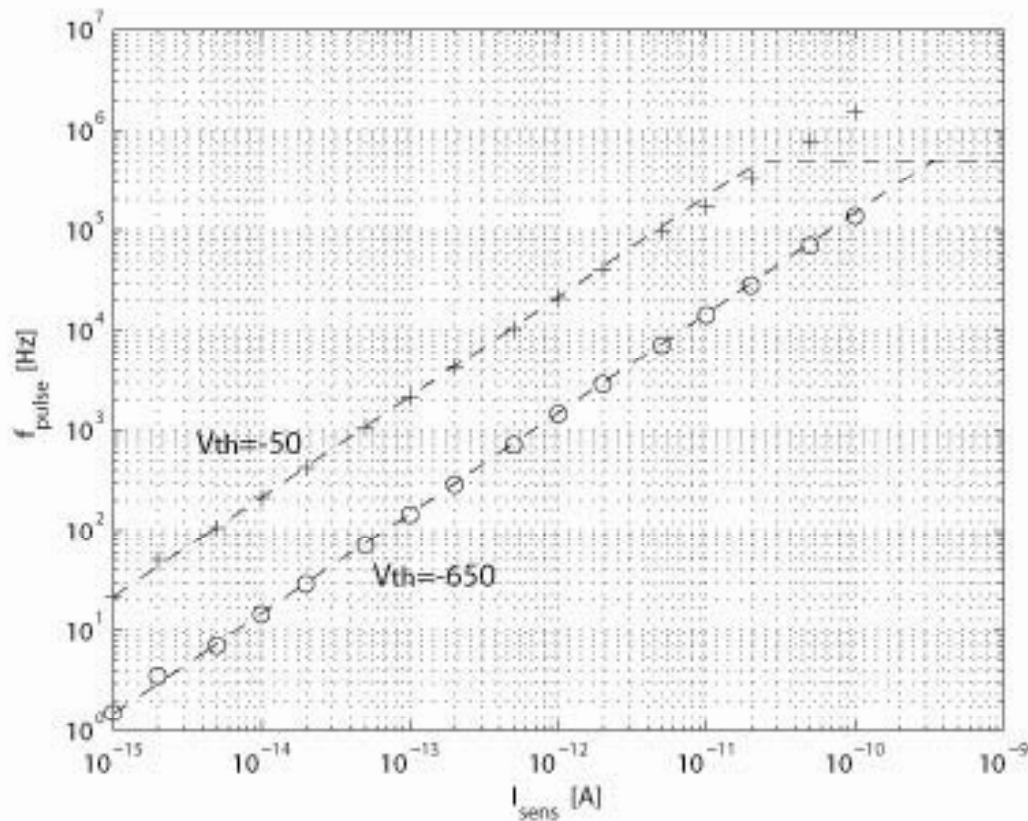
- ▶ First test vehicle prototype:
 - ▲ 1 pre-amp block
 - ▲ 1 PDM block
 - ▲ 10 operative channels with external programming
 - ▲ 20 full channels with serial interface
- ▶ 035um CMOS 2P 4M technology (AMS-C35)
- ▶ Bump bonding

CMOS Integration and Simulation Results

- ▶ Second version with enhanced performance and compact layout:



CMOS Integration and Simulation Results



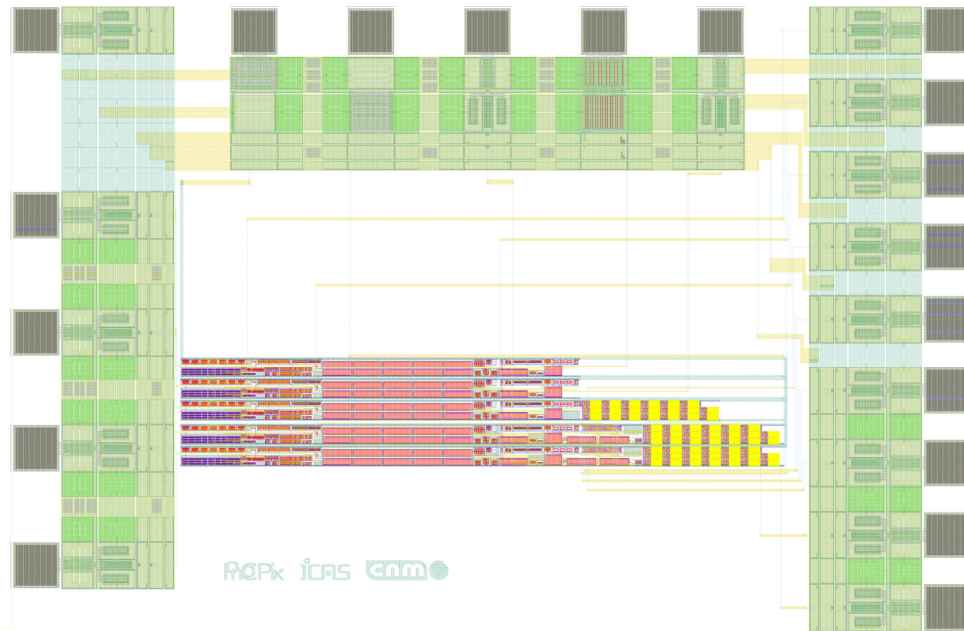
- ▲ High Linearity of the PDM
- ▲ High sensitivity (20Hz/fA)

CMOS Integration and Simulation Results

Parameter	Value	Units
<i>Channel pitch</i>	45	μm
<i>Silicon area</i>	0.054	mm^2
<i>Acquisition time</i>	1 : 100	ms
<i>Equivalent input noise (@100ms)</i>	0.4	fA_{rms}
<i>Instantaneous dynamic range</i>	120	dB
<i>Overall dynamic range</i>	100	dB
<i>Threshold range (V_{th})</i>	$\pm 50 : \pm 650$	mV
<i>Threshold step (ΔV_{th})</i>	± 10	mV
<i>Supply voltage</i>	3.3	V
<i>Current consumption</i>	110	μA

- ▶ Main performance parameters of the ROIC channel module

CMOS Integration and Simulation Results

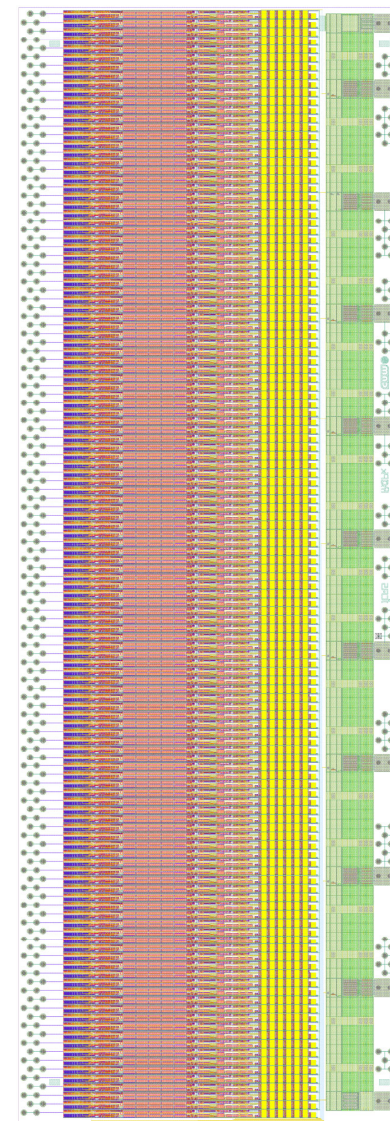
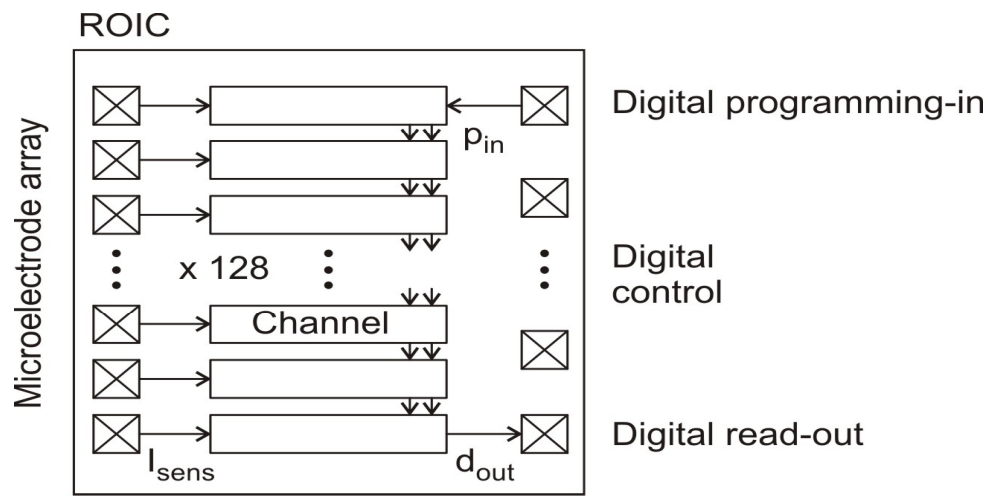


2000 μm x 1300 μm = 2.6mm²

- ▶ Second test vehicle prototype:
 - ▲ 1 pre-amp block
 - ▲ 1 PDM block
 - ▲ 1 operative channel with external programming
 - ▲ 2 full channels with serial interface
- ▶ 035 μm CMOS 2P 4M technology (AMS-C35)
- ▶ Wire bonding

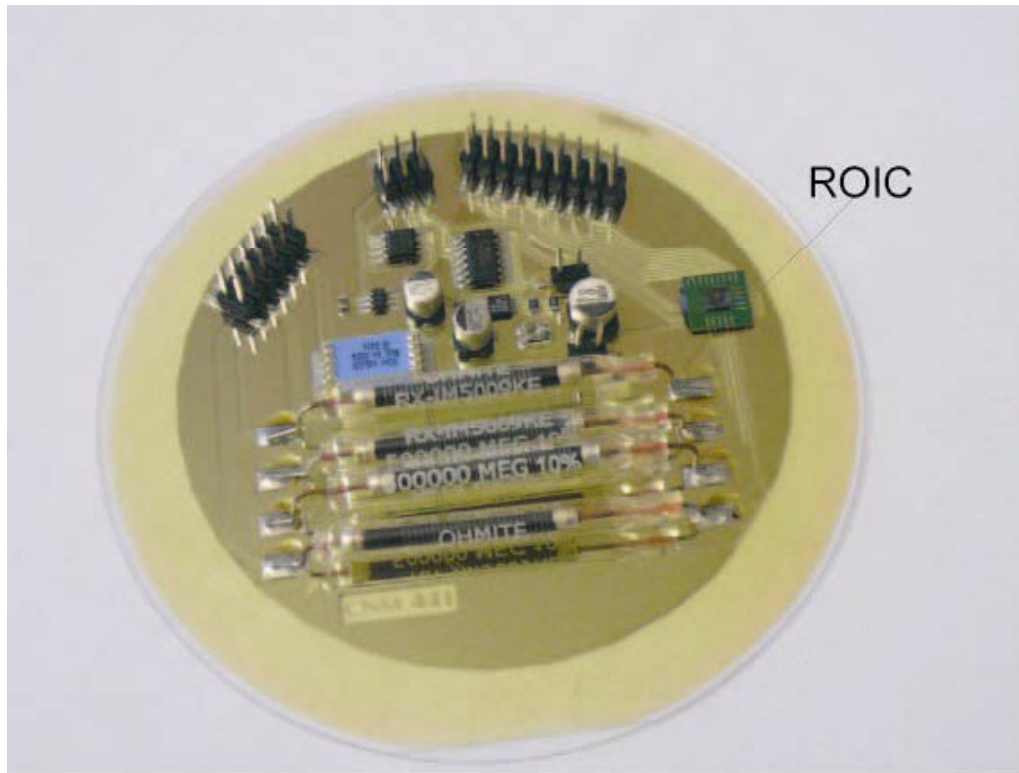
CMOS Integration and Simulation Results

- ▶ Complete 128-channel ROIC
- ▶ 035um CMOS 2P 4M technology (AMS-C35)
- ▶ Bump bonding
- ▶ Size: $5800\mu\text{m} \times 1890\mu\text{m} = 10.96\text{mm}^2$



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Test Environment



- ▲ SiO₂ wafer substrate for low leakage
- ▶ Flip-chip ROIC
- ▲ Wire-bonded ROIC carrier for multiple sample testing
- ▶ SMD bonding by screen printing
- ▶ 500 GΩ glass sealed hermetic resistors for fA stimulus

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Conclusions

- ▶ Digital multi-channel read-out integrated circuit for differential mobility analyzers
- ▶ Dedicated PDM ADC with independent gain programmability and thermal compensation
- ▶ Low current (110 μA) and compact (0.054 mm^2) channel model in 0.35 μm 2P4M CMOS technology
- ▶ Simulation results agrees with the main specifications of the ROIC
- ▶ Experimental results are expected in short

...thanks for your attention!