A 0.18μm CMOS Low-Power Charge-Integration DPS for X-Ray Imaging

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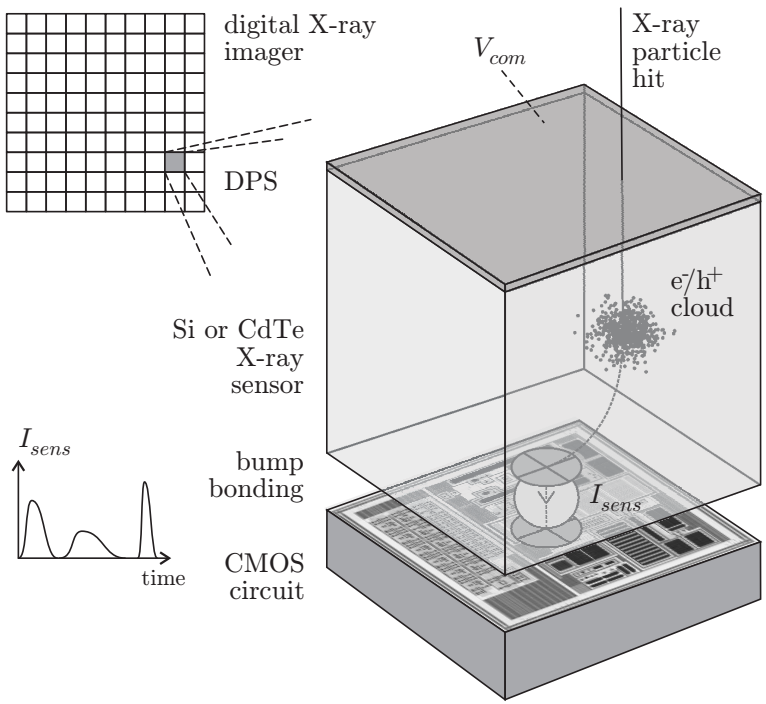
Introduction

- **Hybrid X-ray digital** imagers
- Low-energy (<20keV) medical applications: **mammography**



- DPS circuits for **visible** spectrum:
  - ✘ e^-/h^+ collection
  - ✘ Pulsed X-ray input current (typ. $15ke^-/hit@10\mu s$)
  - ✘ Dark current + gain FPN
  - ✘ Built-in test
- Few DPS for **X-ray** based on **photon-counting**:
  - ✘ Saturation due to pile-up
  - ✘ Losses from charge sharing with neighbors

Introduction

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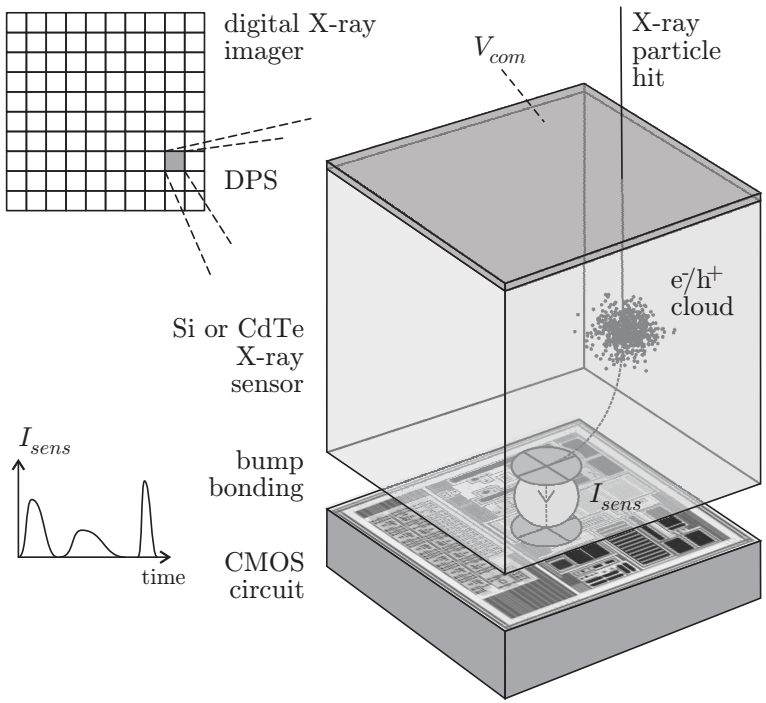
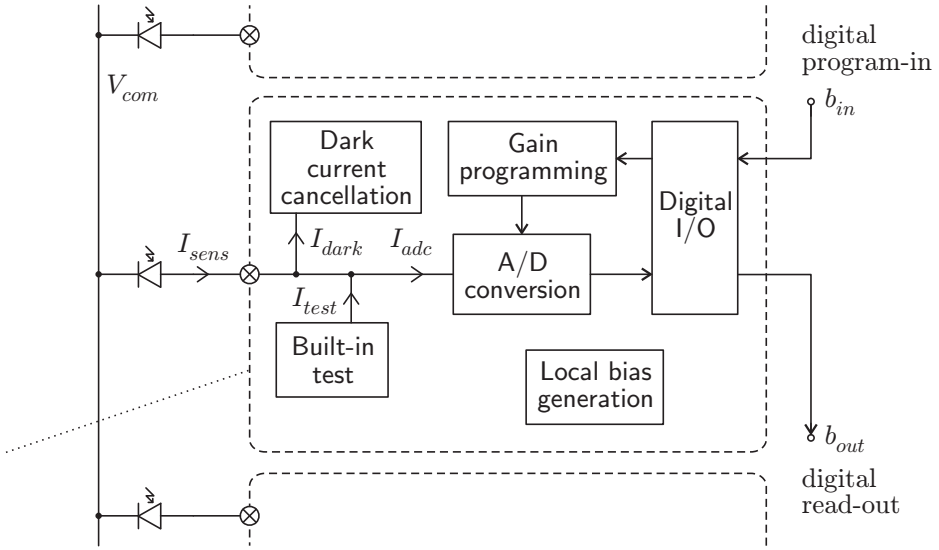
- Low-energy (<20keV) medical applications: **mammography**



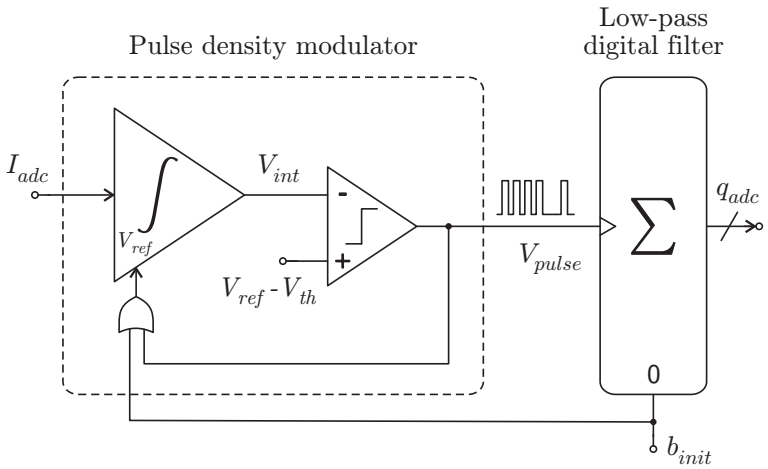
- Novel X-ray **DPS proposal** based on **charge-integration** to solve all plus:
  - ✔ Self-biasing
  - ✔ Lossless A/D conversion



. . . **subthreshold** operation and circuit **reuse** for a **low-power** and **compact** DPS!

Lossless A/D Conversion

- **Predictive** scheme:

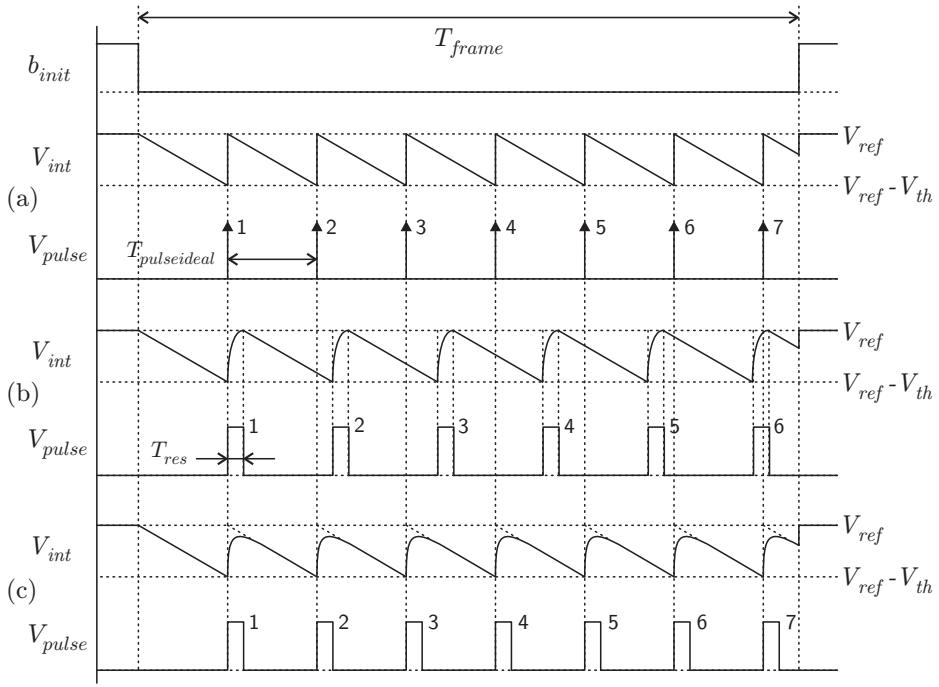


$$q_{adc} = \lfloor n_{adcideal} \rfloor$$

$$n_{adcideal} = \frac{T_{frame}}{T_{pulseideal}} = \frac{T_{frame}}{C_{int}\, V_{th}} \bar{I}_{adc}$$

e.g. 10bit and T_{frame}=10ms
require T_{res}<5ns!

- Under real **low-power** operation:



$$n_{adcreal} = \frac{n_{adcideal}}{1 + \frac{T_{res}}{T_{frame}} n_{adcideal}}$$

$$T_{res} < \frac{T_{frame}}{2q^2_{fullscale}} \quad \text{for } <0.5\text{LSB error}$$

Lossless A/D Conversion

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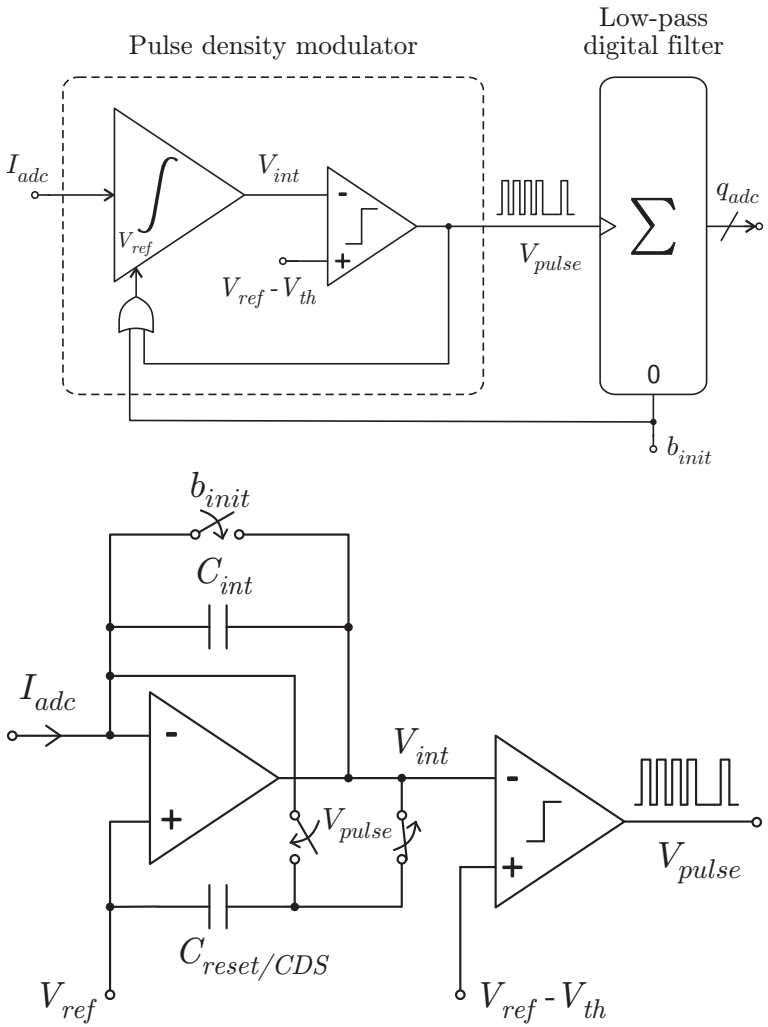

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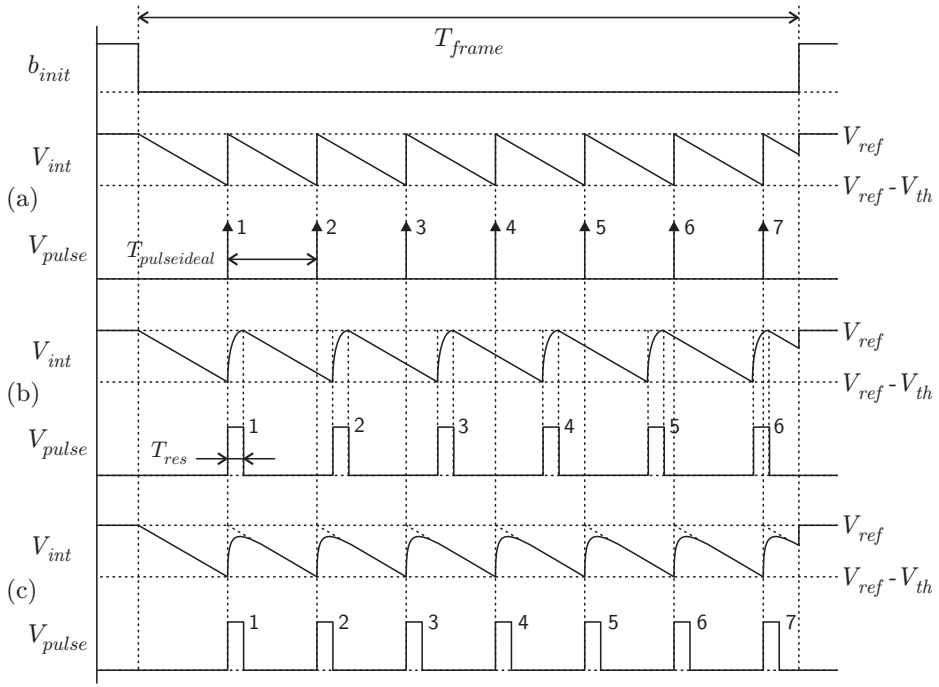
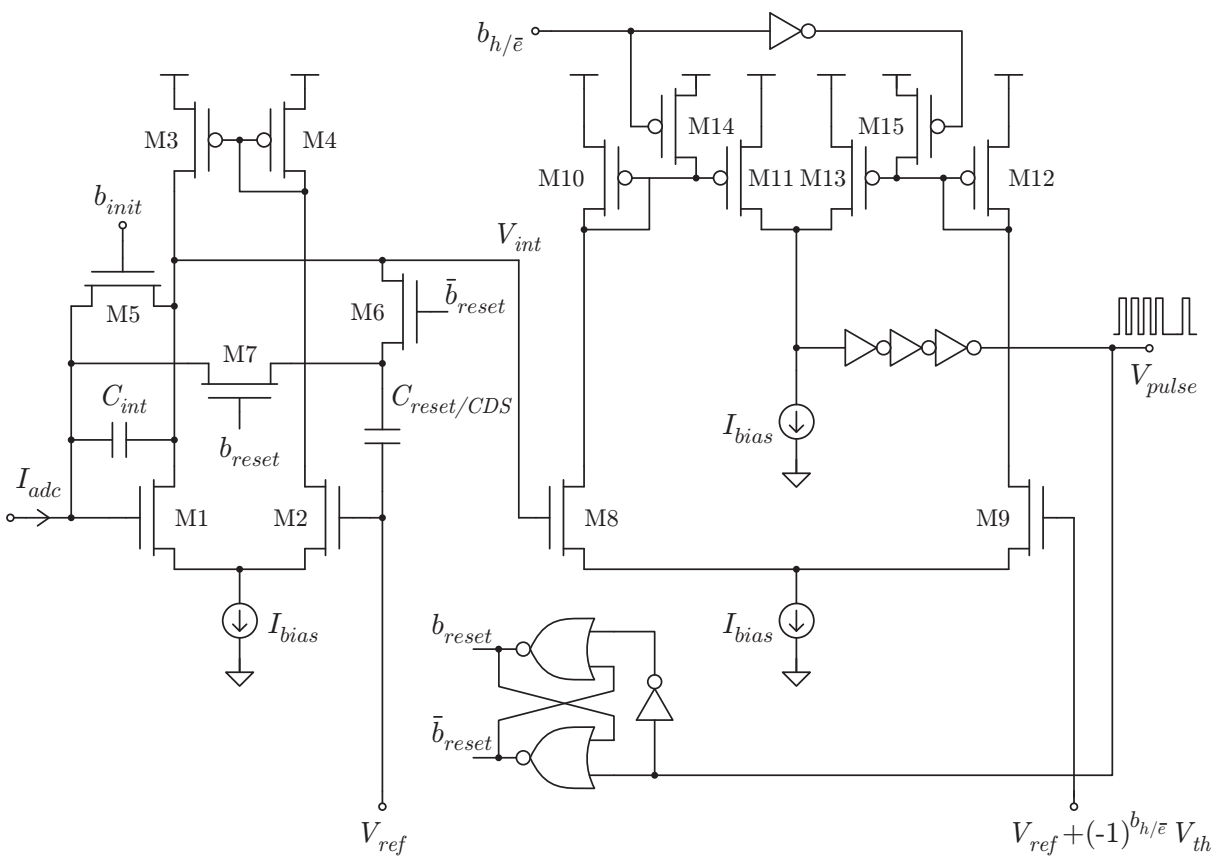


$$n_{adcreal} \equiv n_{adcideal}$$

- ✔ T_{res} independent
- ✔ min(T_{res}) for charge redistribution
- ✔ max(f_{pulse})=$\frac{1}{2\,T_{res}}$

Lossless A/D Conversion

- CMOS **proposal**:

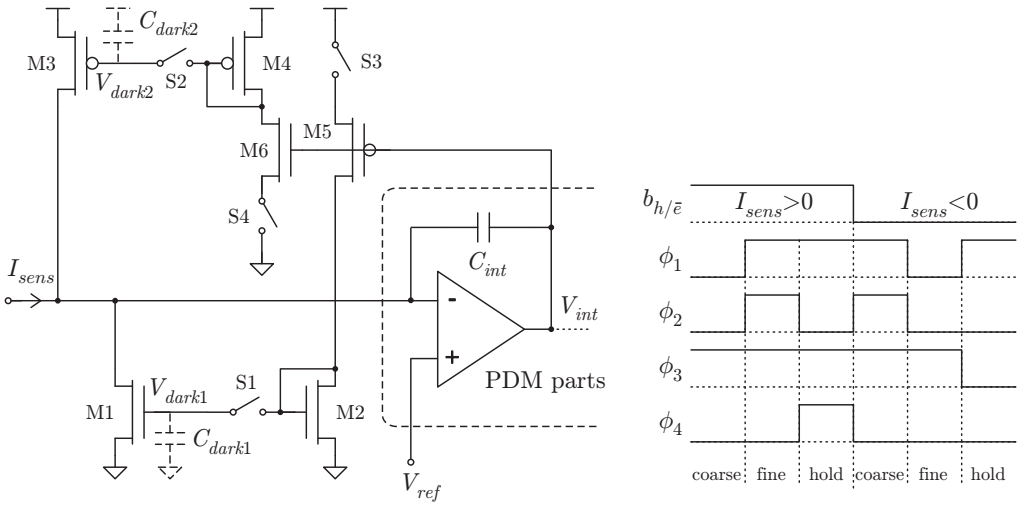


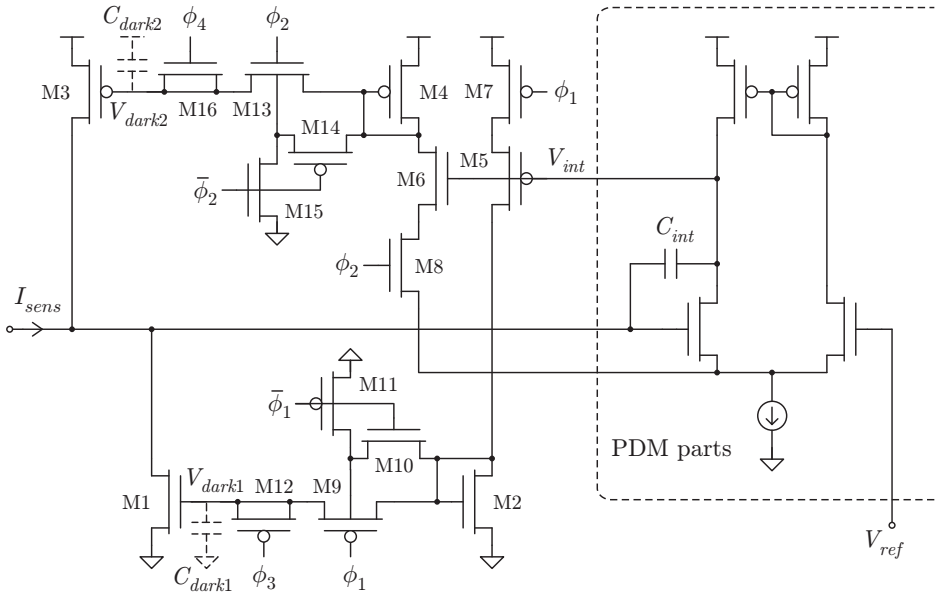
- Capacitive TransImpedance Amplifier (**CTIA**) = M1-4 + C_{int}
- Non-overlapped **reset** by M6-7

✔ $b_{h/\bar{e}}$ for controlling **collection** polarity

✔ Inherent Correlated Double Sampling (**CDS**)

Dark Current Cancellation



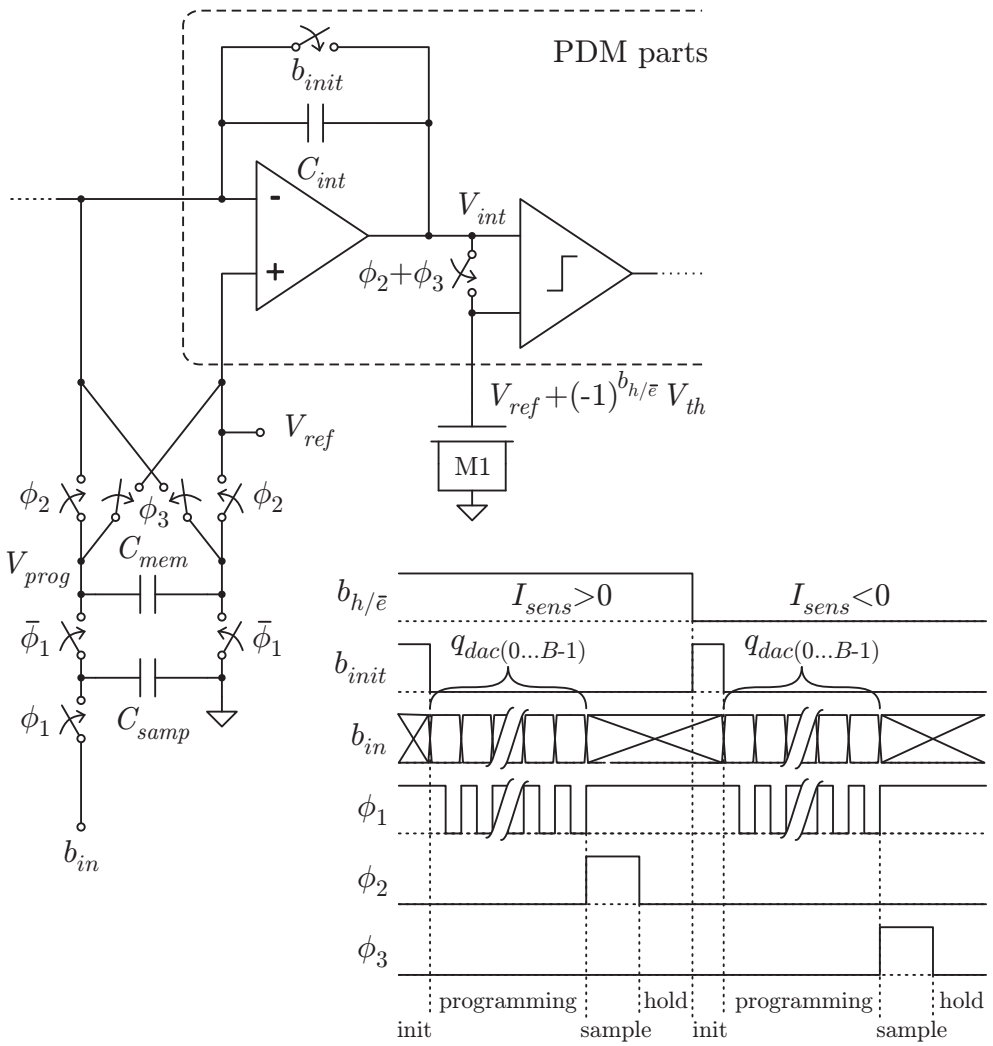


- Current copiers based I_{dark} **auto-calibration**

- ✔ Coarse + fine for **charge injection** compensation
- ✔ Composite switches for long **retention** time (up to 1s)
- ✔ Dual operation for $b_{h/\bar{e}}$
- ✔ ADC PDM parts **reused**
- ✔ CTIA **offset** independent

Gain Programmability

- FPN compensation via individual V_{th} control:



- SC **DAC** based
- ✔ Serial **program-in** during read-out (no speed losses), for $C_{samp} \equiv C_{mem}$:

$$V_{prog} = V_{DD} \sum_{i=0}^{B-1} \frac{q_{dac}(i)}{2^{B-i}} \geq 0$$

- ✔ **Polarity + storage**:

$$V_{th} = \frac{C_{mem}}{C_{int}} V_{DD} \sum_{i=0}^{B-1} \frac{q_{dac}(i)}{2^{B-i}}$$

- ✔ ADC PDM **reused**
- ✔ Built-in **test** through charge injection...

Local Bias Generation

- I_{bias} and V_{ref} DPS **generator**
- PTAT core M1-M4 in weak inversion saturation:

$$V_{bias} = U_t \ln P$$

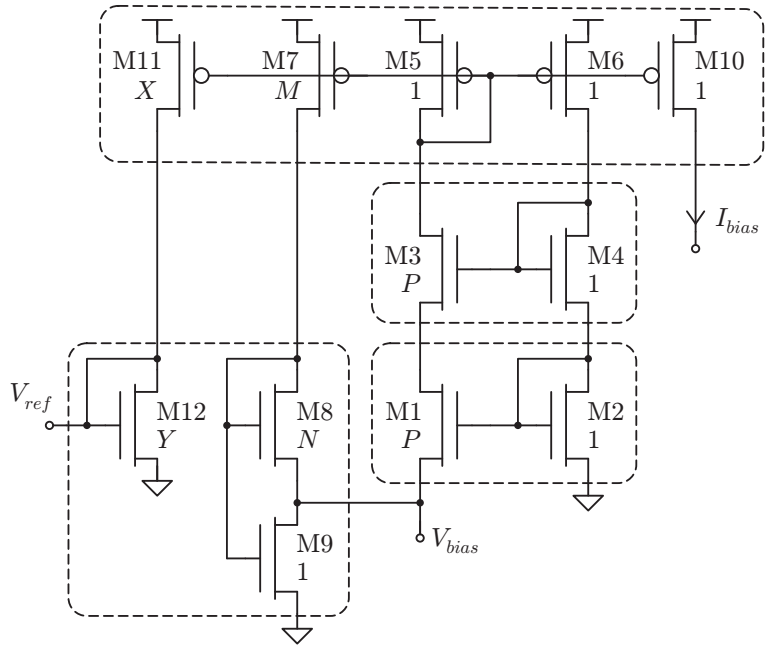
- M8 and M9 in strong inversion saturation and conduction:

$$I_{bias} = QI_{S9} \quad I_{S9} = 2n\beta_9 U_t^2$$

$$Q = \left[\frac{\ln P}{2(M+1)} \left(\sqrt{\frac{M}{N}} + \sqrt{\frac{M}{N} + M + 1} \right) \right]^2$$

- M12 in strong inversion saturation:

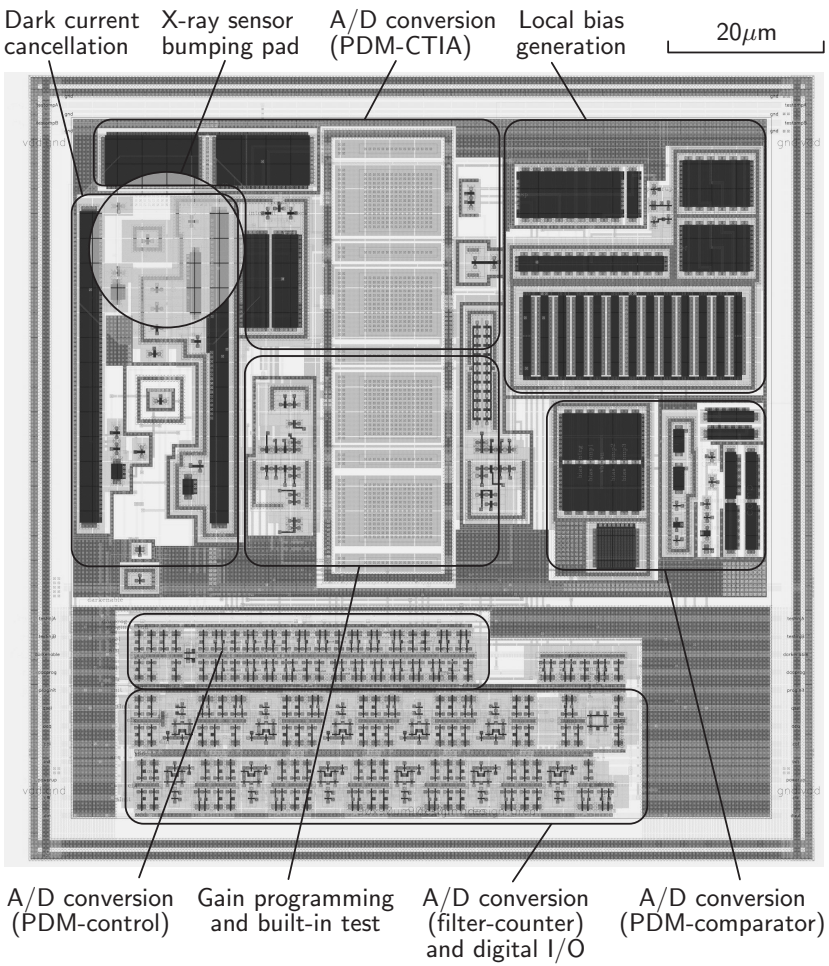
$$V_{ref} = 2n\sqrt{\frac{QX}{Y}}\, U_t + V_{TO}$$



- ✔ I_S-based I_{bias} for **low dependence** on technology
- ✔ V_{ref} **thermal compensation**

CMOS Integration

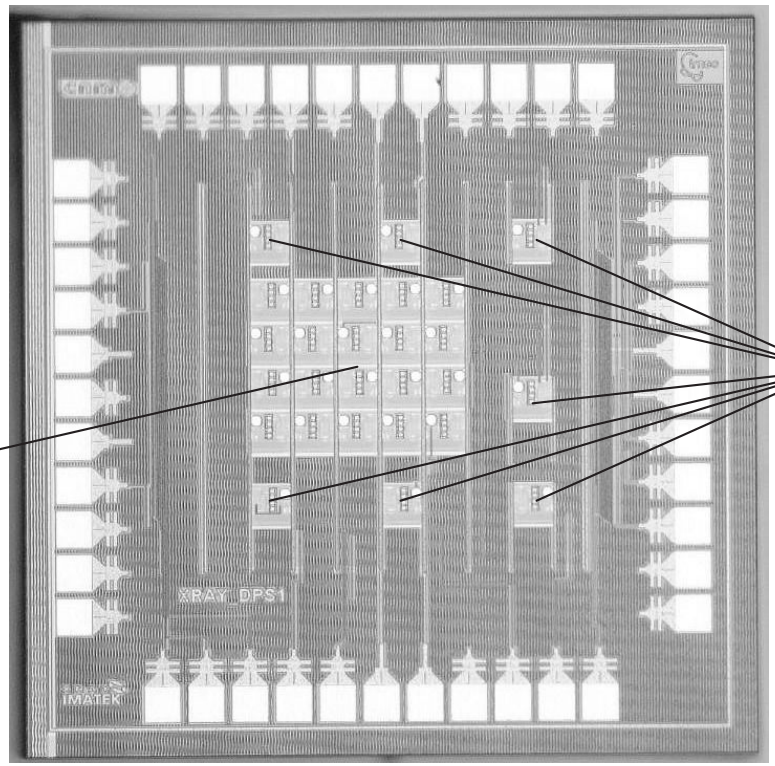
- **DPS cell** layout:



- I_{bias}=250nA
- V_{ref}=670mV
- C_{int}, $C_{reset/CDS}$, C_{mem} and C_{samp}=100fF
- B=(10+1)bit
- 40mV$< V_{th} <$400mV

CMOS Integration

- **DPS test** oriented circuit:



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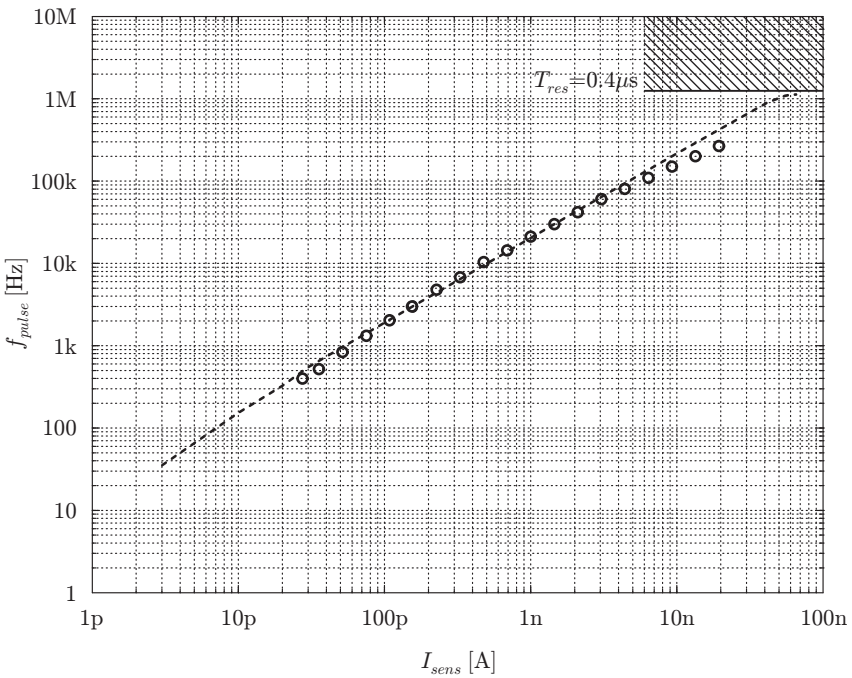
- Single transistor I_{sens} **emulators**
- **0.18μm 1P 6M triple-well** CMOS technology

Experimental Results

- **PDM** transfer function:



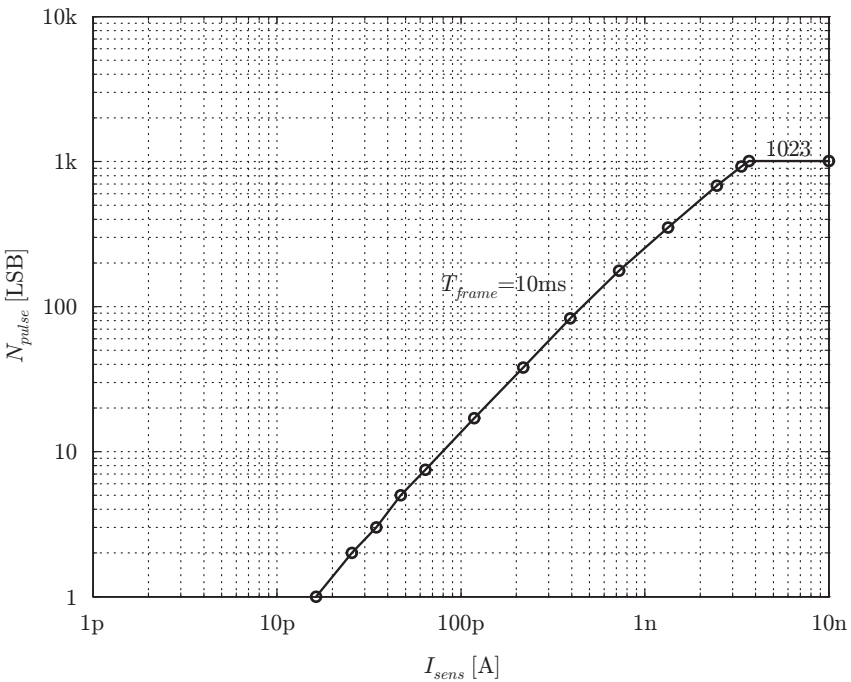
. . . for V_{th}=0.4V ('00010010110').

- **DPS performance**:

Parameter	Value	Units
Supply voltage	1.8	V
Dark current range	0.01 to 20	nA
Transfer gain	<1/50	LSB/ke$^-$
Equivalent noise charge	1.5 to 18	ke$^-_{rms}$
Integration time	**10 to 1000**	**ms**
Output dynamic range	10	bit
Crosstalk	<0.5	LSB
Program-in/read-out speed	50	Mbps
Static power consumption	**5**	**μW**
Bias mismatching ($\pm\sigma$)	<10	%
Silicon area	100×100	μm^2

Experimental Results

- **Overall** transfer function:



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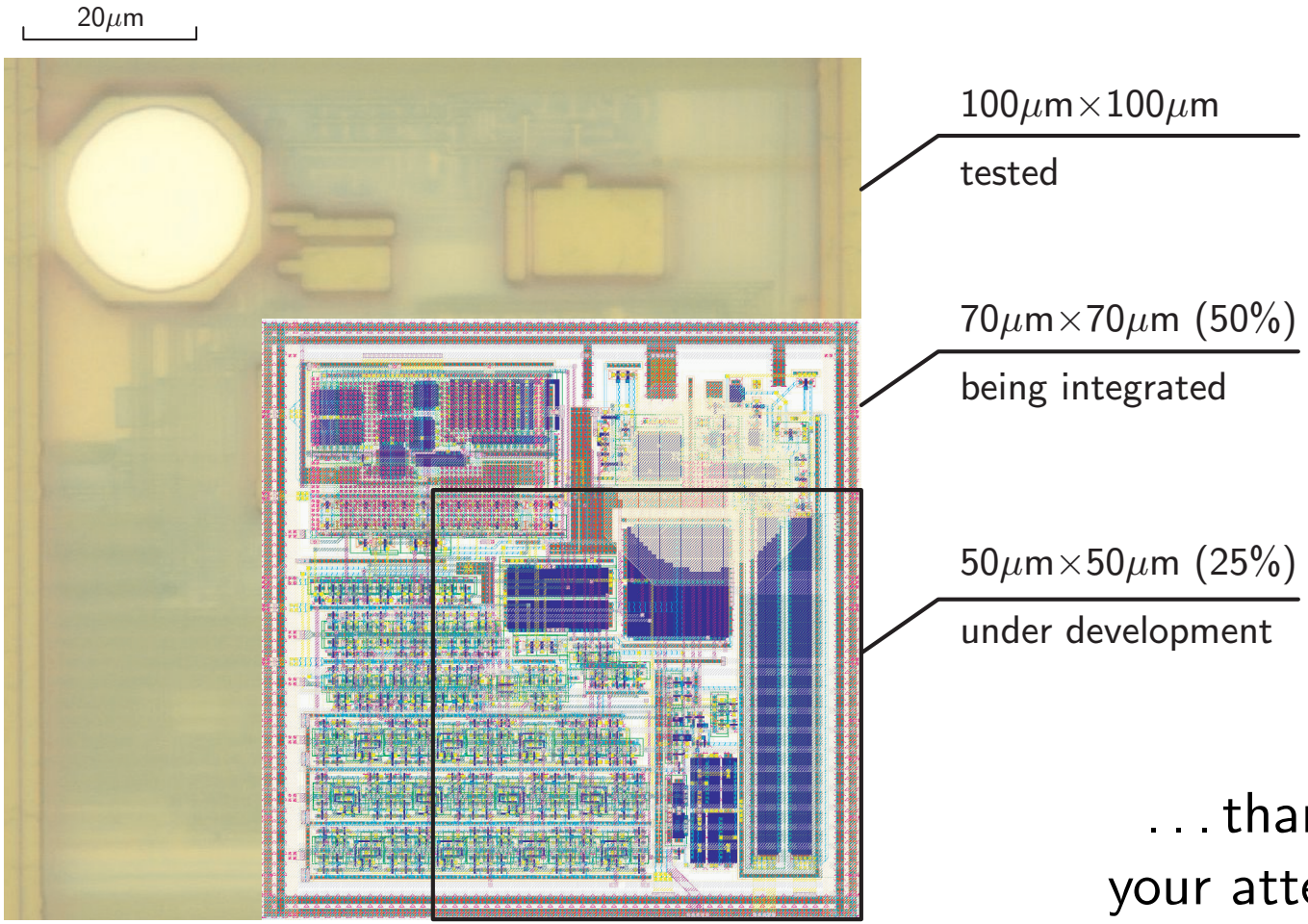
Conclusions

- Novel charge-integration DPS for **X-ray digital imaging**
- In-pixel **lossless A/D conversion**
- **Dark current** automatic compensation
- **FPN cancellation** through digital gain programmability
- **Built-in test** capabilities
- Local analog bias and references for **low crosstalk**
- **Very low-power** CMOS circuits
- Preliminary test results in **0.18μm 1P 6M triple-well CMOS technology**

Future Work

- **Scaling**, **scaling** and **scaling**!



. . . thanks for your attention.