A Sub-μW Fully Programmable CMOS DPS for Uncooled Infrared Fast Imaging

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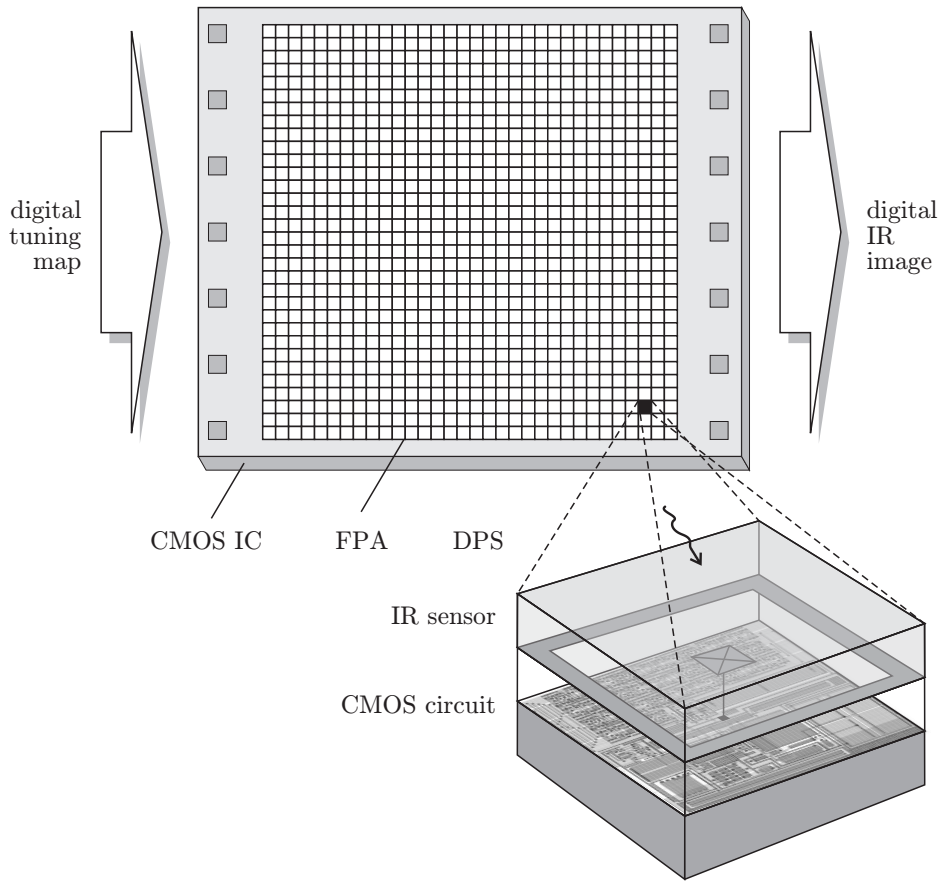
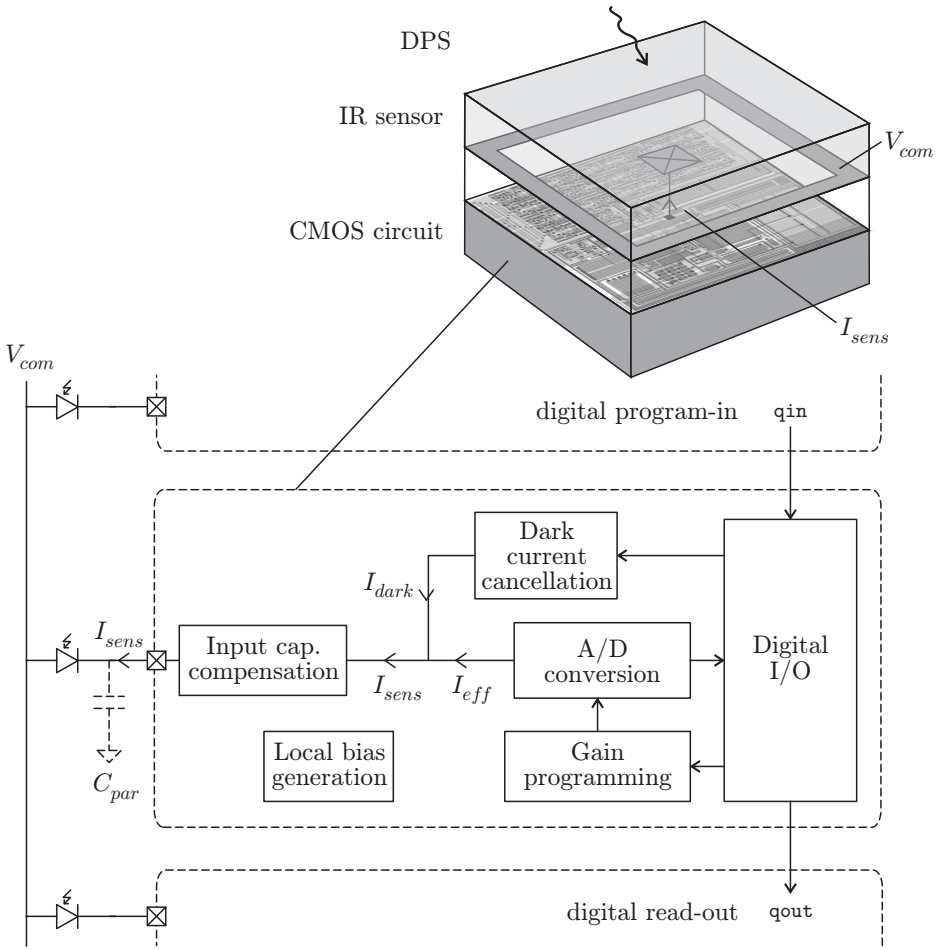
Scenario

- PbSe promising technology for **uncooled IR fast** imaging
- CMOS **post-processing** & **hybrid** solutions
- DPS specs:
  - X Large sensor **capacitance**
  - X High **dark current**
  - ✓ **FPN** compensation
  - ✓ Digital **only** I/O
  - ✓ Very **low-power**



DPS Architecture Proposal

- Input **capacitance** compensation
- **Low-noise** processing:
  - + Built-in A/D conversion
  - + Quiet digital signaling
- **FPN** digital cancellation:
  - + Offset (dark current)
  - + Gain (ADC LSB)
- Inter-pixel **low-crosstalk**:
  - + Digital read-out/program-in
  - + Local analog references



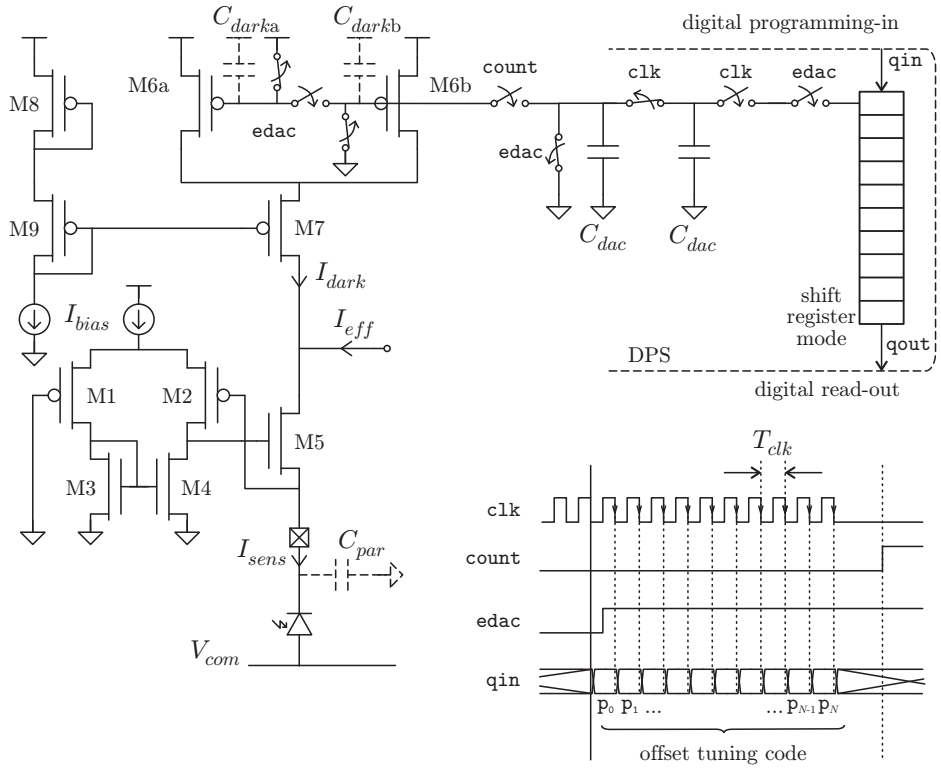
CMOS Realization

- Low input **impedance**:

$$r_{in} \simeq \frac{gm_{d1,2} + gm_{d3,4}}{gm_{g5}\, gm_{g1,2}}$$

$$= \frac{n_N\, n_P\, U_t^2}{I_{sens}} (\lambda_N + \lambda_P)$$

$r_{in} < \text{k}\Omega$ allowing $C_{par} \sim$ pF



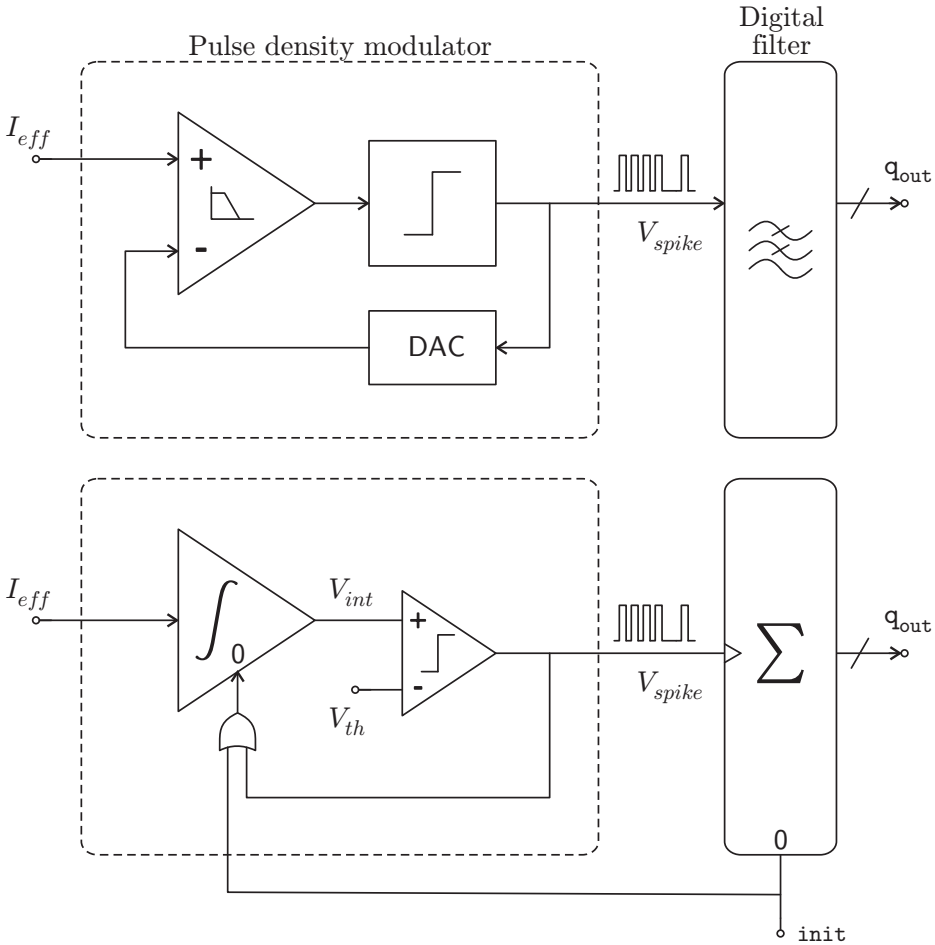
- Dark current **DAC**:

$$V_{GB6} = V_{DD} \left[\frac{C_{dark}}{C_{dark} + C_{dac}} \left(\frac{1}{2} + \frac{C_{dac}}{C_{dark}} \sum_{i=1}^{N} \frac{\mathtt{p}_{N-i}}{2^i} \right) - 1 \right]$$

... stored in **analog memory** $2C_{dac} + C_{darka} + C_{darkb}$ for next two frames.

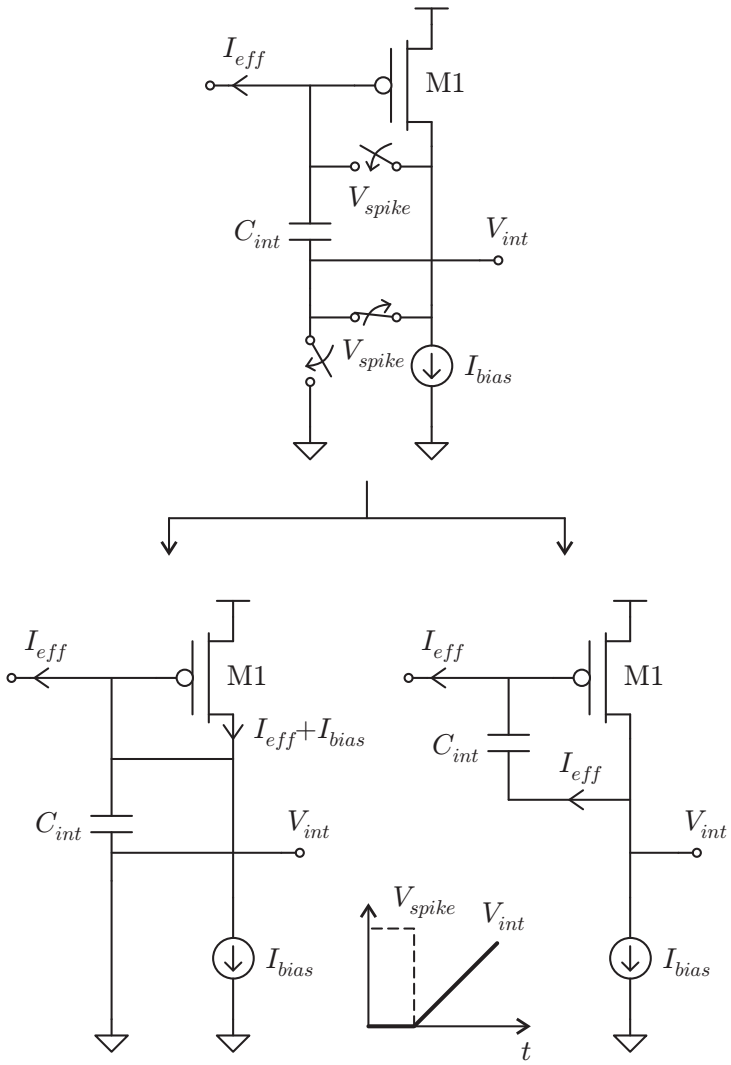
ADC Architecture

- Alternatives:
  - X Direct (flash)
  - X Algorithmic (success.approx.)
  - ✓ **Predictive** ($\Sigma\Delta$)
- **Feedback** = relaxed specs for analog parts
- **Pulse modulator** + digital low-pass **filter**
  - \+ PWM, time to first spike
  - \+ **PDM**, spike counting:
    - ✓ No external **clocks**
    - ✓ **Switching** power $\propto$ signal amplitude



CMOS Blocks

- Compact **CTIA** with **CDS**

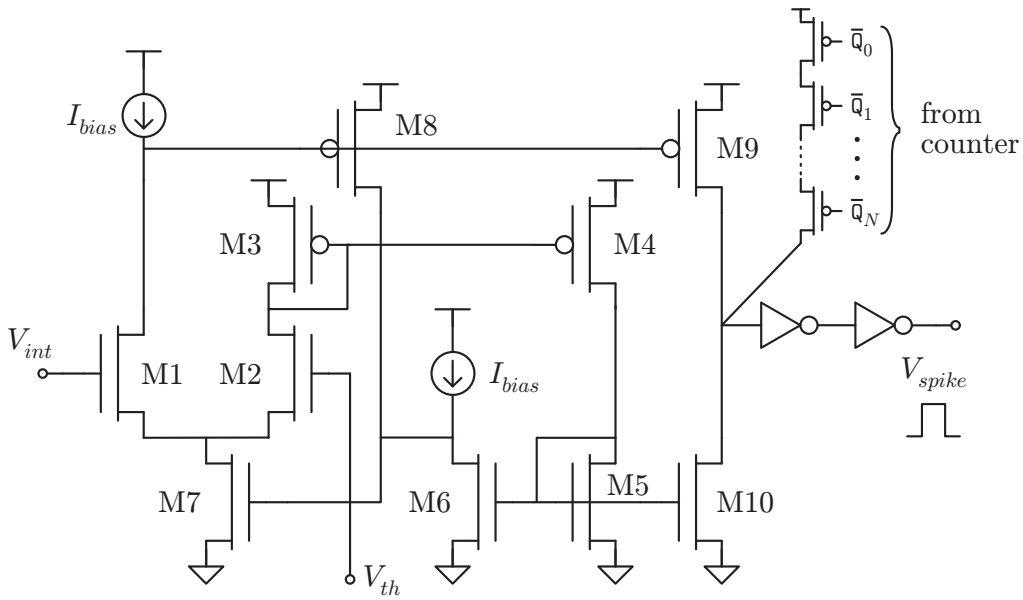


CMOS Blocks

- Compact **CTIA** with **CDS**
- Class-AB **comparator**

$$f_{spike} = \frac{1}{C_{int}\, V_{th}} I_{eff}$$

. . . with **overflow** detector



CMOS Blocks

- Compact **CTIA** with **CDS**
- Class-AB **comparator**

$$f_{spike} = \frac{1}{C_{int}\, V_{th}} I_{eff}$$

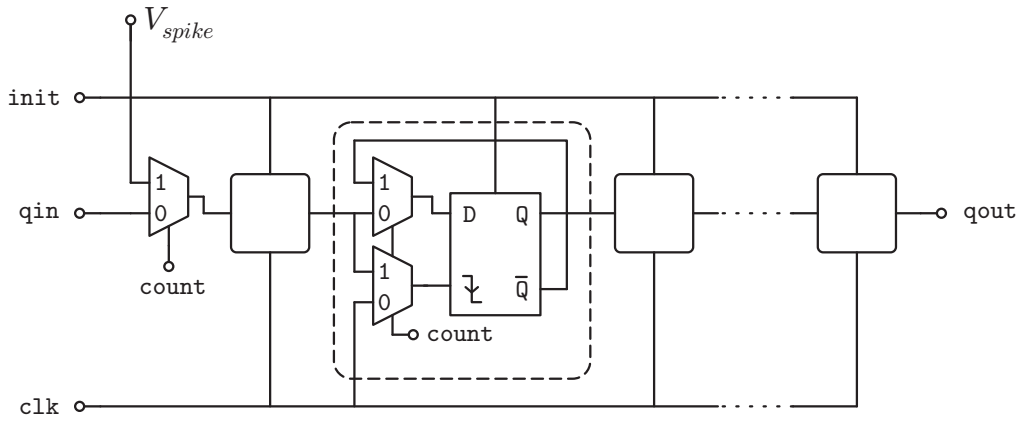
. . . with **overflow** detector

- Digital **counter**

$$\texttt{wout} = \lfloor n_{out} \rfloor$$

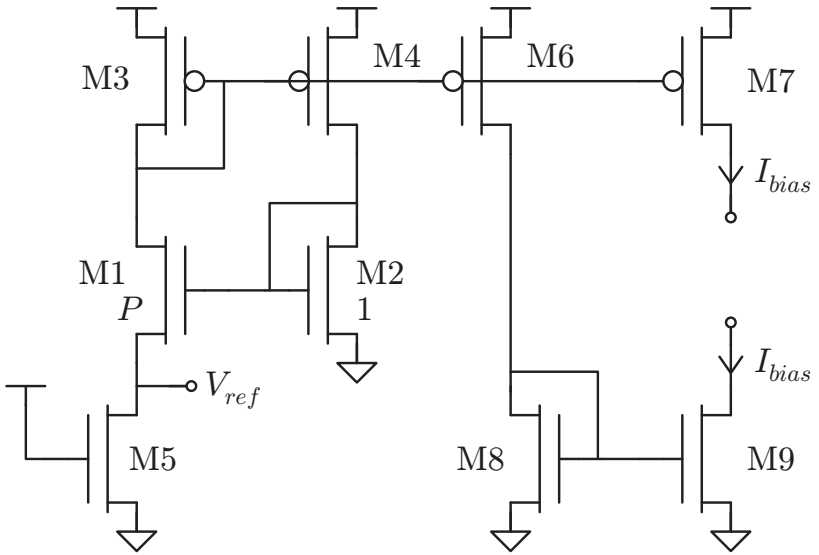
$$n_{out} = \frac{f_{spike}}{f_{frame}} = \frac{T_{frame}}{C_{int}\, V_{th}} I_{eff}$$

. . . reused as **serial I/O**



Built-in Bias Generator

- Reduced inter-pixel **crosstalk**
- FPA low-**connectivity** (number of metal layers)



- **PTAT** core in weak inversion saturation:

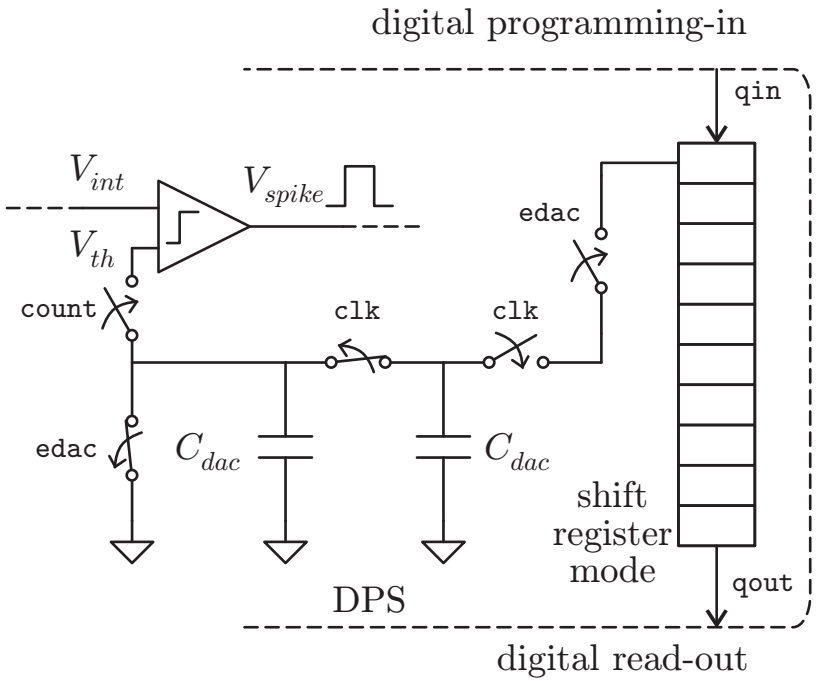
$$V_{ref} = U_t \ln(P)$$

- Large M5 overdrive $\Rightarrow$ process **corners** reduced to β
- Technology **mismatching** due to P (M1-M4)
- MOSFET **load** in strong inversion conduction:

$$I_{bias} \simeq \beta \left(\frac{W}{L}\right)_5 (V_{DD} - V_{TO})\, V_{ref}$$

Digital Programming

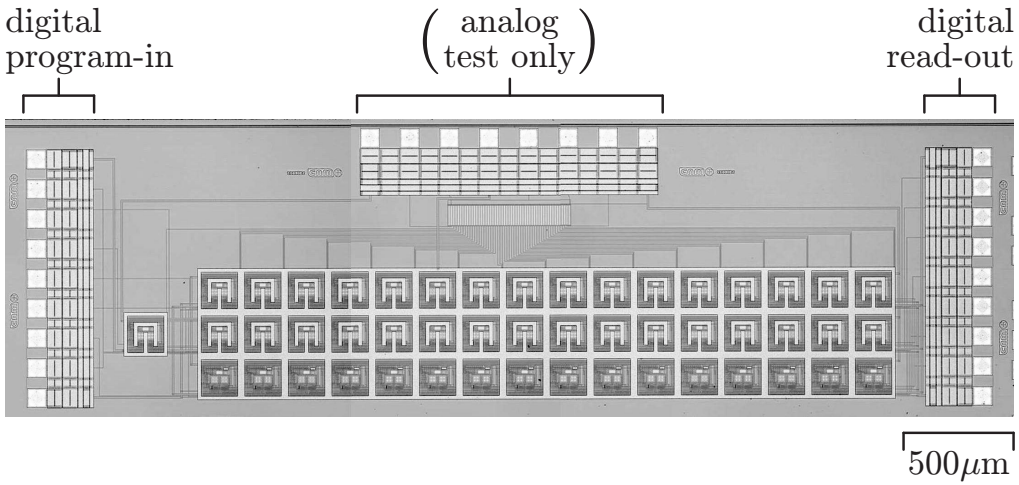
- **Individual** pixel gain tuning through PDM V_{th}
- Program-in + read-out at **no speed costs**
- **Full** FPN compensation
- Optional spatial **AGC**



- **Alternate** frame programming
- DAC can be **shared** with I_{dark}

Electrical Test Vehicle

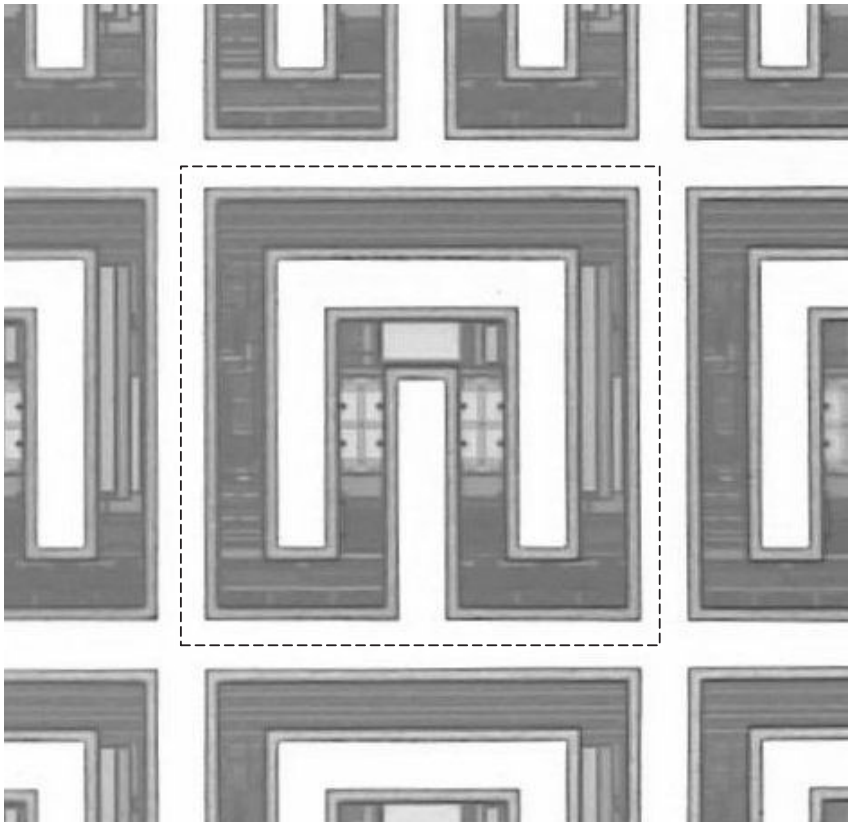
- 0.35μm 2P 4M standard CMOS technology
- PbSe IR sensor **emulators**
- **Design parameters**:
  C_{int}=500fF
  N=10
  P=12
  I_{bias}=60nA
  C_{dac}=300fF



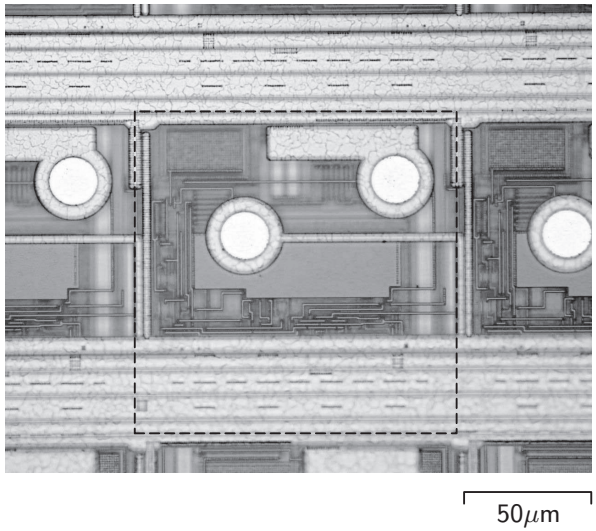
- Overall **performance**:

Description	Value	Units
Dark current range	0.5-2	μA
Max. input capacitance	15	pF
Signal range	1-1000	nA
Integration time	1	ms
Crosstalk	<0.5	LSB
Programming/read-out speed	10	Mbps
Supply voltage	3.3	V
Static power consumption	**<1**	μW
Biasing deviations ($\pm\sigma$)	$\pm$15	%

DPS Realizations



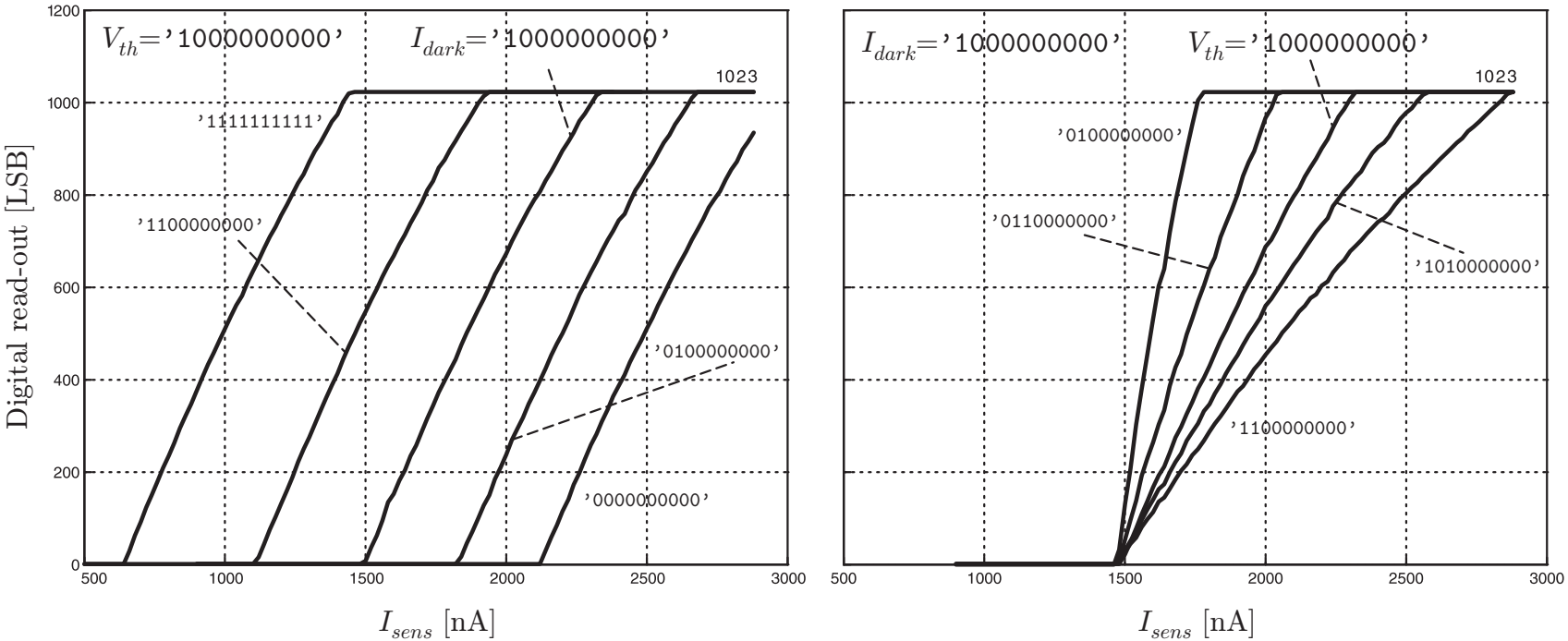
CMOS **post-processing**
(200μm$\times$200μm)



Hybrid bump bonding
(130μm$\times$130μm)

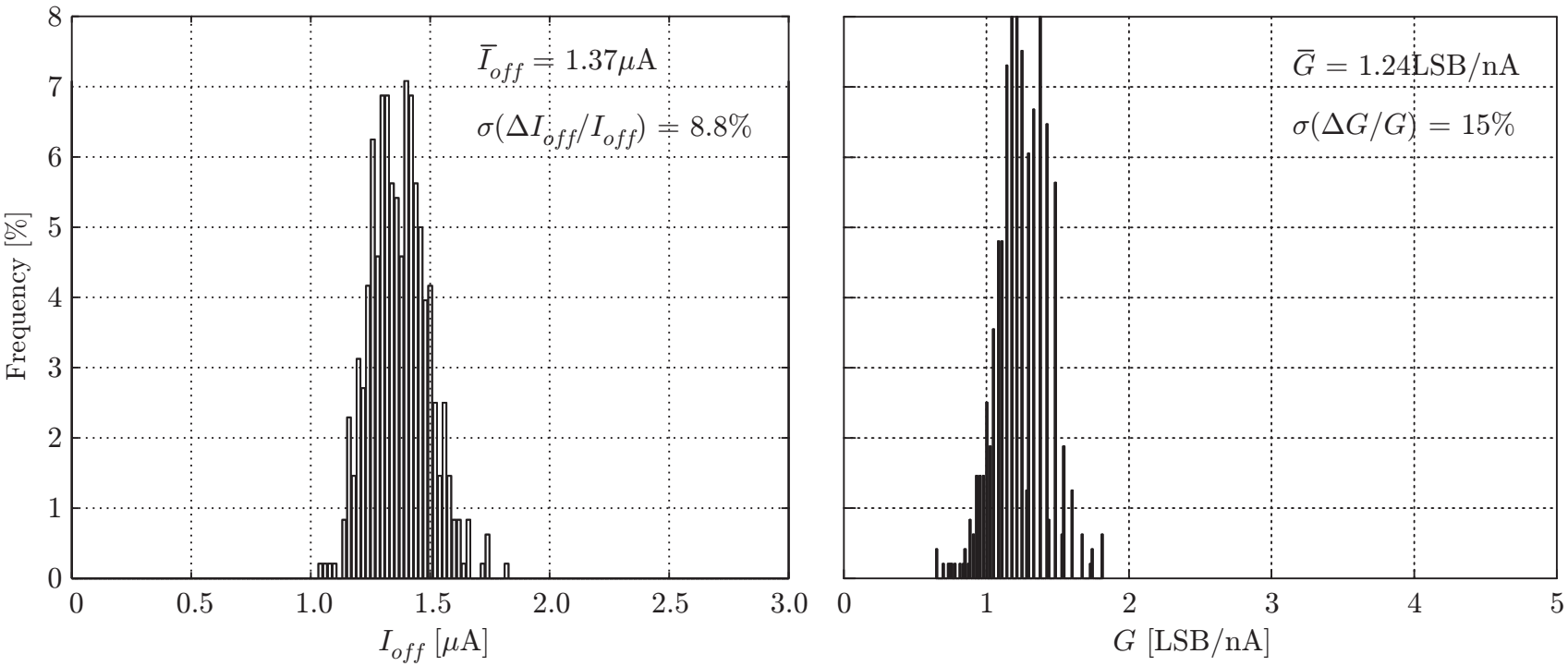
A/D Transfer Functions

- Full programmable in **offset** (I_{dark}) and **gain** (V_{th}):



Statistical FPN

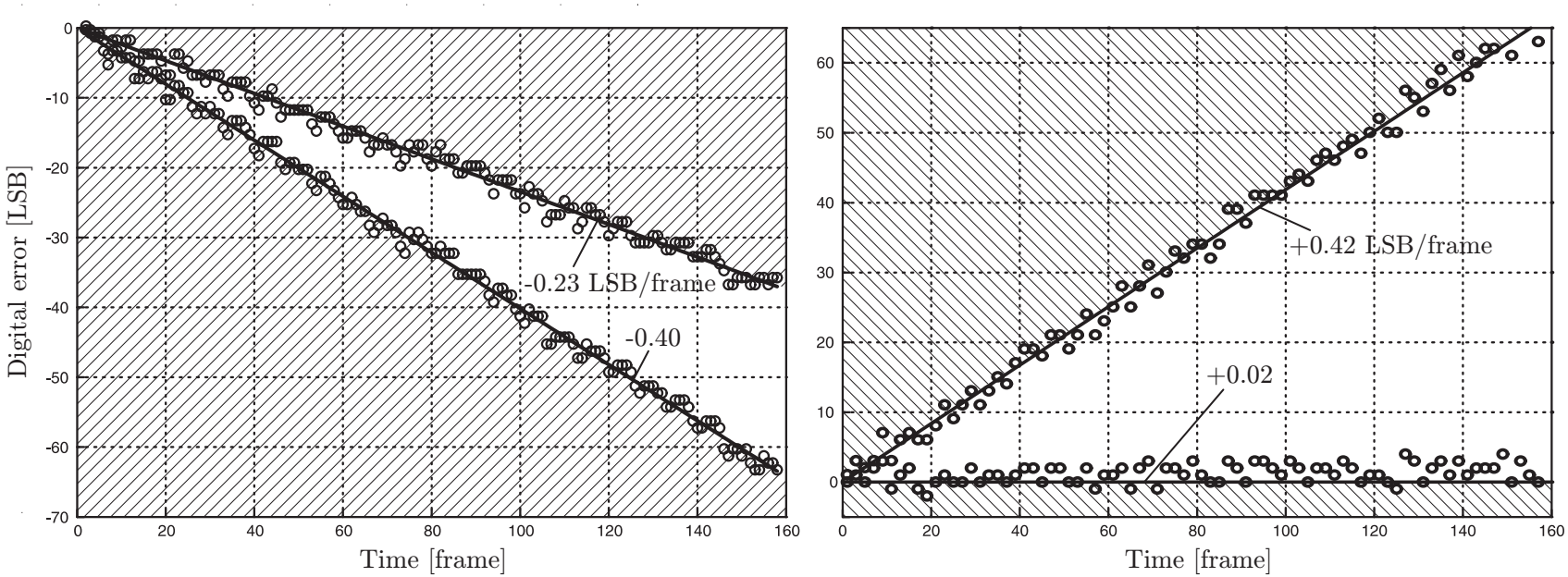
- From **480** DPS cells programmed at I_{dark}='1000000000' and V_{th}='1000000000':



. . . showing the motivation for the offset and gain **tuning**!

Analog Memory Retention

- Range of I_{dark} and V_{th} memory **leakage** rate inside the DPS:



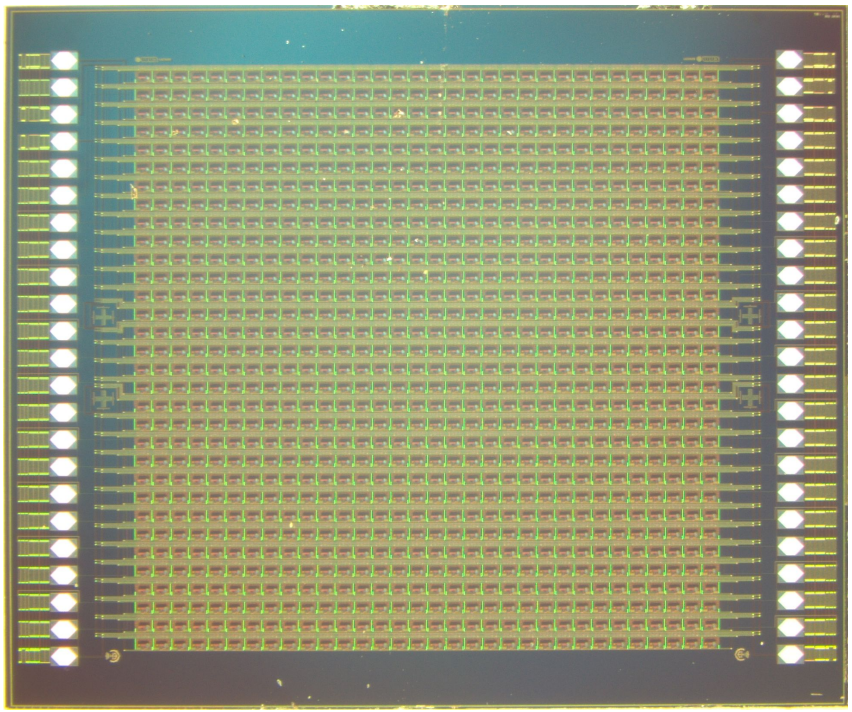
. . . retention times are large enough for **alternate** frame programming!

Conclusions

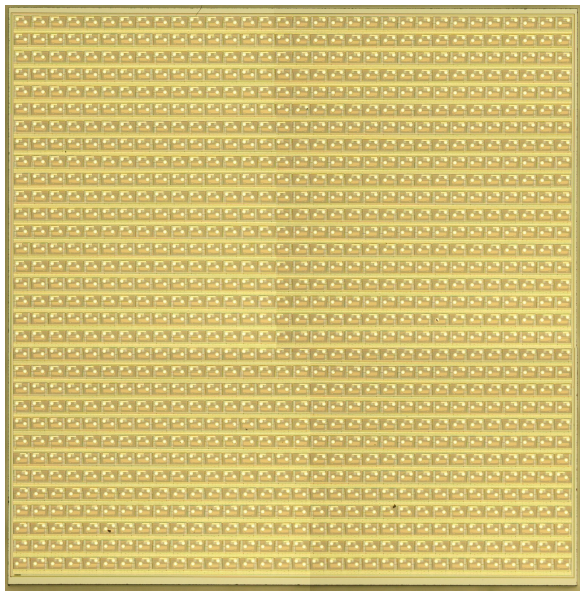
- Novel DPS for **uncooled IR fast** imaging.
- Sensor **capacitance** and **dark current** compensation.
- Compact **spike-counting** A/D converter with **CDS**.
- Digitally controlled **full FPN** compensation.
- Local analog bias **generator**.
- **Very low-power** CMOS circuits.
- Monolithic and hybrid DPS in **0.35μm 2P 4M**.
- Electrical **experimental** results.

Current Status

- 32×32 135μm-pitch **FPAs** ready for PbSe and optical test:



by CMOS **post-processing**



by **modular** flip-chip

- Working on **next generation**: further down scaling with **AER**...