A Sub-1μW Fully Programmable CMOS DPS for Uncooled Infrared Fast Imaging

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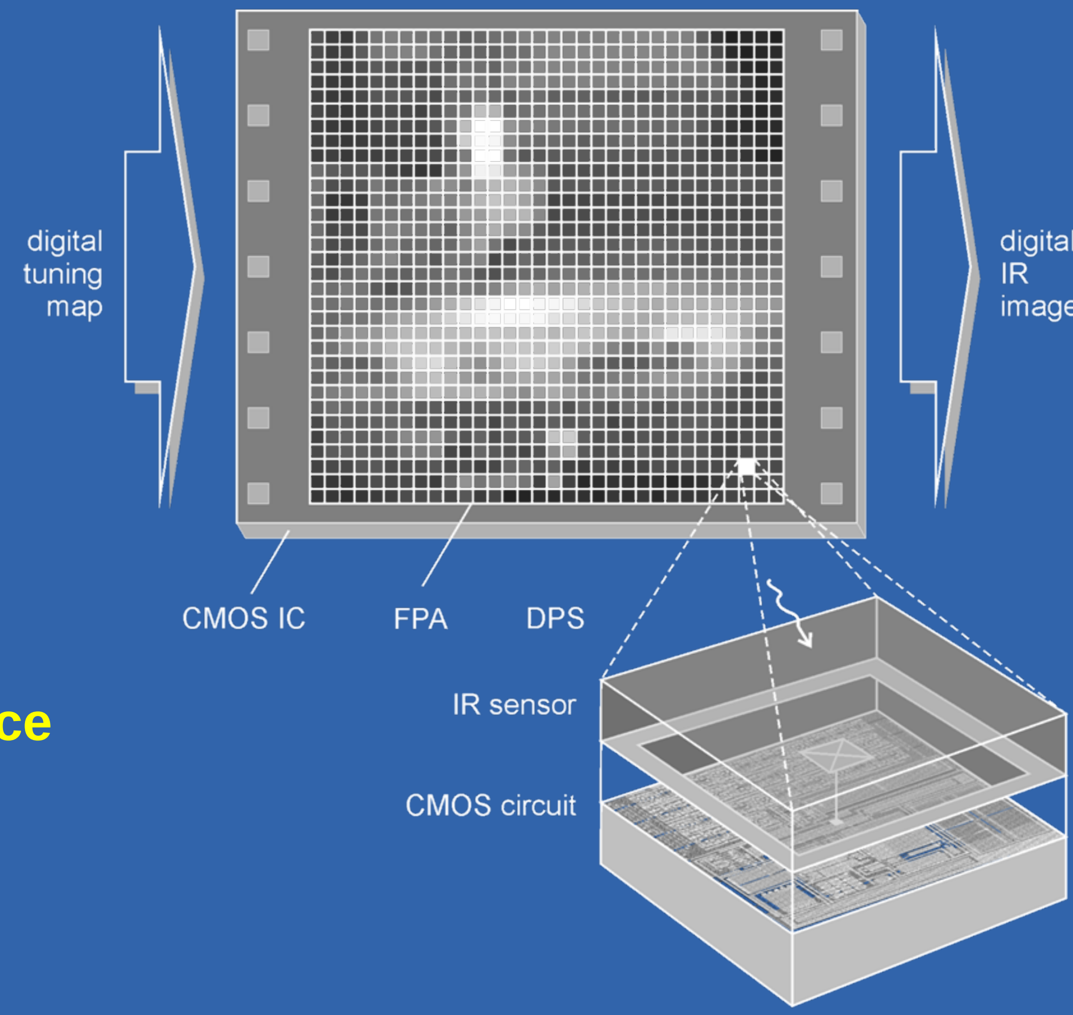
1 Introduction

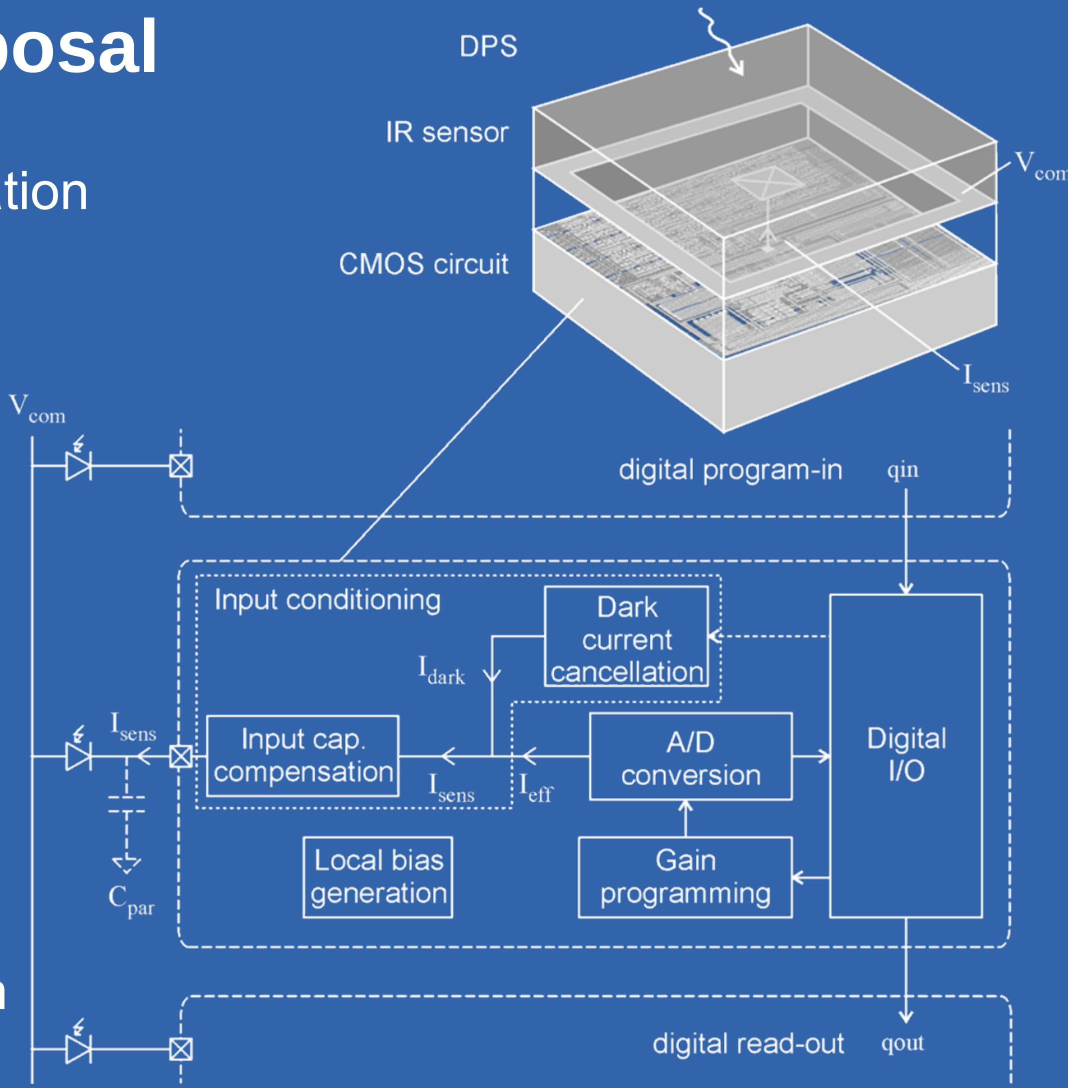
Scenario

- **Uncooled IR fast** imaging: **PbSe** technology
- CMOS **post-processing** & **hybrid** solutions
- DPS specs:
  - ✗ Large sensor **capacitance**
  - ✗ High **dark current**
  - ✓ **FPN** compensation
  - ✓ **Digital** only I/O
  - ✓ Very **low-power**



DPS Architecture Proposal

- **Input capacitance** compensation
- **Low-noise** processing:
  - Built-in A/D conversion
  - Quiet digital signaling
- **FPN** digital cancellation:
  - Offset (dark current)
  - Gain (ADC LSB)
- Inter-pixel **low-crosstalk**:
  - Digital read-out/program-in
  - Local analog references



CMOS Realization

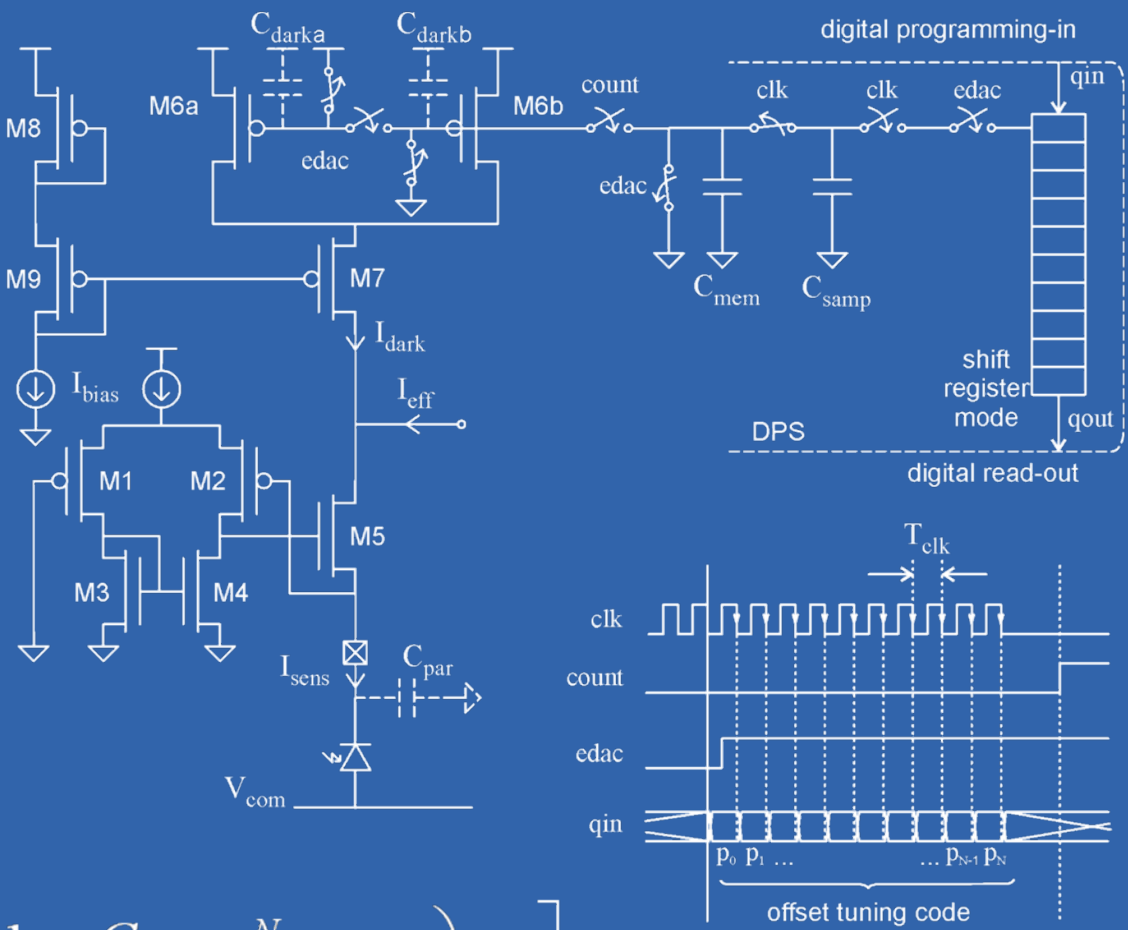
- **Low input** impedance:

$$r_{in} \simeq \frac{g_{md1,2}+g_{md3,4}}{g_{mg5}\,g_{mg1,2}}$$

$$= \frac{n_N n_P U_t^2}{I_{sense}}\left(\lambda_N+\lambda_P\right)$$

$r_{in} <$ kΩ allowing $C_{par} \sim$ pF

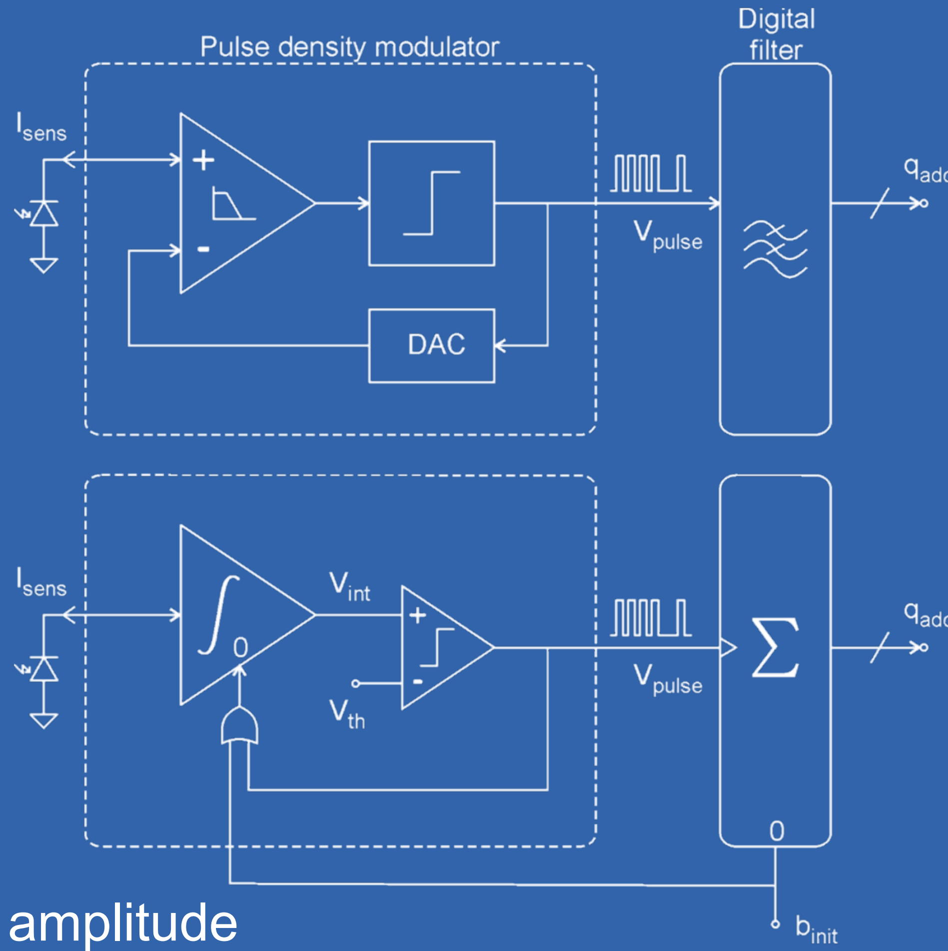
- Dark current **DAC** (analog memory):



$$V_{GB6} = V_{DD}\left[\frac{C_{dark}}{C_{dark}+C_{DAC}}\left(\frac{1}{2}+\frac{C_{DAC}}{C_{dark}}\sum_{i=1}^{N}\frac{p_{N-i}}{2^{i}}\right)-1\right]$$

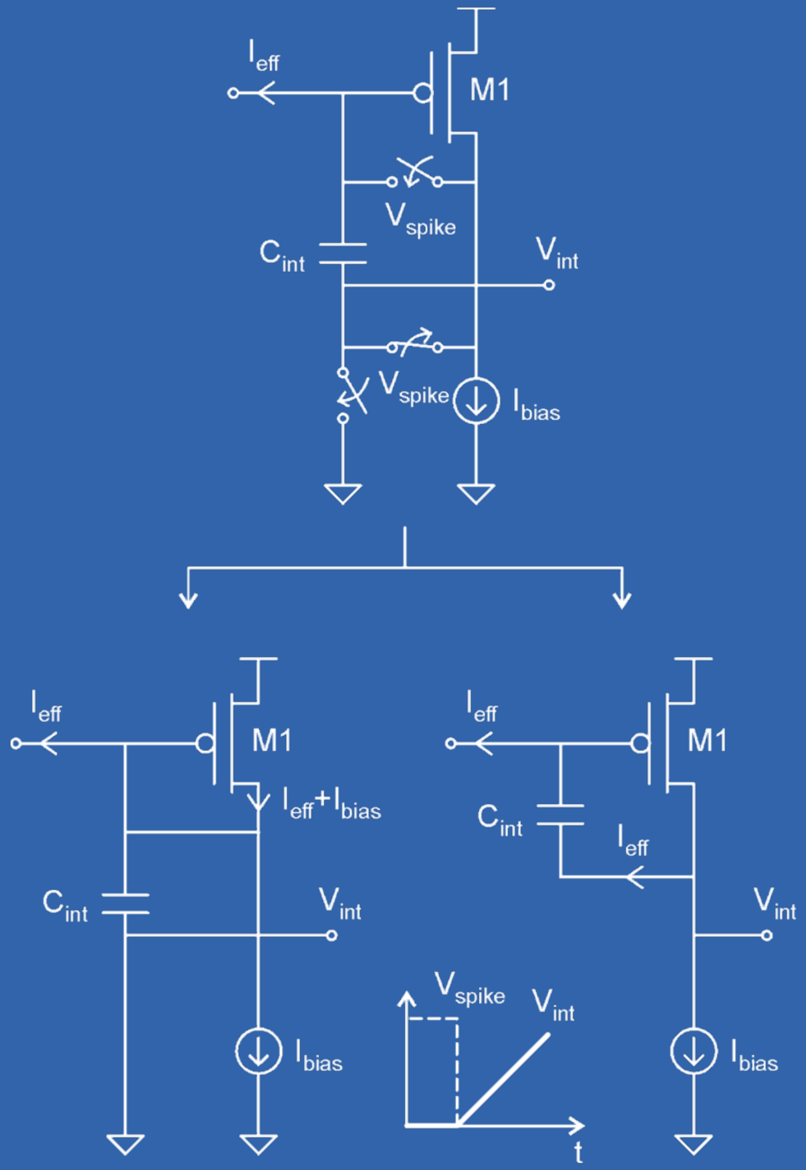
ADC Architecture

- Alternatives:
  - ✗ Direct (flash)
  - ✗ Algorithmic (success. approx.)
  - ✓ **Predictive** (ΣΔ)
- **Feedback** = relaxed analog specs
- **Pulse modulator** + digital LPF:
  - PWM, time to first spike
  - **PDM**, spike counting:
    - ✓ **No external** clocks
    - ✓ Switching **power** –> signal amplitude



CMOS Blocks

- Compact **CTIA** with **CDS**

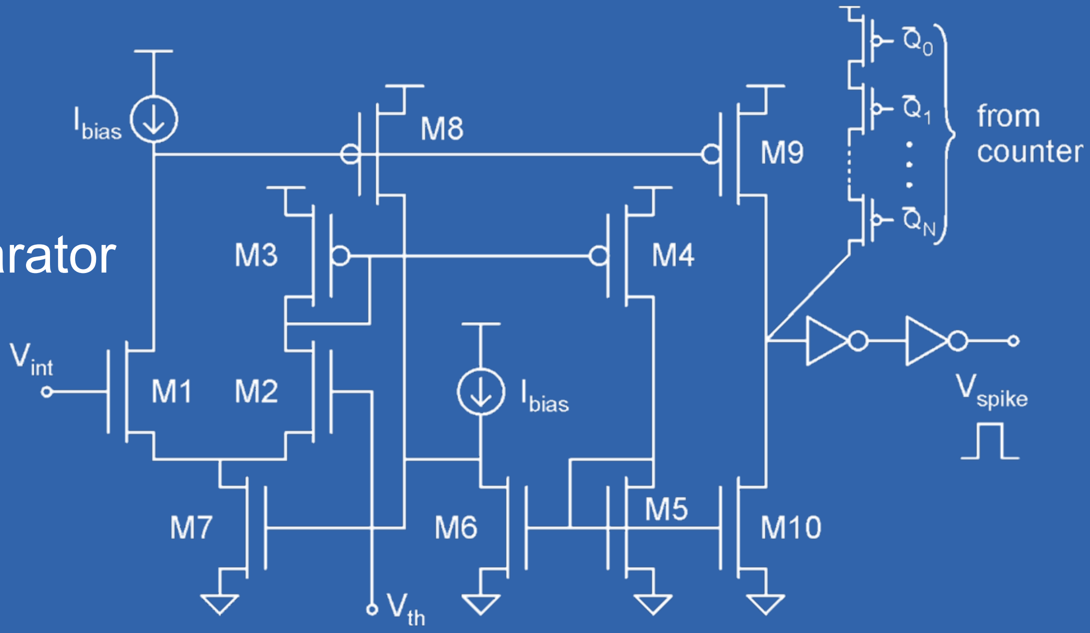


CMOS Blocks

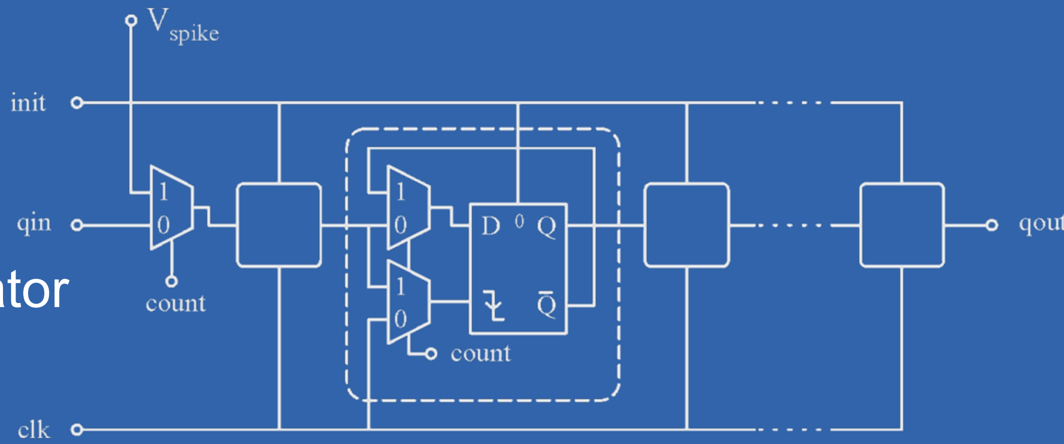
- Compact **CTIA** with **CDS**
- **Dynamically-biased** comparator

$$f_{spike} = \frac{1}{C_{int} V_{th}} I_{eff}$$

…with **overflow** detector



CMOS Blocks



- Compact **CTIA** with **CDS**
- **Dynamically-biased** comparator

$$f_{spike} = \frac{1}{C_{int} V_{th}} I_{eff}$$

…with **overflow** detector

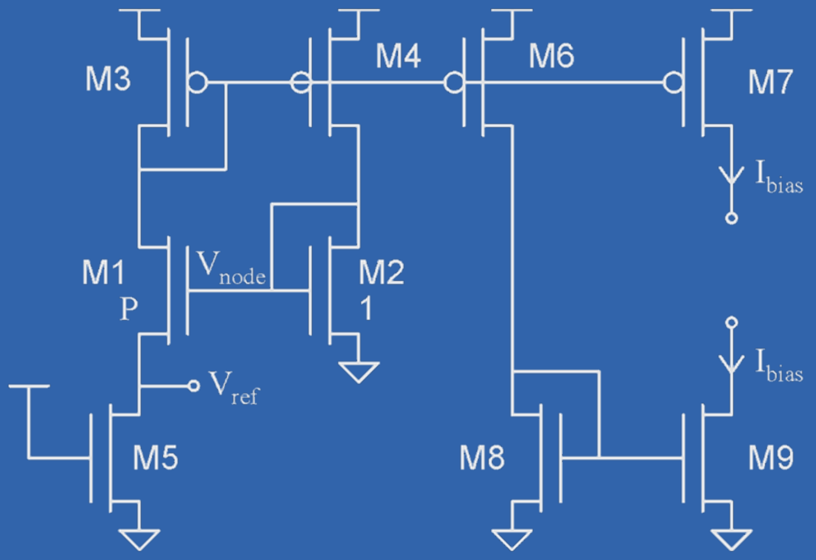
- Digital **counter**

$$\mathbf{wout} = \lfloor n_{out} \rfloor$$

$$n_{out} = \frac{f_{spike}}{f_{frame}} = \frac{T_{frame}}{C_{int} V_{th}} I_{eff}$$

…reused as **serial I/O**

Built-in Bias Generator



- **Reduced** inter-pixel **crosstalk**
- FPA **low-connectivity** (num. metal layers)
- **PTAT** core in weak inversion saturation:

$$V_{ref} = U_t \ln(P)$$

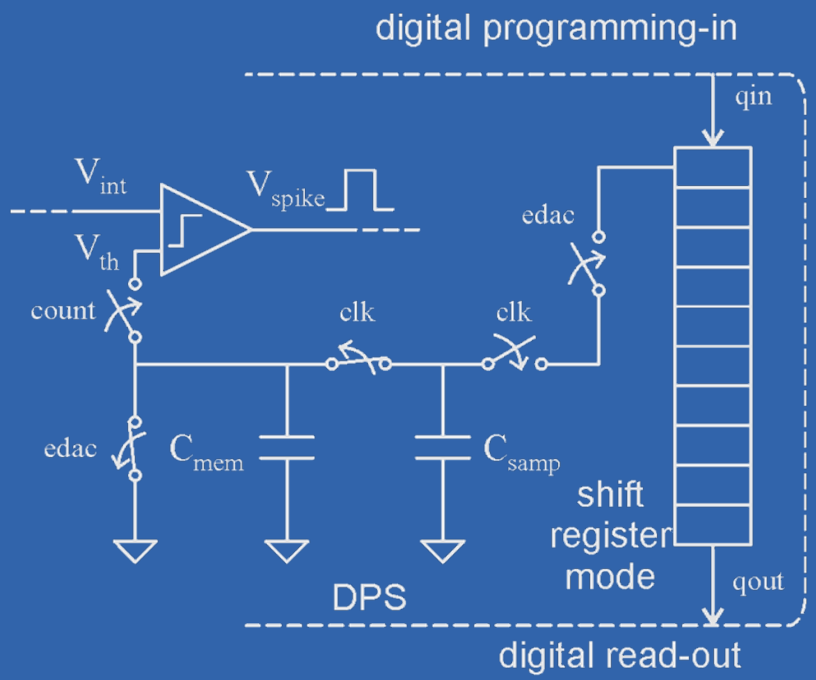
- MOSFET **load** in strong inversion conduction:

$$I_{bias} \simeq \beta \left(\frac{W}{L}\right)_5 \left(V_{DD} - V_{TO}\right) V_{ref}$$

- Large M5 overdrive: process **corners** reduced to ***β***
- Technology **mismatching** due to ***P*** (M1-M4)

Digital Programming

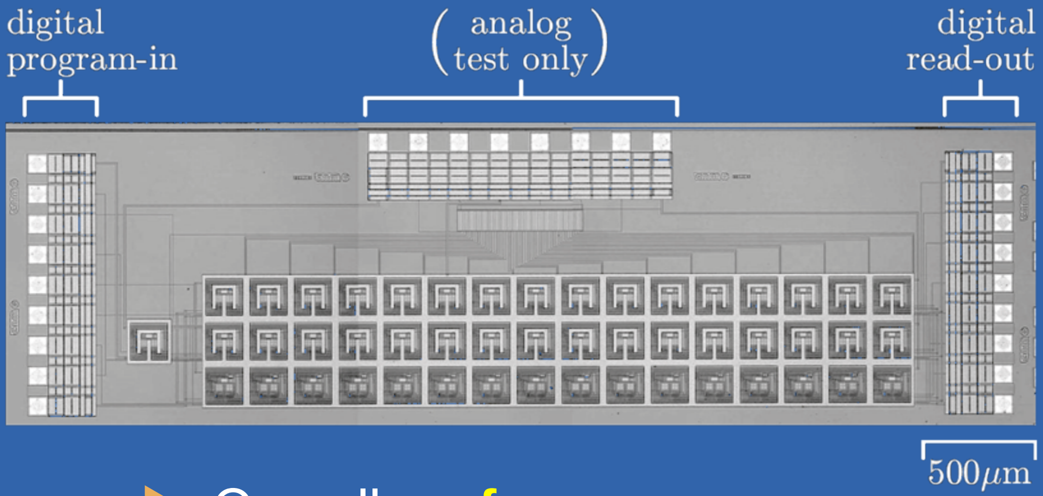
- **Individual** pixel gain **tuning** (PDM V_{th})
- Program-in + read-out at **no speed costs**
- **Full FPN** compensation
- Optional spatial **AGC**



- **Alternate** frame programming
- DAC can be **shared** with I_{dark}

Electrical Test Vehicle

- 0.35μm 2P 4M **standard CMOS** technology
- PbSe IR sensor **emulators**



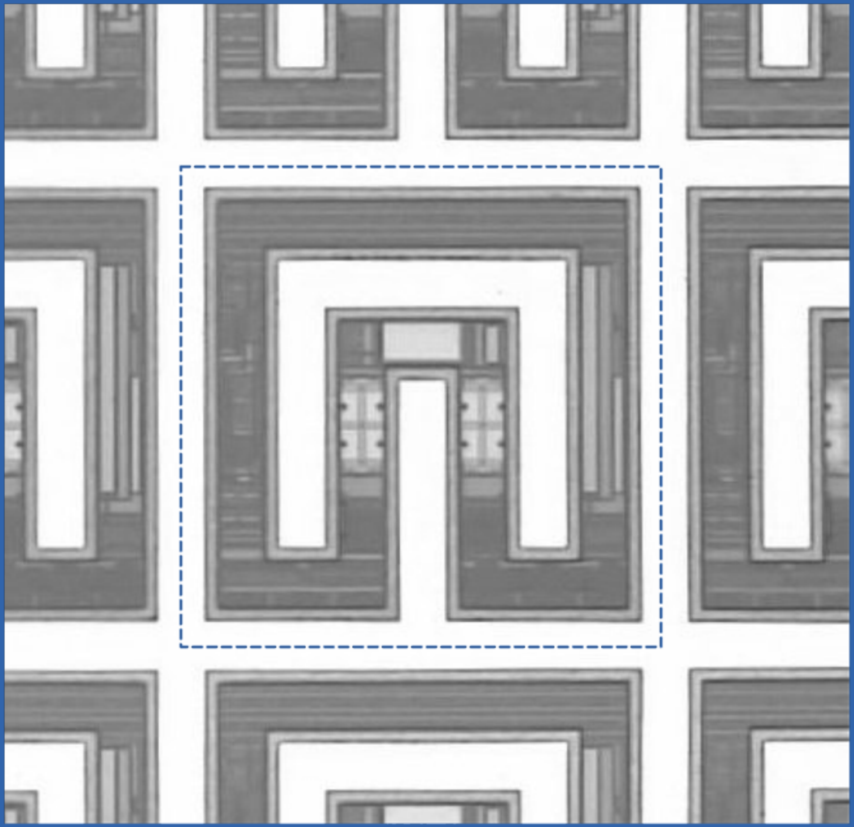
- **Design parameters**:

  C_{int}=500fF
  N=10
  P=12
  I_{bias}=60nA
  C_{dac}=300fF

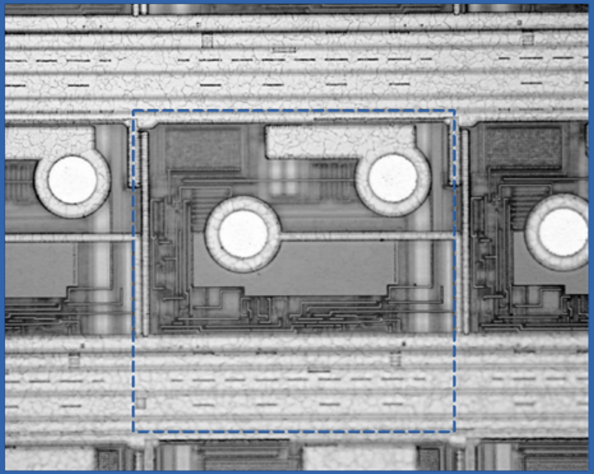
- Overall **performance**:

Description	Value	Units
Dark current range	0.5-2	μA
Max. input capacitance	15	pF
Signal range	1-1000	nA
Integration time	1	ms
Crosstalk	<0.5	LSB
Programming/read-out speed	10	Mbps
Supply voltage	3.3	V
Static power consumption	<1	μW
Biasing deviations (±σ)	±15	%

DPS Releases



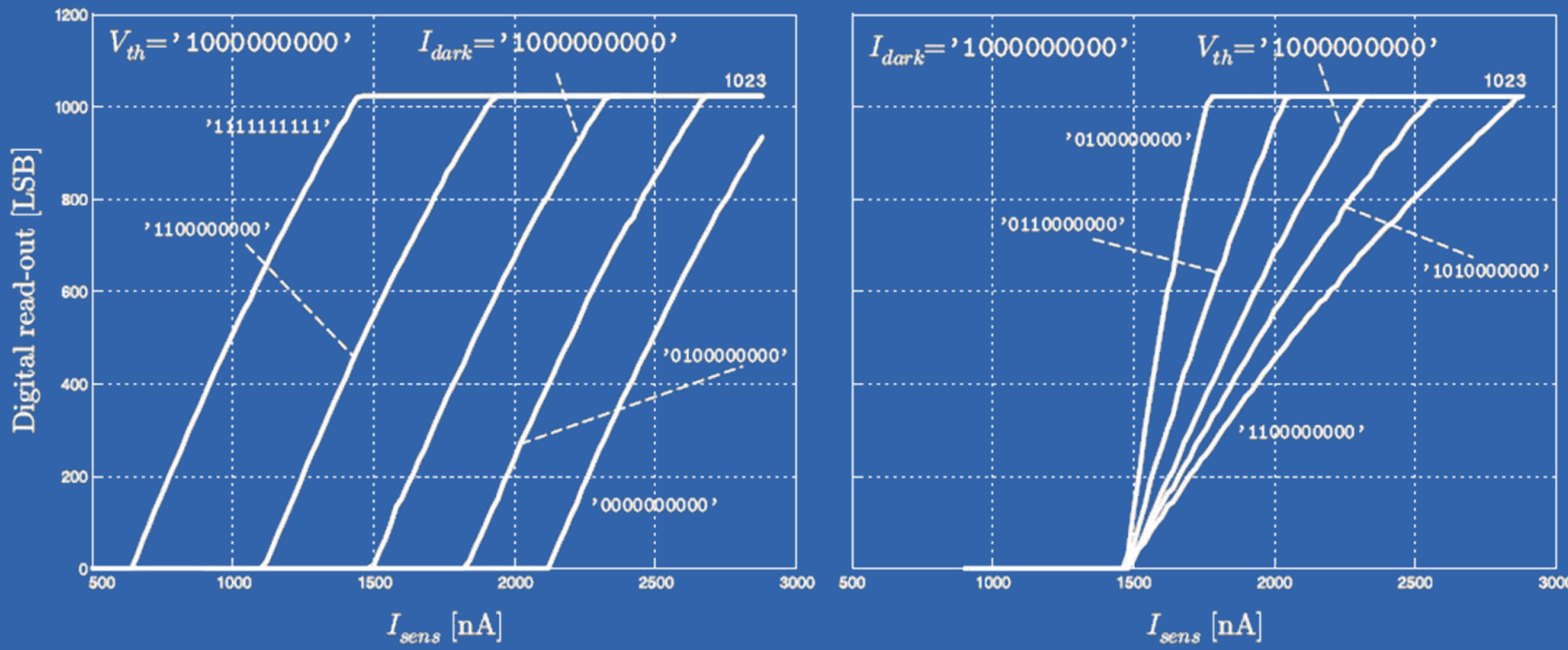
CMOS **post-processing**
(200μm×200μm)



Hybrid bump bonding
(130μm×130μm)

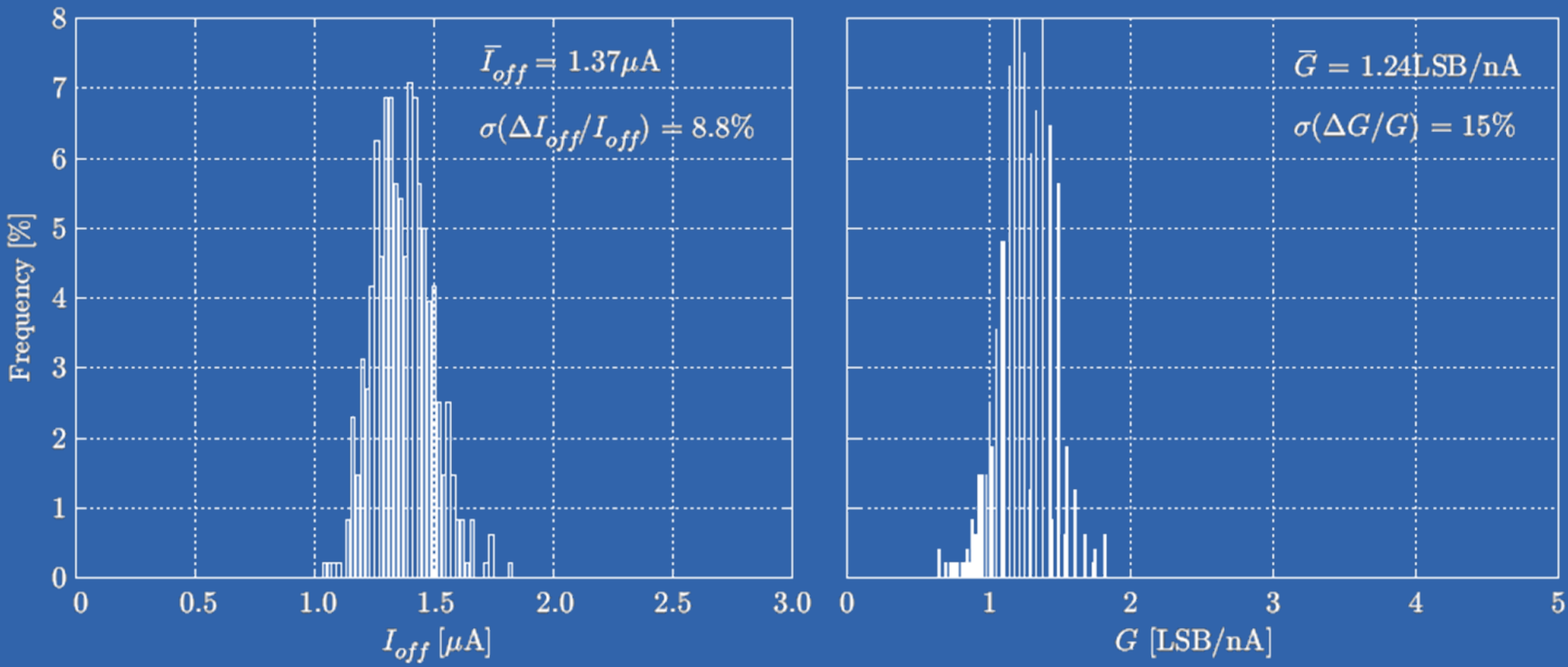
A/D Transfer Functions

- Full programmable **offset** (I_{dark}) & **gain** (V_{th})



Statistical FPN

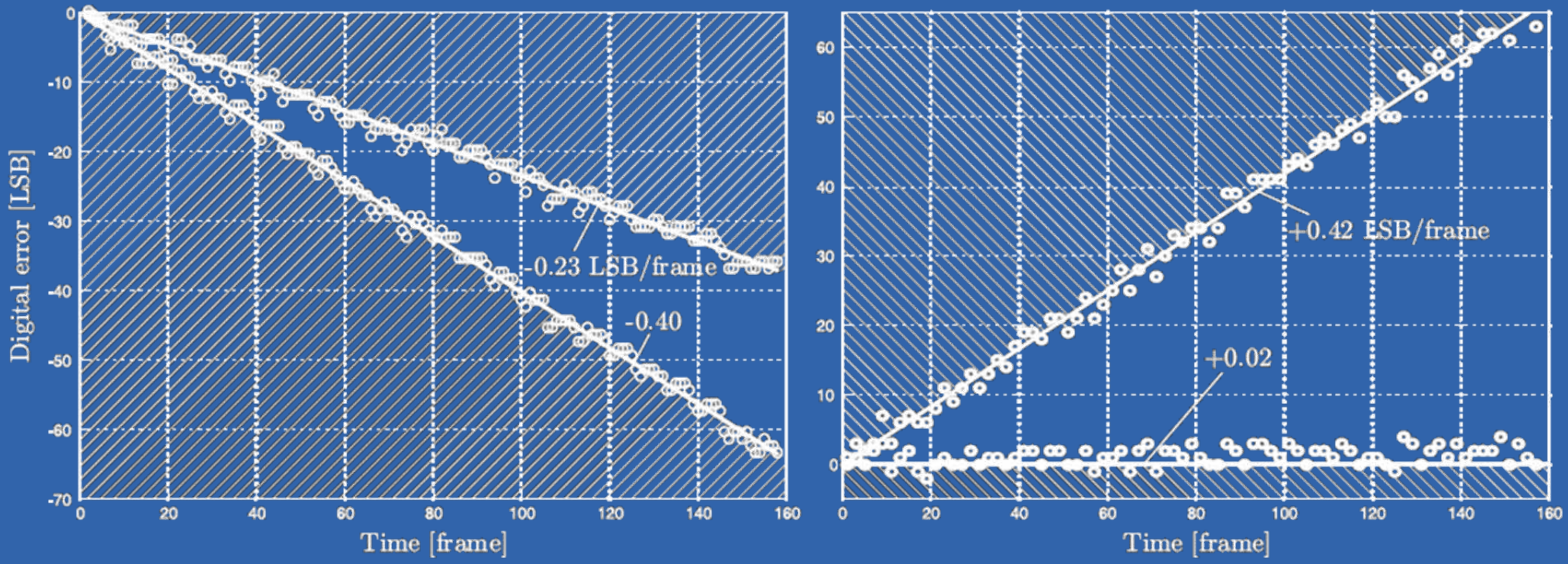
- **480** DPS cells , I_{dark}='1000000000' and V_{th}='1000000000'



…showing motivation for offset & gain **tuning**!

Analog Memory Retention

- DPS I_{dark}, V_{th} memory **leakage** rate:



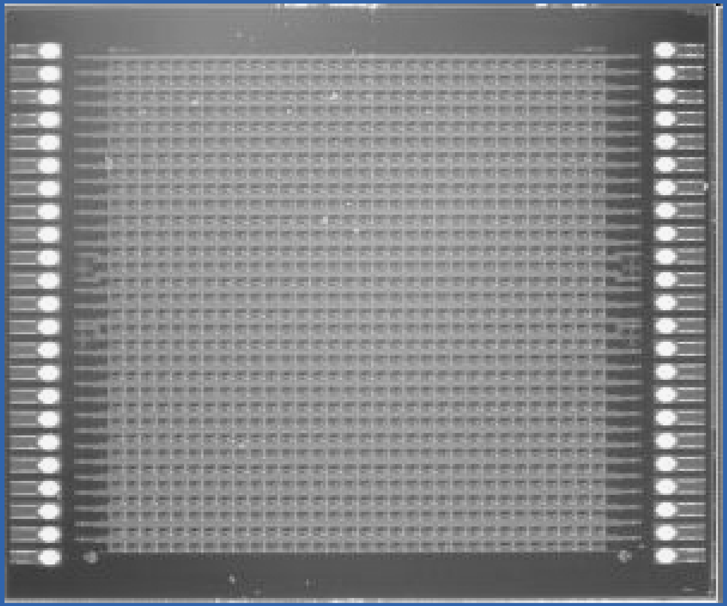
…large enough for **alternate** frame programming!

Conclusions

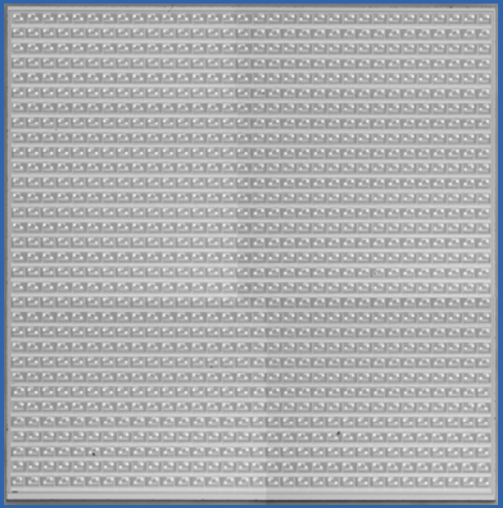
- Novel DPS for **uncooled IR fast** imaging.
- Sensor **capacitance** and **dark current** compensation.
- Compact **spike-counting** A/D converter with **CDS**.
- Digitally controlled **full FPN** compensation.
- **Local** analog **bias** generator.
- **Very low-power** CMOS circuits.
- **Monolithic** and **hybrid** DPS in 0.35μm 2P 4M.
- **Electrical** experimental **results**.

Current Status

- 32 x 32 135μm-pitch **FPAs** ready for PbSe and optical test:



By CMOS **post-processing**



By **modular** flip-chip

- Working on next generation: further down scaling with AER…

Thank you for your attention!!!