

A $0.35\mu\text{m}$ 1.25V Piezo-Resistance Digital ROIC for Liquid Dispensing MEMS

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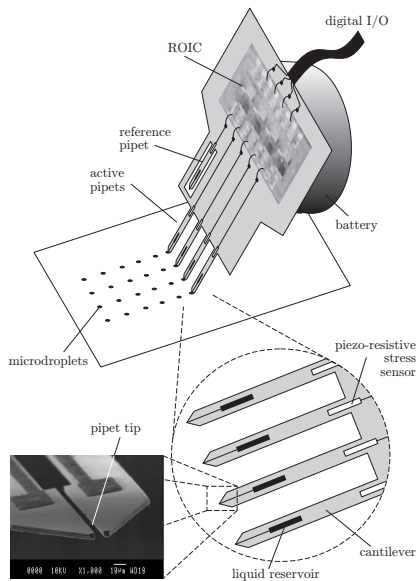
May 2008

- 1 Introduction
- 2 Input Gain Balancing
- 3 Differential Pre-Amplification
- 4 Integrating A/D Conversion
- 5 CMOS Integration
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Bioplume Scenario

- ▶ Liquid dispensing **MEMS** for μ droplet patterning
- ▶ Integrated **piezo-resistive** stress sensor to control **positioning**
- ▶ Dummy-based **differential reading** to cancel T/M/E disturbing signals
- ▶ Multi channel digital **ROIC**
- ▶ **Low-power** to prevent drying
- ▶ **Low-voltage** for single cell battery operation

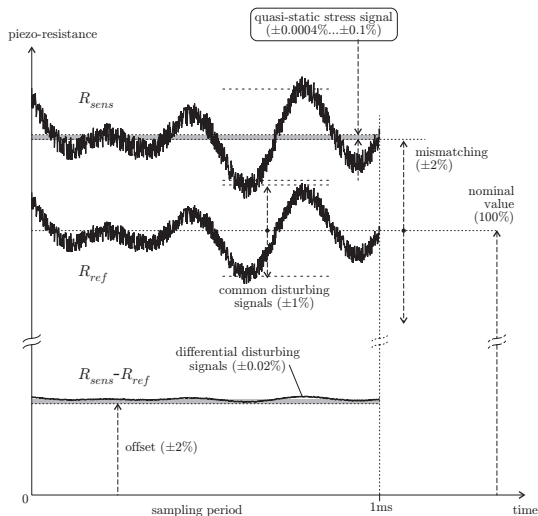


Integrated piezo-resistance

- ▶ Nominal value: $5\text{K}\Omega$ to $10\text{K}\Omega$
100% ($\pm 20\%$)
- ▶ Quasi-static stress signal (9bit):
 $\pm 0.0004\% \dots \pm 0.1\%$
- ▶ Technology mismatching: $\pm 2\%$
- ▶ Dynamic disturbing signals: $\pm 1\%$

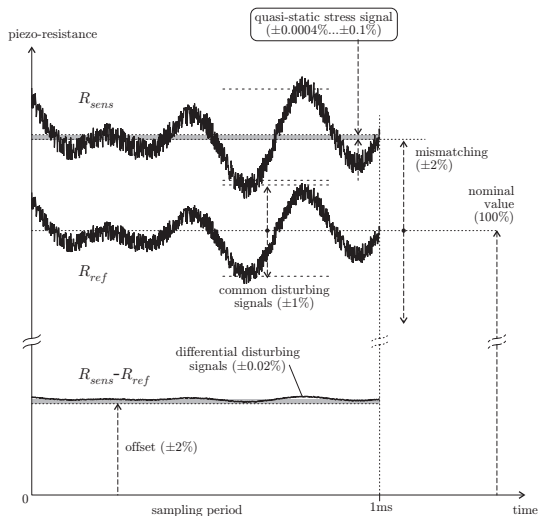


$\pm 0.02\%$ (50LSB) dynamic residual!



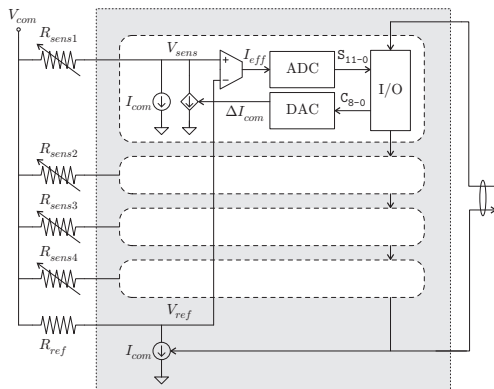
Gain Balancing Strategy

- ▶ Maximum gain compensation: $\pm 2\%$
- ▶ Gain accuracy: $\pm 0.0002\% / 2\% = \pm 0.01\%$
- ▶ Gain **dynamic range**: $2\% / 0.01\% = (8+1)\text{bit}$
- ▶ Residual dynamic disturbing: $\pm 0.25\text{LSB}$
- ▶ Residual DC: $\pm 25\text{LSB}$ compensated by digital post-processing



ROIC Architecture

- ▶ **Parallel** processing to reduce noise bandwidth
- ▶ Overall **programmable** sensitivity (I_{com})
- ▶ Differential gain **balancing** through sensor bias (ΔI_{com})
- ▶ **OTA** pre-amplification
- ▶ **Integrating** A/D conversion
- ▶ **Digital only** read-out/program-in
- ▶ **Independent** references to avoid crosstalk



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Input Gain Balancing

- ▶ Calibration through DAC: $\Delta I_{com}(C_{8-0})$

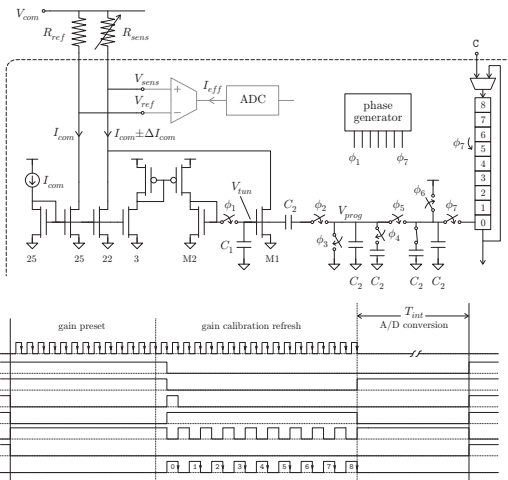
- ▶ Gate tuning:

$$\Delta V_{tun} = \frac{C_2}{C_1 + C_2} \left(V_{prog} - \frac{V_{DD}}{2} \right)$$

- ▶ Compensation of **piezo mismatch + OTA unbalance**

- ▶ Repeated before every acquisition

- ▶ Design parameters:
 $C_1=9\text{pF}$, $C_2=0.5\text{pF}$



$$V_{sens} - V_{ref} = I_{com} \left[R_{sens} \left(1 \pm \frac{\Delta I_{com}}{I_{com}} \right) - R_{ref} \right]$$

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OTA Preamplifier

- ▶ Differential V to **single ended** I

$$I_{eff} = G_m (V_{sens} - V_{ref})$$

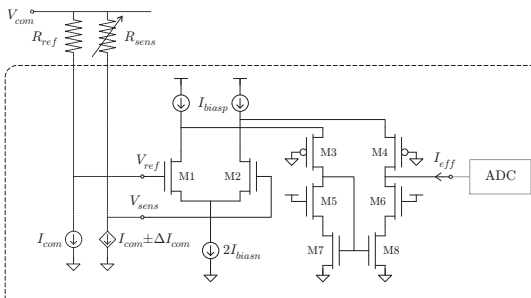
- ▶ Equivalent input **low-noise**

- ▶ Large **diff.** gain (in subthreshold):

$$G_m = \frac{I_{biasn}}{nU_t}$$

- ▶ High **common** rejection ratio
- ▶ Design parameters:

$$I_{biasp,n} = 56\mu\text{A}, 44\mu\text{A}$$



$$DR(V_{sens}) \sim 1\text{mV}/4\mu\text{V}$$

$$(R_{sens} \sim 5\text{k}\Omega \text{ and } I_{com} \sim 200\mu\text{A})$$

OTA Preamplifier

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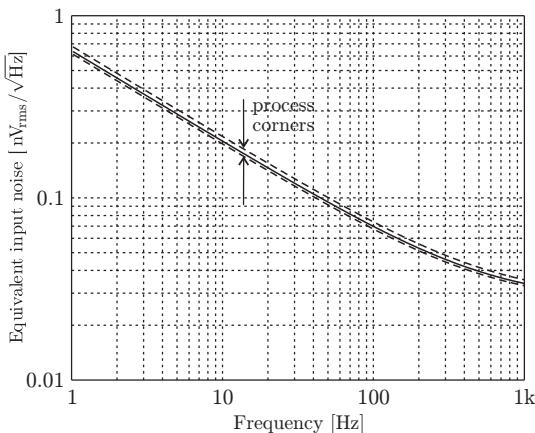
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$$V_{neq} \simeq 2\mu\text{V}_{rms} \text{ up to } 1\text{kHz}$$

$$(V_{nres} \sim 0.4\mu\text{V}_{rms} \text{ for } R_{sens} = 10\text{k}\Omega)$$

OTA Preamplifier

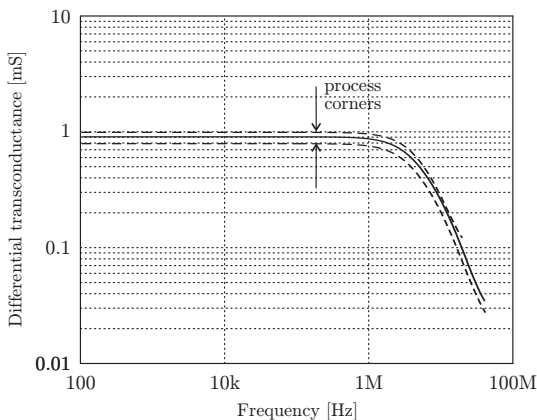
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$$G_m \geq 0.8\text{mS}$$

$$DR(I_{eff}) \sim 1\mu A/4nA$$

OTA Preamplifier

- ▶ Differential V to **single ended** I

$$I_{eff} = G_m (V_{sens} - V_{ref})$$

- ▶ Equivalent input **low-noise**
- ▶ Large **diff.** gain (in subthreshold):

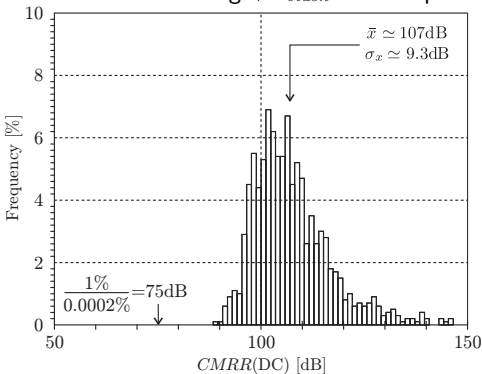
$$G_m = \frac{I_{biasn}}{nU_t}$$

- ▶ High **common** rejection ratio
- ▶ Design parameters:
 $I_{biasp,n} = 56\mu A, 44\mu A$

$$\frac{1}{CMRR} = \frac{\Delta G_m}{G_m} \left(1 - \frac{1}{1 + \frac{1}{2nG_m R_{tail}}} \right)$$

$$CMRR \rightarrow \infty \text{ for } \Delta G_m \rightarrow 0 \text{ or } R_{tail} \rightarrow \infty$$

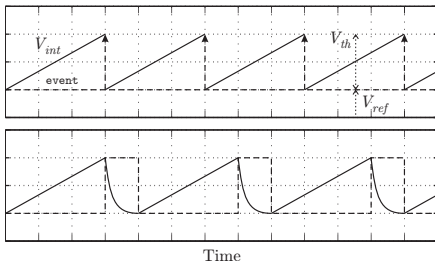
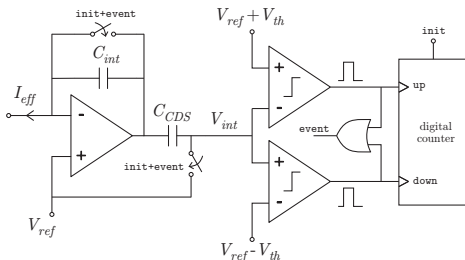
MOSFET mismatching + I_{biasn} finite impedance



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A/D Conversion

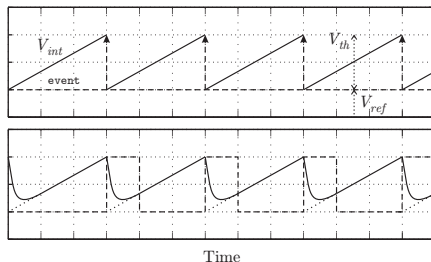
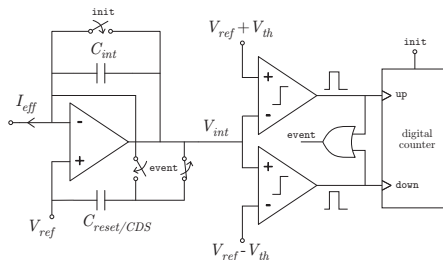
- ▶ Spike counting:
PDM+digital filter
- ▶ **CDS** for
low-frequency noise
suppression
- ▶ **Low-voltage**
switching \Rightarrow
large **reset times**
- ▶ Design parameters:
 $C_{int} = 4\text{pF}$,
 $V_{th} = 312\text{mV}$
- ✗ Classic PDM:
reset-time
non-linearity



Upper range **saturation** of the A/D curve!

A/D Conversion

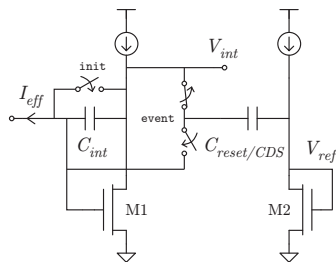
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- ▶ Design parameters:
 $C_{int} = 4\text{pF}$,
 $V_{th} = 312\text{mV}$
- ✓ **New insensitive PDM**



$$S_{11-0} = \pm \frac{I_{eff} T_{int}}{C_{int} V_{th}} = \pm \frac{G_m T_{int}}{C_{int} V_{th}} I_{com} \left[R_{sens} \left(1 \pm \frac{\Delta I_{com}}{I_{com}} \right) - R_{ref} \right]$$

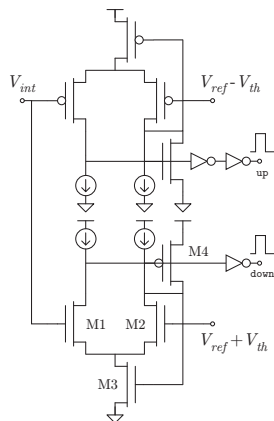
Low-Voltage CMOS Blocks

- Compact **CTIA** with **CDS**



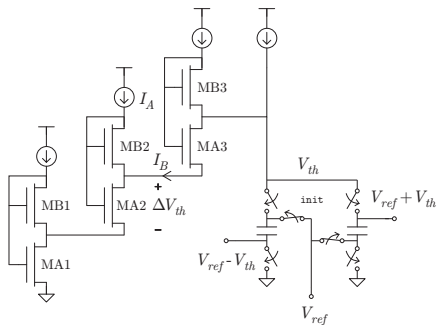
Low-Voltage CMOS Blocks

- ▶ Compact **CTIA** with **CDS**
- ▶ Class-AB window **comparator**



Low-Voltage CMOS Blocks

- ▶ Compact **CTIA** with **CDS**
- ▶ Class-AB window **comparator**
- ▶ Modular and floating threshold **generator**



$$\Delta V_{th} = U_t \ln \left[\frac{(W/L)_B}{(W/L)_A} \left(1 + \frac{I_B}{I_A} \right) + 1 \right]$$

MA : weak inversion conduction

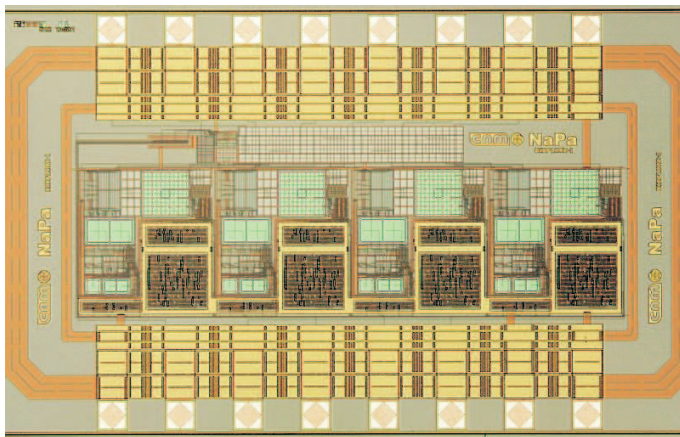
MB : weak inversion saturation

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ROIC Integration

▶ 0.35 μm 2P 4M CMOS technology

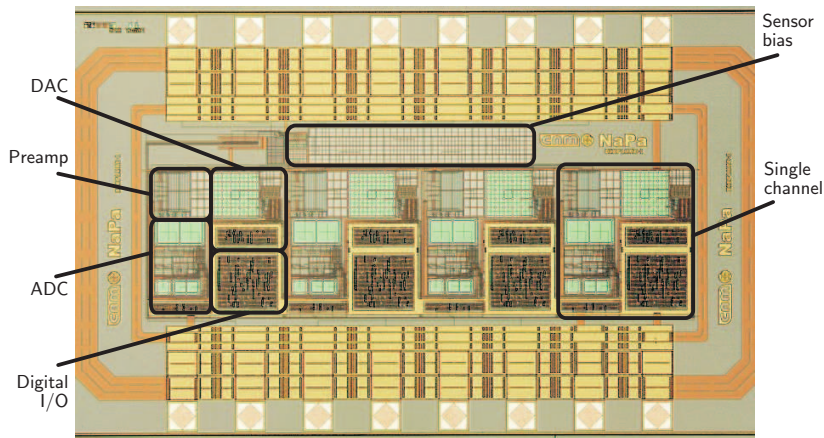
2.4mm \times 1.3mm = 3.1mm²



ROIC Integration

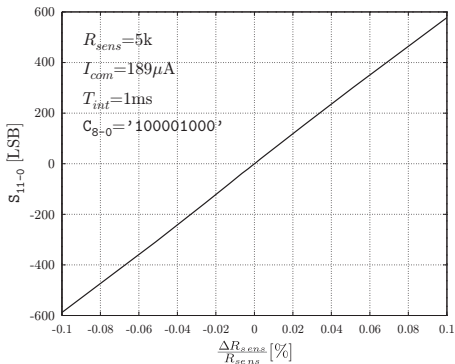
▶ 0.35 μm 2P 4M CMOS technology

2.4mm \times 1.3mm = 3.1mm²



Results

- ▶ **MEMS + ROIC** integration not completed yet. . .
- ▶ Meanwhile, results from **post-layout** simulation
- ▶ 4 channel power supply: **1.5mW** at **1.25V**
- ▶ Ideally:



$$\left| \frac{S_{11-0}}{\Delta R_{sens}/R_{sens}} \right| = \frac{G_m T_{int}}{C_{int} V_{th}} I_{com} R_{sens} \equiv \frac{0.8mS \times 1ms}{4pF \times 312mV} \times 189\mu A \times 5k\Omega \simeq 6kLSB/\%$$

V_{th} PTAT and G_m 1/PTAT. If $I_{com,bias}$ **PTAT** $\Rightarrow S_{11-0} \neq f(T)$



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Conclusions

- ▶ **Quad-channel ROIC** for integrated **piezo-resistive** sensors.
- ▶ Sensor balancing by **digital gain tuning**.
- ▶ Robust built-in **A/D conversion**.
- ▶ **Low-voltage** and **low-power** CMOS circuit realization.
- ▶ Integration in **0.35 μm 2-poly 4-metal** technology.
- ▶ **Post-layout** electrical simulation results.