A Self-Biased and FPN-Compensated Digital APS for Hybrid CMOS Imagers

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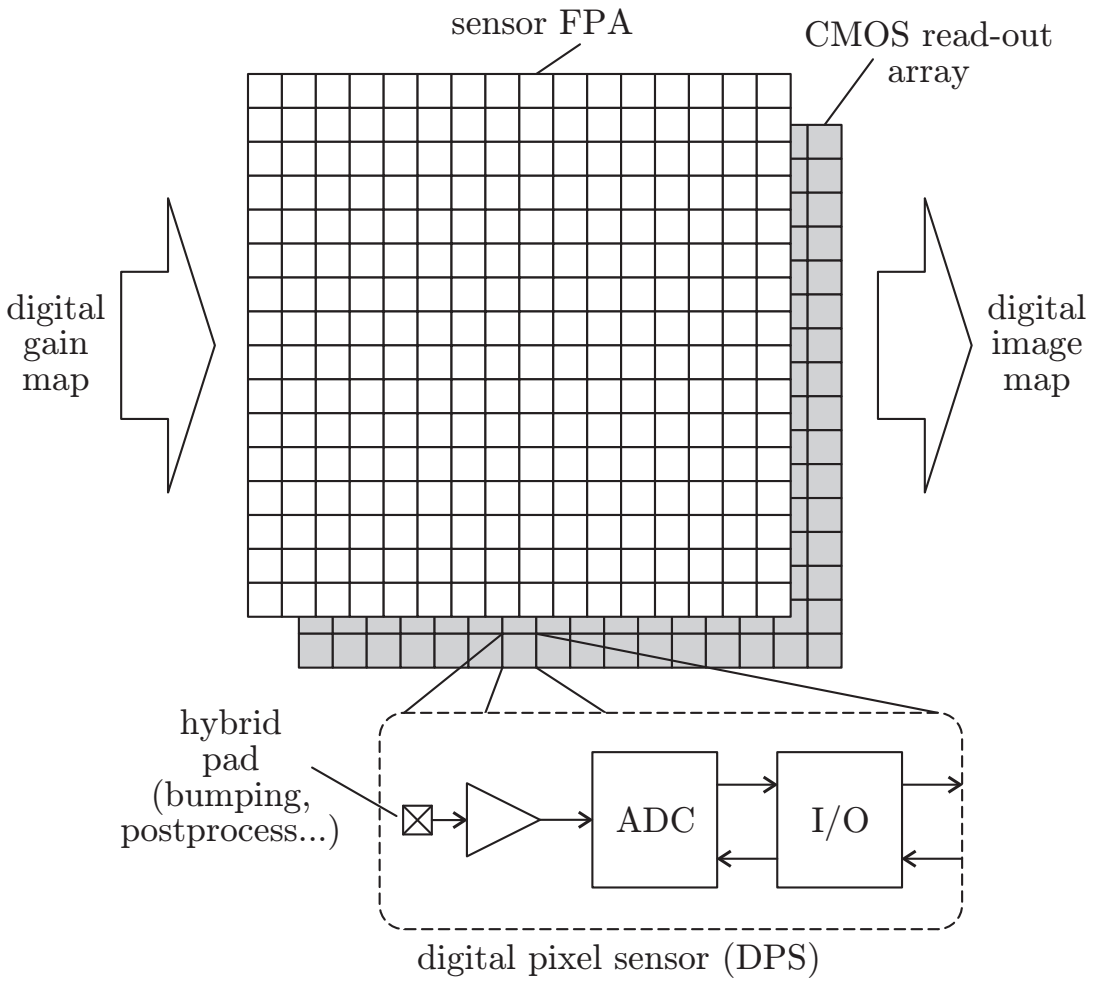
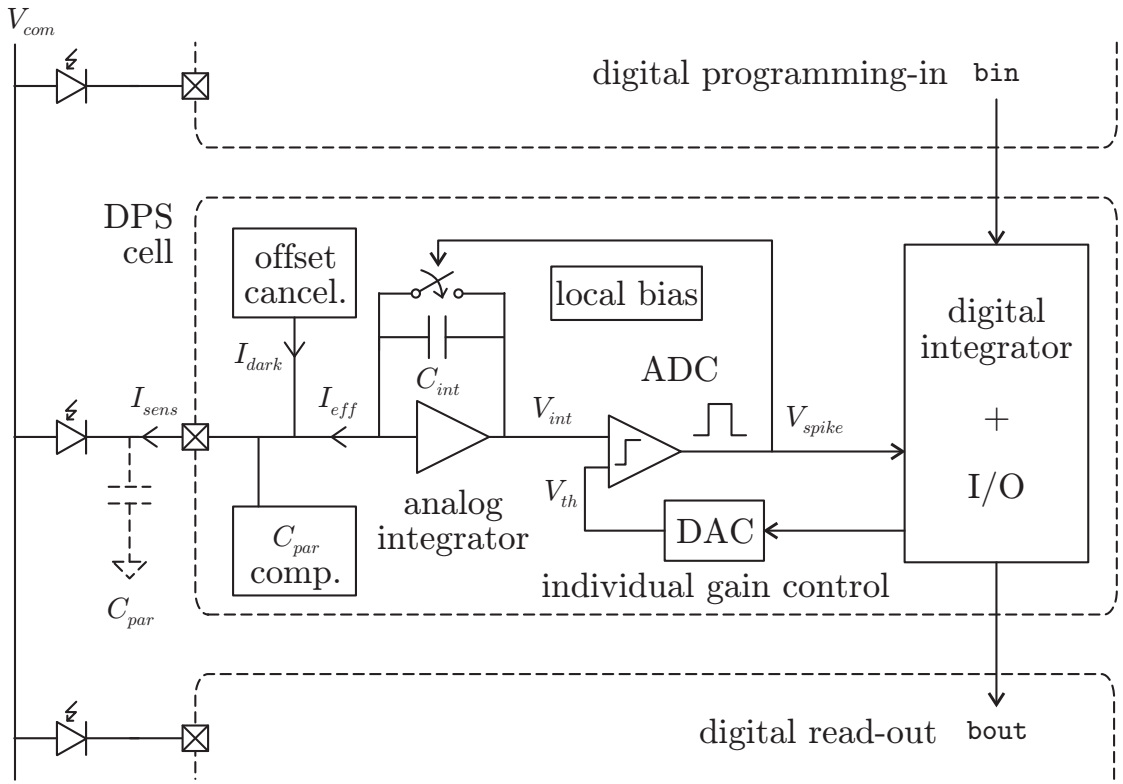
Scenario



Active pixel requirements

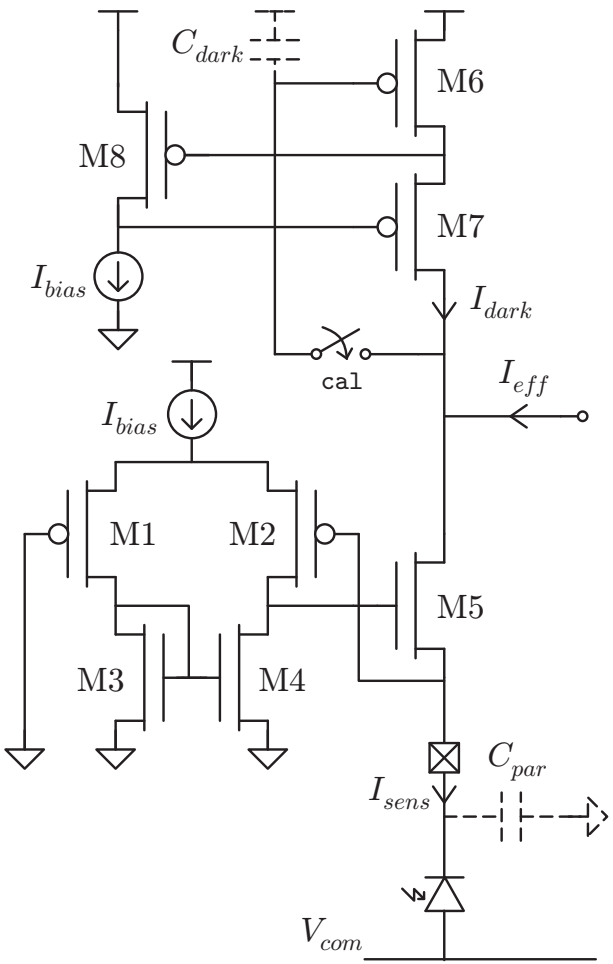
- Hybrid imager ⇒ **high input cap**
- Room temp. IR ⇒ **large dark current**
- FPA signal integrity ⇒ **digital only I/O**
- FPN compensation ⇒ **individual pixel gain programmability**
- Large FPA ⇒ **low-power & compact pixel circuits**

Digital pixel sensor (DPS) proposal



- **Automatic** input dark current & capacitance compensation
- **Asynchronous ADC** based on spike counting
- **Individual gain** control:
  - ✓ FPN compensation
  - ✓ Spatial AGC
  - ✓ Updated each frame
  - ✓ No speed reduction
- **Built-in** analog references

Input offset and capacitance compensation



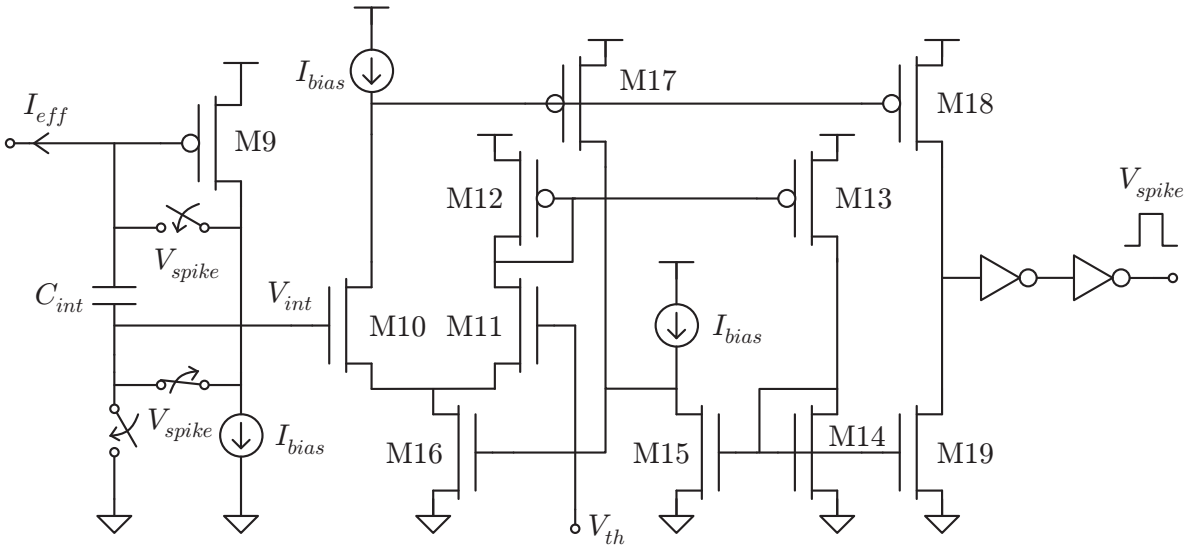
- **Low impedance** input:

$$r_{in} = \frac{1}{gm_{g5}} \left(\frac{1}{n + \frac{gm_{g1,2}}{gm_{d1,2}+gm_{d3,4}}} \right) \ll 1\text{k}\Omega$$

so, C_{par} can be >10pF...

- Regulated cascode dark current **copier**:
  - ✓ Mismatch insensitive
  - ✓ Large dark-to-signal ratio $\sim \frac{1\mu\text{A}}{1\text{nA}}$

Integrating ADC

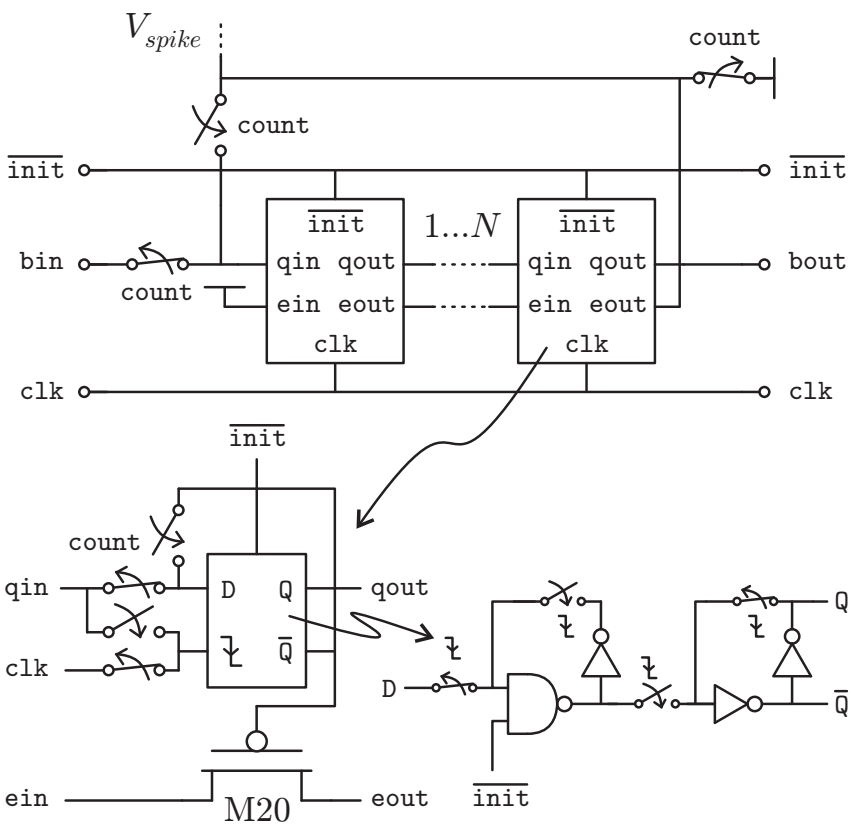


- **Fast reset** times can be obtained. Ideally:

$$f_{spike} = \frac{1}{C_{int}\, V_{th}} I_{eff}$$

- **3-switch** reset CTIA stage:
  - ✓ More parasitic insensible
  - ✓ Constant input voltage
  - ✓ CDS implementation
  - ✓ Low-power Class-AB
- **Dynamic bias** comparator
- C_{int} linearity not needed

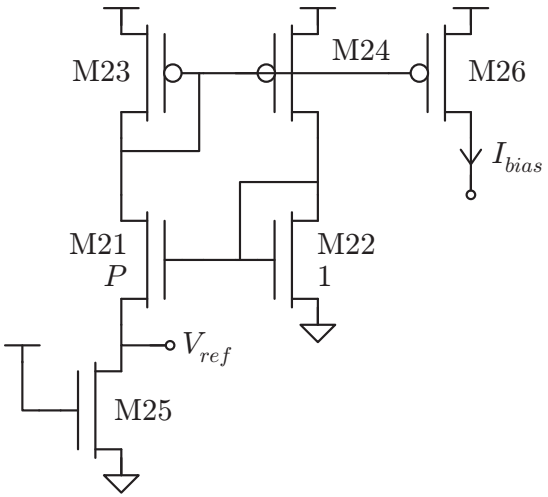
Digital integrator and I/O



- Circuit **reuse**:
  - ✓ Ripple counter
  - ✓ Shift register
- **Modular** design
- **Overflow** detector
- In case of no overflow:

$$\texttt{wout} = \frac{f_{spike}}{f_{frame}} = \frac{T_{frame}}{C_{int}\,V_{th}}\,I_{eff}$$

Self-biasing



(M21-M22 in weak inv. + M25 in strong inv.)

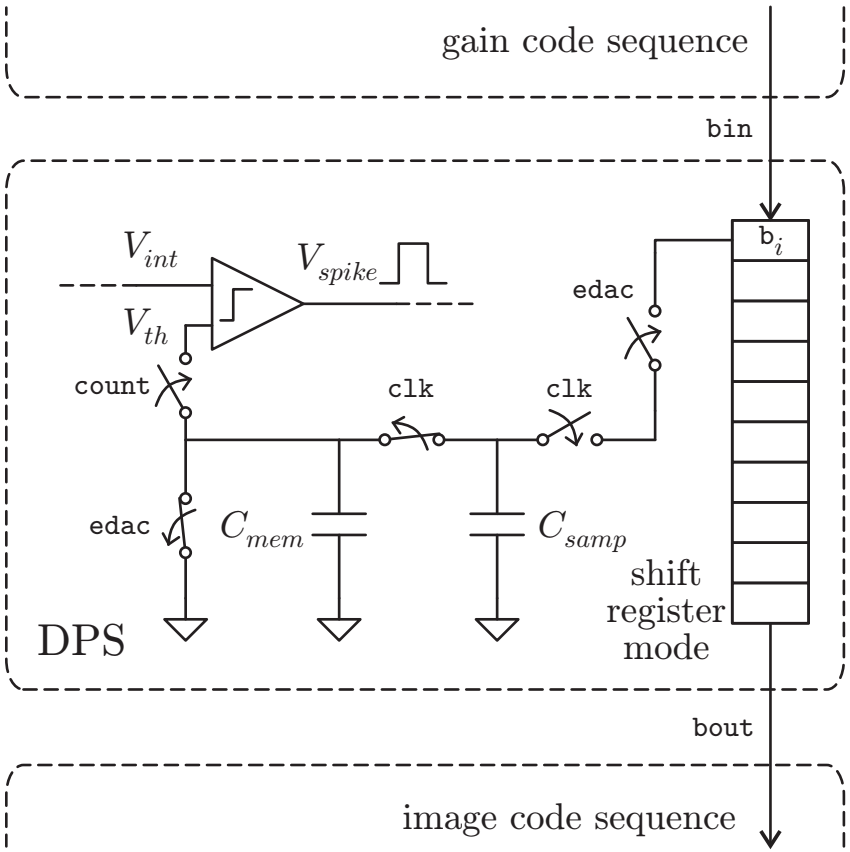
$$V_{ref} = U_t \ln(P)$$

$$I_{bias} \simeq \beta \left(\frac{W}{L}\right)_{25} (V_{DD} - V_{TO})\, V_{ref}$$

- **Local** I/V reference:
  - ✓ Low crosstalk
  - ✓ Compact circuit
- Low **process** sensitivity
- Bias **mismatching** between DPS cells:

$$\sigma\left(\frac{\Delta V_{ref}}{V_{ref}}\right) = \frac{1}{\sqrt{(WL)_{21,22}}} \frac{A_{VTO}}{n V_{ref}}$$

FPN compensation

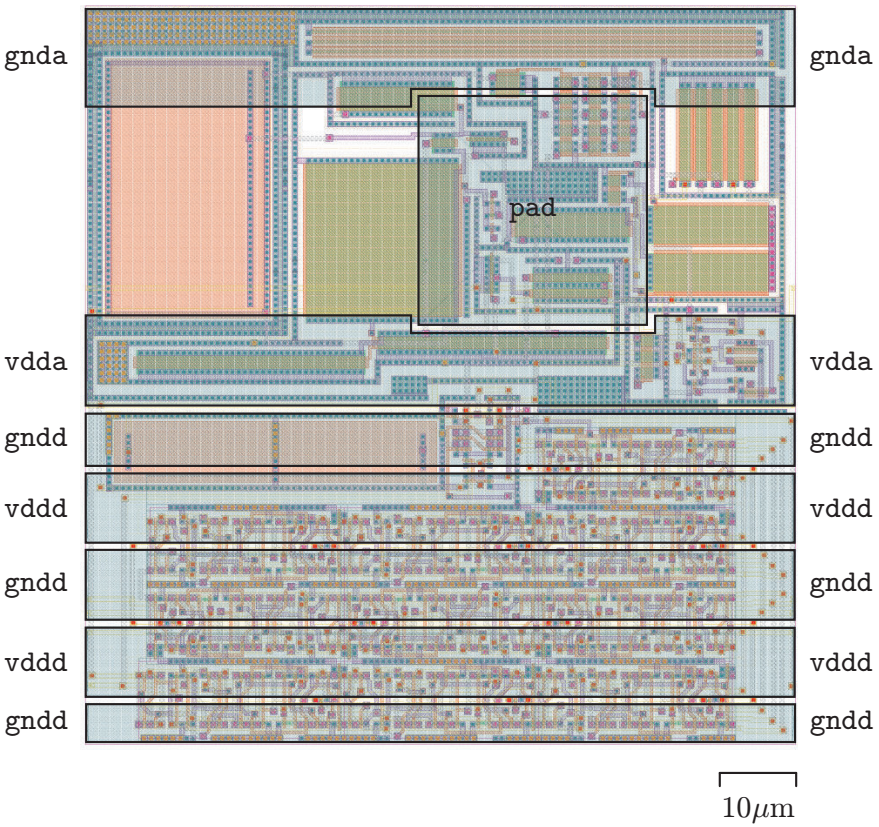


- Offset cancellation already addressed by the input copier
- Built-in **DAC** for gain correction:

$$V_{th} = V_{DD} \sum_{i=1}^{N} \frac{\mathrm{b}_{N-i}}{2^i}$$

  - ✓ No speed reduction
  - ✓ Individual for each DPS
  - ✓ Changeable each frame
- Suitable for **spatial AGC**

CMOS integration (first version)



100μm×100μm

- Room temperature PbSe **IR sensor** target
- Design **parameters**:

C_{int}	500 fF
N	10 bit
P	12
I_{bias}	**50 nA**
$C_{mem,samp}$	100 fF

- **0.35μm 2-polySi 4-metal** CMOS technology

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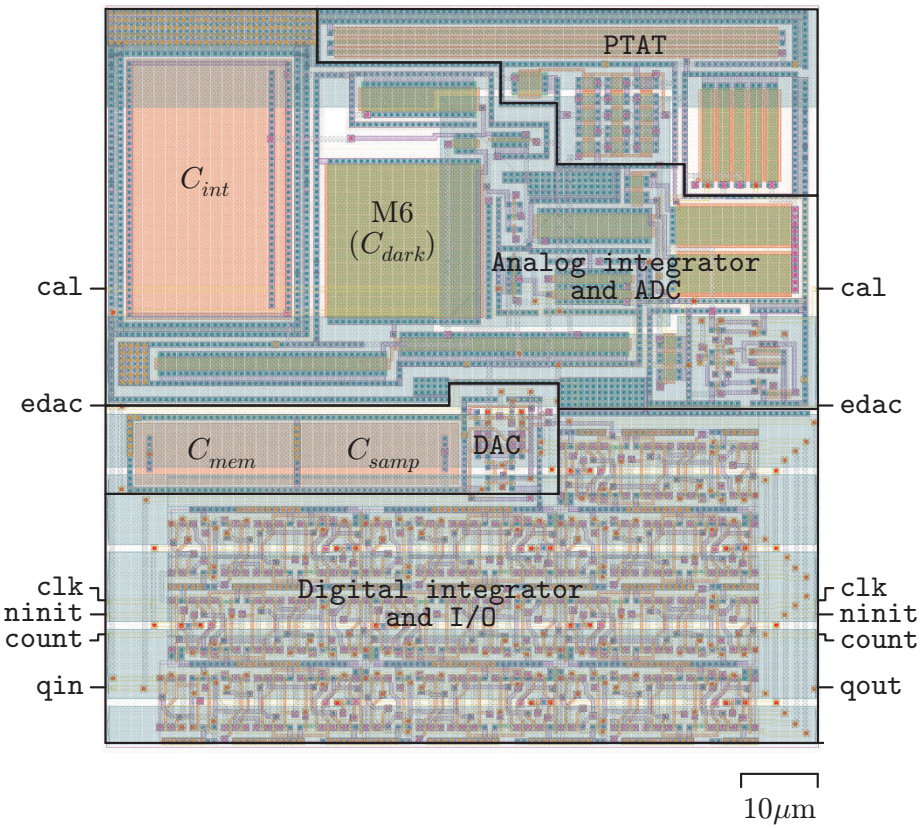

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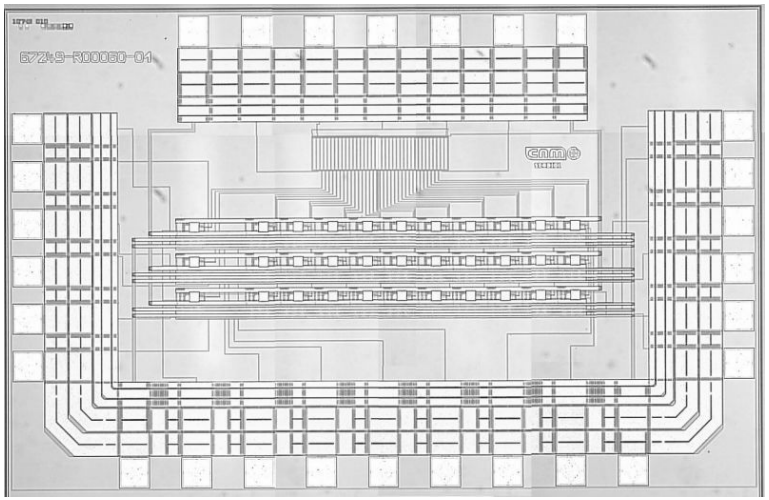
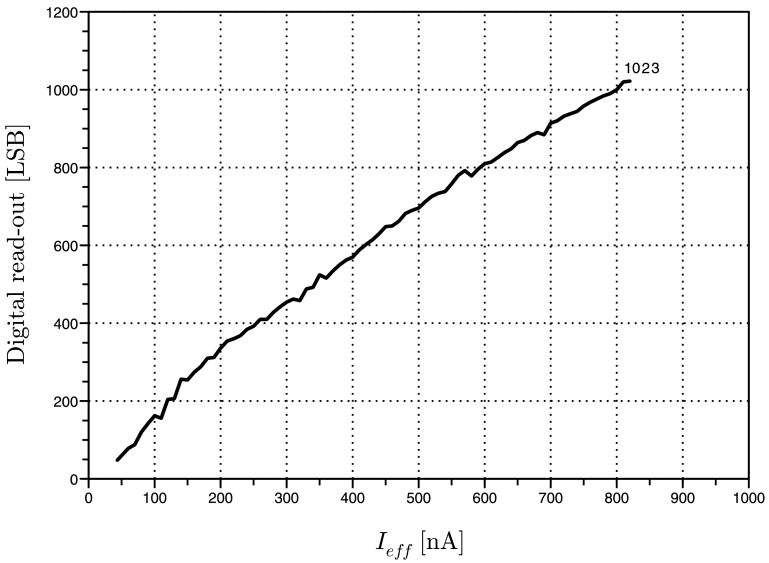
Results (first version)



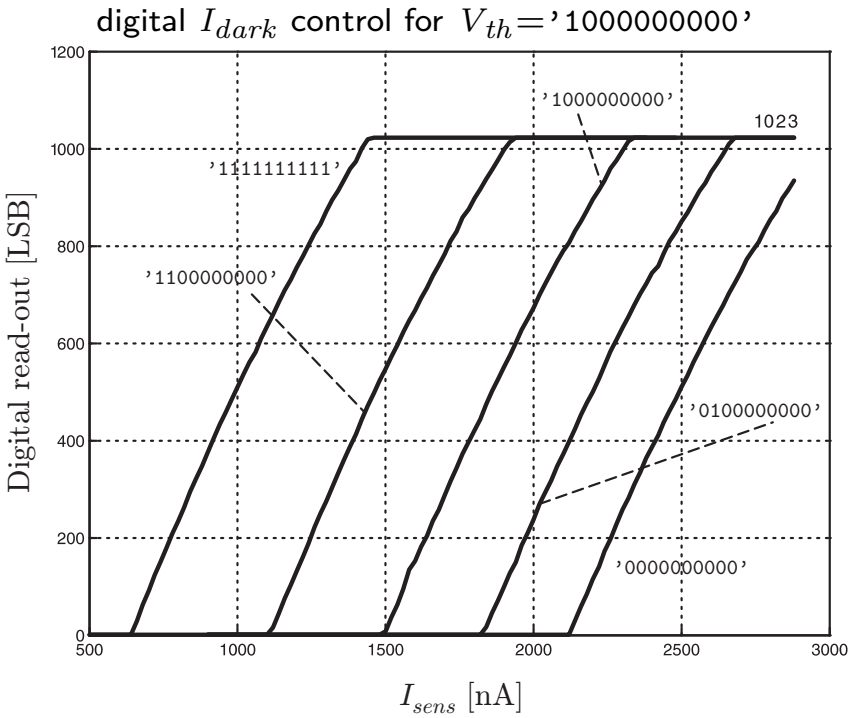


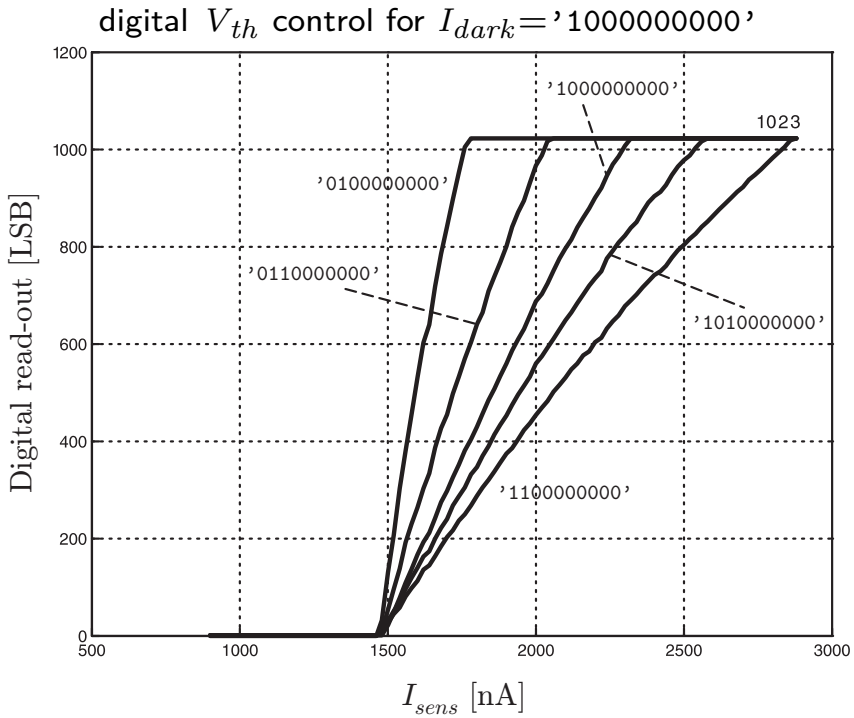
- Test vehicle:
  - ✓ 3×10 pixel **FPA**
  - ✓ NMOS sensor **emulator**
- Performance:

Dark current range	0.1-5 μA
Dark current retention time	**2-10 s**
Max. input capacitance	15 pF
Signal range	1-1000 nA
Integration time	**1 ms**
Crosstalk	<0.5 LSB
Programming/read-out speed	10 Mbps
Supply voltage	3.3 V
Static power consumption	**<1 μW**
Biasing deviations ($\pm\sigma$)	$\pm$15 %
Total Silicon area	100×100 μm^2

Last minute results (second version)

- **Shared DAC** for programming V_{th} & I_{dark} at alternating frames:





Conclusions

- Novel **low-power** and **digital-only I/O** DPS cell
- **Hybrid** imager compatibility
- Pixel built-in **FPN compensation** and **biasing generation**
- Circuit implementation for **all building blocks**
- **0.35μm 2-polySi 4-metal** CMOS demonstrator