A 1.2V 130μA 10-bit MOS-Only Log-Domain $\Sigma\Delta$ Modulator

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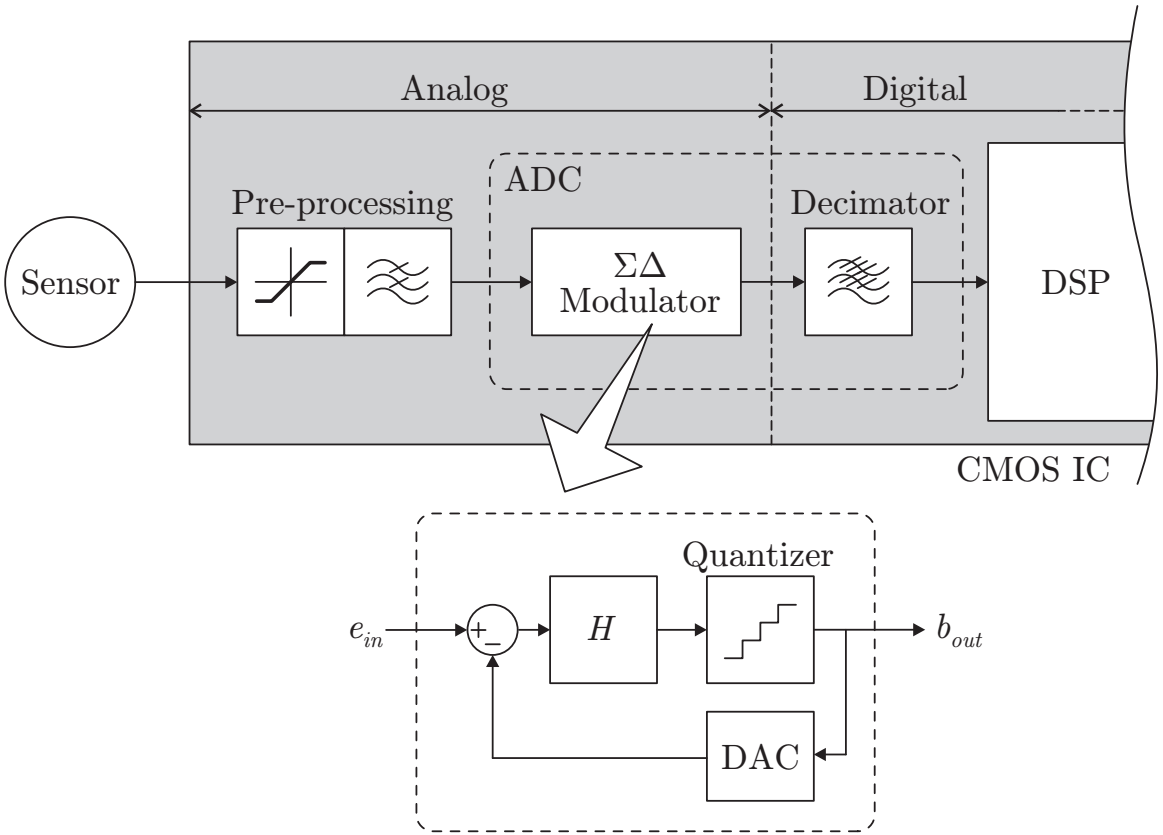
Scenario



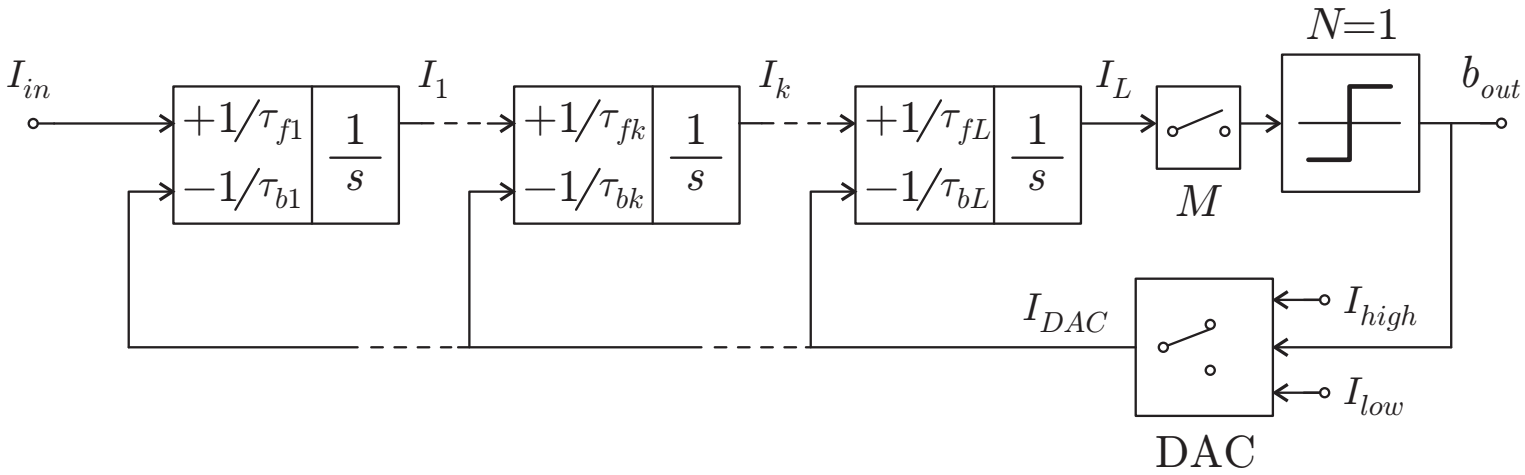
Digital compatibility

- Very **low-voltage** operation
- **Low-cost** CMOS process:
  - X Double poly-Si cap
  - X MIM cap

- Design **parameters**: L-order, M-oversampling and N-bit.

Log-domain proposal

- Continuous-time **current-mode** processing:

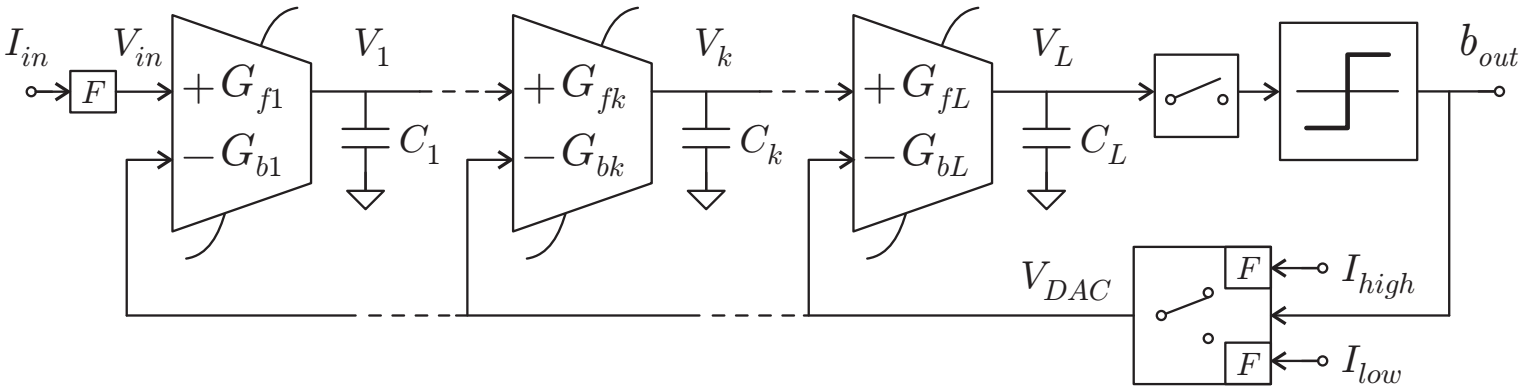


$$\frac{d\overline{I}_{SS}}{dt} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \frac{1}{\tau_{f2}} & 0 & 0 & 0 \\ 0 & \frac{1}{\tau_{fk}} & 0 & 0 \\ 0 & 0 & \frac{1}{\tau_{fL}} & 0 \end{bmatrix} \overline{I}_{SS} + \begin{bmatrix} \frac{1}{\tau_{f1}} \\ 0 \\ 0 \\ 0 \end{bmatrix} I_{in} - \begin{bmatrix} \frac{1}{\tau_{b1}} \\ \frac{1}{\tau_{b2}} \\ \frac{1}{\tau_{bk}} \\ \frac{1}{\tau_{bL}} \end{bmatrix} I_{DAC}$$

$$\overline{I}_{SS} = [I_1 I_2 \cdots I_k \cdots I_L]^{\mathsf{T}}$$

Log-domain proposal

- Inner **voltage compression**: low-voltage & non-linear (**MOS**) cap



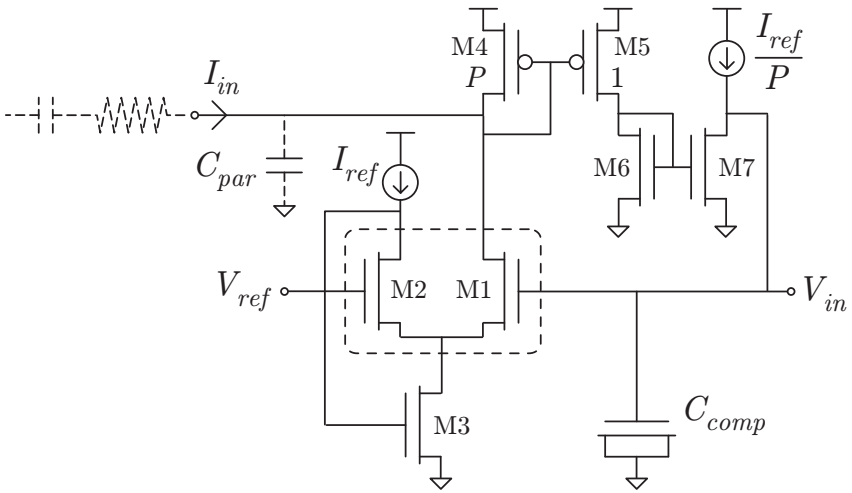
$$i = F(v) = e^v$$

- Implemented operating MOSFET in **subthreshold** (w.i.sat.):

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad I_S = 2n\beta \left(\frac{W}{L}\right) U_t^2$$

$$i = \frac{I_D}{I_S} \quad \overset{F}{\longleftrightarrow} \quad v = \frac{V_{GB}}{nU_t}$$

Input compressor



Note: dashed MOSFETs working in weak inversion.

- Reference levels: I_{ref} and V_{ref}
- **Low-impedance** input for optional linear V/I conversion
- Parasitic input cap **compensation**:

$$I = F(V) = I_{ref}\, e^{\frac{V - V_{ref}}{nU_t}} \qquad I > 0$$

$$V_{in} = V_{ref} + nU_t \ln\left(\frac{I_{in}}{I_{ref}} + 1\right) \qquad |I_{in}| < I_{ref}$$

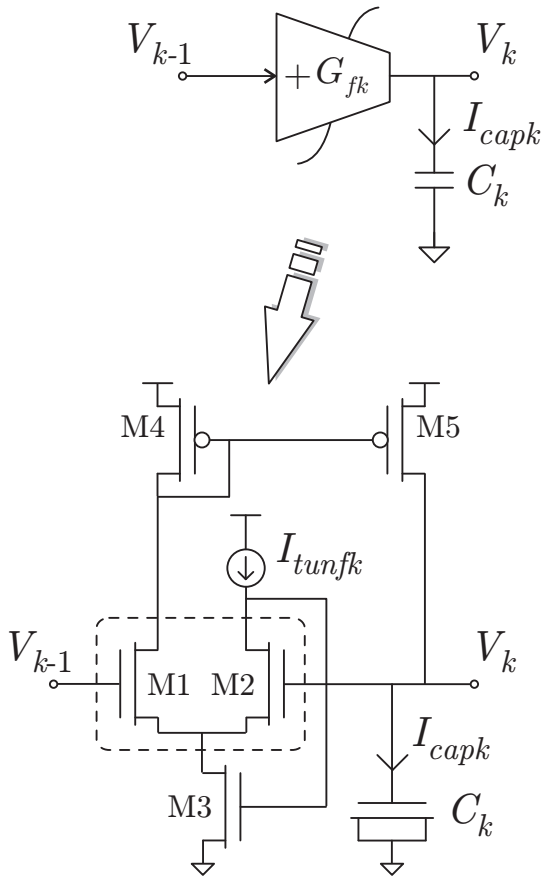
$$\zeta = \frac{1}{2}\sqrt{\frac{PC_{comp}}{C_{par}}}$$

Differential integrator with built-in DAC

- **Single** coefficient:

$$\frac{dI_k}{dt} = \frac{1}{\tau_{fk}} I_{k-1} \quad \overset{F}{\longleftrightarrow} \quad \frac{dV_k}{dt} = \frac{nU_t}{\tau_{fk}} e^{\frac{V_{k-1}-V_k}{nU_t}}$$

$$\frac{dQ_k}{dt} = \underbrace{C_k \frac{dV_k}{dt}}_{I_{capk}} = \underbrace{I_{tunfk} e^{\frac{V_{k-1}-V_k}{nU_t}}}_{G_{fk}}$$



- **Tuning** parameter:

$$I_{tunfk} = \frac{nU_t C_k}{\tau_{fk}}$$

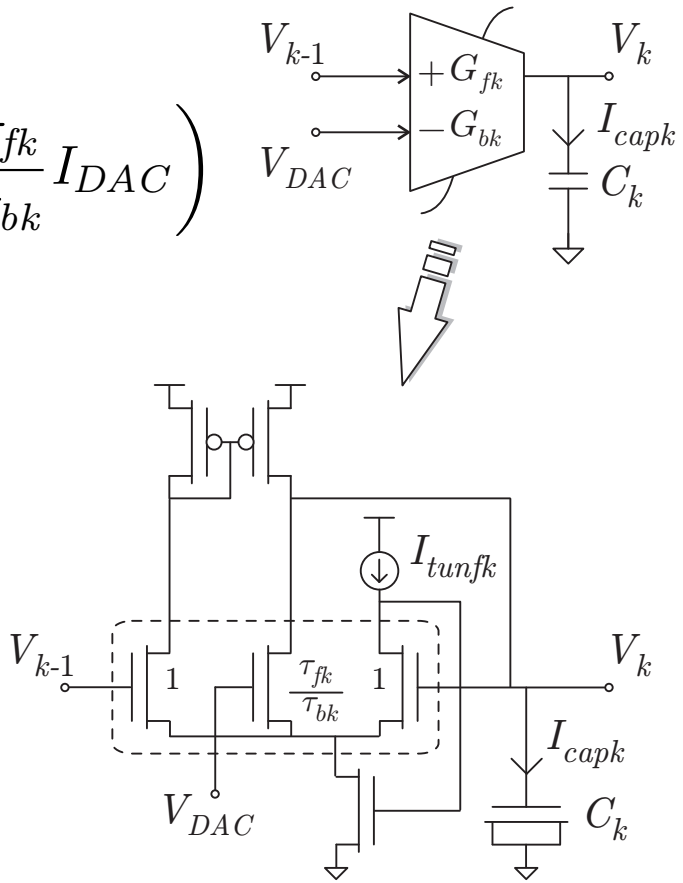
- Voltage compression allows grounded **NMOS** capacitors

Differential integrator with built-in DAC

- **Multiple** coefficients:

$$\frac{dI_k}{dt} = \frac{1}{\tau_{fk}} I_{k-1} - \frac{1}{\tau_{bk}} I_{DAC} \equiv \frac{1}{\tau_{fk}} \left(I_{k-1} - \frac{\tau_{fk}}{\tau_{bk}} I_{DAC} \right)$$

$$I_{capk} = I_{tunfk} e^{\frac{-V_k}{nU_t}} \left(e^{\frac{V_{k-1}}{nU_t}} - \frac{\tau_{fk}}{\tau_{bk}} e^{\frac{V_{DAC}}{nU_t}} \right)$$



- Gain weight $\equiv$ **geometrical ratio**
- Half circuit **shared** between integrator coefficients

Differential integrator with built-in DAC

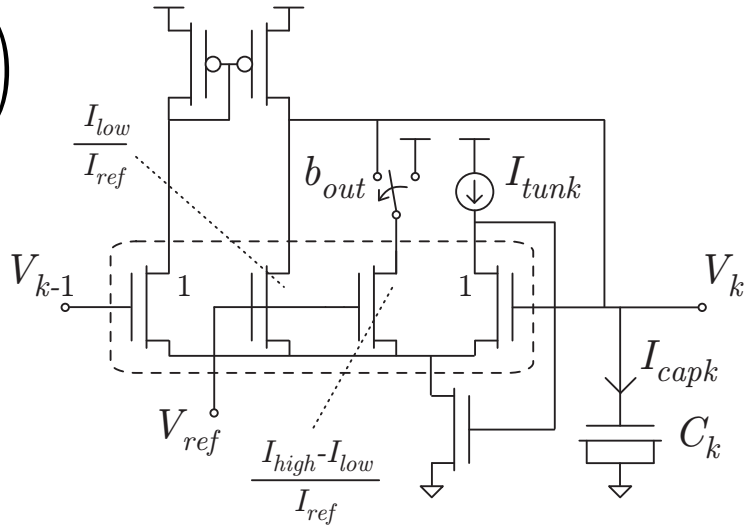
- In practice, $\tau_k \doteq \tau_{fk} \equiv \tau_{bk}$:

$$I_{capk} = I_{tunk} e^{\frac{-V_k}{nU_t}} \left(e^{\frac{V_{k-1}}{nU_t}} - e^{\frac{V_{low,high}}{nU_t}} \right) \qquad b_{out} = 0, 1$$

- **Current switching** DAC:

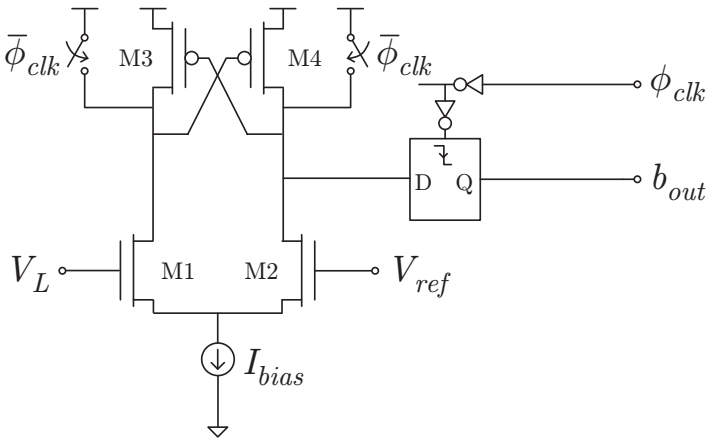
$$I_{capk} = I_{tunk} e^{\frac{-V_k}{nU_t}} \left(e^{\frac{V_{k-1}}{nU_t}} - \frac{I_{low,high}}{I_{ref}} e^{\frac{V_{ref}}{nU_t}} \right)$$

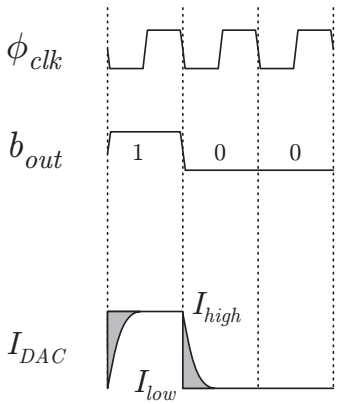
- **Fast** settling time
- **Low cross-talk**



Quantizer

- Equivalent 1-bit **expander**



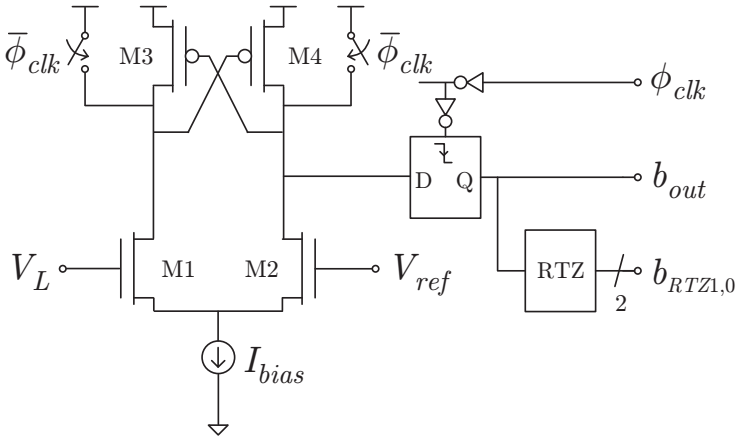


Waveform asymmetry

- **Return-to-zero** approach
- **DAC** implementation:

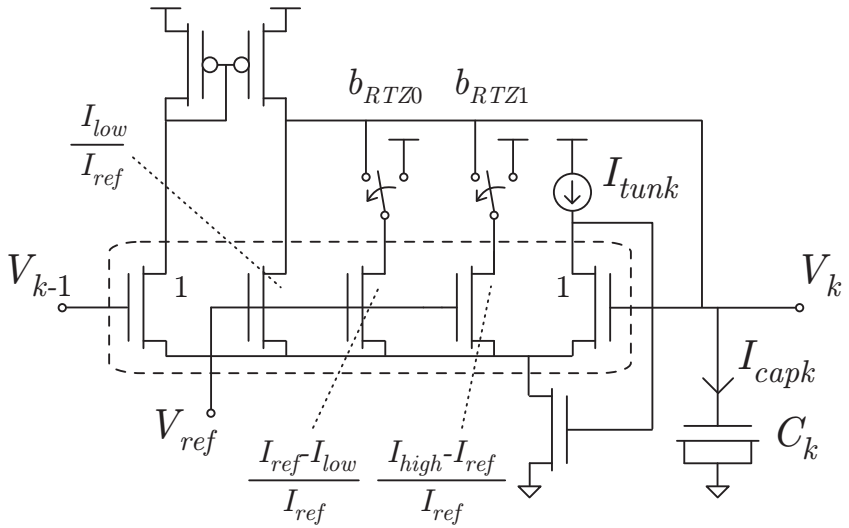
Quantizer

- Equivalent 1-bit **expander**

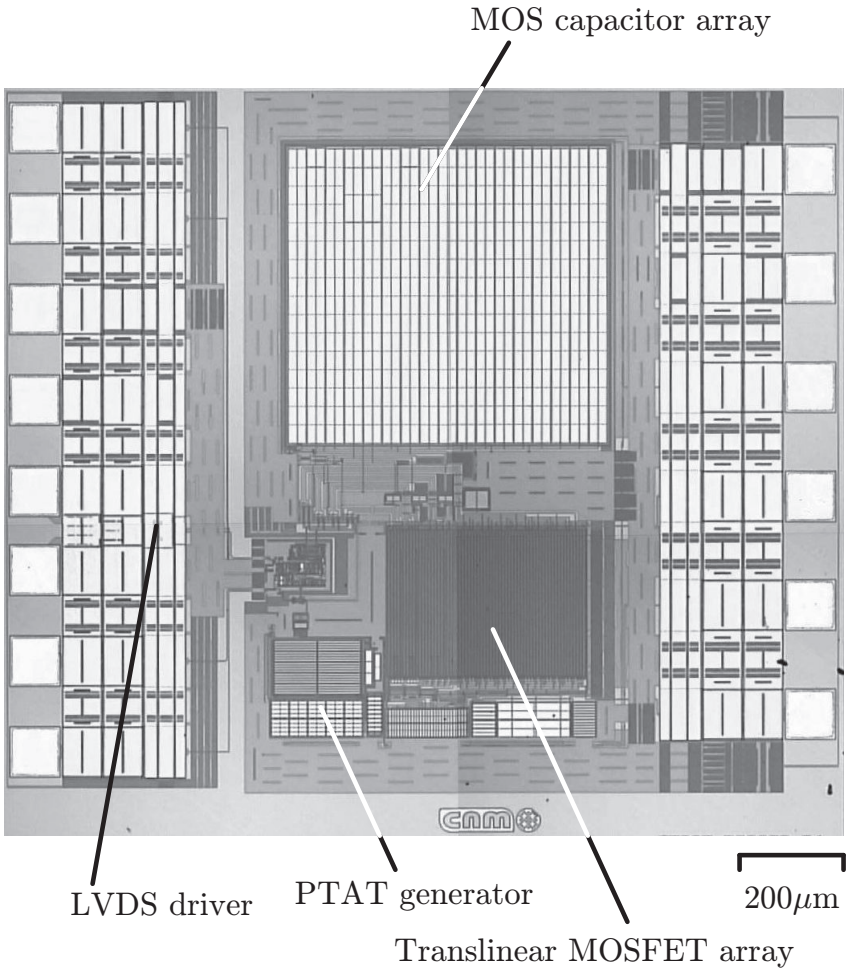


Waveform asymmetry

- **Return-to-zero** approach
- **DAC** implementation:



CMOS integration



- **4th-order 64-times 1-bit** $\Sigma\Delta$ topology
- **PTAT** reference for I_{tunk}
- **LVDS** out for low bulk-noise
- Core size: 700μm$\times$1150μm (**0.8mm^2**)
- 0.35μm **1-polySi** 3-metal **digital** CMOS technology

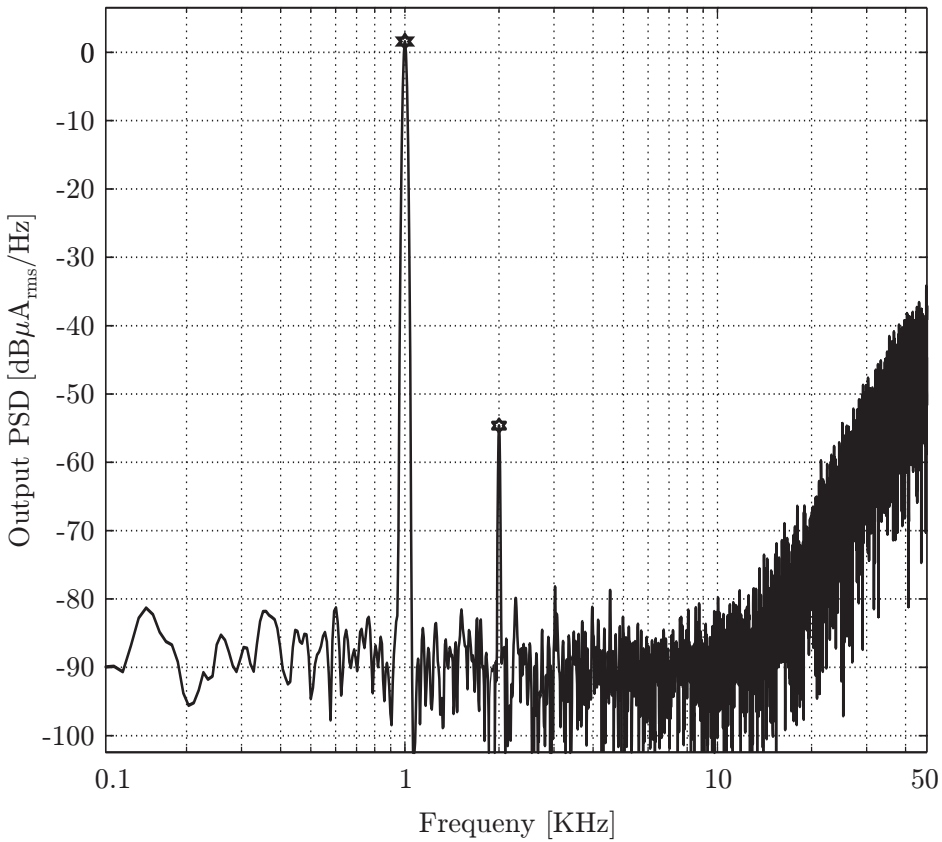
Results

- Design **parameters**:

V_{ref}	0.7 V
I_{ref}	7 μA
$I_{low,high}$	1, 13 μA
$I_{tun1,2,3,4}$	7, 1, 1, 1 μA
$C_{1,2,3,4}$	1052, 150, 60, 60 pF
$(W/L)_{trans}$	$\frac{I_D}{\mu A} \times \frac{273}{1.5} \frac{\mu m}{\mu m}$

- Sampled-time optimal coefficients
- **1MHz** sampling frequency
- **High-value** MOS capacitors

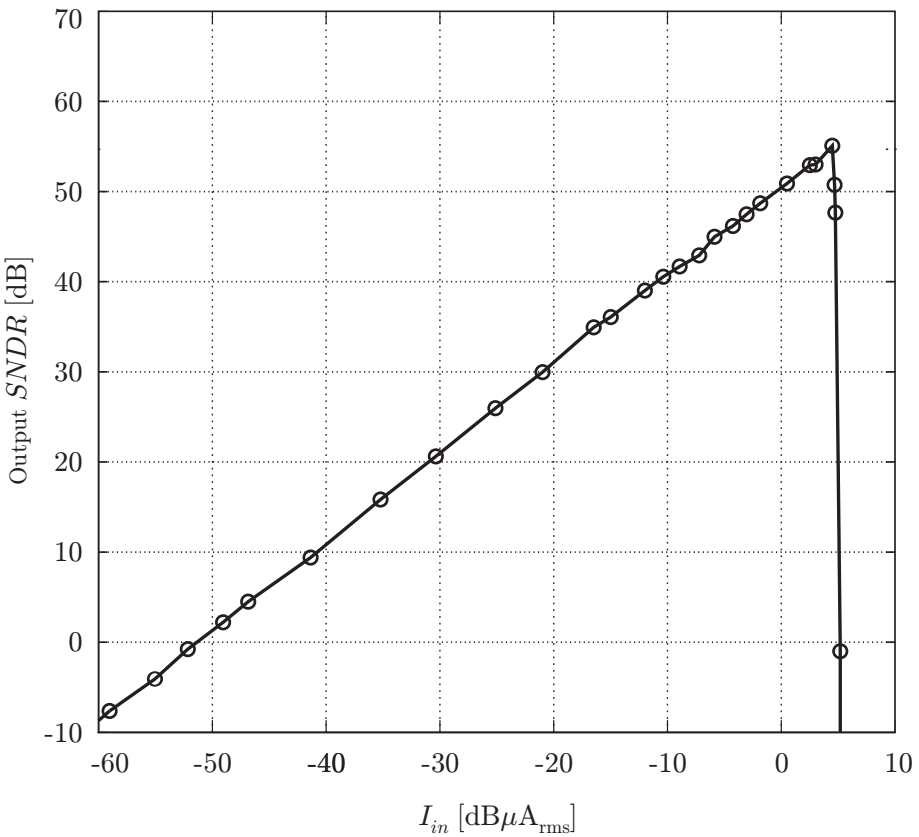
- Experimental **PSD**:



Half full-scale ($1.2\mu A_p$) & 33% RTZ

Results

- Experimental **DR**:



1kHz input & 8kHz bandwidth

- **Performance**:

Input full-scale	2.2 μA_p
Input bandwidth	8 kHz
Sampling frequency	1 MHz
DAC RTZ code	33 %
Dynamic range	9-10 bit
Supply voltage	1.2 V
$V_{TON}+\|V_{TOP}\|$	1.2 V
Power consumption	160 μW
Silicon core area	0.8 mm^2

- Better results in short due to lab update

Conclusions

- Novel **low-voltage MOS-only** ΣΔ Modulator
- **Log-domain** & **subthreshold** MOSFET based
- Circuit implementation for all **building blocks**
- Demonstrator in 0.35μm **1-polySi digital** CMOS technology