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A 60ns 500×12 0.35μm CMOS Low-Power Scanning Read-Out IC for Cryogenic Infra-Red Sensors

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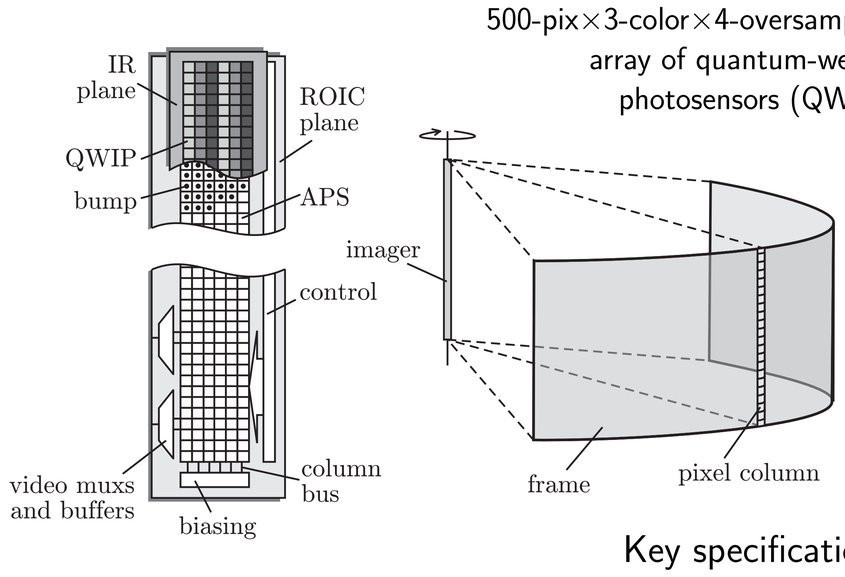
1.Introduction

CMOS read-out IC (ROIC) for a 500-pix×3-color×4-oversampling array of quantum-well IR photosensors (QWIPs)

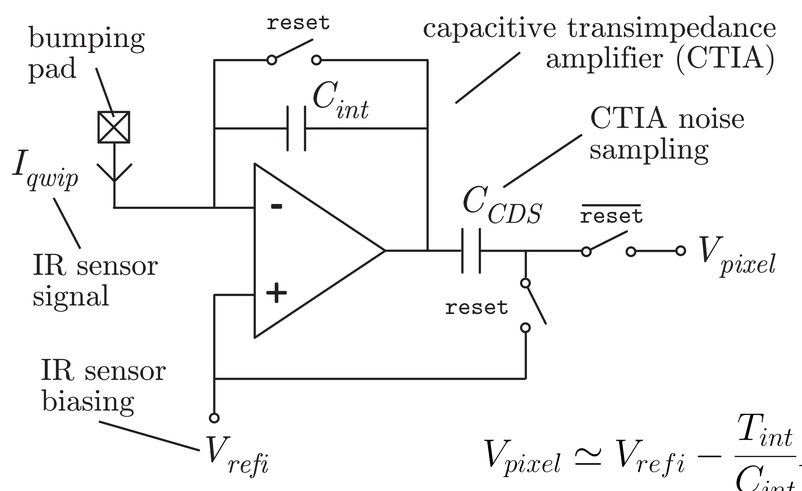


Key specifications:

- Cryogenic operation → **low-power** pixel
- Low-cost → **scanning** type and **CMOS** integration
- Real-time video → **high-speed** multiplexing
- High-resolution → **compact** pixel area
- High-sensitivity → correlated double sampling (**CDS**) and time delay integration (**TDI**)

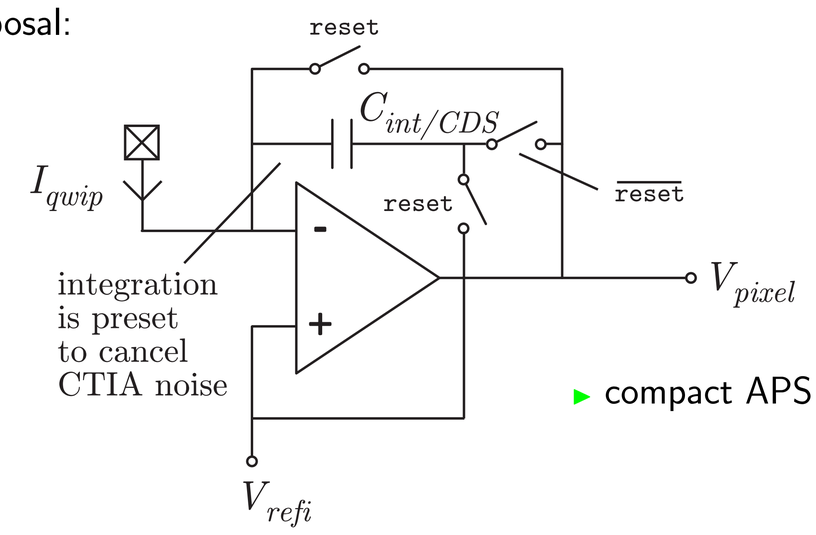
2.Active Pixel Sensor (APS)

- Classic integrator and CDS cancellation scheme:



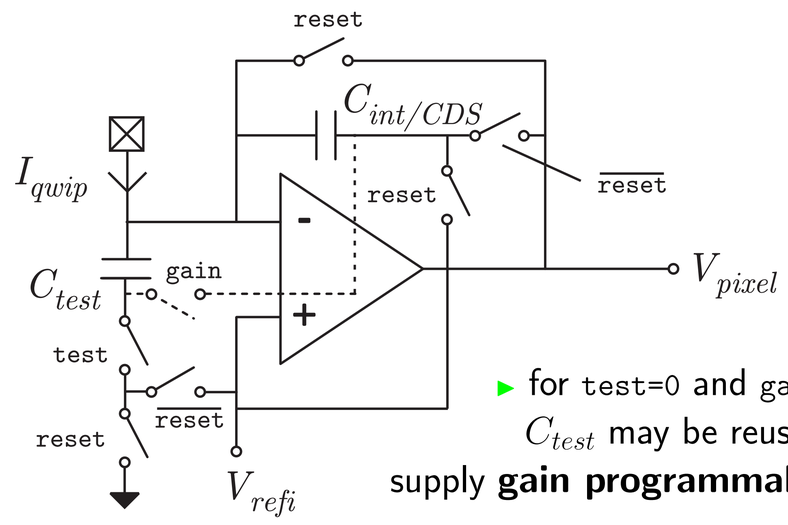
$$V_{pixel} \simeq V_{refi} - \frac{T_{int}}{C_{int}} I_{qwip}$$

- **Single-capacitor** proposal:



▸ compact APS area

- Proposed **embedded pixel-test** based on SC:

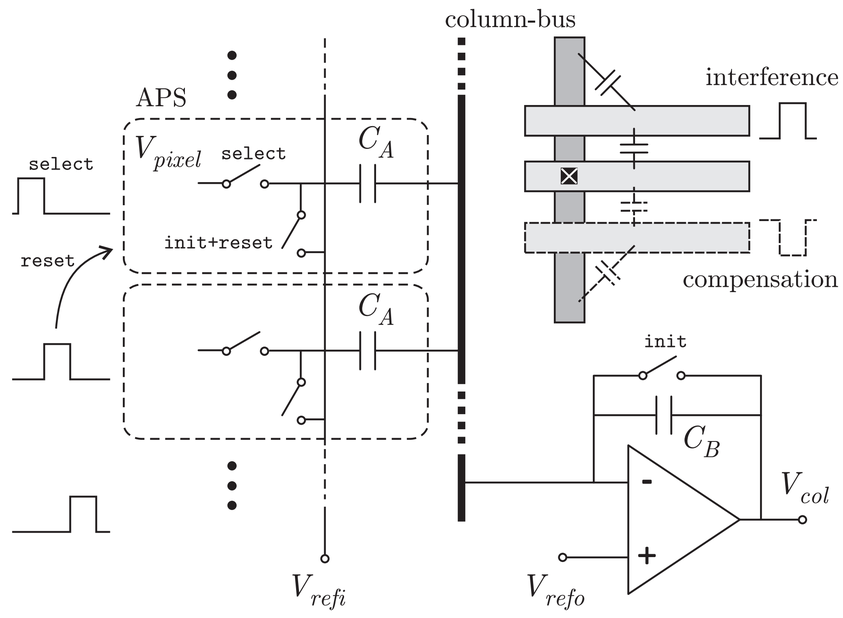


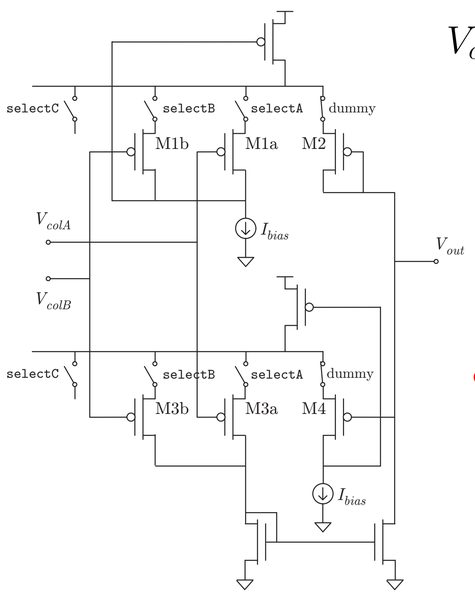
▸ for test=0 and gain=1, C_{test} may be reused to supply **gain programmability**

▸ for test=1, $V_{pixel} = \left(1 - \frac{C_{test}}{C_{int/CDS}}\right) V_{refi}$

3.Video Composition

- Pixel multiplexing in the **charge-domain**:



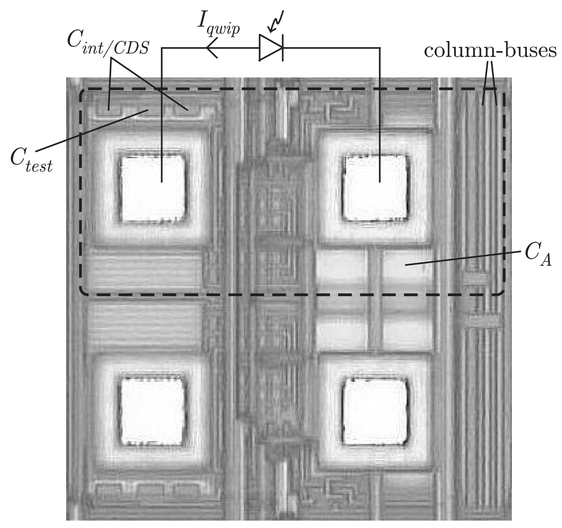


$$V_{col} = V_{refo} + \frac{C_A}{C_B}(V_{refi} - V_{pixel})$$

- ▸ scaling + shifting
- ▸ low-power APS specs
- ▸ constant voltage bus
- ▸ interference compensation

- Pseudo-differential **Class-AB** column multiplexing+buffering
  - ▸ low quiescent power
  - ▸ shared circuit area

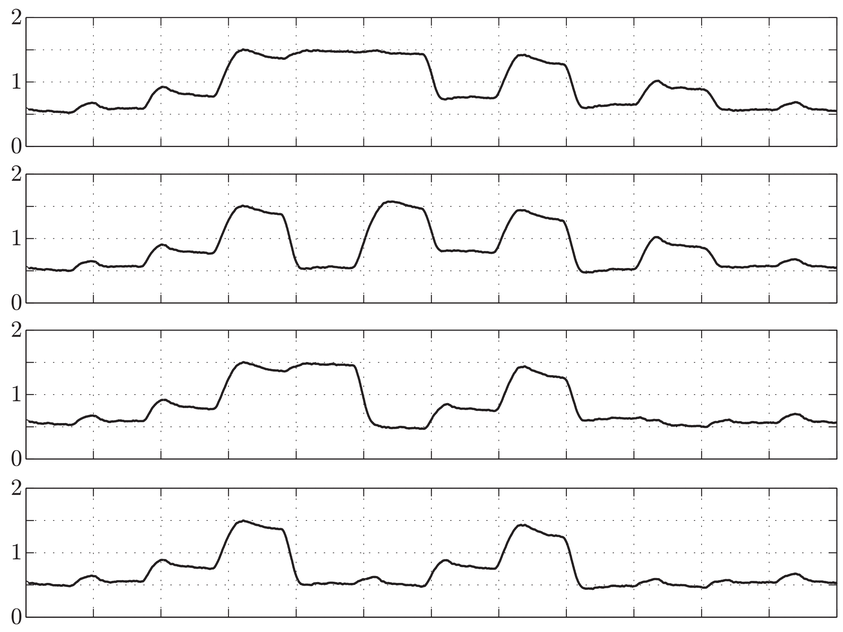
4.CMOS Integration



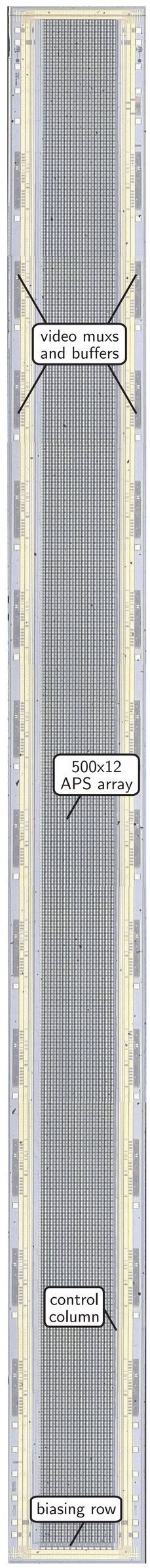
- **50μm×100μm** APS:

0.35μm CMOS 2P 3M
I_{qwip}<5nA, 77K temp.
T_{int}=15μs
I_{DD}=6μA
$C_{int/CDS}$=120fF
C_{test}=60fF
C_A=0.96pF

- **Video** multiplexing: C_B=0.55pF, T_{mux}=60ns



5.SoC



- 25×2mm^2
- 500pix×12pix
- 6000 bump-pads
- 250K MOSFETs
- LVDS signaling
- 65mA@3.3V 77K

6.Conclusions

- **Low-power** and **compact** ROIC for **cryogenic** sensors
- Novel built-in **CDS** and **test** per pixel + **charge** mux
- **Adaptable** framing (e.g. 2560×500@25fps)
- Fully integration in **standard CMOS** technology

[1] E.Seebacher, "Cryogenic C35 SPICE Models, Private communications from Austria Micro Systems," Sep 2003.