Modeling All-MOS Log-Domain ΣΔ A/D Converters

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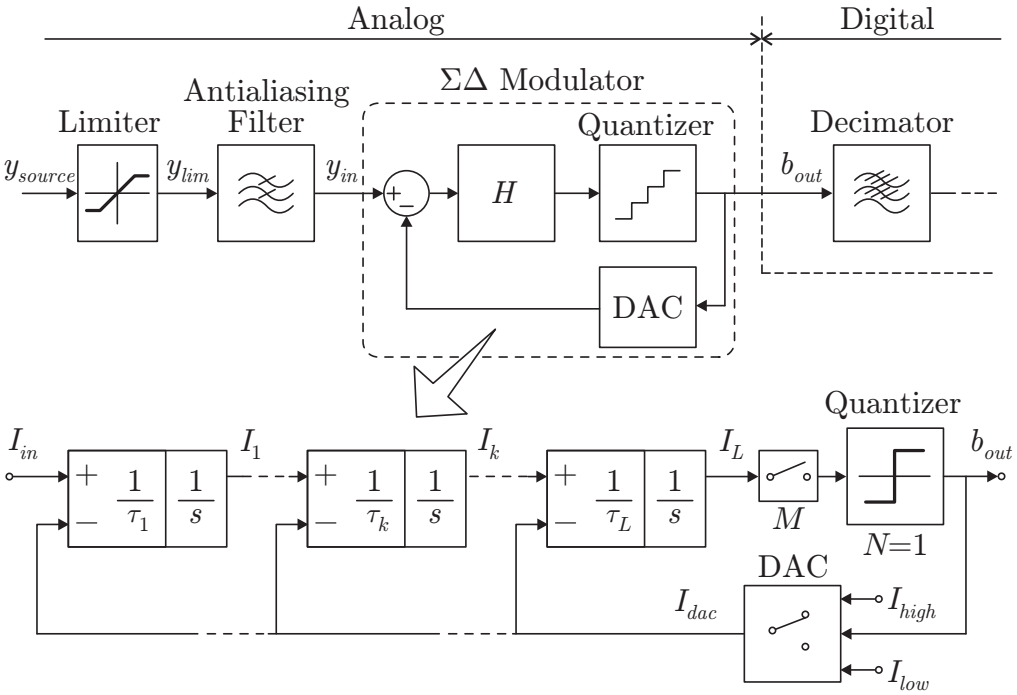
ΣΔ Modulator Architecture



$$\frac{\mathrm{d}I_k}{\mathrm{d}t} = \frac{1}{\tau_k}(I_{k-1} - I_{dac})$$

CMOS Log Domain

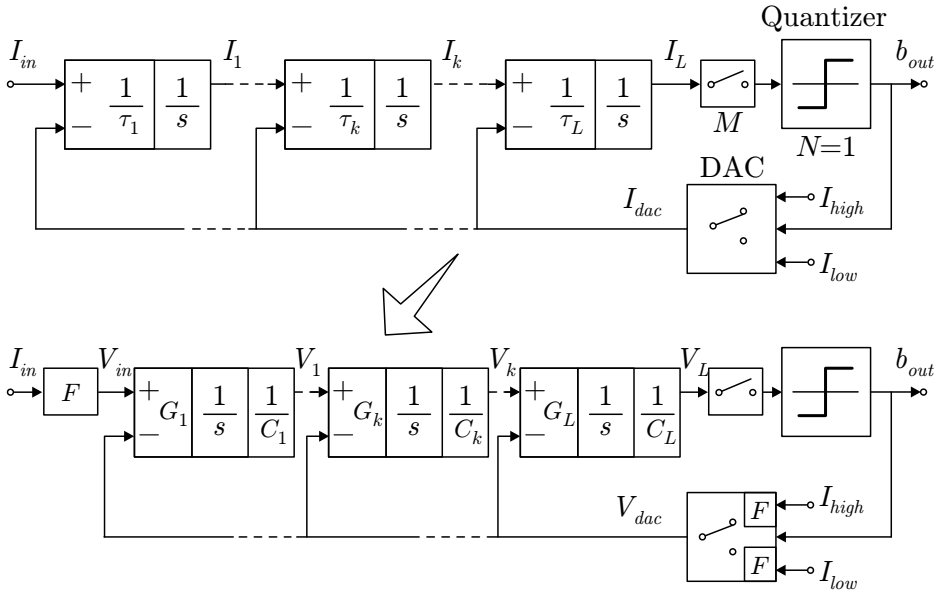
- ✔ Very low-voltage
- ✔ Low-power
- ✔ MOS-only

Simulation Issues

- ✘ High-accuracy
- ✘ Continuous-time
- ✘ Oversampling
- ✘ Pseudo-periodic

. . . need for high-level (but device-based) analytical modeling!

CMOS Log-Domain Processing

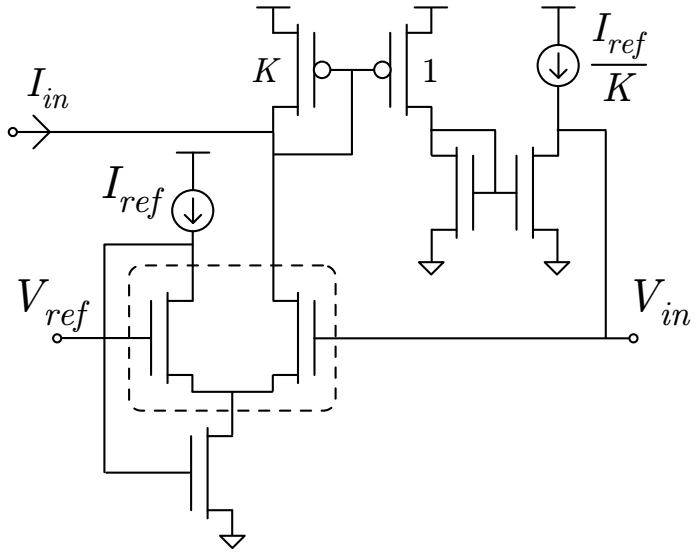


Weak inversion and forward saturation:

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}}$$

$$I_S = 2n\beta\left(\frac{W}{L}\right)U_t^2 \qquad IC = \frac{I_D}{I_S}$$

Input Compressor



$$I = F(V) = I_{ref} e^{\frac{V-V_{ref}}{nU_t}} \qquad I > 0$$

Class-A operation: $|I_{in}| < I_{ref}$

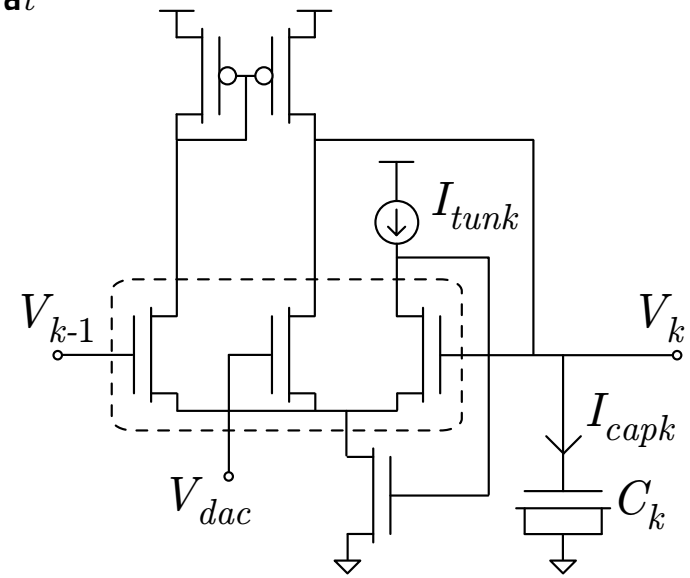
$$V_{in} = V_{ref} + nU_t \ln\left(\frac{I_{in}}{I_{ref}} + 1\right)$$

Differential Integrator

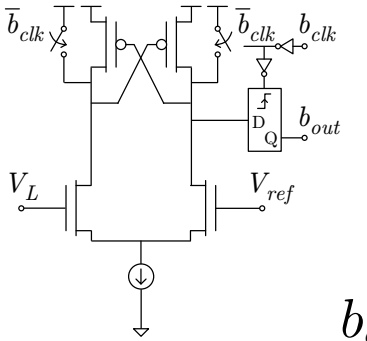
$$\frac{\mathrm{d}I_k}{\mathrm{d}t} = \frac{1}{\tau_k}(I_{k-1} - I_{dac})$$

$$\frac{\mathrm{d}V_k}{\mathrm{d}t} = \frac{nU_t}{\tau_k} e^{\frac{V_{k-1}-V_k}{nU_t}} - \frac{nU_t}{\tau_k} e^{\frac{V_{dac}-V_k}{nU_t}}$$

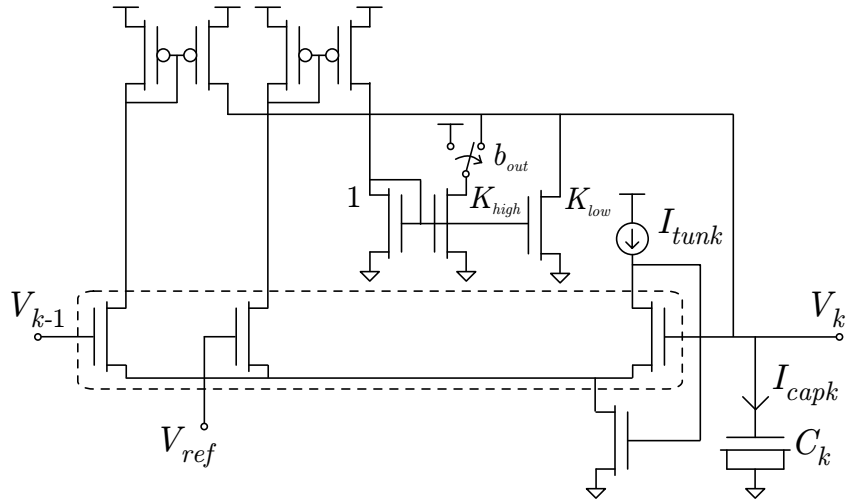
$$\underbrace{\frac{\mathrm{d}Q_k}{\mathrm{d}t}}_{C_k \frac{\mathrm{d}V_k}{\mathrm{d}t}} = \underbrace{I_{tunk}}_{\frac{nU_t C_k}{\tau_k}} e^{\frac{-V_k}{nU_t}} \left(e^{\frac{V_{k-1}}{nU_t}} - e^{\frac{V_{dac}}{nU_t}} \right)$$



Quantizer and Built-in DAC



$$b_{out} = \begin{cases} 1 & V_L > V_{ref} \\ 0 & V_L \leq V_{ref} \end{cases}$$



$$V_{dac} = V_{ref} + nU_t \ln\left(\frac{I_{high} b_{out} + I_{low} \bar{b}_{out}}{I_{ref}}\right)$$

Thermal Noise

- PSD in Class-A:

$$\frac{\mathrm{d}i_{Dn}^2}{\mathrm{d}f} = 4KT\frac{g_{ms}}{2} \equiv 2qI_D$$

- Input compressor:

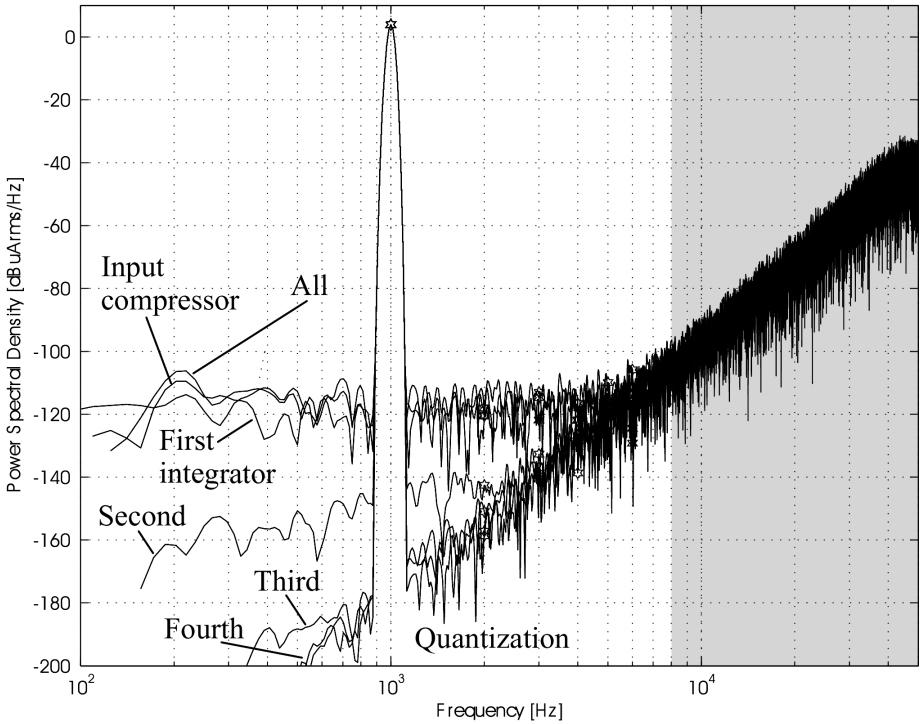
$$\frac{\mathrm{d}v_{inn}^2}{\mathrm{d}f} \simeq 4q\frac{(nU_t)^2}{I_{ref}}$$

- Integrator+DAC:

$$\frac{\mathrm{d}i_{capkn}^2}{\mathrm{d}f} \simeq 2q(2+K_{low}+b_{out}K_{high})I_{tunk}$$

$$K_{low} = \frac{I_{low}}{I_{tunk}} \quad K_{high} = \frac{I_{high}-I_{low}}{I_{tunk}} \equiv \frac{I_{full}}{I_{tunk}}$$

- Block contributions:



$$SNR \propto +3\mathrm{dB}/oct(I_{ref})$$

Moderate Inversion

- Degradation of the e^x:

$$I_D = I_S \ln^2\left(1 + e^{\frac{V_{GB}-V_{TO}}{2nU_t}} e^{-\frac{V_{SB}}{2U_t}}\right)$$

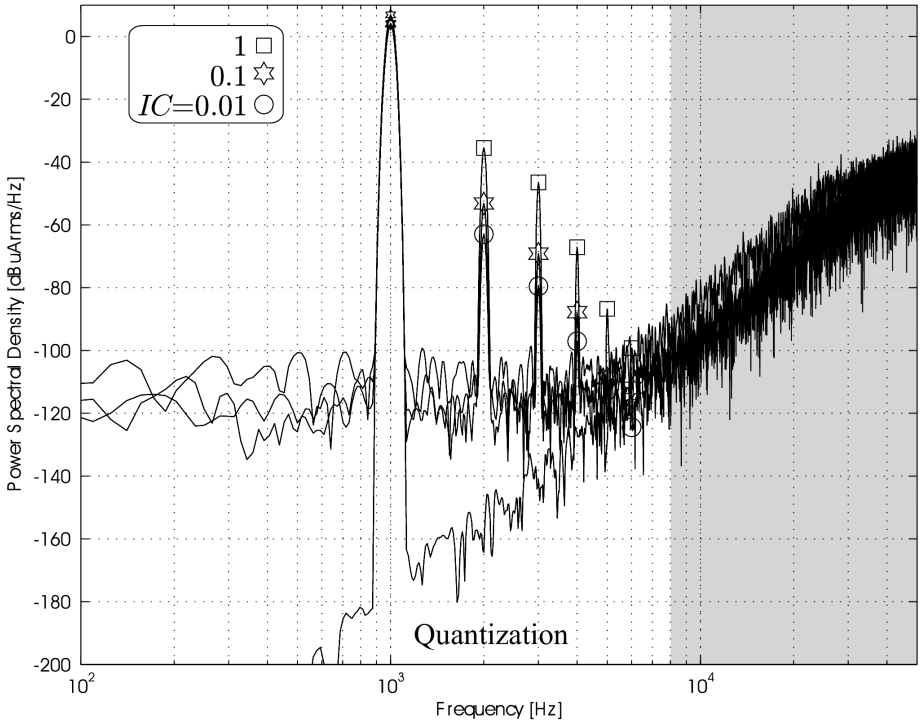
- Input compressor:

$$V_{in} = V_{ref} + nU_t \ln\left(\frac{e^{\sqrt{\frac{I_{in}+I_{ref}}{I_S}}} - 1}{e^{\sqrt{\frac{I_{ref}}{I_S}}} - 1}\right)^2$$

- Integrator+DAC:

$$I_{capk} = I_S \ln^2\left[1 + e^{\frac{V_{k-1}-V_k}{2nU_t}}\left(e^{\sqrt{\frac{I_{tunk}}{I_S}}} - 1\right)\right] - I_S \ln^2\left[1 + e^{\frac{V_{dac}-V_k}{2nU_t}}\left(e^{\sqrt{\frac{I_{tunk}}{I_S}}} - 1\right)\right]$$

- Inversion coefficient dependence:



$$SDR \quad \Leftarrow \quad IC = \frac{I_D}{I_S}$$

MOS Capacitors

- Non-linear capacitors:

$$\frac{\mathrm{d}Q_k}{\mathrm{d}t} = \left(C_k + \frac{\mathrm{d}C_k}{\mathrm{d}V_k}V_k\right)\frac{\mathrm{d}V_k}{\mathrm{d}t}$$

- NMOS capacitance:

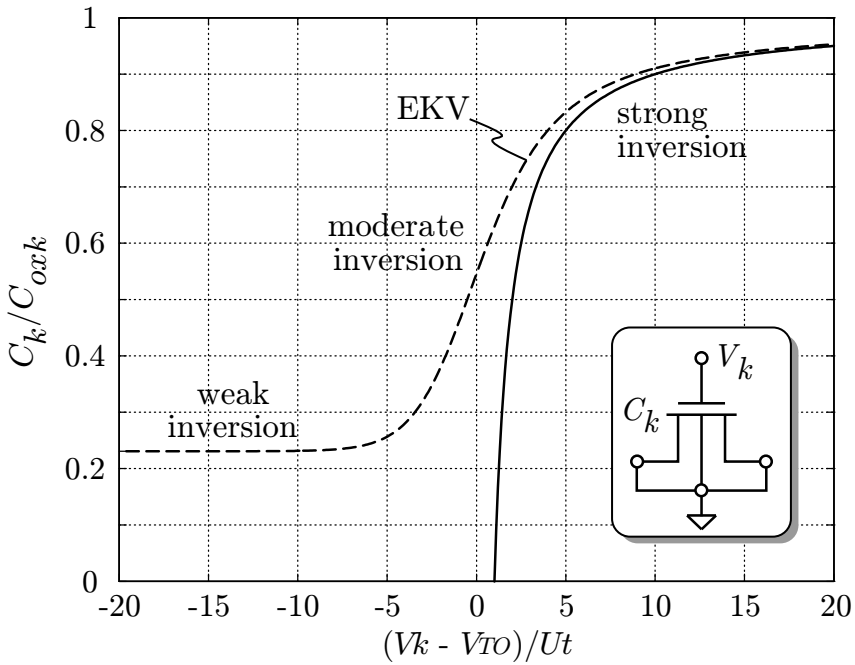
$$C_k \simeq C_{oxk}\left(1 - \frac{U_t}{V_k - V_{TO}}\right)$$

- Integrator ODE:

$$\frac{\mathrm{d}V_k}{\mathrm{d}t} = \frac{I_{tunk}}{C_{oxk}}\frac{e^{\frac{-V_k}{nU_t}}}{1 + \frac{V_{TO}U_t}{(V_k - V_{TO})^2}}\left(e^{\frac{V_{k-1}}{nU_t}} - e^{\frac{V_{dac}}{nU_t}}\right)$$

$$SDR \Leftarrow V_{ref} - V_{TO}$$

- Strong inversion asymptote:



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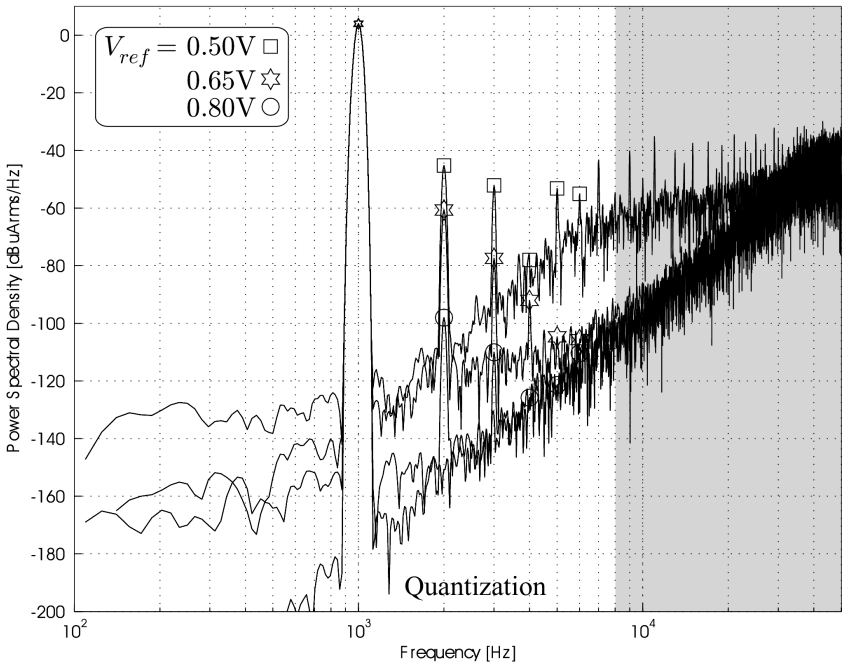
- Integrator ODE:

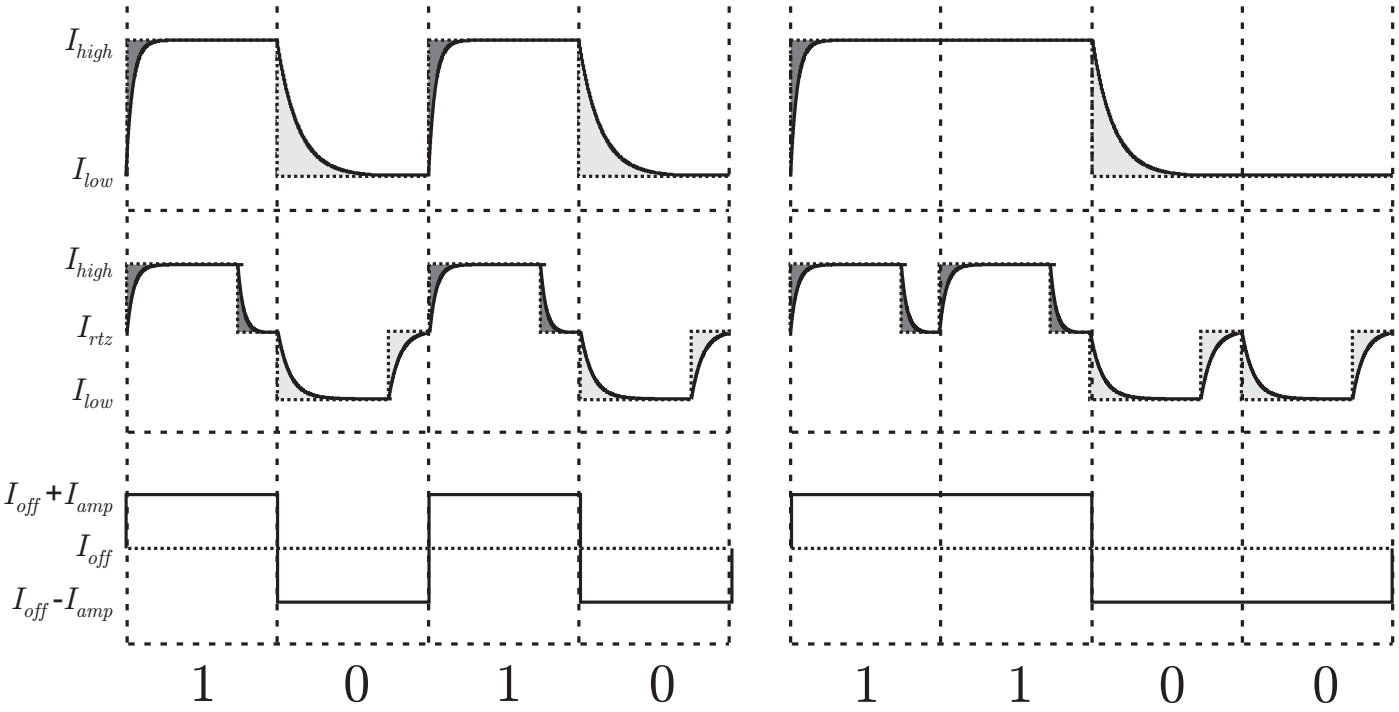
$$\frac{\mathrm{d}V_k}{\mathrm{d}t} = \frac{I_{tunk}}{C_{oxk}}\frac{e^{\frac{-V_k}{nU_t}}}{1 + \frac{V_{TO}U_t}{(V_k - V_{TO})^2}}\left(e^{\frac{V_{k-1}}{nU_t}} - e^{\frac{V_{dac}}{nU_t}}\right)$$

- OP dependence ($V_{TON} \simeq 0.5$V):



$$SDR \quad \Leftarrow \quad V_{ref} - V_{TO}$$

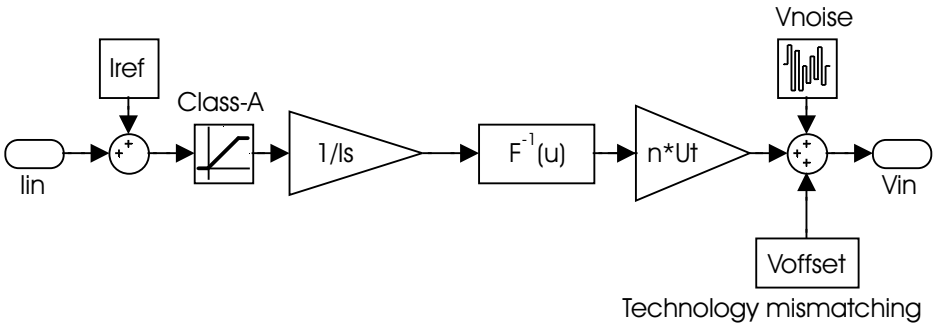
DAC Waveform Asymmetry



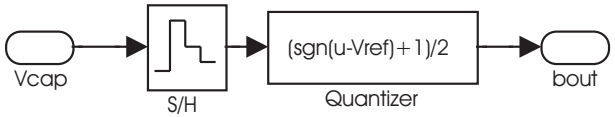
- ✗ WA signal dependencies
  ⇓
  In-band noise injection!
- ✓ Return-to-zero (I_{rtz}) techniques

Equivalent model: input offset (I_{off}) + full-scale reduction (I_{amp})

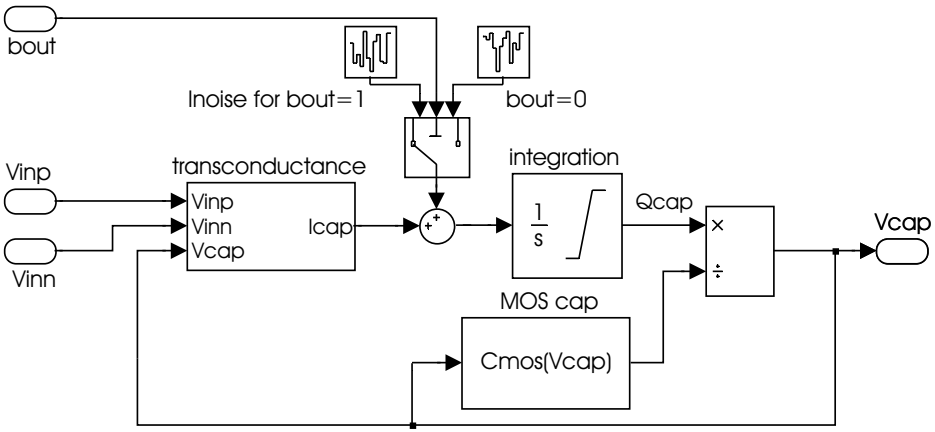
Block Models (e.g. Simulink)



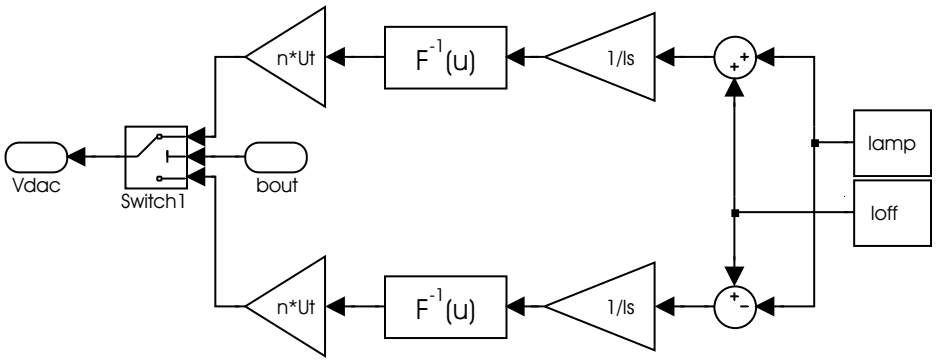
Input compressor



Quantizer



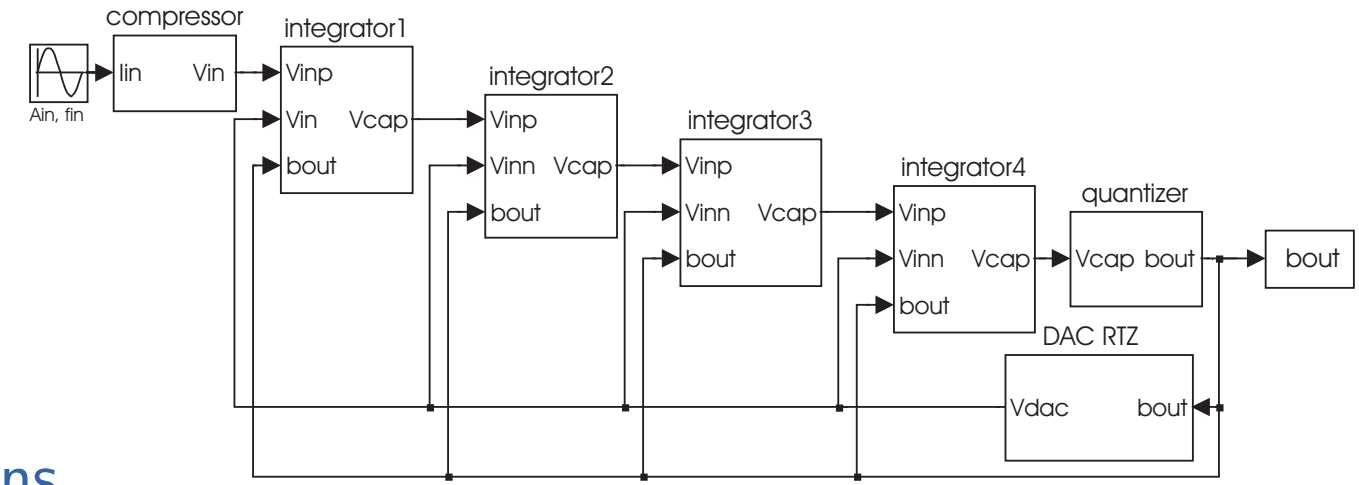
Integrator



DAC (common to optimize simulation speed)

Architecture

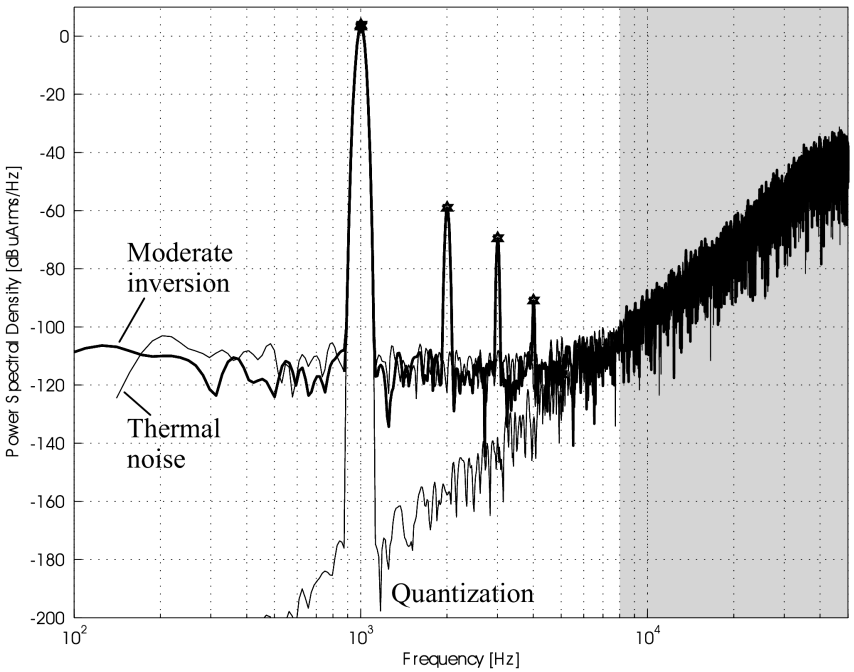
A 4th-order 64× 1bit single-loop ΣΔ modulator:



Specifications

Input full-scale	$6\mu A_{pp}$
Bandwidth	100Hz-8KHz
Sampling frequency	1.024MHz
RTZ period	10%-50% programmable
Biasing	I_{ref}=7μA and V_{ref}=0.7V
Tuning	I_{tunk}={7,1,1,1}μA and C_{oxk}={210,30,12,12}×5pF
Supply	V_{DD}=1.2V and $P_D \simeq 160\mu W$
Technology	0.35μm CMOS digital $V_{TON}+\lvert V_{TOP}\rvert \simeq 1.2V$

Design Process

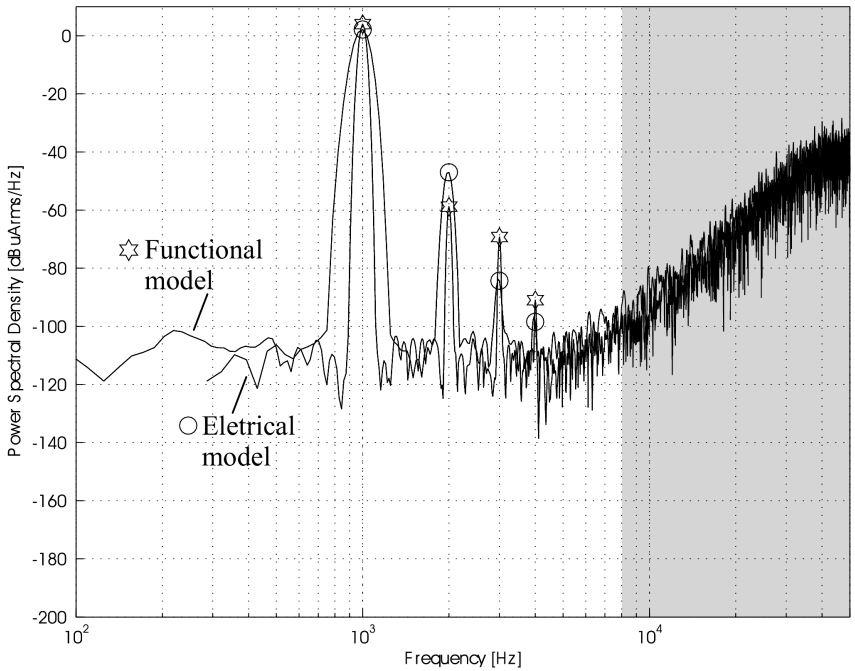


fast high-level model

⇓

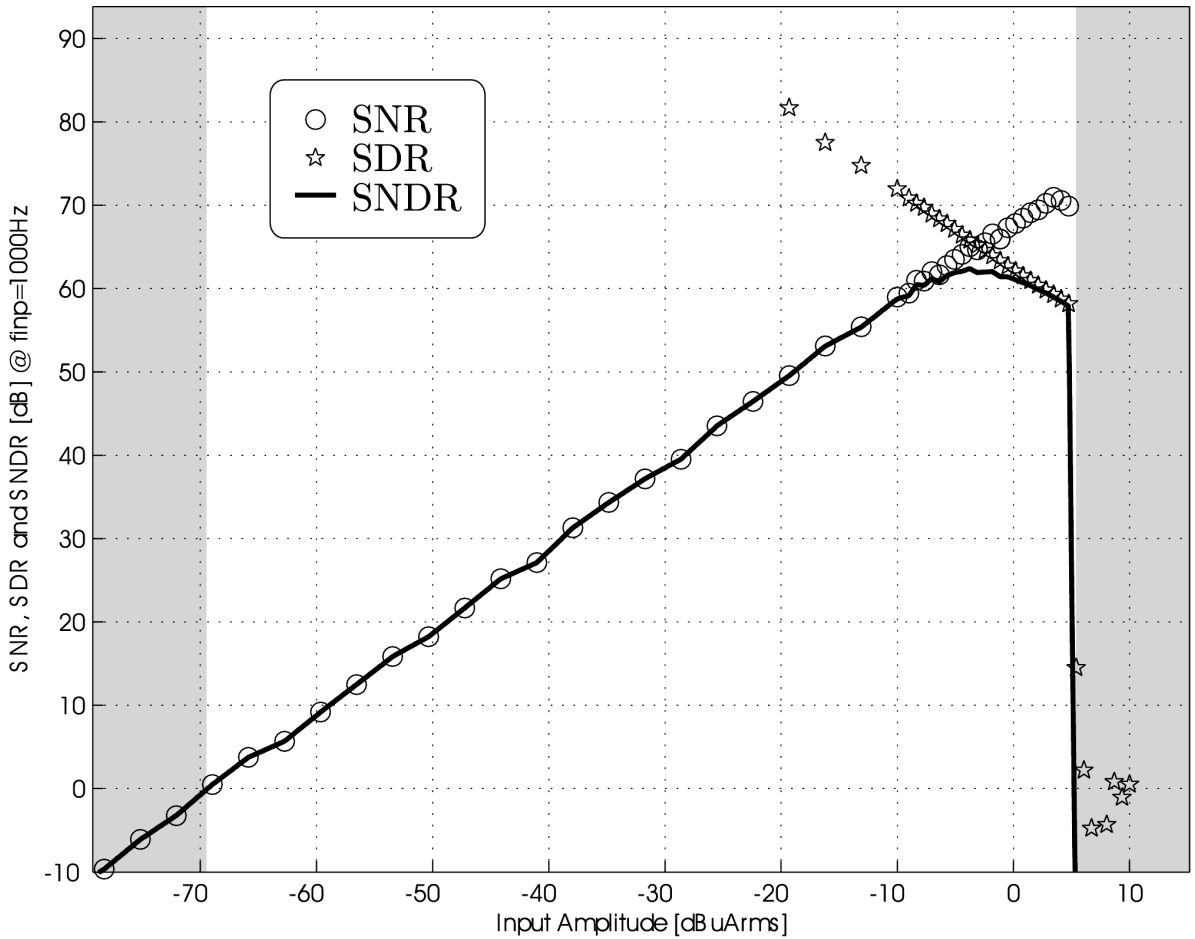
optimal circuit parameters

Functional vs Electrical



SPICE validation

Performance Estimations



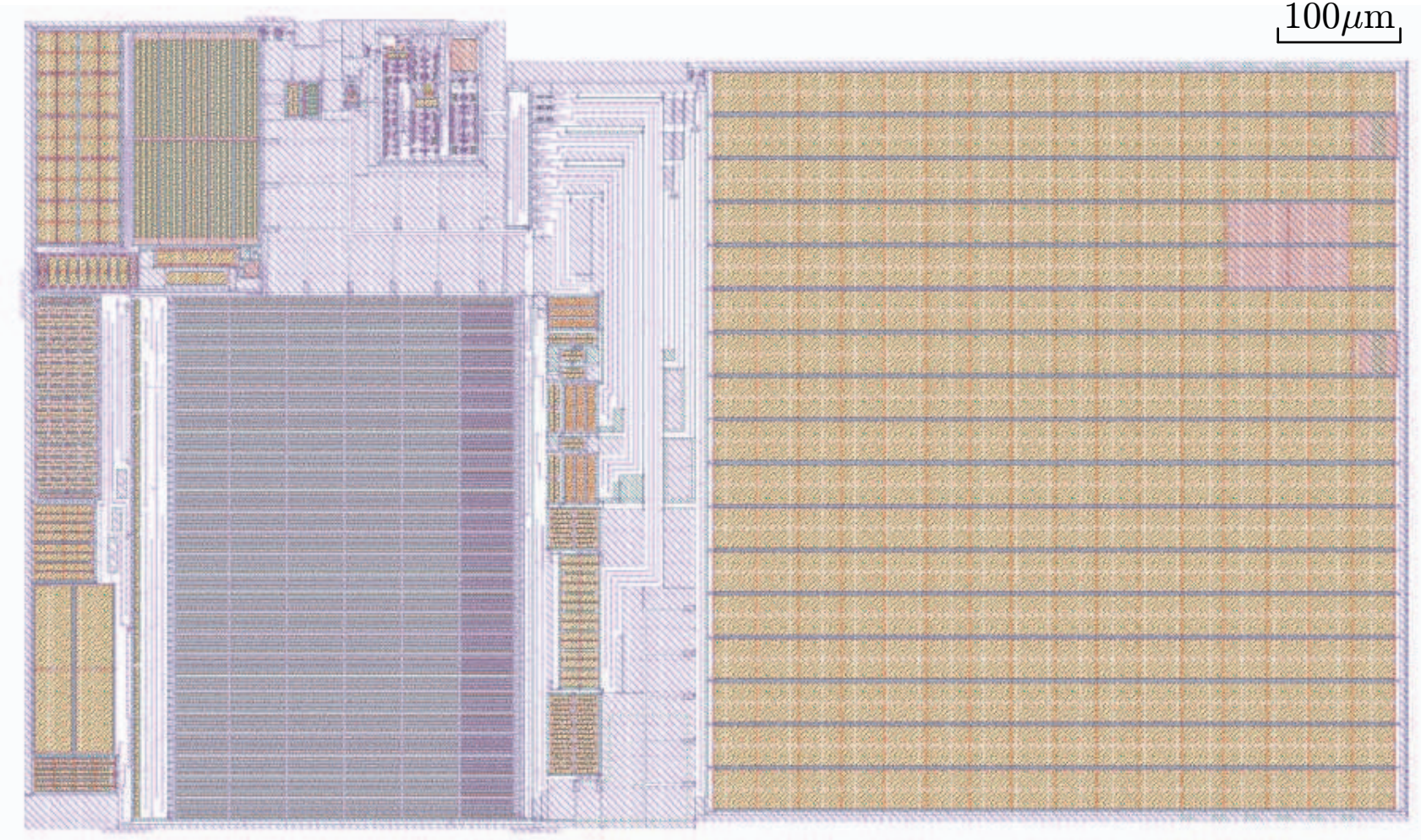
Simulation:

electrical
18 weeks
↓
functional
1 hour

÷3000!

DR=74dB(12b) and $SNDR_{max}$=62dB at -4dBμA_{rms}

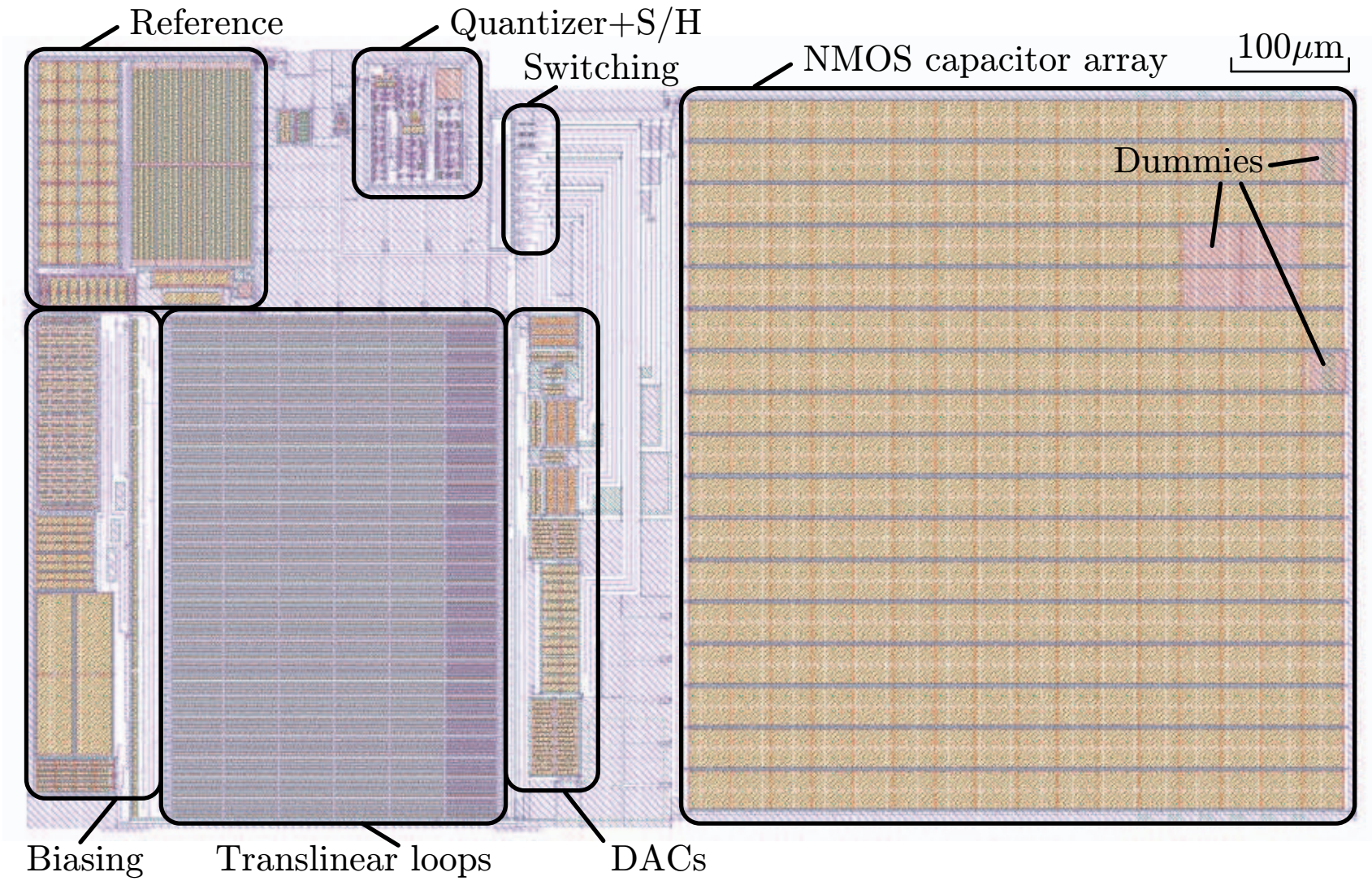
Final Design



Total area: 650μm×1130μm=0.73mm^2

. . . to be integrated soon!

Final Design



Total area: $650\mu m \times 1130\mu m = 0.73 mm^2$

. . . to be integrated soon!

Main Results

- Accurate **high-level** modeling of log-domain CMOS ΣΔ ADCs.
- **Analytical** circuit study + advanced MOSFET models.
- Simulation **speed** improved by more than 1000 times.
- Independent evaluation of each **non-ideality or block** effect.
- ADC **complete** performance estimations can be iterated.
- **Example** for a 4th-order 64× 1bit single-loop ΣΔ modulator.