Exact Design of All-MOS Log Filters

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Introduction

Low-voltage MOS-C log circuits

Generalization to non-linear capacitors

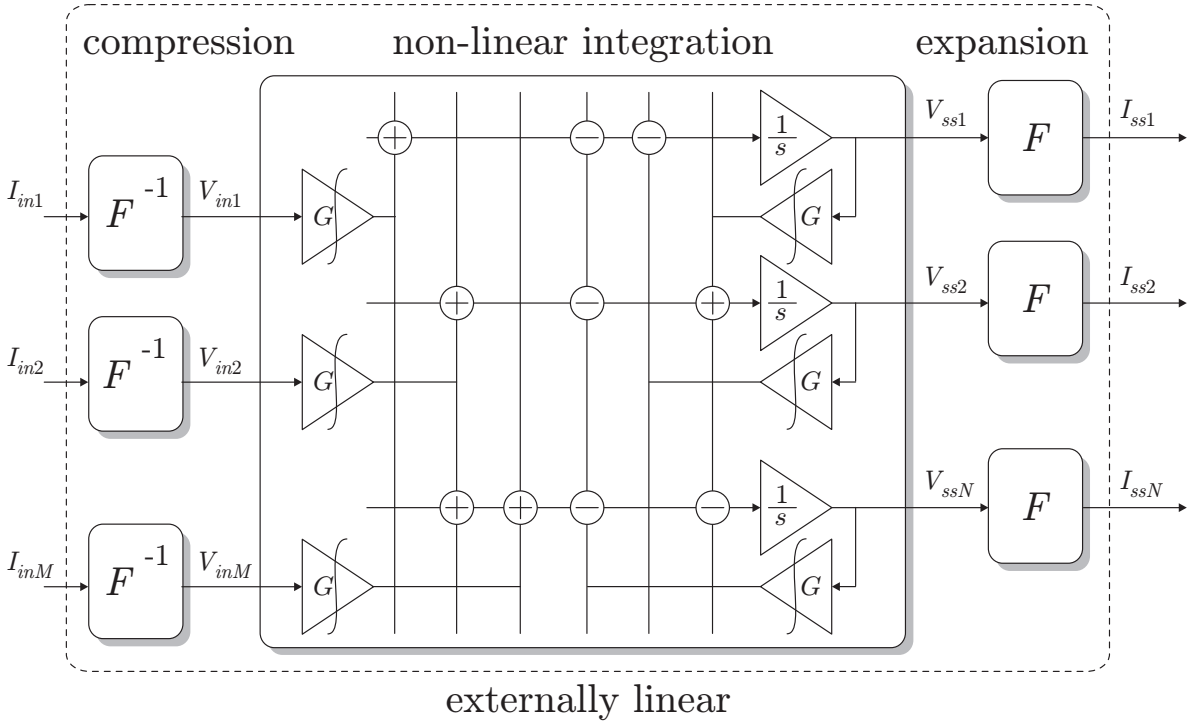
Exact all-MOS proposal

Design examples

Conclusions

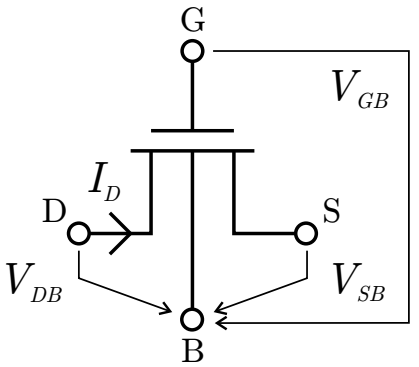
Instantaneous companding filters

$$\frac{d\bar{I}_{ss}}{dt} = \bar{A}\bar{I}_{ss} + \bar{B}\bar{I}_{in} \qquad \bar{I}_{out} = \bar{C}\bar{I}_{ss} + \bar{D}\bar{I}_{in}$$



- ✓ High-frequency (bipolar)
- ✓ Low-voltage
- ? Non-linear capacitors

MOS log-mapping



weak inversion:

$$V_{SB,DB} \gg \frac{V_{GB}-V_{TO}}{n}$$

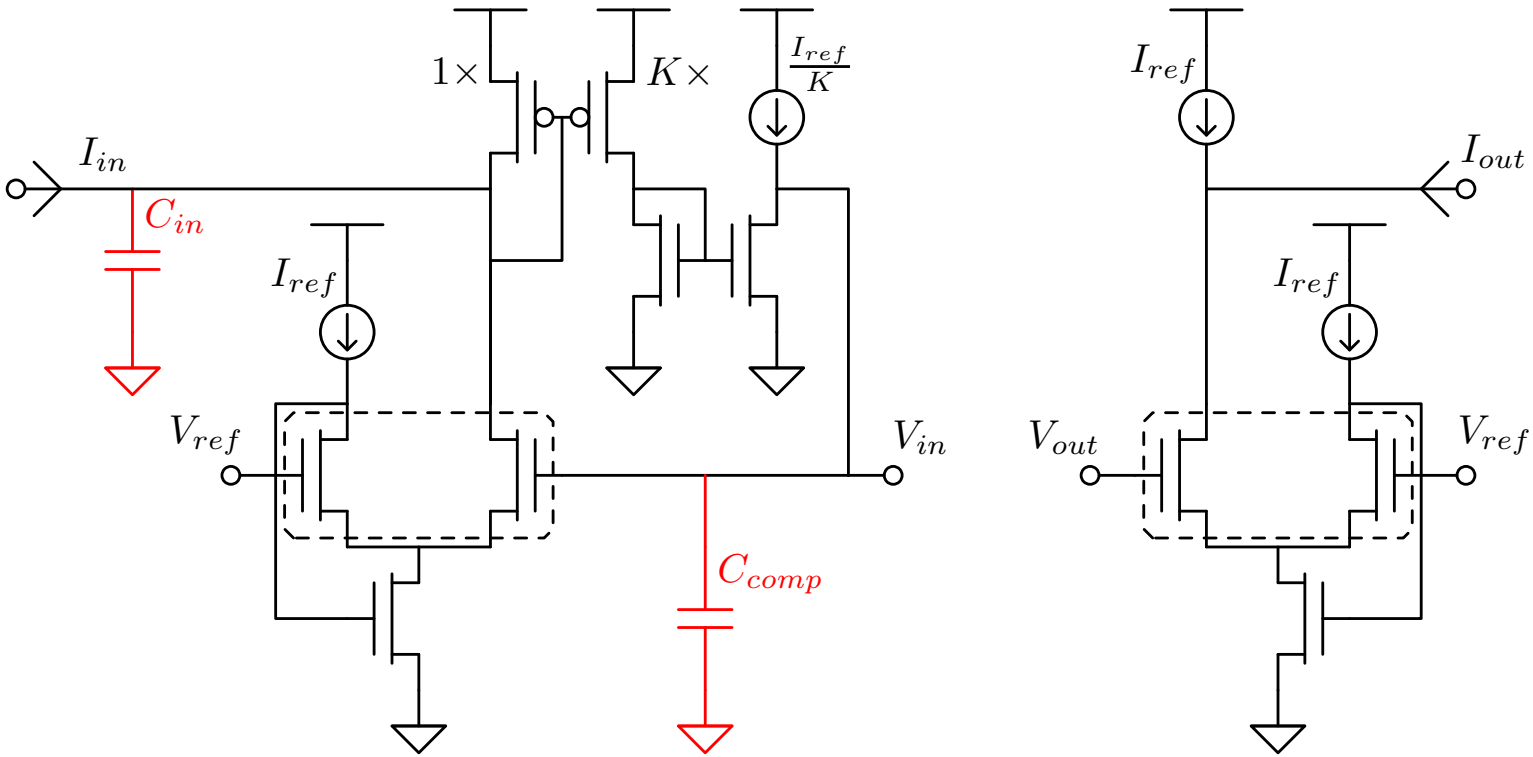
forward saturation:

$$V_{DB} - V_{SB} \gg U_t$$

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}}$$

$$I_S = 2n\beta U_t^2 \quad IC = \frac{I_D}{I_S}$$

Compressors and expanders



- Companding function: $I = F(V) = I_{ref} e^{\frac{V - V_{ref}}{nU_t}} \qquad I > 0$
- Class-A operation: $I_{max} \equiv \frac{I_{ref}}{2}$
- Frequency compensation of input parasitics: $\zeta = \frac{1}{2}\sqrt{\frac{KC_{comp}}{C_{in}}}$

Integrators

$$\bar{A} = \begin{bmatrix} & \cdots & \\ +\frac{1}{\tau_{21}} & -\frac{1}{\tau_{22}} & +\frac{1}{\tau_{23}} \\ & \cdots & \end{bmatrix}$$

single-coefficient linear ODE:

$$\frac{dI_{out}}{dt} = \pm\frac{1}{\tau} I_{in}$$

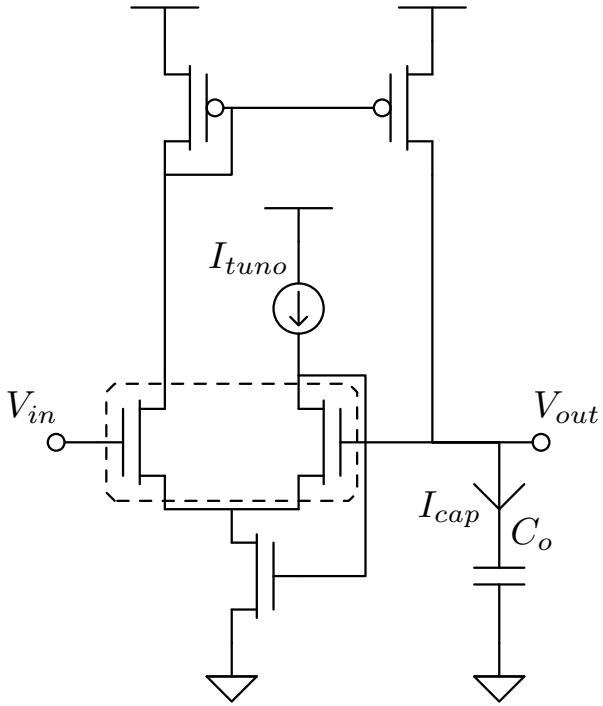
non-linear ODE in the compressed domain:

$$\frac{dV_{out}}{dt} = \pm\frac{nU_t}{\tau} e^{\frac{V_{in}-V_{out}}{nU_t}}$$

circuit realization in the Q-domain:

$$\frac{dQ_{out}}{dt} = \underbrace{C_o \frac{dV_{out}}{dt}}_{I_{cap}} = \pm I_{tuno} e^{\frac{V_{in}-V_{out}}{nU_t}}$$

$$I_{cap} = G(V_{in}, V_{out}) \qquad \tau = \frac{nU_t C_o}{I_{tuno}}$$



- Single phase ($+\frac{1}{\tau}$ case)
- Operating point ensured by the $\bar{A}$ matrix
- Half of G can be shared by the same row of $\bar{A}$
- Valid only for grounded linear capacitors

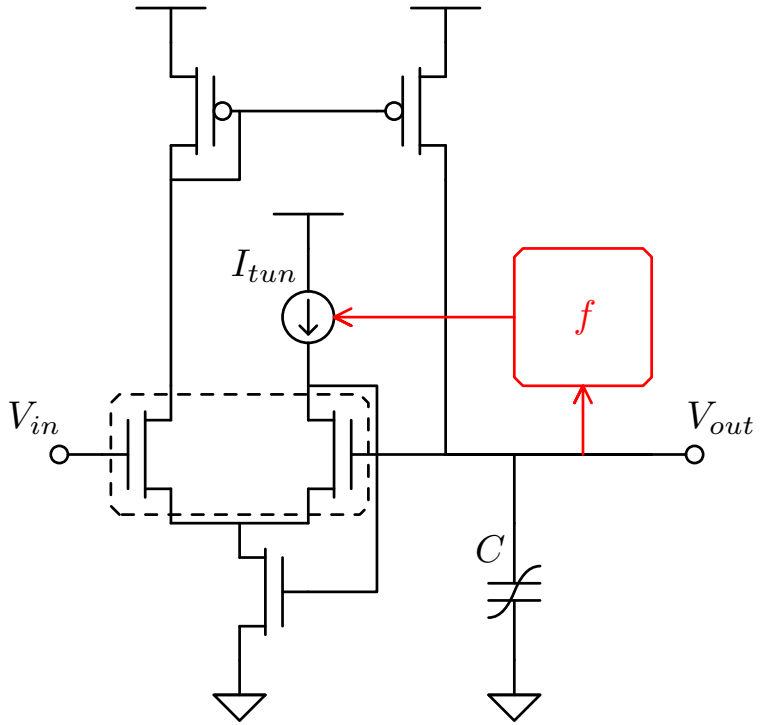
Voltage-dependent capacitors

$$\frac{dQ_{out}}{dt} = C\frac{dV_{out}}{dt} + \frac{dC}{dt}V_{out}$$

$$\frac{dQ_{out}}{dt} = \left(C + \frac{dC}{dV_{out}}V_{out}\right)\frac{dV_{out}}{dt}$$

distortion due to:

- Signal swing (V_{out})
- Non-constant capacitance ($\frac{dC}{dV_{out}}$)



Tuning compensation strategy

$$\frac{I_{tun}}{I_{tuno}} = \frac{C}{C_o} + \frac{dC}{dV_{out}}\frac{V_{out}}{C_o} \doteq f(V_{out})$$

- Valid for non-abrupt C-V
- Linear case reduction:

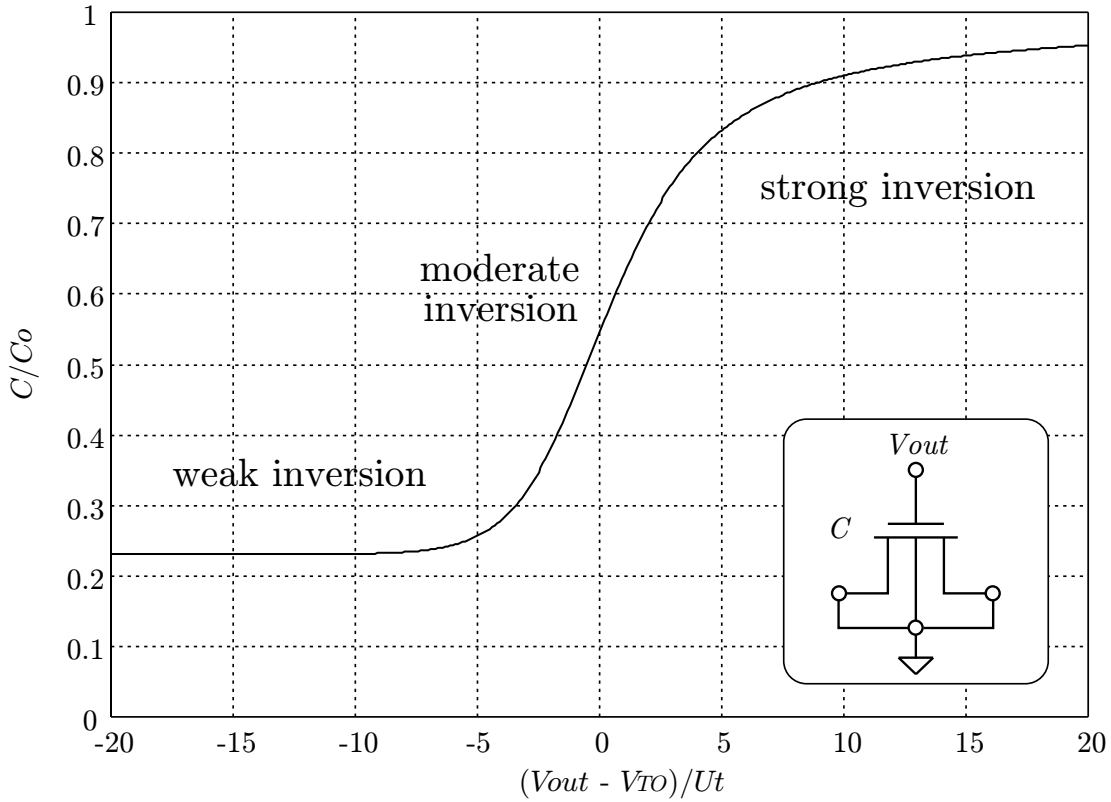
$$\frac{dC}{dV_{out}} = 0 \qquad I_{tun} \equiv I_{tuno}$$

Grounded NMOS device

- Single poly-Si structure ✓
- Digital process compatible ✓
- High-density [F/m^2] ✓

$$C_{gate} \gg C_{poly-poly}$$

- Strong non-linearity around V_{TO} ×
- Low-voltage versus distortion ?
  (i.e. V_{ref} vs V_{TO})



Analytical compensation

all-regions quasi-static C_{GG}:

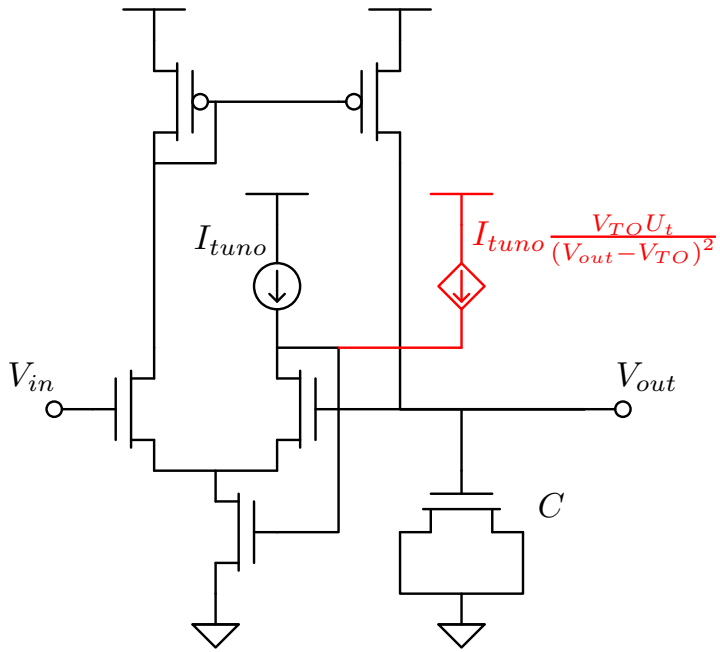
$$C = C_o \frac{\frac{n-1}{n} + 2\sqrt{IC}\left(1 - e^{-\sqrt{IC}}\right)}{1 + 2\sqrt{IC}\left(1 - e^{-\sqrt{IC}}\right)}$$

$$IC = \ln^2\left(1 + e^{\frac{V_{out} - V_{TO}}{2nU_t}}\right)$$

for $V_{out,ref} \geq V_{TO}$ (i.e. $IC \gg 1$):

$$\frac{C}{C_o} = 1 - \frac{U_t}{V_{out} - V_{TO}}$$

$$\frac{I_{tun}}{I_{tuno}} = 1 + \frac{V_{TO}U_t}{(V_{out} - V_{TO})^2}$$



equivalent to add
a positive signal-dependent
tuning current...

Circuit realization

$$\frac{I_{tun}}{I_{tuno}} = 1 + \frac{V_{TO}U_t}{(V_{out} - V_{TO})^2}$$

matched device in strong inversion:

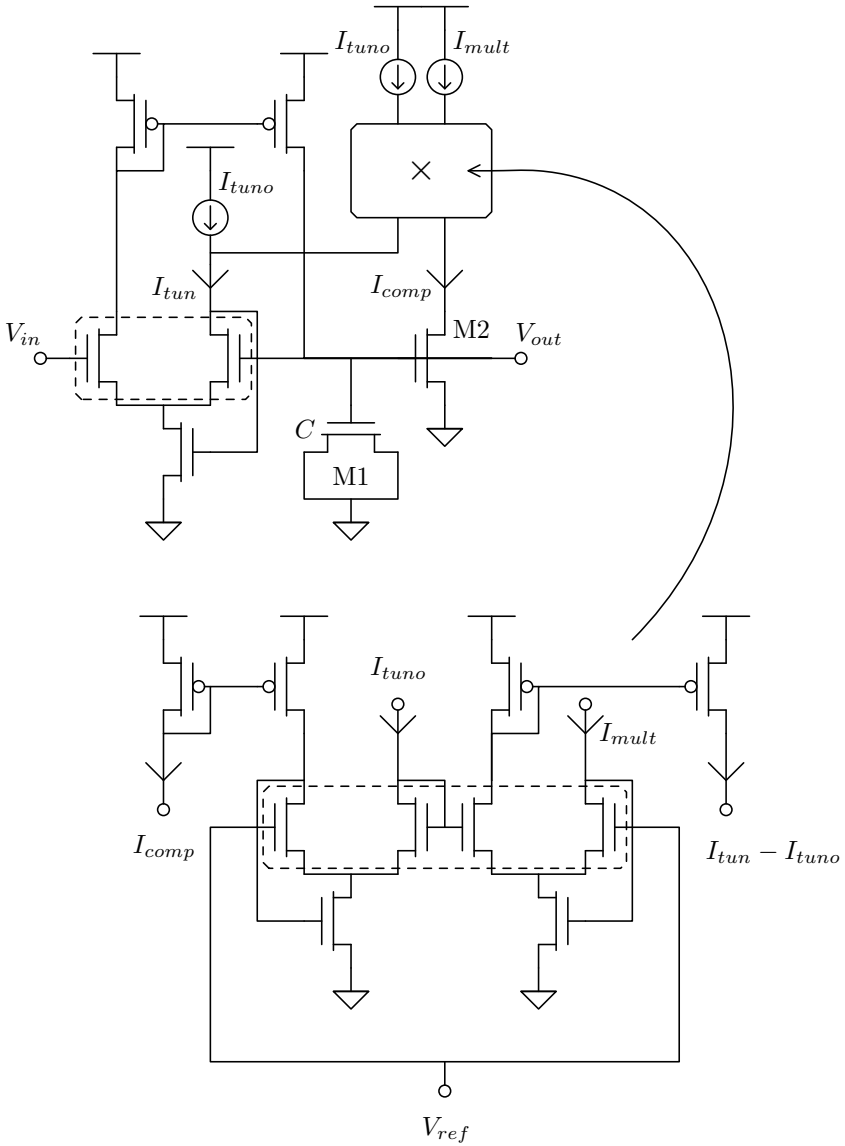
$$I_{comp} = \frac{\beta_2}{2n}(V_{out} - V_{TO})^2$$

$$I_{tun} = I_{tuno} + \frac{I_{tuno}}{I_{comp}}\frac{I_{S2}V_{TO}}{(2n)^2U_t}$$

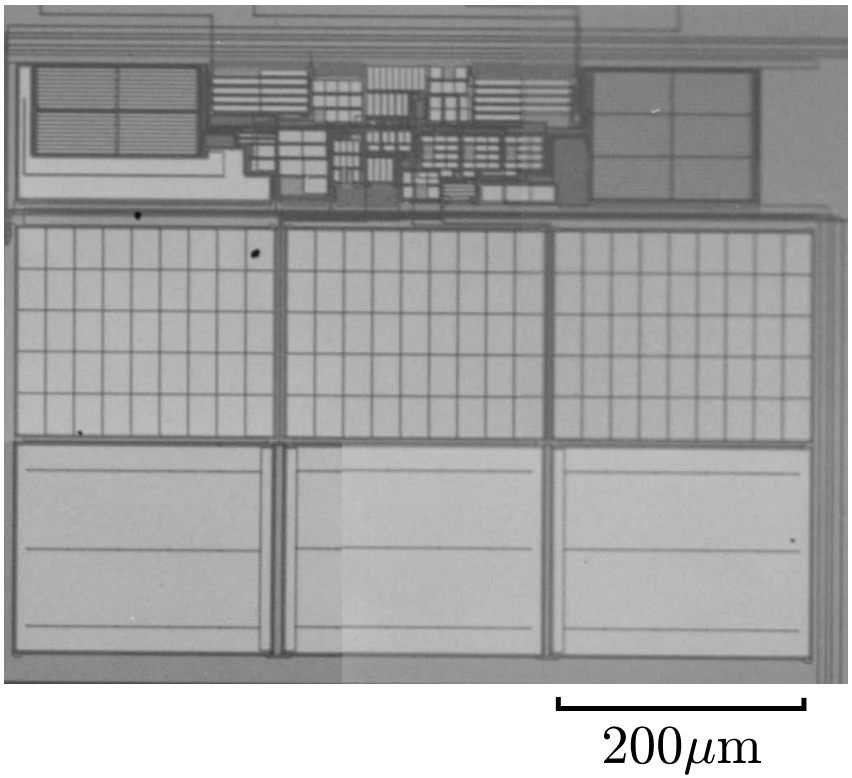
tuning compensation synthesis:

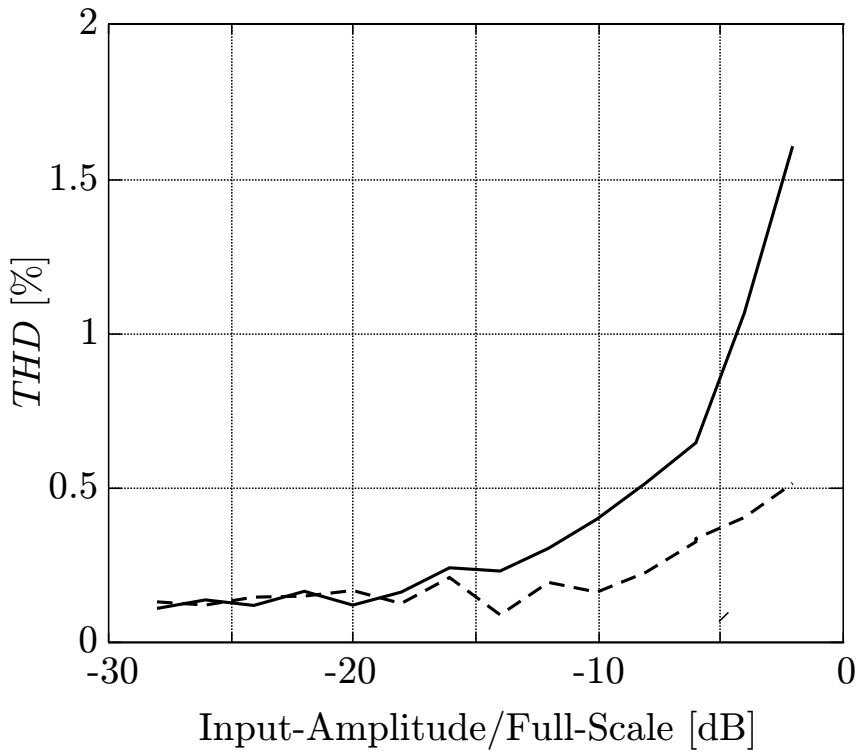
$$I_{tun} = I_{tuno} + \frac{I_{tuno}I_{mult}}{I_{comp}}$$

$$I_{mult} = I_{S2}\frac{V_{TO}}{(2n)^2U_t}$$



Third-order low-pass filter

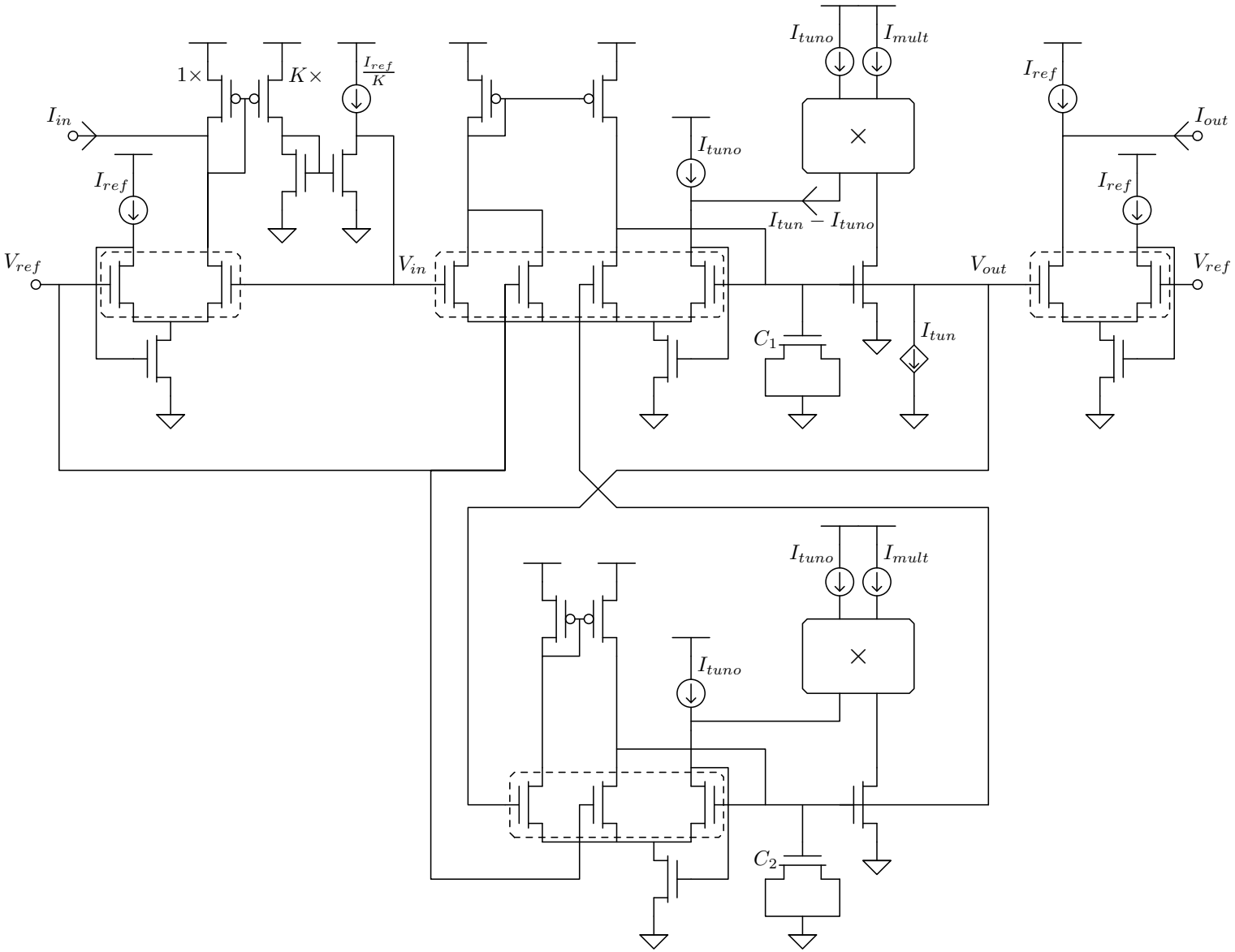




- 0.35μm technology
- Poly-Si(dashed) versus NMOS(solid) results

- $f_{-3dB} = 8$KHz $\quad f_{in} = 2$KHz
- V_{DD} =1.2V $\quad V_{ref}$ =0.6V

Second-order band-pass filter



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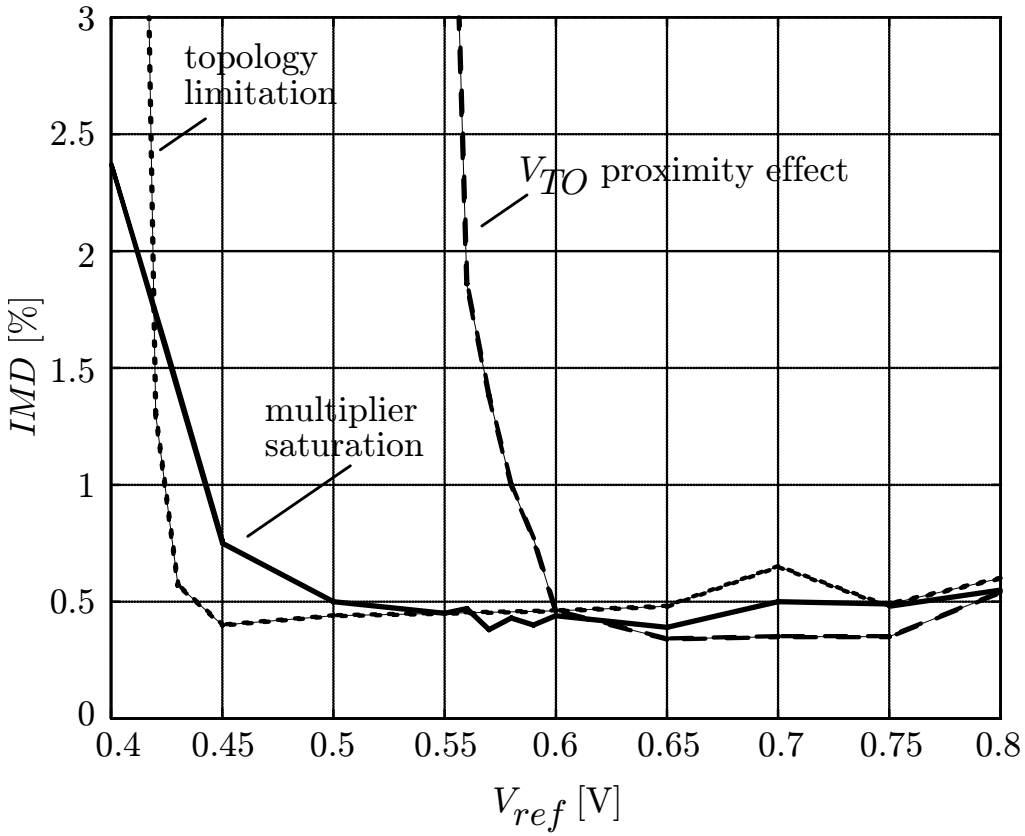
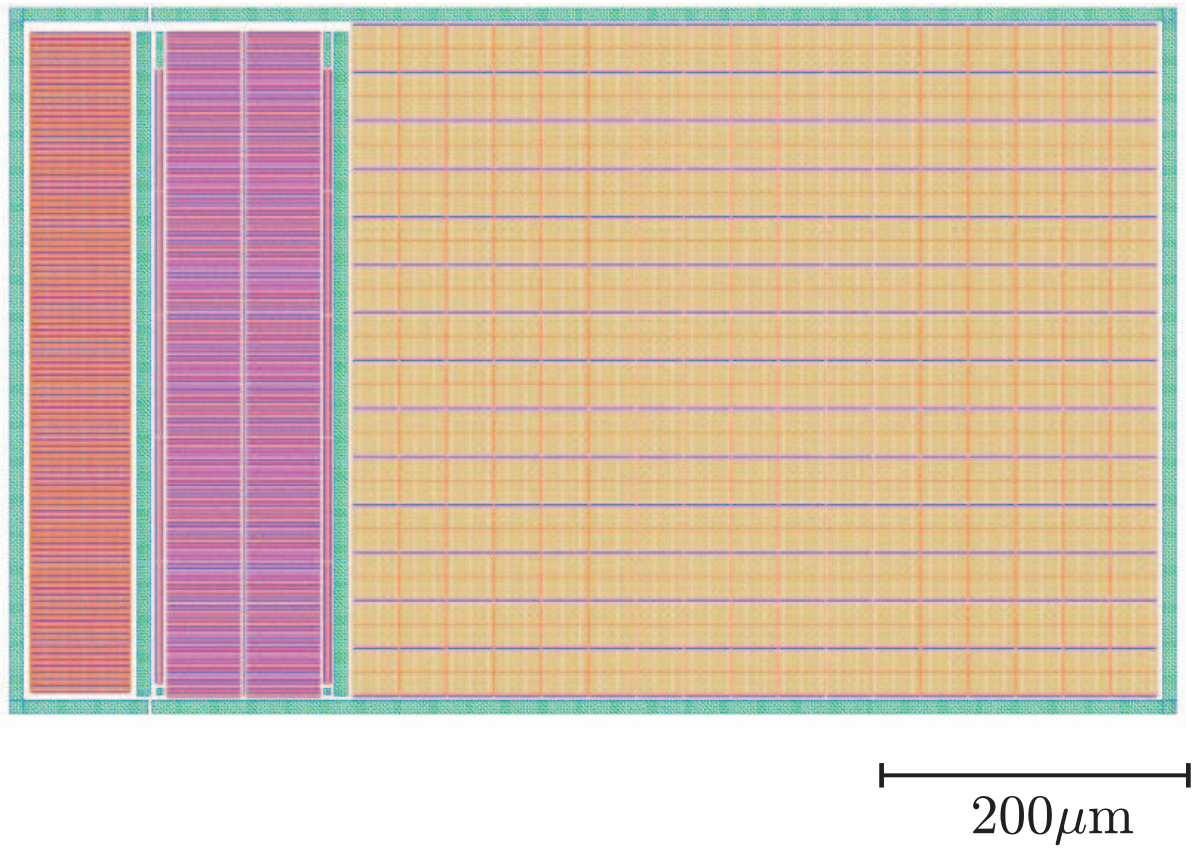


- $f_o = 50$KHz and $Q = 1$
- $f_{in1} = 46$KHz
  $f_{in2} = 54$KHz
- Half full-scale input
- V_{DD} =1.2V
- 0.35μm technology

- Ideal poly-Si (dotted)
- Simple NMOS (dashed)
- NMOS with tuning compensation (solid)

Second-order band-pass filter



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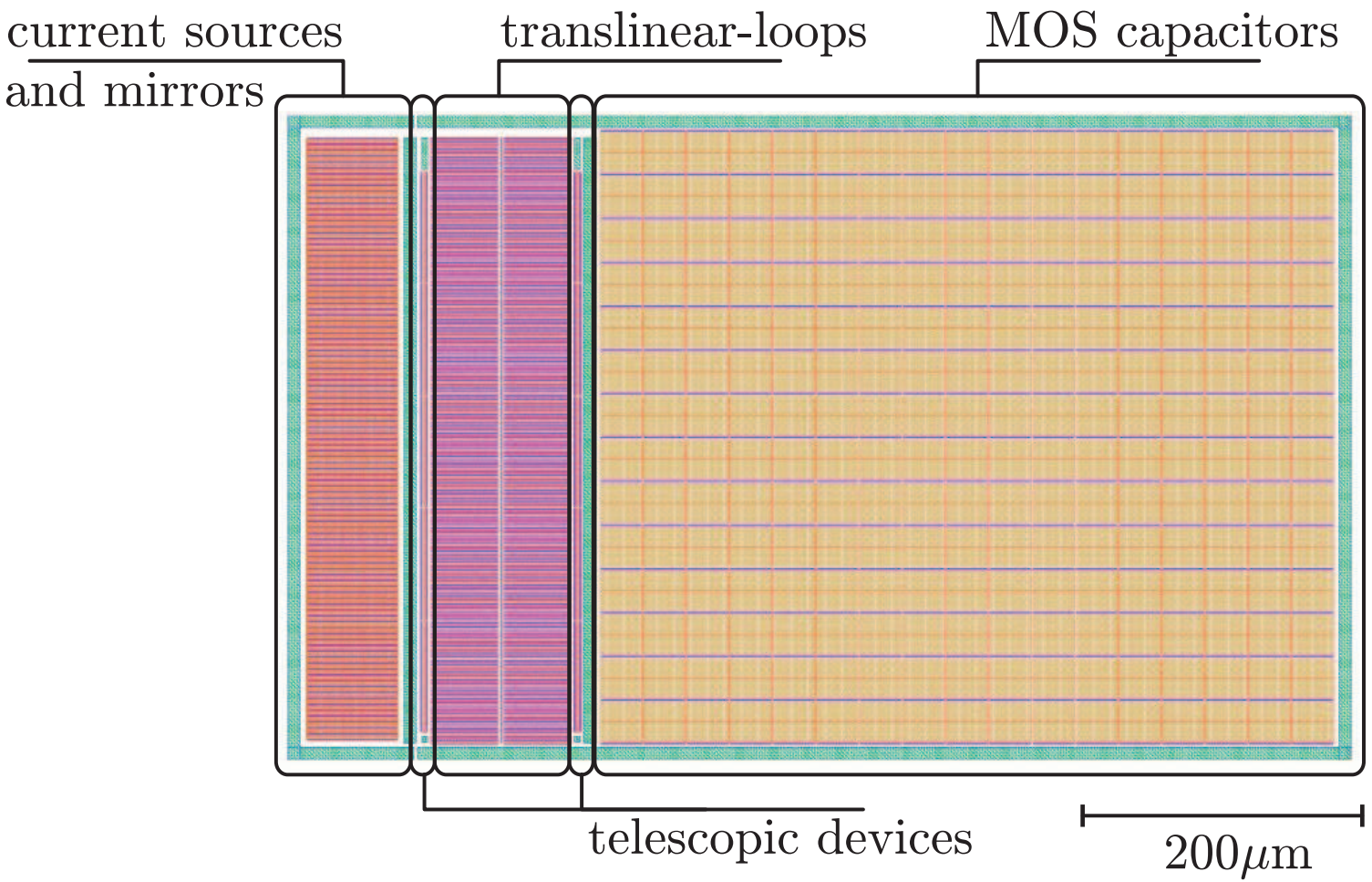
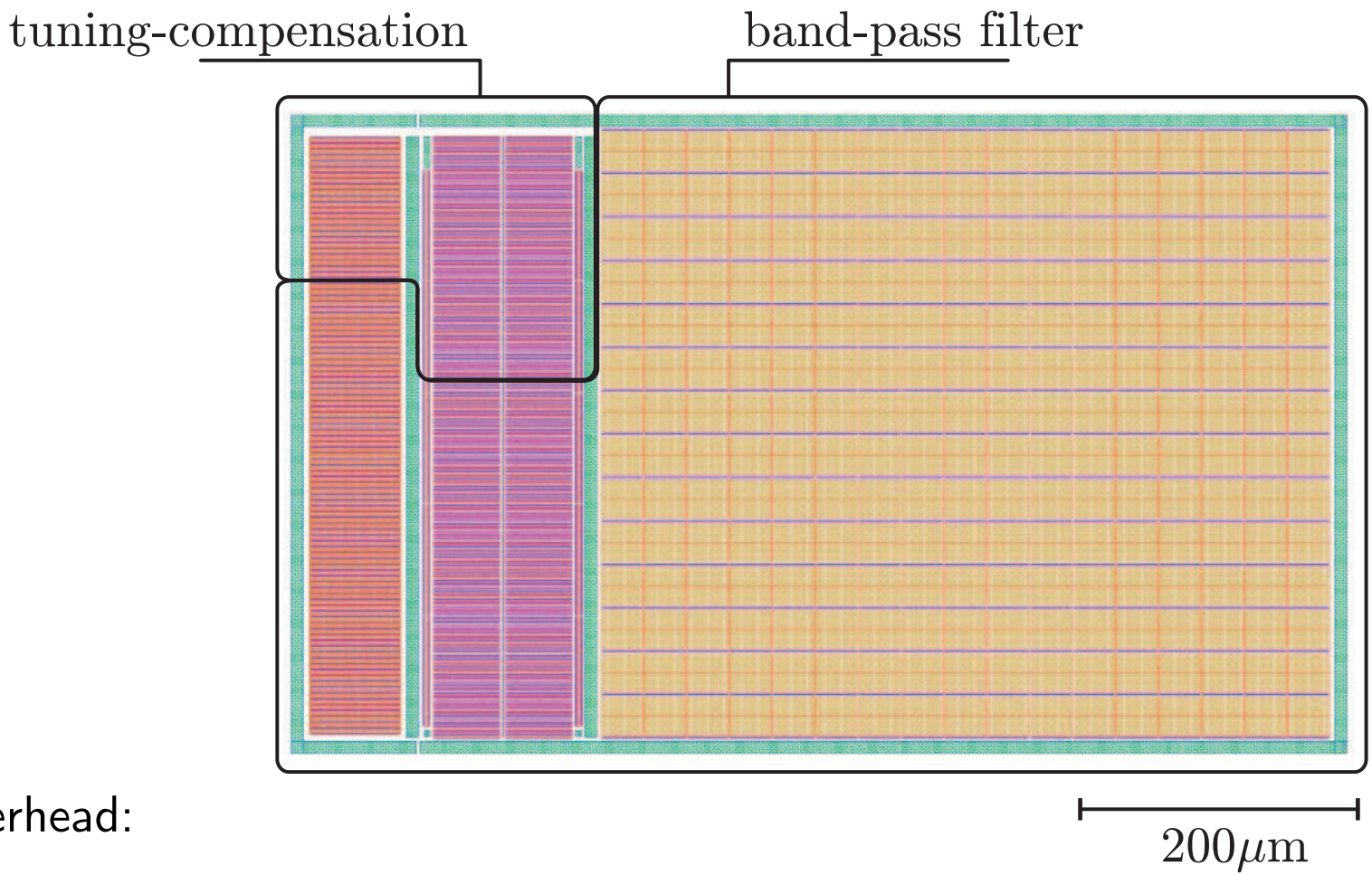


Second-order band-pass filter



Overhead:

- Si area (no-routing) $\sim$0.04mm^2 (12% of 0.33mm^2)
- Static power $\sim$50μW (33% of 150μW)

- **Analytical design** of all-MOS log filters based on compensation of tuning currents
- Suitable for **very low-voltage** applications
- Compatible with **digital technologies**
- Area & power overhead proportional to **filter order**
- Technology dependence **not critical**
- **Sub-micron** low-voltage examples

- Extension to **Class-AB** operation?...