Design of Low-Power CMOS Read-Out ICs for Large Arrays of Cryogenic Infra-Red Sensors

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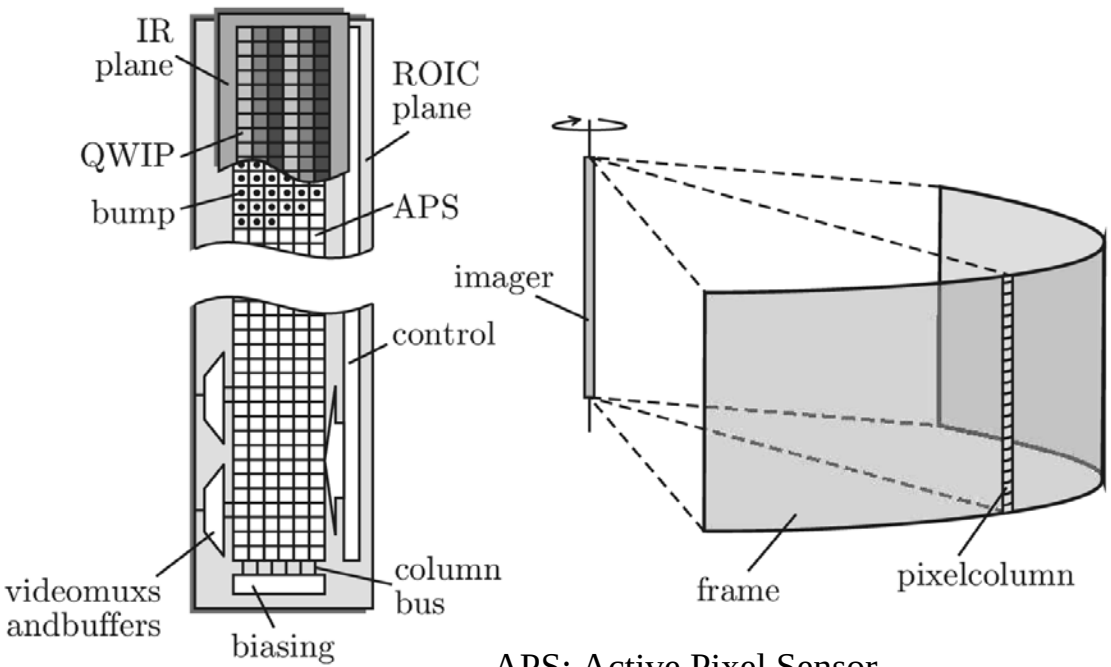
System Architecture Options

- **Focal Plane Array**
  - large Si area-> High cost
  - low production yield
  - large power requirement
  - low speed circuitry
- **Scanning System**
  - lower cost Good!
  - better yield Good!
  - lower power figure Good!
  - high speed circuitry



APS: Active Pixel Sensor

several column to perform a time delay integration (TDI):

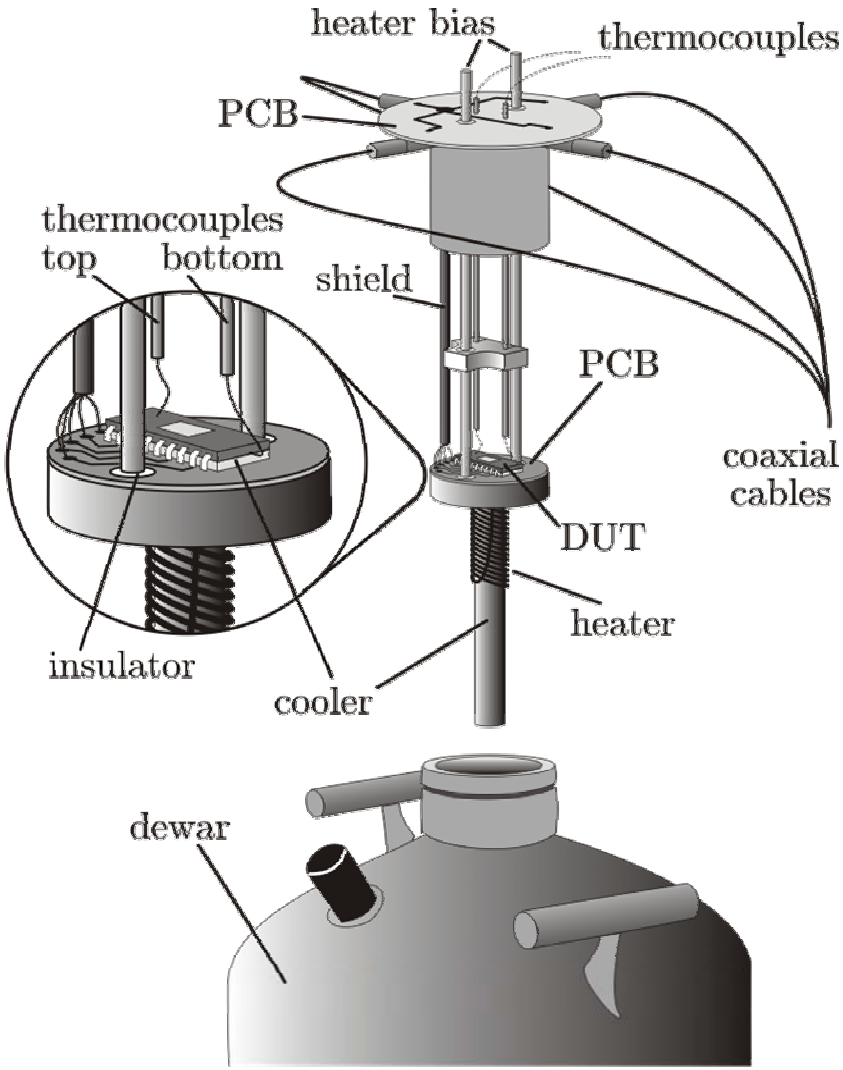
$$SNRimprovement = \sqrt{n}$$

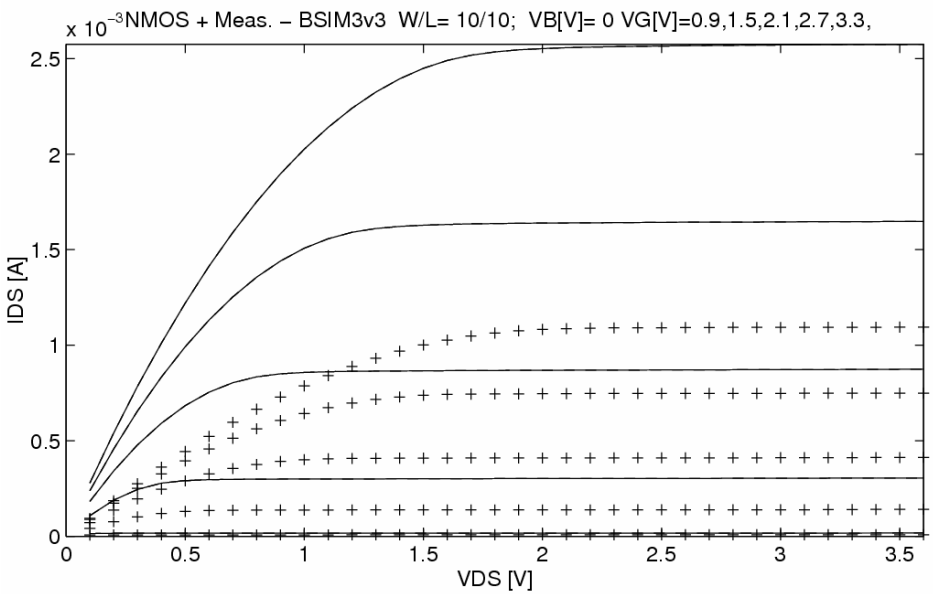
n : number of column

$\Rightarrow$ Matrice of APS

Scalable design!

Cryogenic CMOS Model





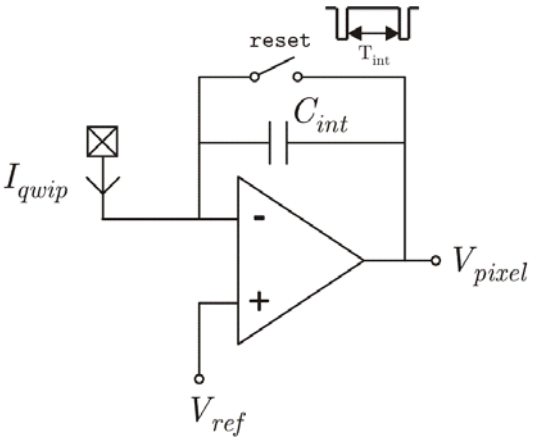
BSIM3v3 parameters need to be corrected:

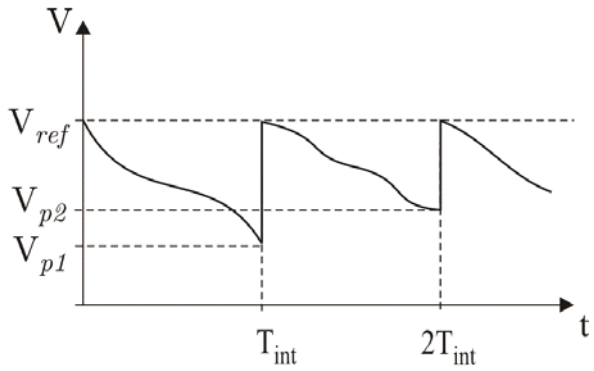
- UTE $$\frac{\mu_0(T)}{\mu_0(\mathrm{TNORM})} = \left(\frac{T}{\mathrm{TNORM}}\right)^{\mathrm{UTE}}$$

- PRT $$R_{dsw}(T) = R_{dsw}(\mathrm{TNORM}) + \mathrm{PRT}\left(\frac{T}{\mathrm{TNORM}} - 1\right)$$

Low Noise Pre-amplification: APS (1)

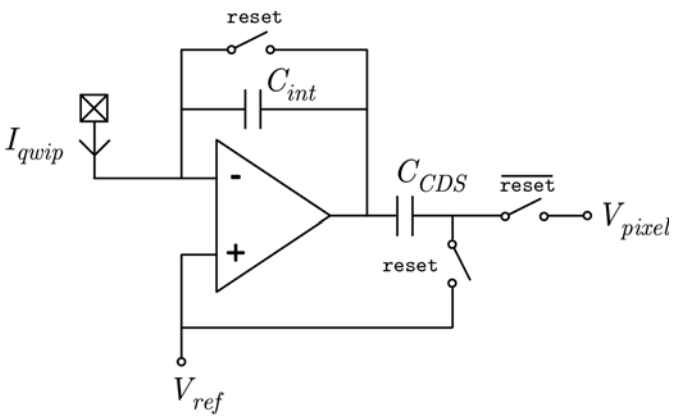
- Achieved through a capacitive transimpedance amplifier (CTIA).



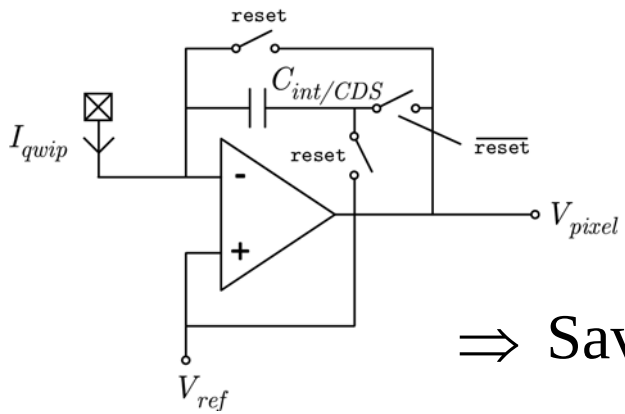


$$V_{pixel} \simeq V_{ref} - \frac{T_{int}}{C_{int}} \cdot I_{qwip}$$

- An extra correlated double sampling (CDS) stage eliminates *KTCint* noise.
  - Classical circuit:



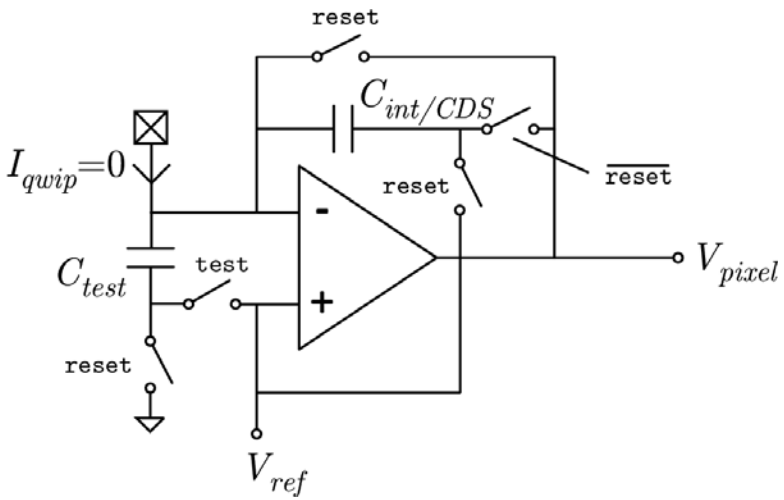
  - New single capacitor implementation:



$\Rightarrow$ Save Area!

Low Noise Pre-amplification: APS (1)

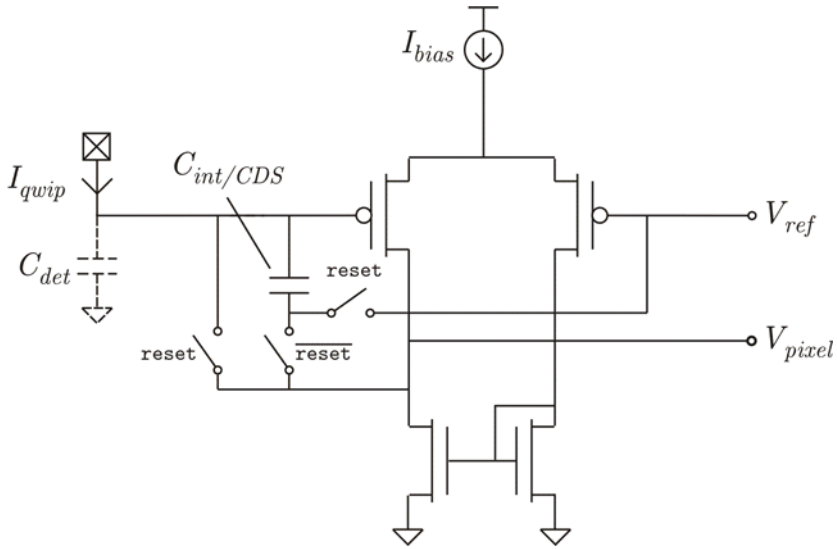
- Build-in pixel-test:



$$V_{pixel} = \left(1 - \frac{C_{test}}{C_{int/CDS}}\right) V_{refi}$$

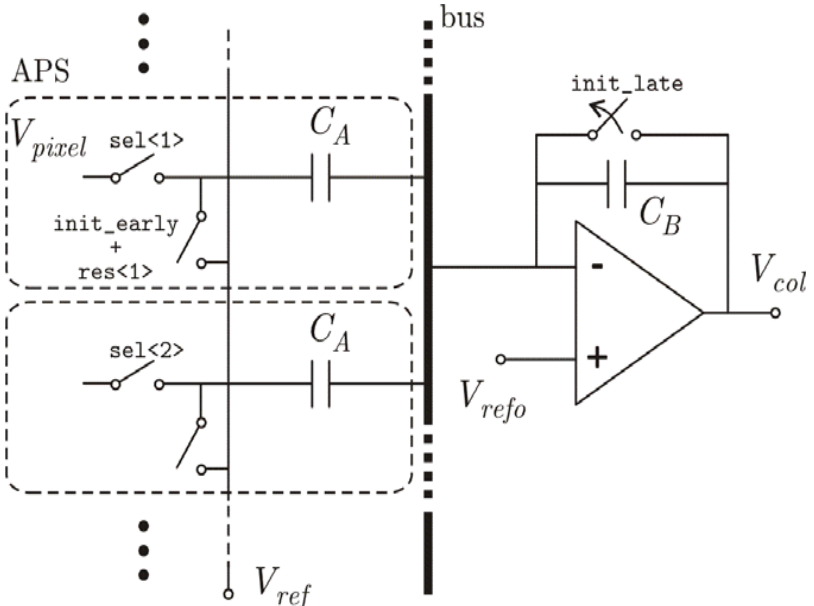
C_{test} can be reuse to supply several programmable CTIA gains.

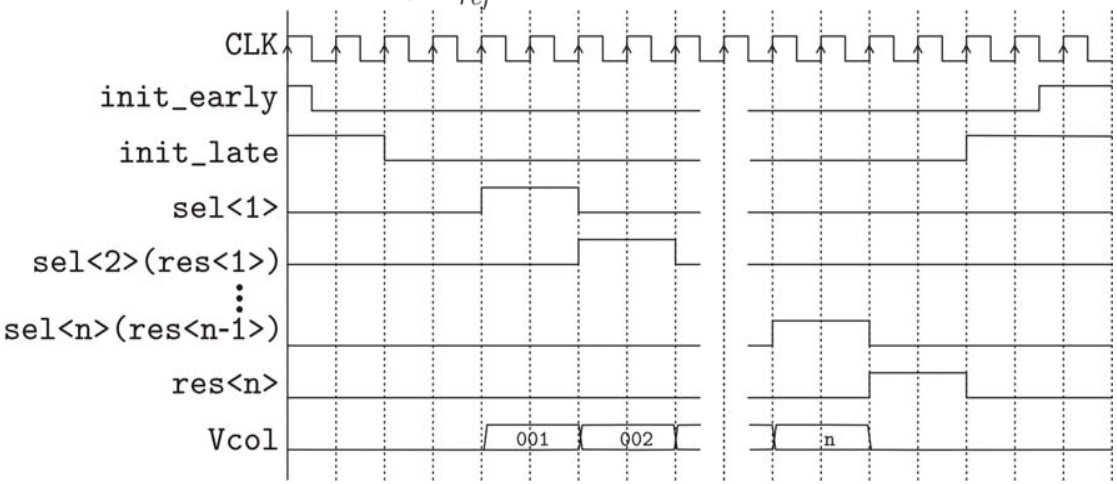
- Transistor level:



Open loop gain has to be high enough to lower the input impedance and assure a high current injection efficiency.

APS Charge-Multiplexing (1)



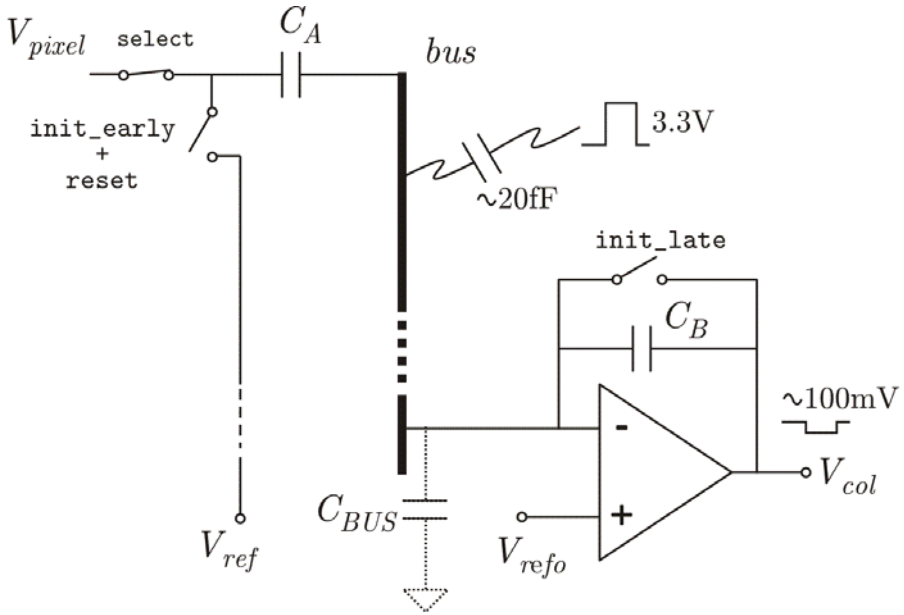


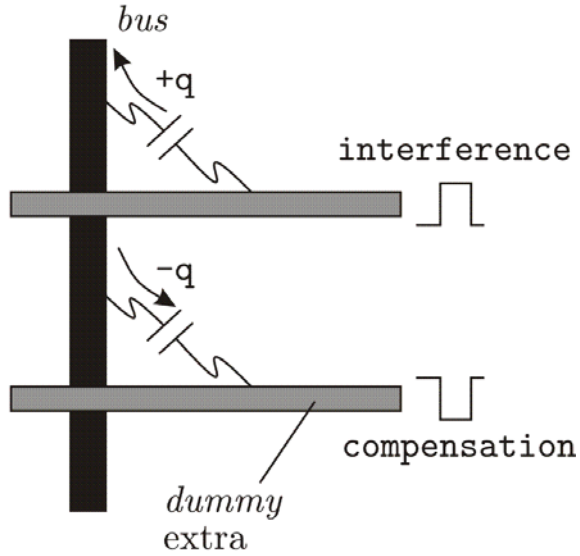
Advantages:

- Reduces cross talk
- Low power
- Possibility of level-shifting and amplification

$$V_{col} = V_{refo} + \frac{C_A}{C_B}\left(V_{ref} - V_{pixel}\right)$$

APS Charge-Multiplexing (2)





Main drawback:

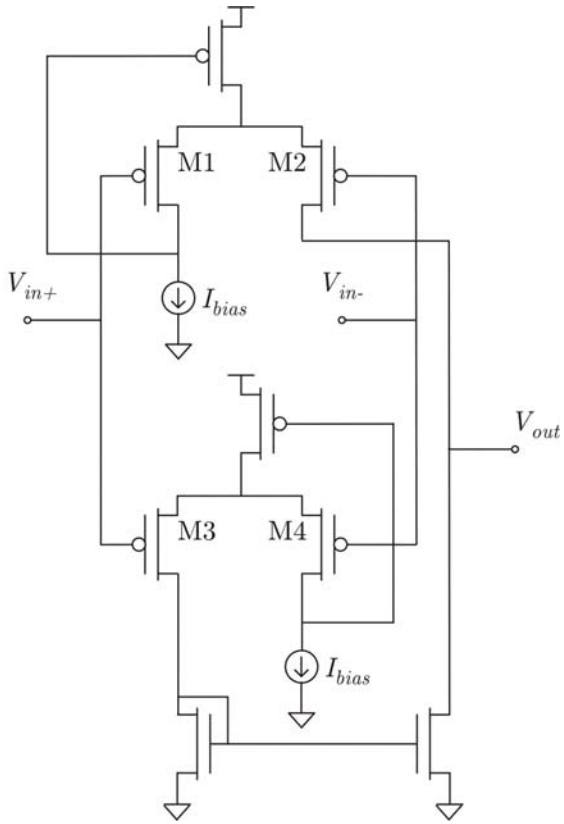
- highly sensitive to digital coupling with the bus
- Need high gain and high bandwidth opamp:

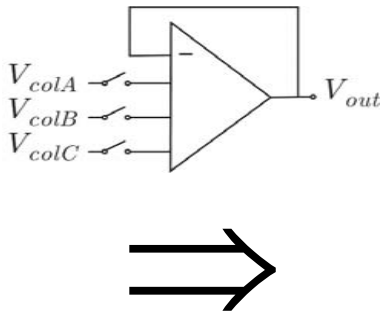
⇒ Careful layout !!!

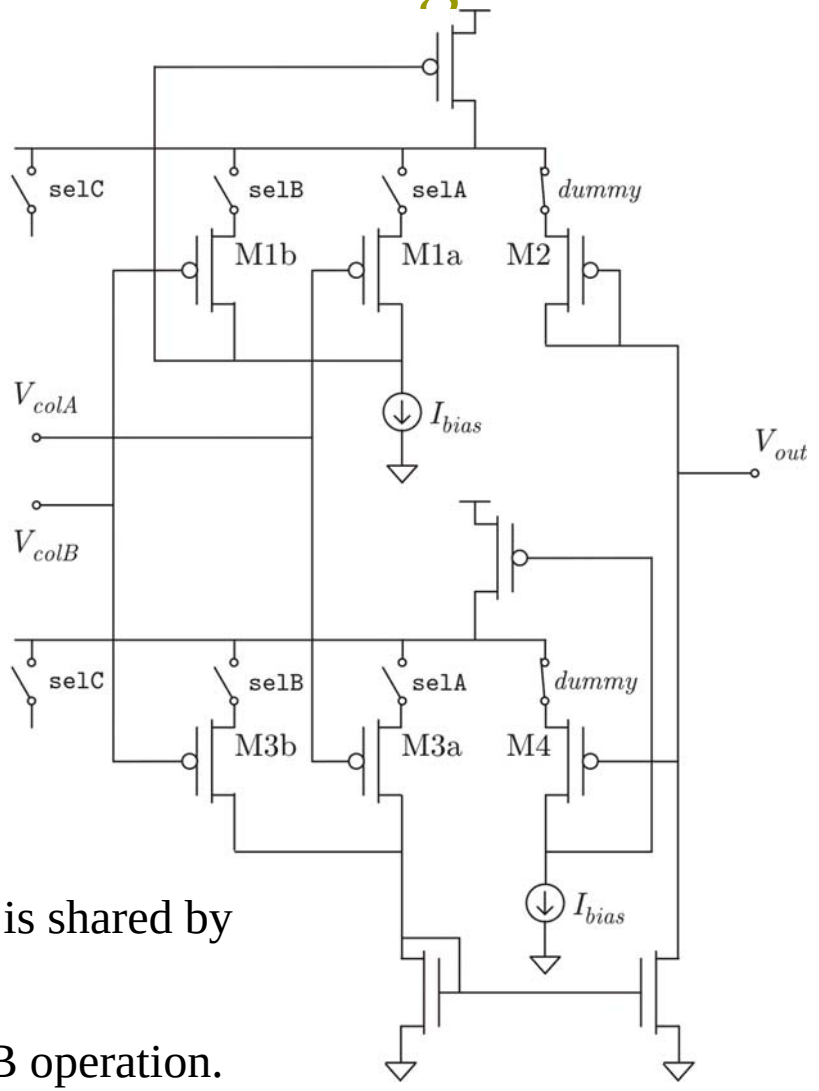
interferences compensation

hopefully, cryogenic temperature increase gm!!

Video Multiplexing and Buffering

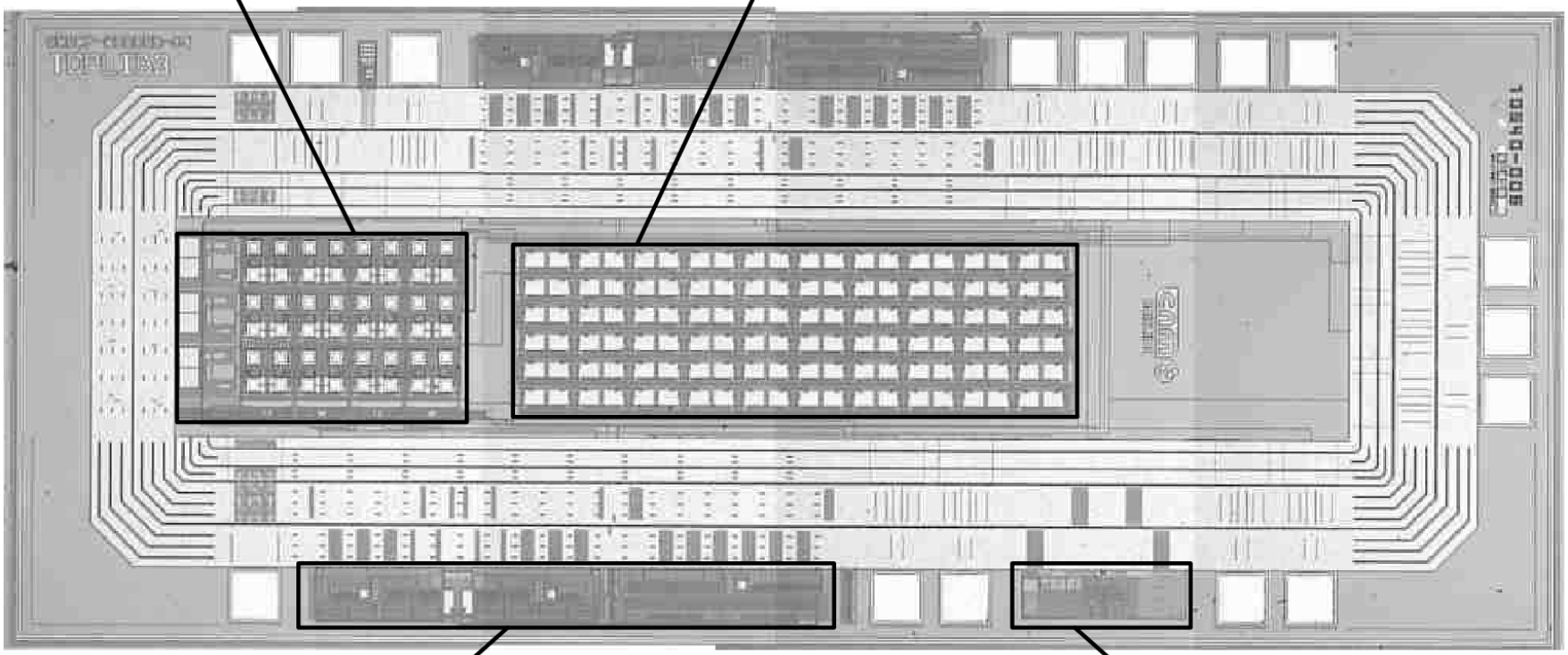


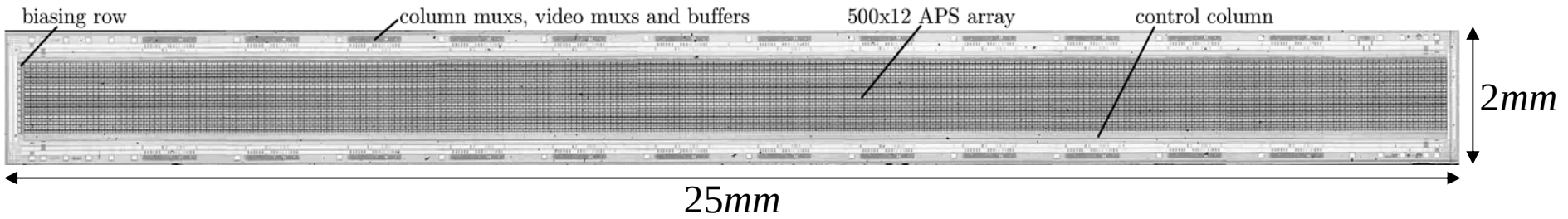




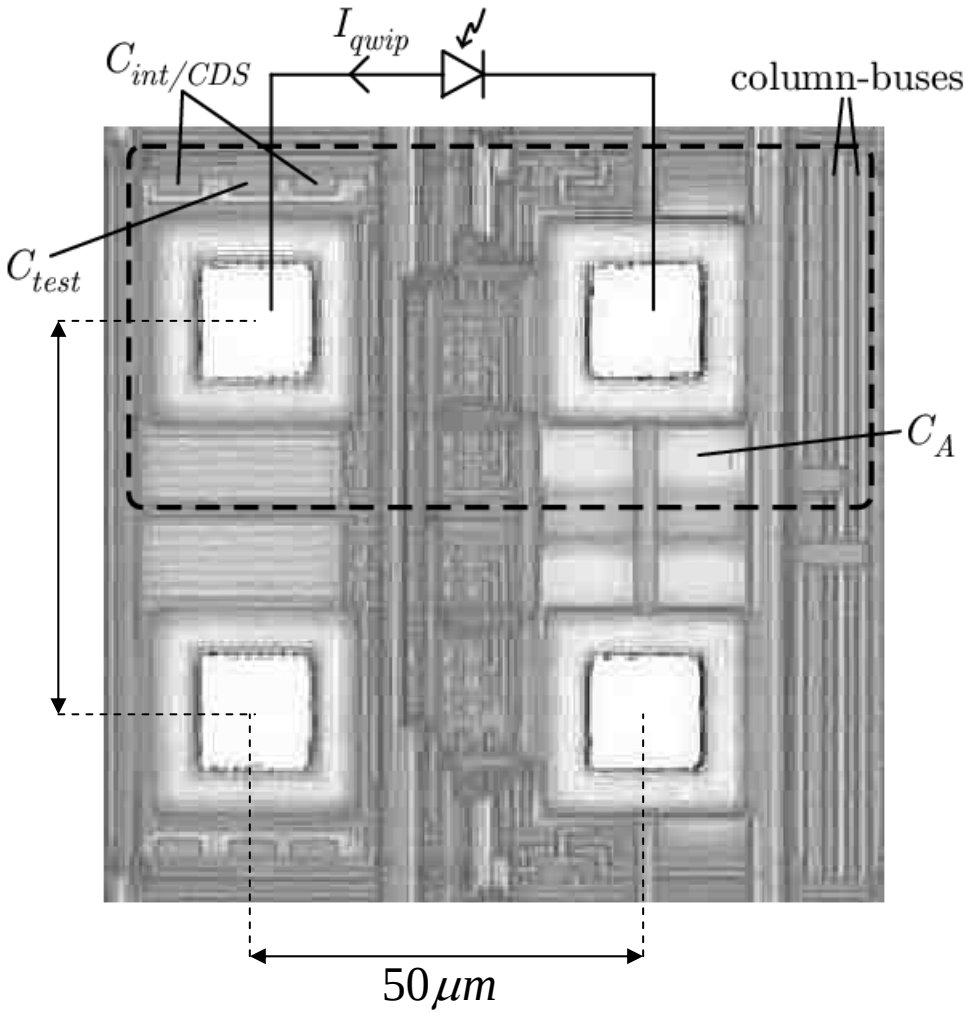
- Low-power and compact design: half the circuitry is shared by several columns.
- Pseudo-differential follower which allow Class-AB operation.

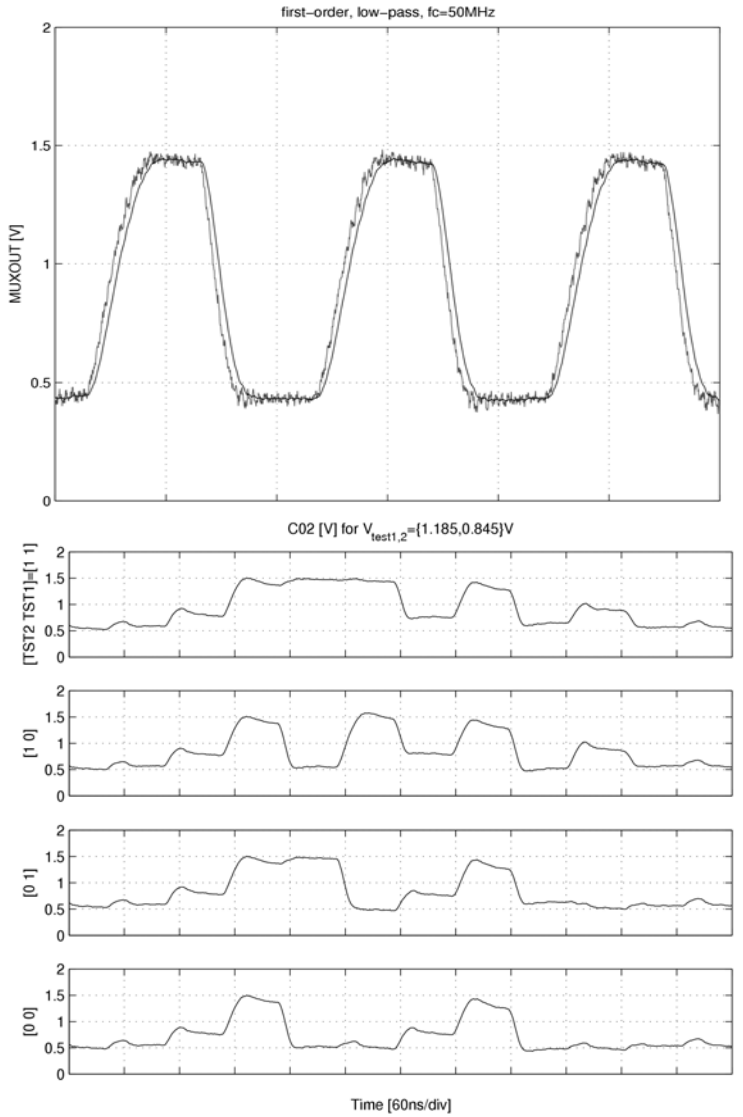
System On Chip Realization





Experimental Result and Testing





Specifications

Parameter	Value	Units
Supply voltage	3.3	V
Temperature operation	77	K
Array size	500x12	$pixels^2$
Pixel pitch	50	µm
Integration time	15.6	µs
Video sampling (dual output)	60	ns/pixel
Video resolution	10	bit
Typical frame	640x500@100	$pixels^2$@fps
Power consumption	210	mW
Silicon Area	51	mm^2

Conclusion

- Scanning ROIC architecture
- operate at Cryogenic temperature
- High-resolution
- Novel low power, compact CMOS circuits