1V sub-100μW 12b all-MOS $\Sigma\Delta$ A/D Converters in the Log-Domain

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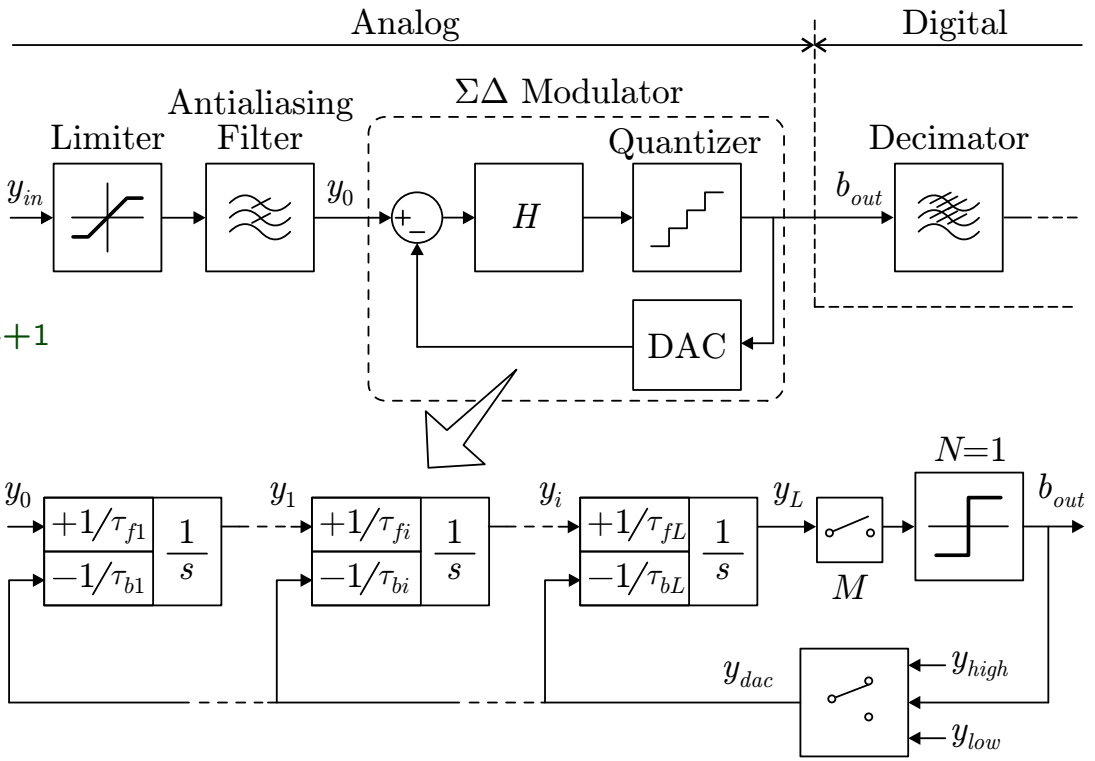
- Portable and mixed SoCs → low-power ΣΔ ADCs
- Digital CMOS technologies → low-voltage all-MOS

$$DR_{ideal} = \frac{3\pi}{2}\left(2^N - 1\right)^2 (2L+1)\left(\frac{M}{\pi}\right)^{2L+1}$$

M-oversampling ratio

L-order frequency selective H-stage

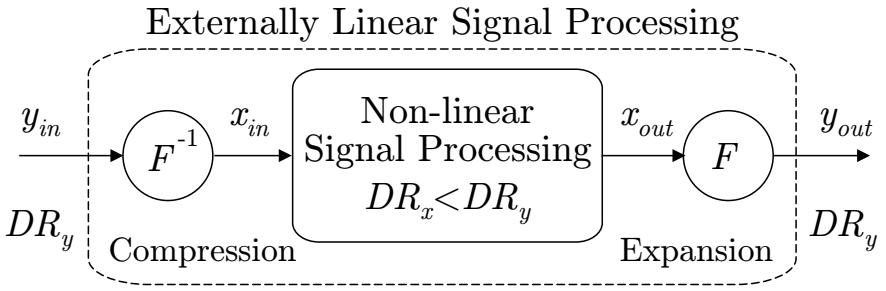
N-bit quantization



- 1bit → no linearity problems at Quantizer/DAC
- Single-stage → compact circuits

$$\frac{d\overline{Y}_{ss}}{dt} = \begin{bmatrix} 0 & 0 & 0 \\ \frac{1}{\tau_{fi}} & 0 & 0 \\ 0 & \frac{1}{\tau_{fL}} & 0 \end{bmatrix} \overline{Y}_{ss} + \begin{bmatrix} \frac{1}{\tau_{f1}} \\ 0 \\ 0 \end{bmatrix} y_0 + \begin{bmatrix} -\frac{1}{\tau_{b1}} \\ -\frac{1}{\tau_{bi}} \\ -\frac{1}{\tau_{bL}} \end{bmatrix} y_{dac}$$

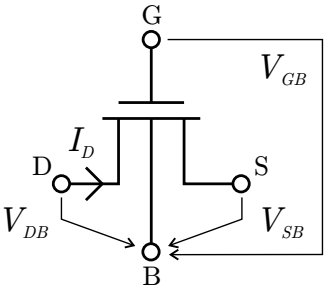
▶ Instantaneous Companding theory



$$y = F(x) = e^x$$

$$\frac{dy_i}{dt} = \frac{1}{\tau_{fi}} y_{i-1} \quad \overset{F}{\longleftrightarrow} \quad \frac{dx_i}{dt} = \frac{1}{\tau_{fi}} e^{x_{i-1}-x_i}$$

▶ MOSFET operating in subthreshold



weak inversion

$$V_{SB,DB} \gg \frac{V_{GB}-V_{TO}}{n}$$

forward saturation

$$V_{DB} - V_{SB} \gg U_t$$

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad I_S = 2n\beta U_t^2$$

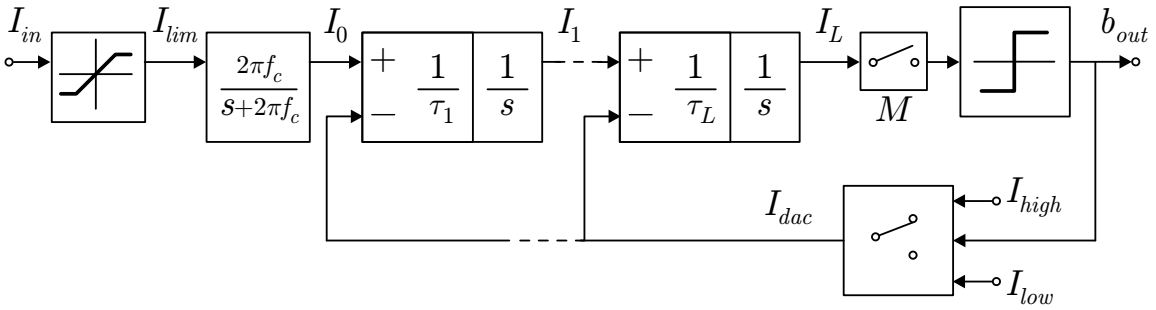
GD, SD or BD Companding:

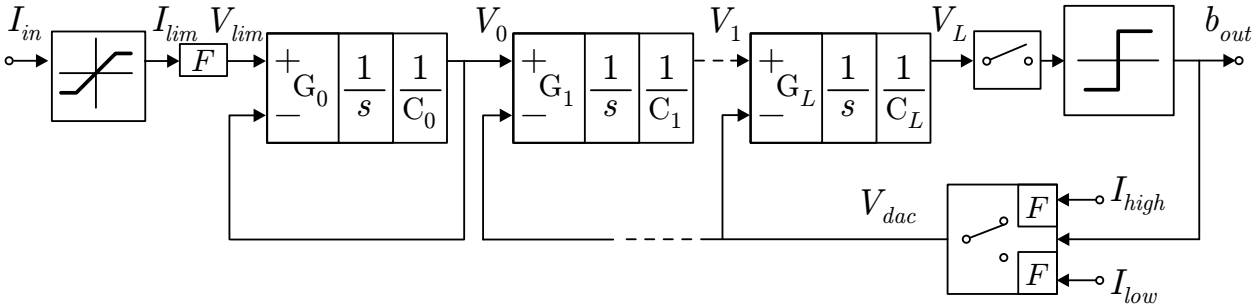
$$y_i = \frac{I_{Di}}{I_S} \quad \overset{F}{\longleftrightarrow} \quad x_i = \frac{V_{GBi}}{nU_t}$$

▶ Pros & cons:

- Internal DR_V compression → True low-voltage operation √
  Compatible with non-linear caps (e.g.MOS) √
- Subthreshold operation → Low-power consumption √
  Low-frequency applications (typ.<1MHz) ×

- CMOS circuit techniques for:
  - Input compressor and limiter
  - Anti-aliasing filter
  - Modulator integrator
  - Modulator quantizer
  - Modulator DAC





- Target specs:
  - Very low-voltage (1V)
  - Digital Technology (MOS-only)
  - Audio bandwidth
  - Low-power (sub-100μW)

- Application example: Hearing Aids

- Input compressor

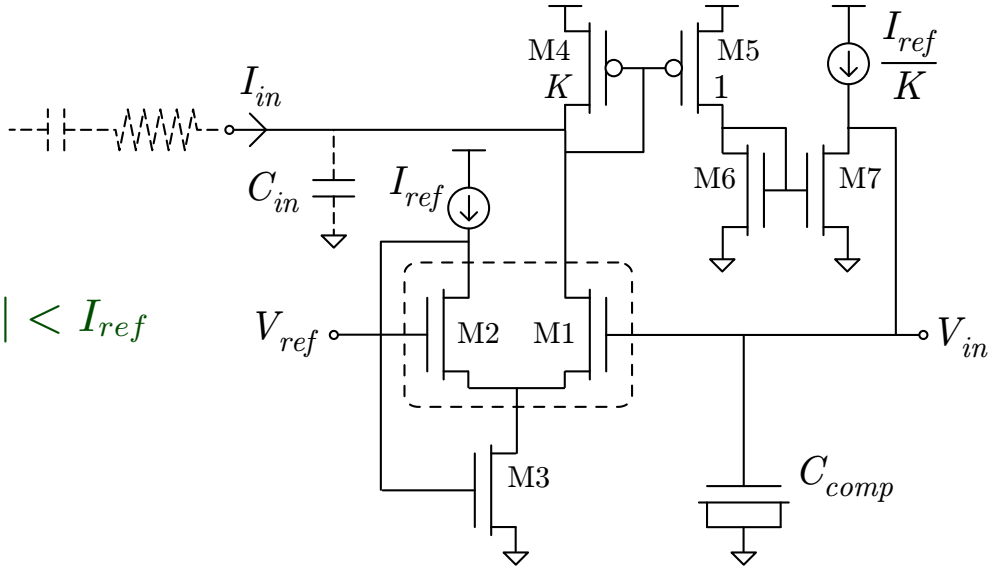
$$I = F(V) = I_{ref} e^{\frac{V - V_{ref}}{nU_t}} \qquad I > 0$$

Class-A operation:

$$V_{in} = V_{ref} + nU_t \ln\left(\frac{I_{in}}{I_{ref}} + 1\right) \qquad |I_{in}| < I_{ref}$$

Simple frequency compensation:

$$\zeta = \frac{1}{2}\sqrt{\frac{KC_{comp}}{C_{in}}}$$

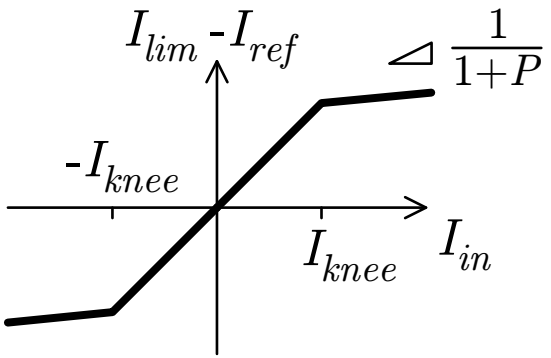


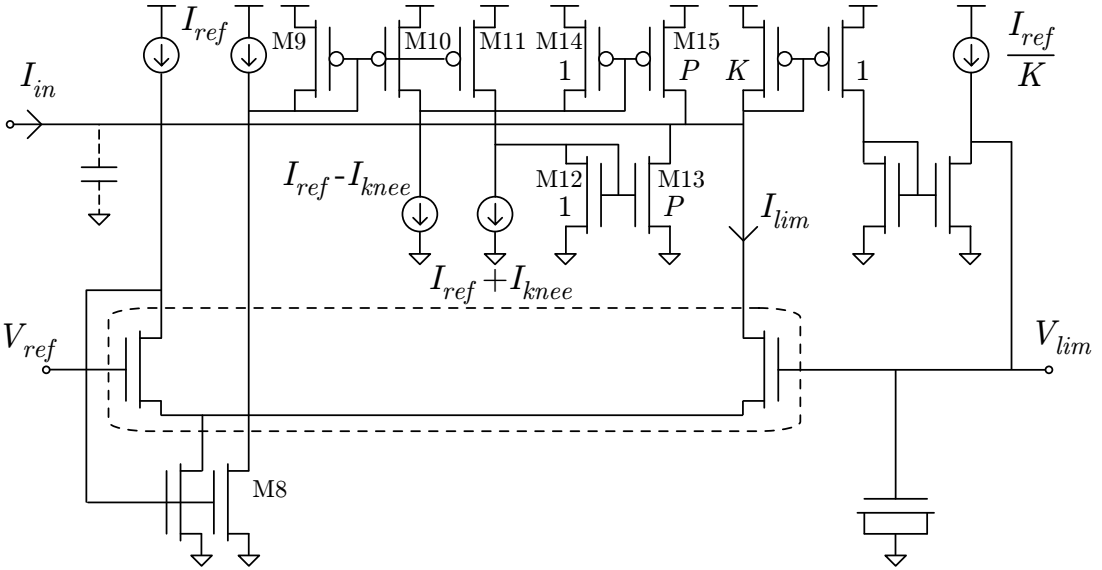
- I_{ref} defines full-scale in Class-A
- V_{ref} optimizes low-voltage operation
- Low input impedance (<1KΩ) for optional linear $V \rightarrow I$ conversion at input

- Input compressor with limiter

$$I_{lim} = \begin{cases} I_{ref} + I_{in} & |I_{in}| \leq I_{knee} \\ I_{ref} + \dfrac{I_{in} \pm P I_{knee}}{1+P} & |I_{in}| > I_{knee} \end{cases}$$

piece-wise transfer function:





- I_{knee} selects the input threshold
- P defines compression ratio

- Anti-aliasing filter

I-domain 1st-order low-pass ODE:

$$\frac{\mathrm{d}I_0}{\mathrm{d}t} = -2\pi f_c I_0 + 2\pi f_c I_{lim}$$

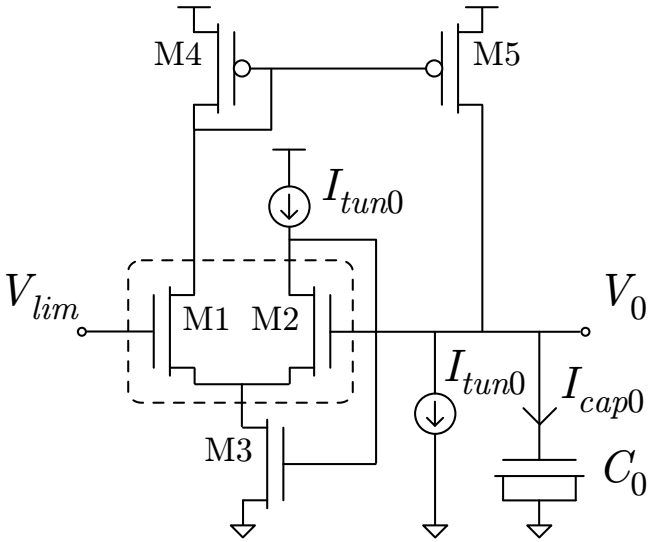
V-domain non-linear ODE:

$$\frac{\mathrm{d}V_0}{\mathrm{d}t} = -2\pi f_c n U_t + 2\pi f_c n U_t e^{\frac{V_{lim}-V_0}{nU_t}}$$

Q-domain circuit ODE:

$$\frac{\mathrm{d}Q_0}{\mathrm{d}t} = \underbrace{C_0\frac{\mathrm{d}V_0}{\mathrm{d}t}}_{I_{cap0}} = -I_{tun0} + I_{tun0}e^{\frac{V_{in}-V_0}{nU_t}}$$

$$f_c = \frac{1}{2\pi}\frac{I_{tun0}}{nU_t C_0}$$



- Tuning parameter I_{tun0}
- Thermal cancellation for f_c through PTAT I_{tun0}
- Non-linear NMOS capacitor C_0

- Modulator Integrator

I-domain ODE for the τ_{fi} case:

$$\frac{\mathrm{d}I_i}{\mathrm{d}t} = \frac{1}{\tau_{fi}} I_{i-1}$$

V-domain non-linear ODE:

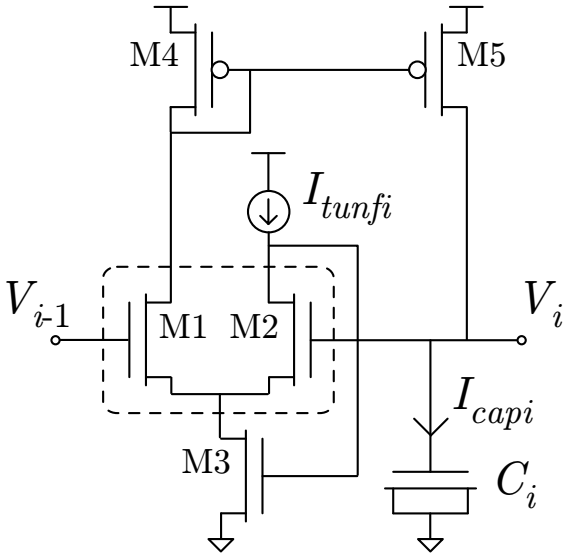
$$\frac{\mathrm{d}V_i}{\mathrm{d}t} = \frac{nU_t}{\tau_{fi}} e^{\frac{V_{i-1}-V_i}{nU_t}}$$

Q-domain circuit ODE:

$$\frac{\mathrm{d}Q_i}{\mathrm{d}t} = \underbrace{C_i \frac{\mathrm{d}V_i}{\mathrm{d}t}}_{I_{capi}} = I_{tunfi} e^{\frac{V_{i-1}-V_i}{nU_t}}$$

$$\tau_{fi} = \frac{nU_t C_i}{I_{tunfi}}$$

positive τ_{fi} case:



- Tuning parameter I_{tunfi}
- Thermal cancellation for τ_{fi} through PTAT I_{tunfi}
- Non-linear NMOS capacitor C_i

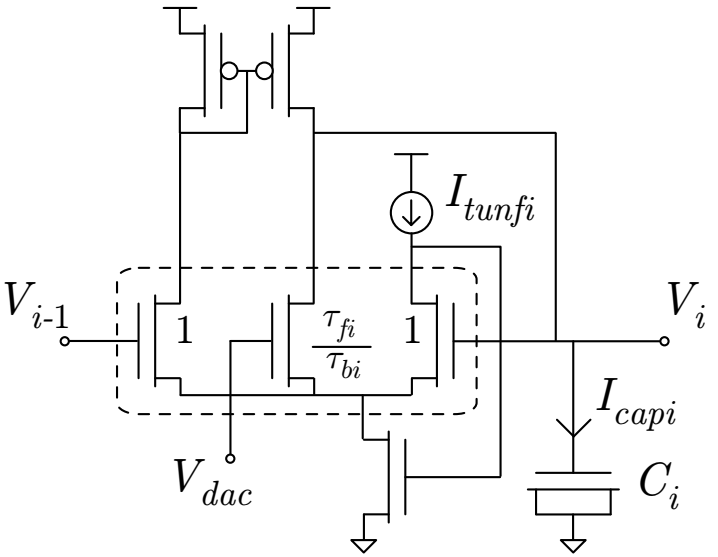
Log-mapping (i.e. $I > 0$) $\rightarrow$ coefficients only charge xor discharge caps!

- Modulator Integrator

ΣΔ modulator case ($\tau_{fi}>0$ $\tau_{bi}<0$):

OP designed at SS-matrix level:

$$\frac{\mathrm{d}\overline{I}_{ss}}{\mathrm{d}t} = \begin{bmatrix} 0 & 0 & 0 \\ \frac{1}{\tau_{fi}} & 0 & 0 \\ 0 & \frac{1}{\tau_{fL}} & 0 \end{bmatrix} \overline{I}_{ss} + \begin{bmatrix} \frac{1}{\tau_{f1}} \\ 0 \\ 0 \end{bmatrix} I_0 + \begin{bmatrix} -\frac{1}{\tau_{b1}} \\ -\frac{1}{\tau_{bi}} \\ -\frac{1}{\tau_{bL}} \end{bmatrix} I_{dac}$$



In general, matrix transformation may be required to ensure DC solution for $I > 0\ldots$

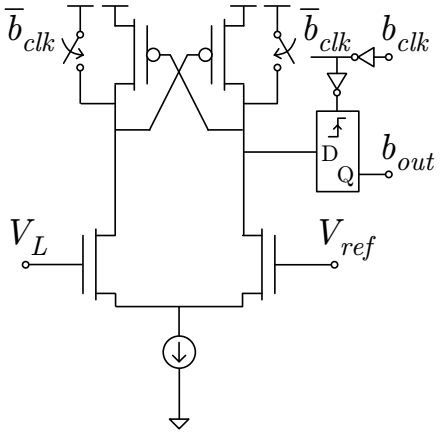
Differential integrator:

Coefficients of the same row can share half circuitry

$$\frac{\mathrm{d}Q_i}{\mathrm{d}t} = \underbrace{C_i \frac{\mathrm{d}V_i}{\mathrm{d}t}}_{I_{capi}} = \boxed{I_{tunfi} e^{\frac{-V_i}{nU_t}}} \left(e^{\frac{V_{i-1}}{nU_t}} - \frac{\tau_{fi}}{\tau_{bi}} e^{\frac{V_{dac}}{nU_t}} \right)$$

- Modulator Quantizer

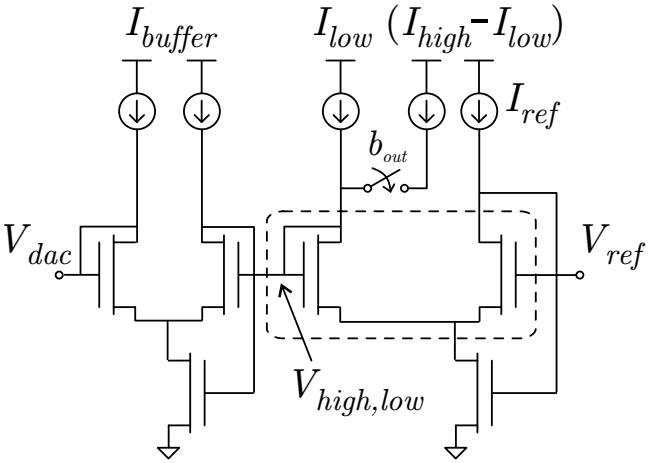
$$b_{out} = \begin{cases} 1 & \text{for } V_L > V_{ref} \\ 0 & \text{for } V_L < V_{ref} \end{cases}$$



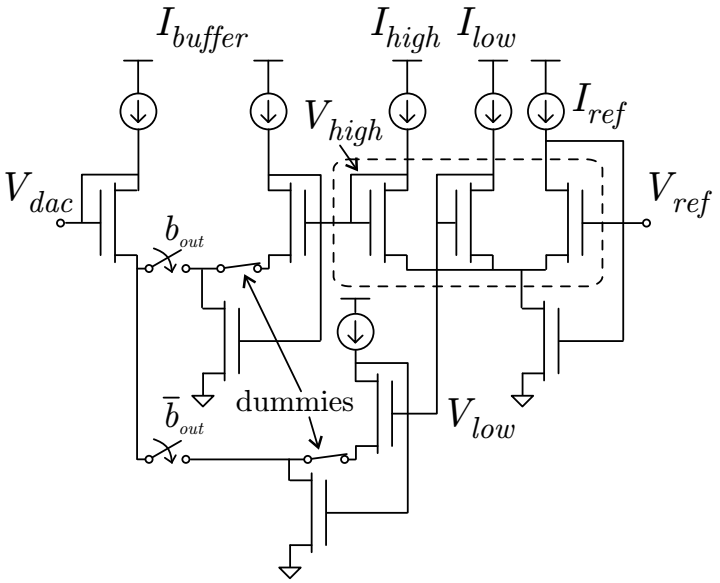
- Modulator DAC

$$V_{dac} = V_{ref} + \begin{cases} nU_t \ln\left(\frac{I_{high}}{I_{ref}}\right) & \text{for } b_{out} = 1 \\ nU_t \ln\left(\frac{I_{low}}{I_{ref}}\right) & \text{for } b_{out} = 0 \end{cases}$$

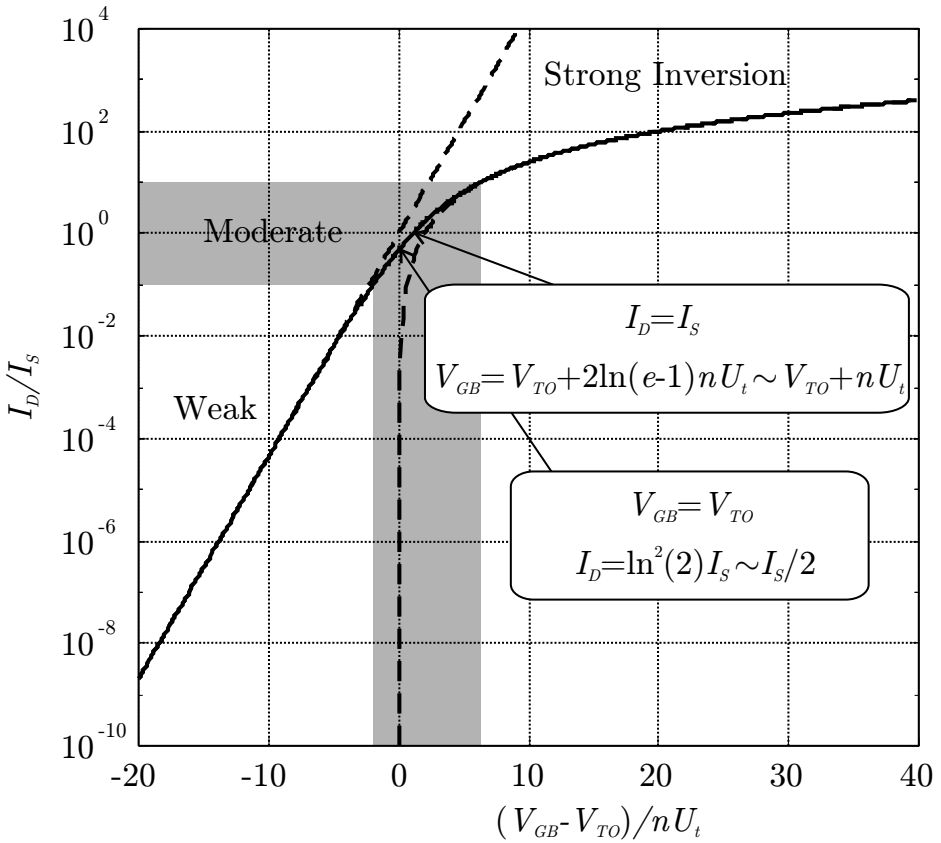
I-domain switching scheme:



V-domain switching scheme:



- Moderate Inversion

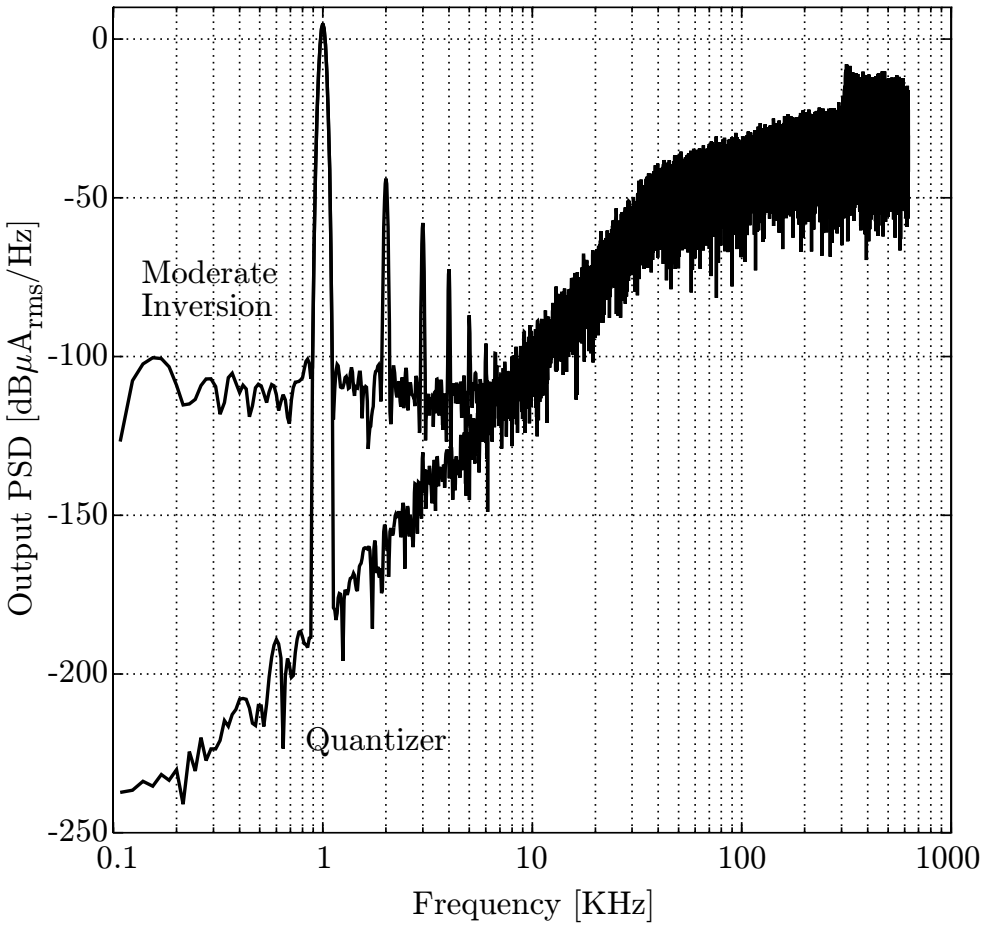


$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad IC = \frac{I_D}{I_S} \ll 1$$

$$\downarrow$$

$$I_D = I_S \ln^2\left(1 + e^{\frac{V_{GB}-V_{TO}}{2nU_t}} e^{-\frac{V_{SB}}{2U_t}}\right)$$

- e^x degradation causes signal distortion
- Wide (W/L) to keep devices in deep weak inversion even at full-scale



- Thermal Noise

Equivalent Drain-current noise PSD:

$$\frac{\mathrm{d}i_{Dn}^2}{\mathrm{d}f} = 4KT\frac{g_{ms}}{2}$$

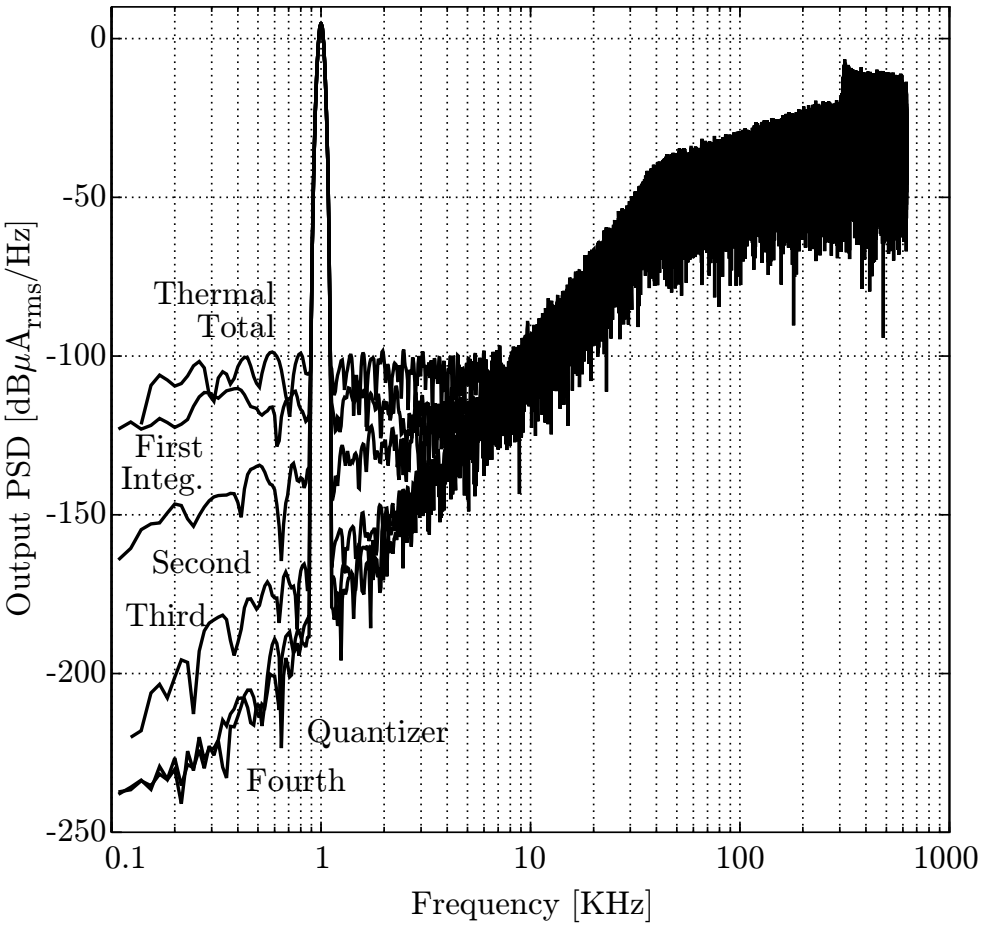
At similar biasing, dominant devices are those in weak inversion where $(g_{ms}/I_D)_{max}$:

$$\frac{\mathrm{d}i_{Dn}^2}{\mathrm{d}f} = 2qI_D \qquad \frac{\mathrm{d}v_{GBn}^2}{\mathrm{d}f} = 2q\frac{(nU_t)^2}{I_D}$$

Main blocks are the compressor, anti-aliasing, 1st integrator and DAC, so:

$$I_{ref} \equiv I_{tun0} \equiv I_{tunf1} \equiv I_{buffer}$$

. . . block contributions:



- Class-A operation results in:

$$SNR \propto +3\mathrm{dB/oct}(I_{ref})$$

- NMOS Capacitors

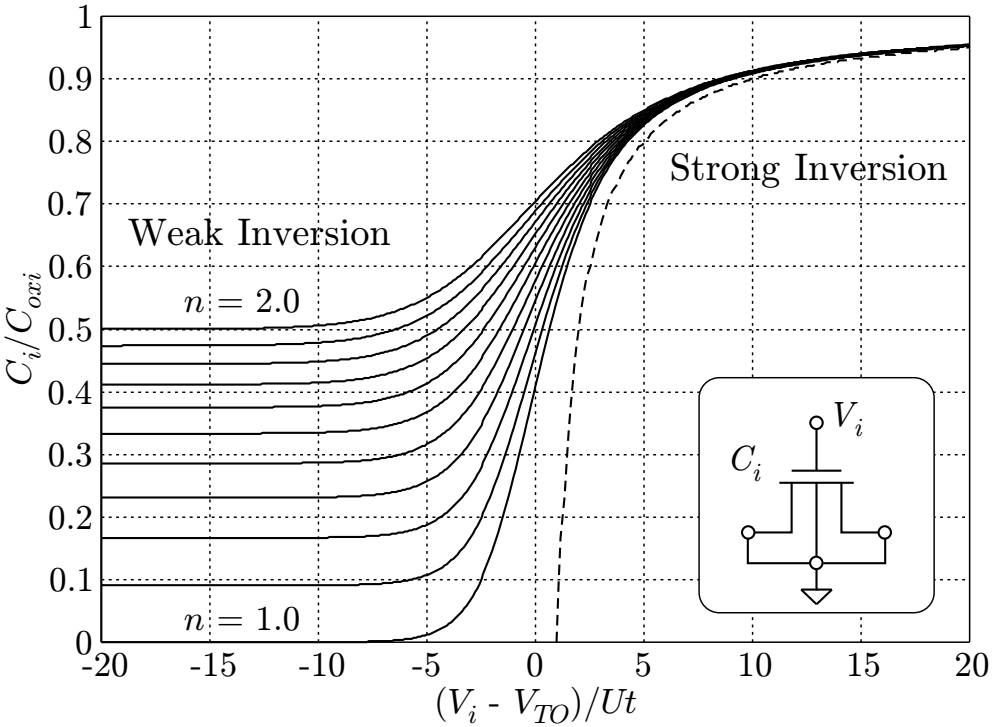
Quasi-static Gate-to-Gate NMOS capacitance in all regions ($V_{SB,DB}$=0):

$$C_i = C_{oxi}\frac{\frac{n-1}{n} + 2\sqrt{IC}\left(1 - e^{-\sqrt{IC}}\right)}{1 + 2\sqrt{IC}\left(1 - e^{-\sqrt{IC}}\right)}$$

$$IC = \ln^2\left(1 + e^{\frac{V_i - V_{TO}}{2nU_t}}\right)$$

for strong inversion (IC>1):

$$C_i \simeq C_{oxi}\left(1 - \frac{U_t}{V_i - V_{TO}}\right)$$



- Minimizing non-linearity through proper biasing: $V_{ref} > V_{TO}$

Non-exact processing:

$$\frac{dQ_i}{dt} = \left(C_i + \frac{dC_i}{dV_i}V_i\right)\frac{dV_i}{dt} \quad \longrightarrow \quad \frac{dV_i}{dt} = \frac{I_{tuni}}{C_{oxi}}\frac{e^{\frac{-V_i}{nU_t}}}{1 + \frac{V_{TO}U_t}{(V_i - V_{TO})^2}}\left(e^{\frac{V_{i-1}}{nU_t}} - e^{\frac{V_{dac}}{nU_t}}\right)$$

- Waveform Asymmetry

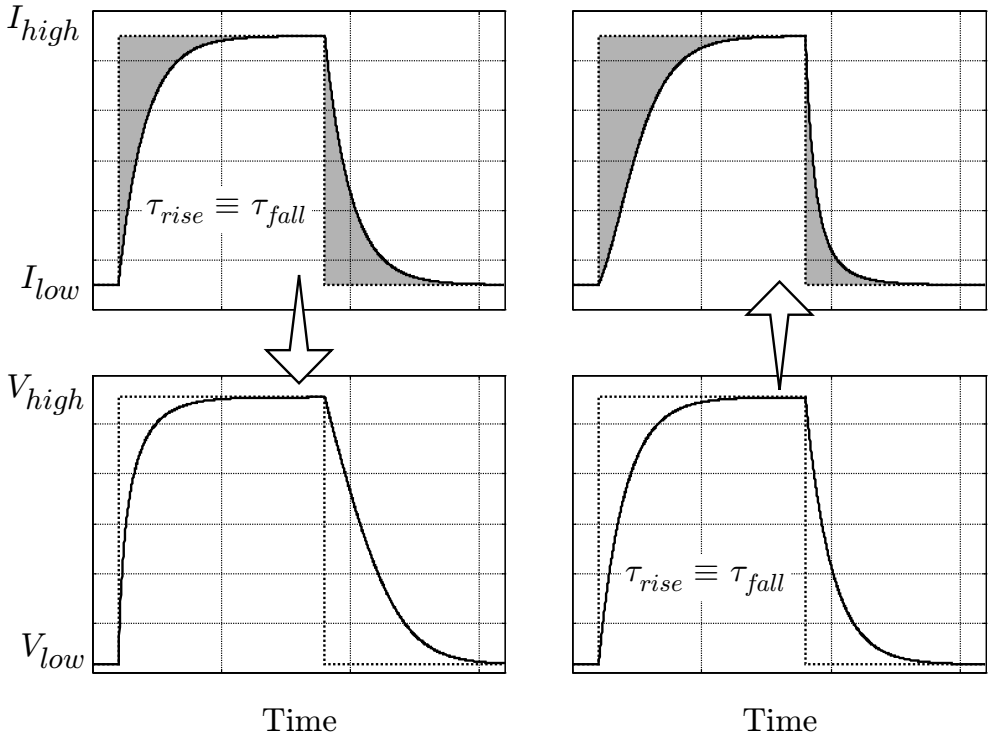
  Unbalanced DAC symbols: $WA \doteq \dfrac{\int_{1/f_s}(I_{dac0\to1}-I_{low})\mathrm{d}t - \int_{1/f_s}(I_{dac1\to0}-I_{high})\mathrm{d}t}{2(I_{high}-I_{low})/f_s} \neq 0$

  First-order model τ_{rise} & τ_{fall} $\surd$ $\times$

  Null WA conditions:

$$\begin{cases} \tau_{fall} = \tau_{rise} & I\text{-switching} \\ \tau_{fall} = \sqrt{\frac{I_{high}}{I_{low}}}\tau_{rise} & V\text{-switching} \end{cases}$$

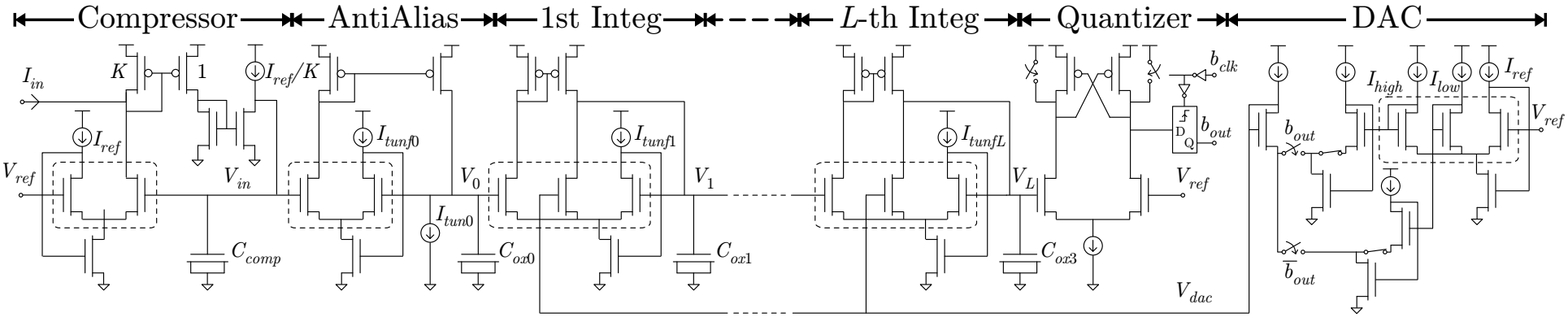
  When code dependent,
  WA generates white noise.



Minimizing WA effects at DAC by: Increasing absolute speed
Achieving symbol symmetry
Ensuring sequence-independence

Design Examples

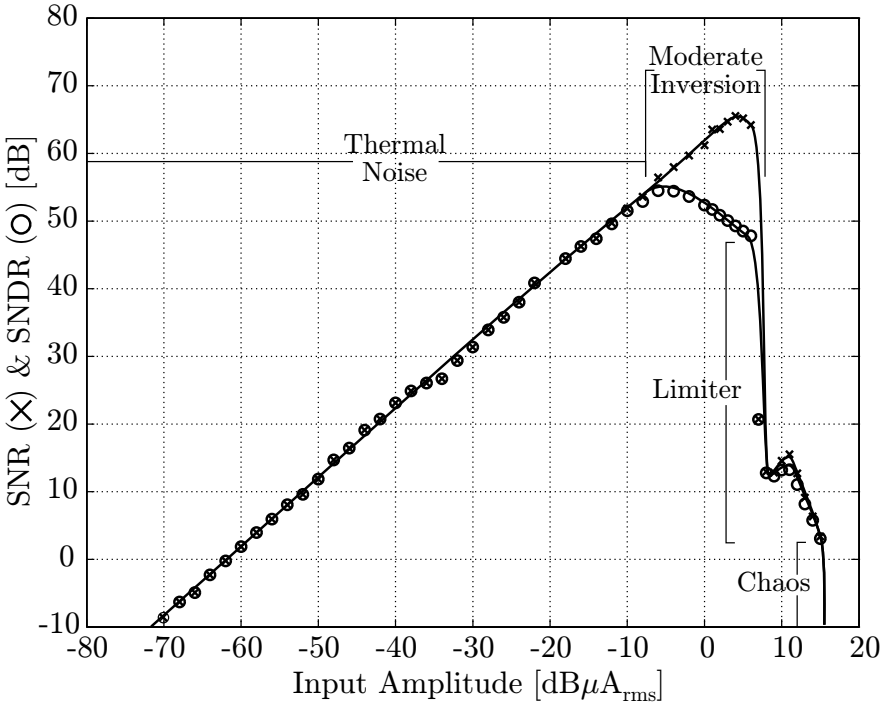
- 3rd- and 4th-order 1bit 64-oversampling ΣΔ ADCs for Hearing Aids:



- Target specs in 0.35μ digital CMOS technology:

Supply Voltage	1.0	V
Max. $V_{TON}+\|V_{TOP}\|$	1.3	V
Input Full-Scale	10	μA_{pp}
Input Bandwidth	0.1-8	KHz
Dynamic Range	73	dB
Power Consumption	75	μW
Si Area	<0.5	mm^2

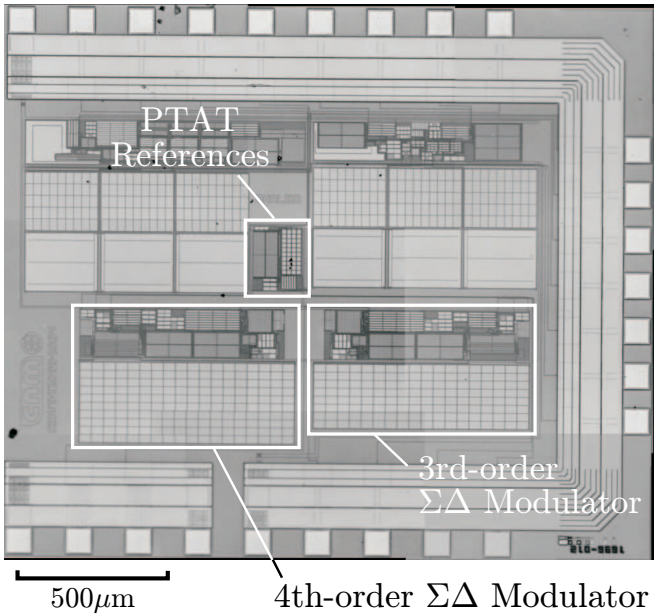
I_{ref}=6μA, $I_{tuni}\epsilon$(0.2,6)μA, $C_{oxi}\epsilon$(80,500)pF



Design Examples

- Prototypes: expected 12b $\longrightarrow$ <10b ☹

  . . . due to not modeling WA !!!



- Proposed solution:

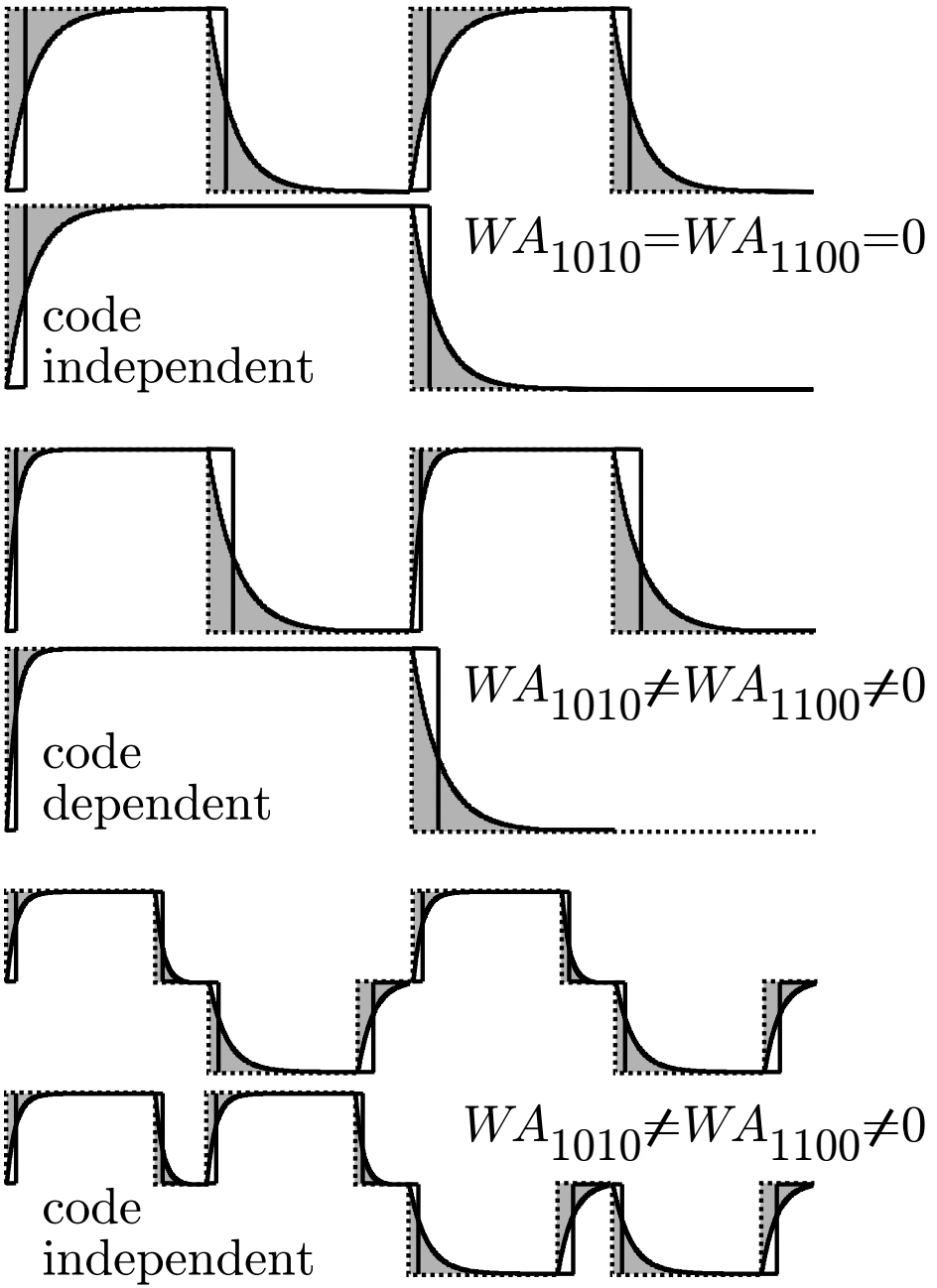
  return-to-zero (t_{rz}) symbols +

  $\tau_{bi}=\frac{t_{rz}}{T_s}\tau_{fi}$ compensation

  $\downarrow$

  code independent WA

- High-level models of new designs return good results. . . ☺



Conclusions

- Possibility of implementing $\Sigma\Delta$ ADCs in the Log-domain using the MOSFET in weak inversion
- Complete set of low-voltage all-MOS basic building blocks
- Detailed modeling of main second-order effects
- Expected 1V@100μA 12b@8KHz realizations in short for audio SoCs (e.g. HAs)
- Circuit technique suitable for digital VLSI technologies

. . . Thank you very much for your attention!